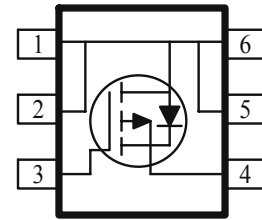
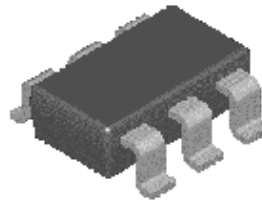


P-Channel 30V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are power switch, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Low Gate Charge
- Fast Switch
- Miniature TSOP-6 Surface Mount Package Saves Board Space

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.112 @ $V_{GS} = 10\text{ V}$	3.4
	0.172 @ $V_{GS} = 4.5\text{ V}$	2.7



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	$T_A=25^\circ\text{C}$	3.4
		$T_A=70^\circ\text{C}$	2.6
Pulsed Drain Current ^b	I_{DM}	± 20	A
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	
Power Dissipation ^a	P_D	$T_A=25^\circ\text{C}$	2.0
		$T_A=70^\circ\text{C}$	1.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	R_{THJA}	$t \leq 5\text{ sec}$	62.5
		Steady-State	110

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			50	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$			112	m Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 2.7 \text{ A}$			172	
Forward Transconductance ^A	g_s	$V_{DS} = 4.5 \text{ V}, I_D = 3.4 \text{ A}$		6		S
Diode Forward Voltage	V_{SD}	$I_S = 0.75 \text{ A}, V_{GS} = 0 \text{ V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 30 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 3.4 \text{ A}$		4.5		nC
Gate-Source Charge	Q_{gs}			1.4		
Gate-Drain Charge	Q_{gd}			2.4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}, R_L = 30 \Omega, I_D = 1 \text{ A},$ $V_{GEN} = 10 \text{ V}$		9		ns
Rise Time	t_r			12		
Turn-Off Delay Time	$t_{d(off)}$			25		
Fall-Time	t_f			14		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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