

**PowerTrench® Power Clip
30 V Asymmetric Dual N-Channel MOSFET**

Features

- Q1: N-Channel
 - Max $r_{DS(on)}$ = 9.6 mΩ at $V_{GS} = 4.5$ V, $I_D = 10$ A
- Q2: N-Channel
 - Max $r_{DS(on)}$ = 2.7 mΩ at $V_{GS} = 4.5$ V, $I_D = 22$ A
 - Low inductance packaging shortens rise/fall times, resulting in lower switching losses
 - MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
 - RoHS Compliant

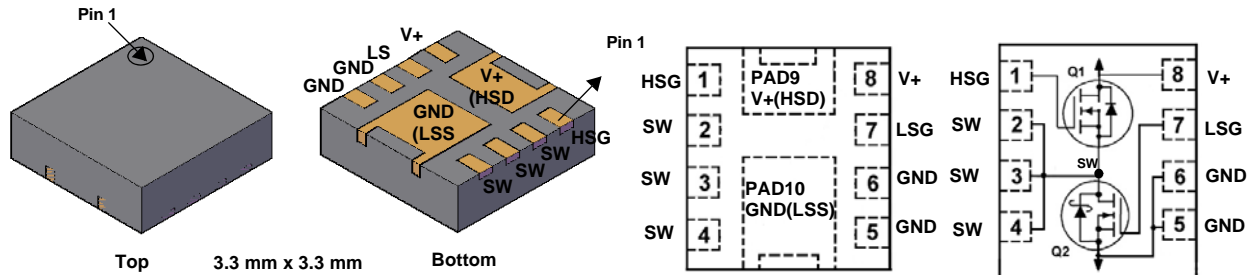


General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	30	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25$ °C	20	55	A
	-Continuous $T_A = 25$ °C	13 ^{1a}	26 ^{1b}	
	-Pulsed	40	100	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	21	97	mJ
P_D	Power Dissipation for Single Operation $T_A = 25$ °C	1.6 ^{1a}	2.0 ^{1b}	W
	Power Dissipation for Single Operation $T_A = 25$ °C	0.8 ^{1c}	0.9 ^{1d}	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	77 ^{1a}	63 ^{1b}	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	151 ^{1c}	135 ^{1d}	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.0	3.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
13CF/15CF	FDPC8013S	Power Clip 33	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		16 20		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$ $V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	Q1 Q2			100 100	nA nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$	Q1 Q2	1.2 1.2	1.5 1.7	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-5 -6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 13\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 13\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	Q1		4.6 6.7 6.6	6.4 9.6 9.2	m Ω
		$V_{GS} = 10\text{ V}$, $I_D = 26\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 22\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 26\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	Q2		1.4 2.0 1.9	1.9 2.7 2.6	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 13\text{ A}$ $V_{DS} = 5\text{ V}$, $I_D = 26\text{ A}$	Q1 Q2		53 168		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1: $V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1 Q2		827 2785		pF
C_{oss}	Output Capacitance	Q2: $V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1 Q2		333 997		pF
C_{riss}	Reverse Transfer Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1 Q2		44 128		pF
R_g	Gate Resistance		Q1 Q2		0.5 0.5		Ω

Switching Characteristics

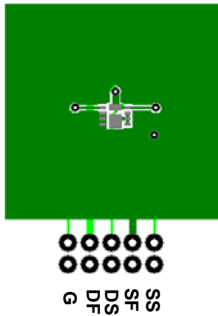
$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 15\text{ V}$, $I_D = 13\text{ A}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		6 11		ns
t_r	Rise Time		Q1 Q2		2 5		ns
$t_{d(off)}$	Turn-Off Delay Time	Q2: $V_{DD} = 15\text{ V}$, $I_D = 26\text{ A}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		16 30		ns
t_f	Fall Time		Q1 Q2		2 4		ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 10 V	Q1 Q2		13 44		nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 4.5 V	Q1 Q2		6 21		nC
Q_{gs}	Gate to Source Gate Charge	Q2 $V_{DD} = 15\text{ V}$, $I_D = 26\text{ A}$	Q1 Q2		2.2 7.2		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		1.9 6.6		nC

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

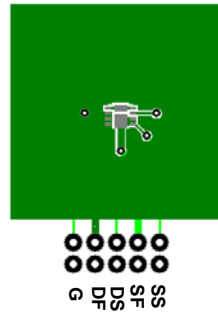
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 13\text{ A}$ (Note 2)	Q1		0.80	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 26\text{ A}$ (Note 2)	Q2		0.77	1.2	
t_{rr}	Reverse Recovery Time	Q1 $I_F = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Q1		22		ns
			Q2		29		
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = 26\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$	Q1		7		nC
			Q2		30		

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 77 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 63 °C/W when mounted on a 1 in² pad of 2 oz copper



c. 151 °C/W when mounted on a minimum pad of 2 oz copper



d. 135 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Q1: E_{AS} of 21 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 1.2\text{ mH}$, $I_{AS} = 6\text{ A}$, $V_{DD} = 23\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 14.5\text{ A}$.

Q2: E_{AS} of 97 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 0.6\text{ mH}$, $I_{AS} = 18\text{ A}$, $V_{DD} = 23\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 32.9\text{ A}$.

4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics (Q1 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

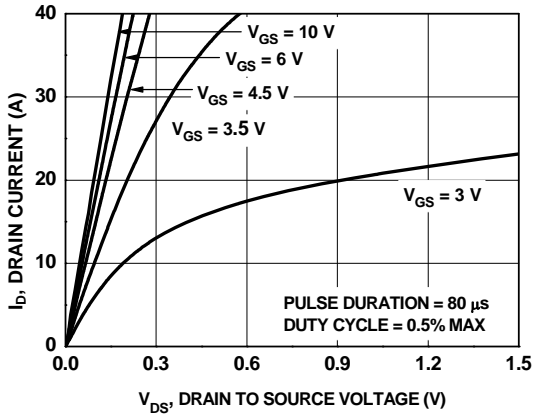


Figure 1. On Region Characteristics

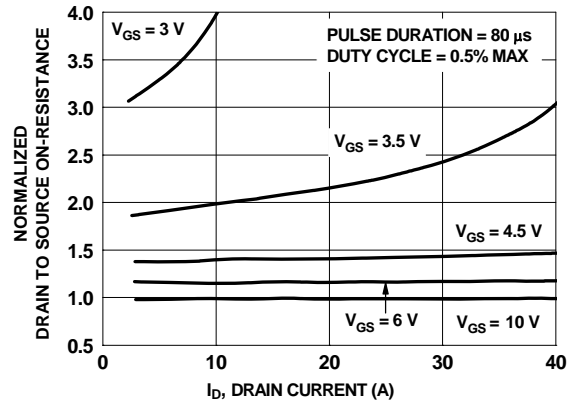


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

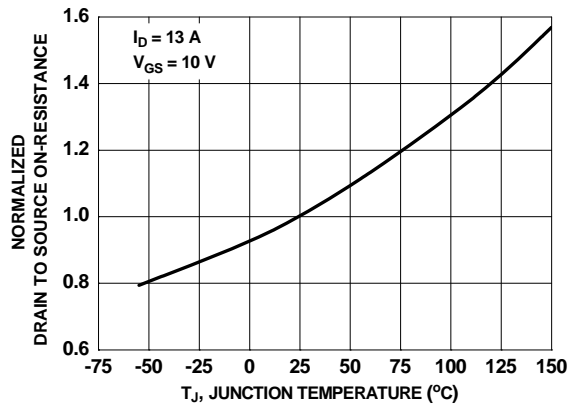


Figure 3. Normalized On Resistance vs Junction Temperature

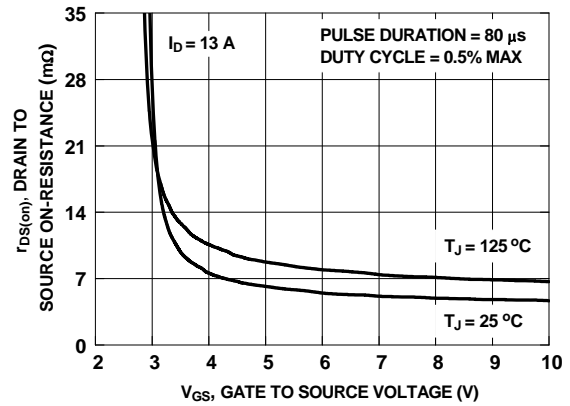


Figure 4. On-Resistance vs Gate to Source Voltage

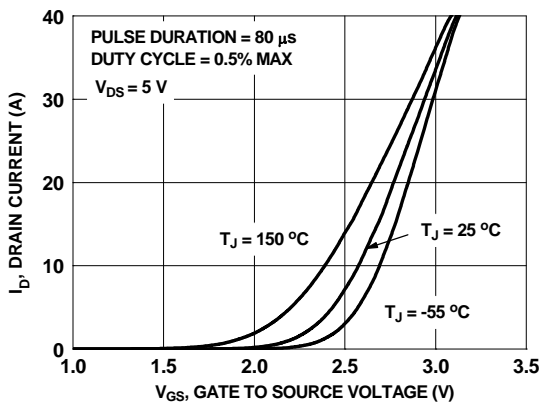


Figure 5. Transfer Characteristics

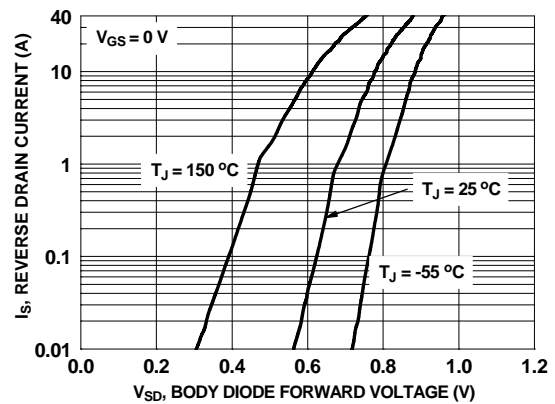


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

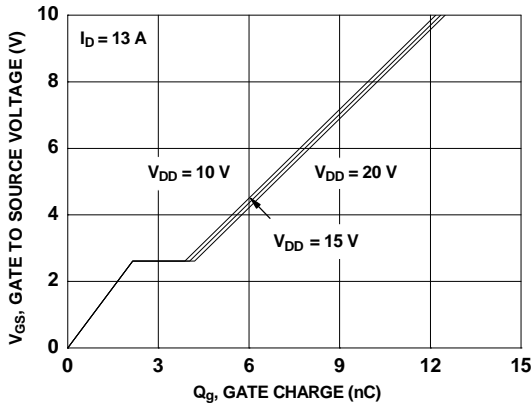


Figure 7. Gate Charge Characteristics

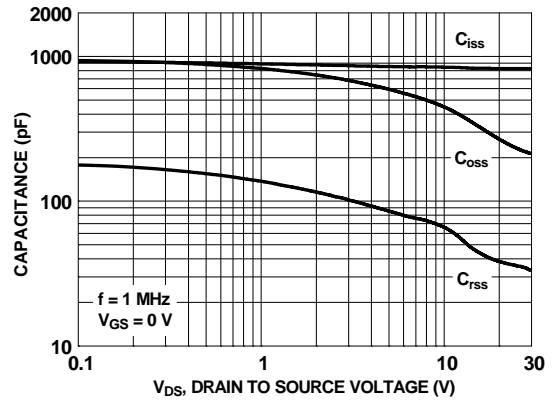


Figure 8. Capacitance vs Drain to Source Voltage

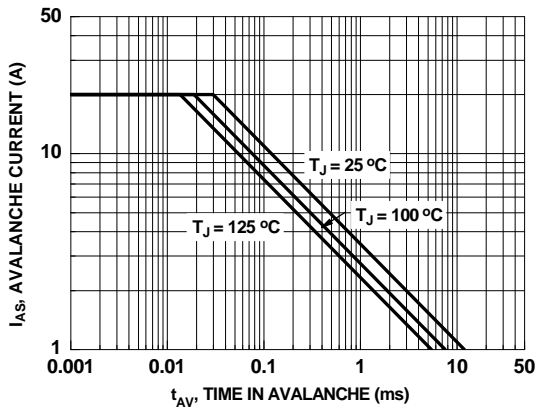


Figure 9. Unclamped Inductive Switching Capability

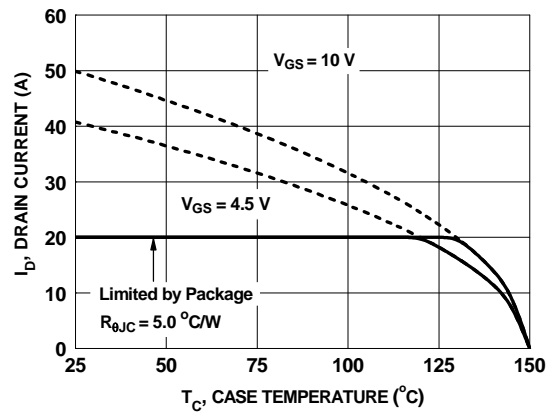


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

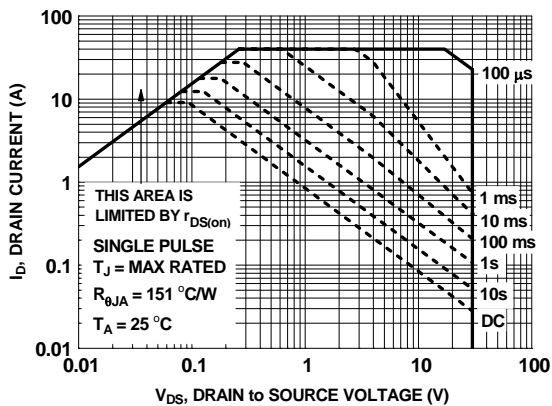


Figure 11. Forward Bias Safe Operating Area

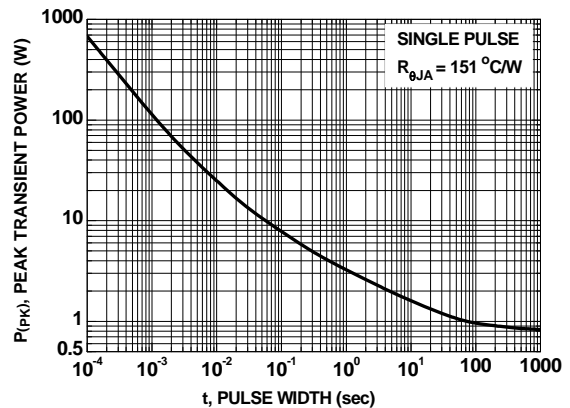


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

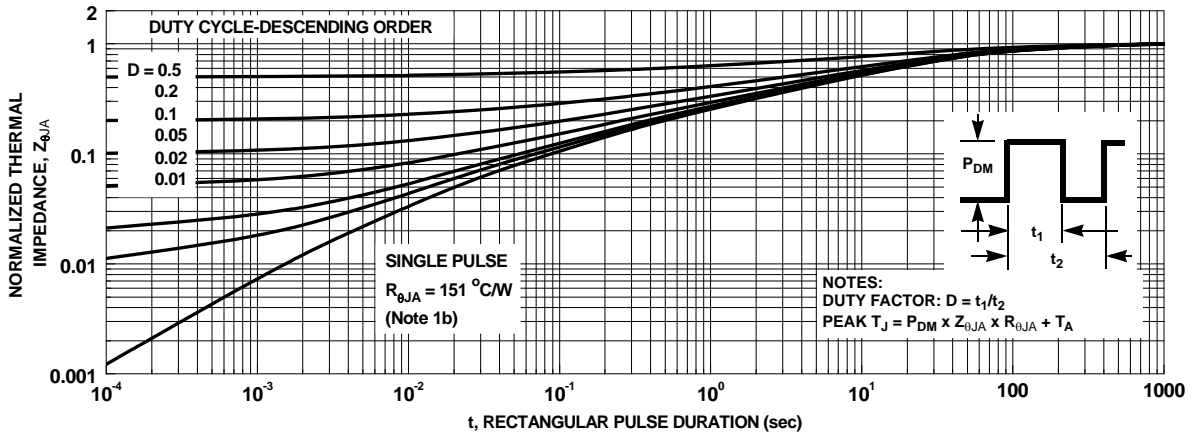


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

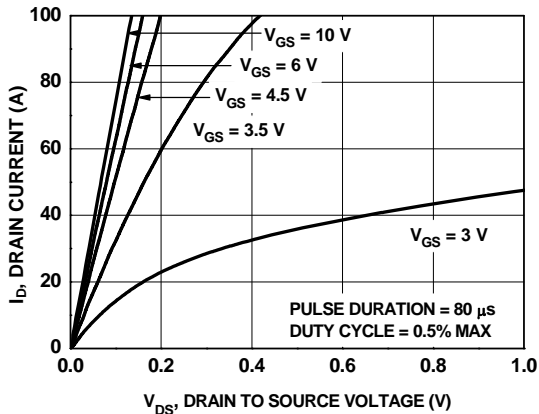


Figure 14. On-Region Characteristics

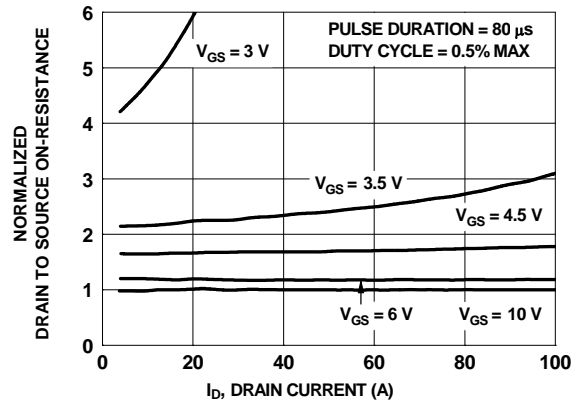


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

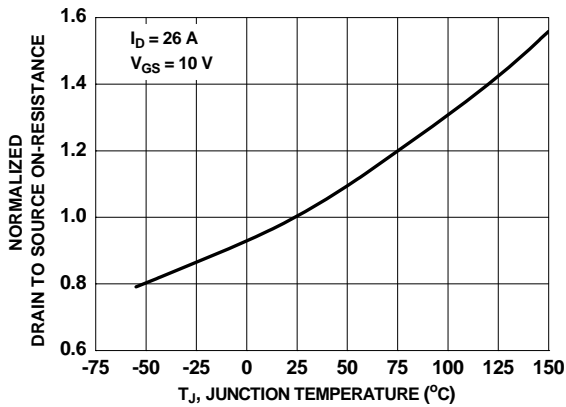


Figure 16. Normalized On-Resistance vs Junction Temperature

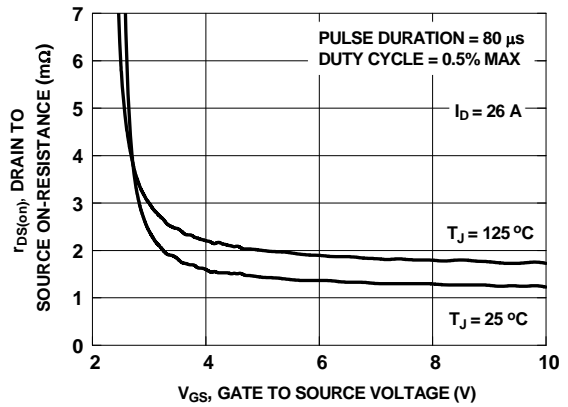


Figure 17. On-Resistance vs Gate to Source Voltage

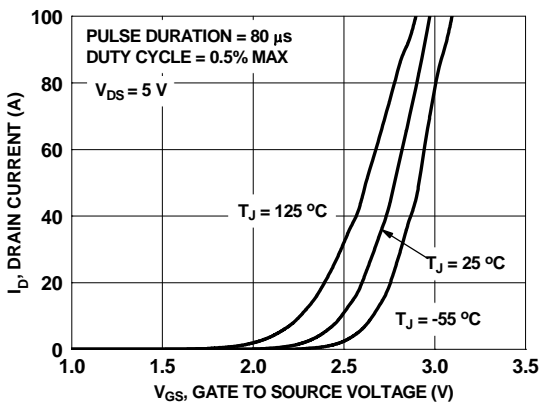


Figure 18. Transfer Characteristics

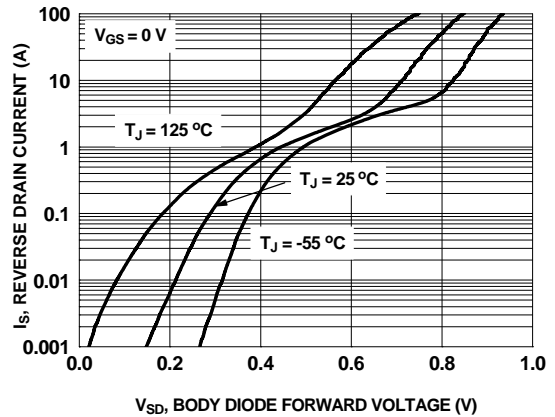


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

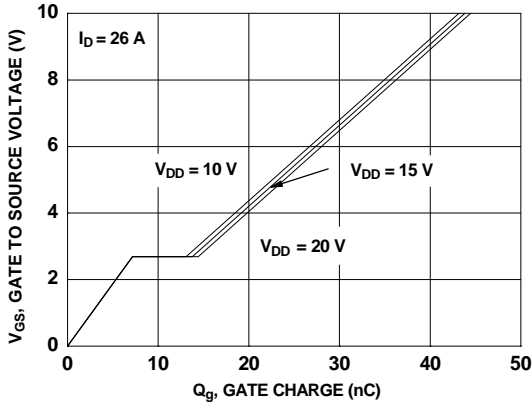


Figure 20. Gate Charge Characteristics

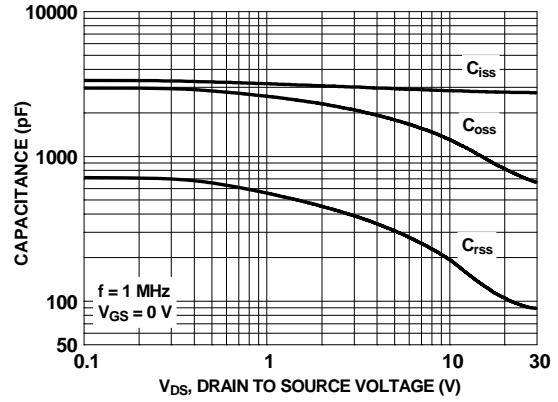


Figure 21. Capacitance vs Drain to Source Voltage

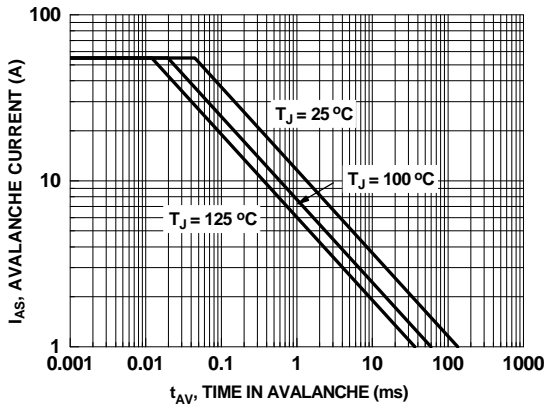


Figure 22. Unclamped Inductive Switching Capability

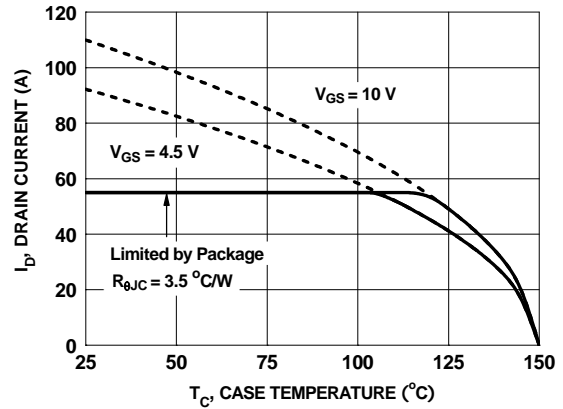


Figure 23. Maximum Continuous Drain Current vs Ambient Temperature

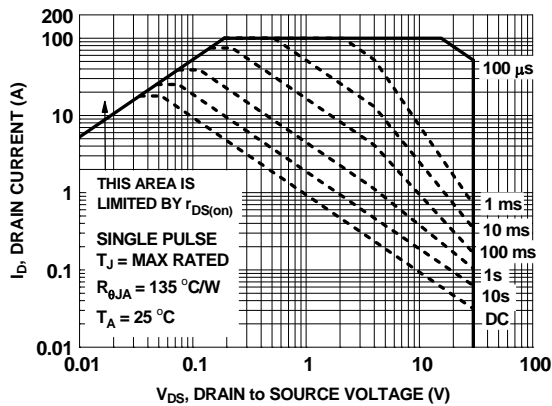


Figure 24. Forward Bias Safe Operating Area

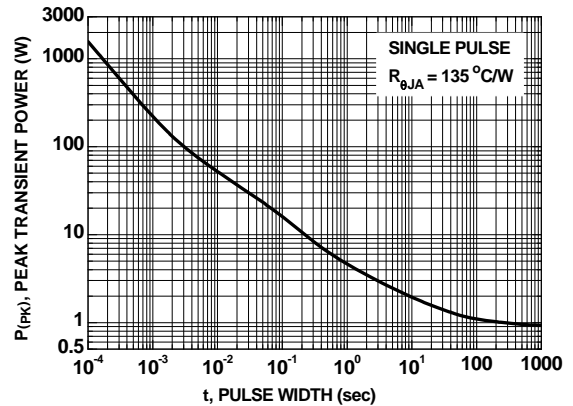


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

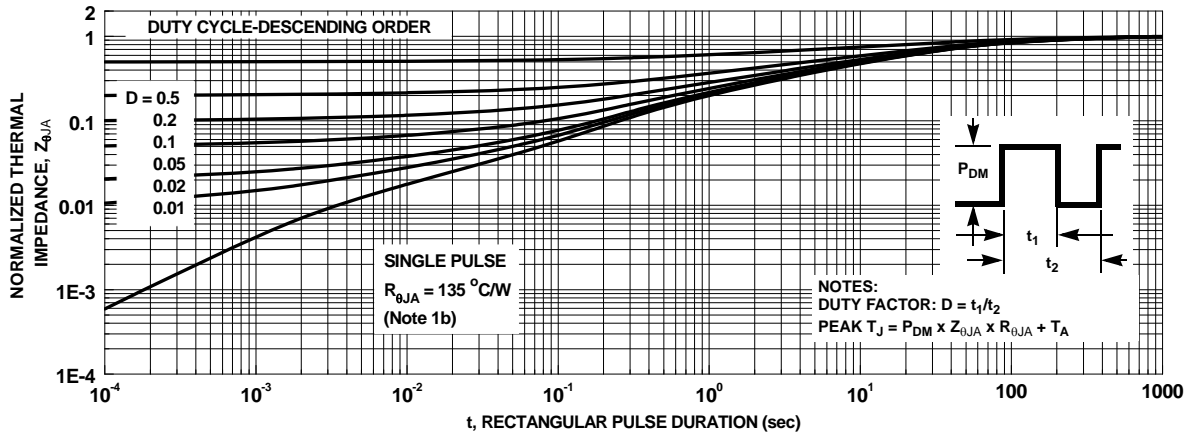


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8013S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

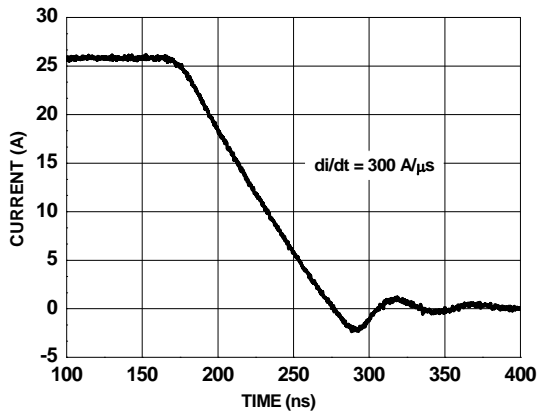


Figure 27. FDPC8013S SyncFET™ body diode reverse recovery characteristic

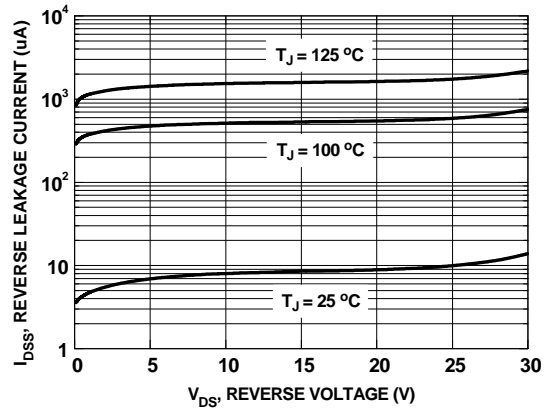
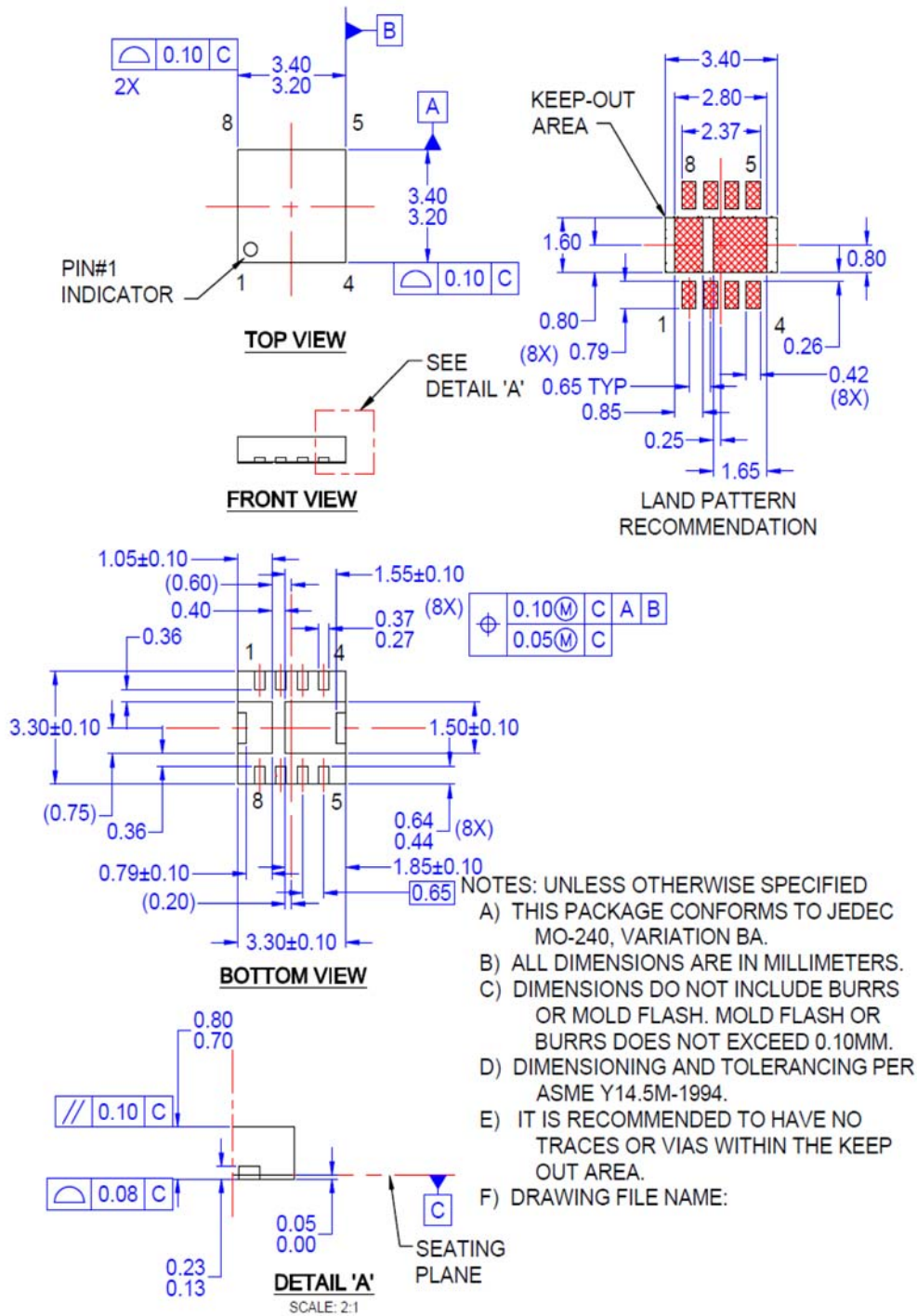


Figure 28. SyncFET™ body diode reverse leakage versus drain-source voltage

Dimensional Outline and Pad Layout





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| AccuPower™ | FRFET® | PowerXS™ | the power® |
| AX-CAP™* | Global Power Resource™ | Programmable Active Droop™ | franchise |
| BitSiC® | Green Bridge™ | QFET® | TinyBoost™ |
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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