Features

- **Fully Supports the IEEE 802.11 Standard**
- **Supports MAC Layer Functions**
- **Individual 64-byte Transmit and 64-byte Receive FIFOs**
- **Integrated ARM7TDMI™ RISC Processor for MAC Layer Functions**
- **Glueless PCMCIA Bus Interface Conforming to PC Card Standard - Feb. 1995**
- **Glueless SRAM Interface for MAC Operations, Supporting up 256K bytes of Memory**
- **Glueless Flash Memory Interface, Supporting up to 256K bytes of Non-volatile Memory for MAC Control Code**
- **Programmable 8/16-bit Wide External Memory Interface**
- **Enciphering/Deciphering of Data by the Implementation of the RC4 Code, Ensures Maximum Privacy of Data**
- **Provides Integrated Physical Attachment Interface (PAI), Supporting Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum Physical-Layer Interfaces**
- **144-pin Thin Quad Flat Pack (TQFP) Package Available for Space Critical Applications, Such as PCMCIA Type 2 Form Factor**

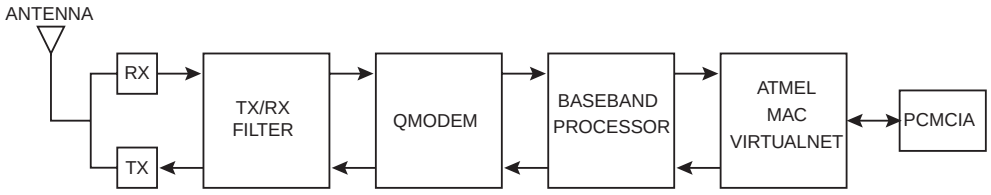
Description

VirtualNet is a single-chip controller that provides all processing and functionality needed for the MAC protocol of wireless LANs (focusing but not limited to the IEEE 802.11 standard). VirtualNet provides a glueless interface conforming to PC Card 95 and can control a variety of physical interfaces.

The VirtualNet chip contains a PCMCIA Bus Interface Unit, a MAC control unit and a Physical Attachment Interface (PAI). The PAI supports Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum physical interfaces providing flexibility to end users.

The incorporation of the ARM7TDMI powerful RISC processor in the MAC control unit of VirtualNet, allows all the necessary MAC functions to be carried out by it and users only need to add the required memory and physical layer in order to deliver a fully functional wireless LAN connection.

Figure 1. Typical VirtualNet Application



Single-Chip Wireless LAN Media Access Controller

VirtualNet™ AT76C501

Summary

A complete datasheet is available under NDA. Please contact:

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Rev. 1136BS–04/99

Overview

ARM Core

VirtualNet contains the ARM7TDMI core, a 32-bit RISC processor. The ARM core can execute the sophisticated firmware needed to implement IEEE 802.11 MAC protocol functionality. ARM7TDMI supports two alternative instruction sets. Powerful 32-bit code can be executed by the processor in ARM operating mode. However, a 16-bit instruction subset is also available in THUMB mode. THUMB mode can be selected to exploit full processor power with limited external memory resources. Note that the ARM7TDMI operating mode can be changed at run time with negligible overhead.

PCMCIA Interface Unit

VirtualNet PCMCIA interface unit implements a PCMCIA 2.1/JEIDA 4.2 compatible 8-bit wide PC-card front-end interface. The PCMCIA interface unit provides the host with master access to VirtualNet registers and memory (SRAM and Flash) that accompanies a complete VirtualNet-based design. The PCMCIA interface unit contains a number of general purpose registers to allow configuration and/or status information exchange between the host and VirtualNet firmware. Moreover, the PCMCIA interface unit provides the host and the ARM core with the capability to raise interrupts to each other.

Consequently, the host driver software uses the PCMCIA interface unit to initialize VirtualNet, to exchange configuration information with VirtualNet firmware, to monitor VirtualNet operation, to receive network indications and to transfer network data from/to network data buffers in SRAM.

External Memory Interface (EMI)

The external memory interface (EMI) is used by VirtualNet to gain access to the Flash and SRAM memory that accompanies a complete VirtualNet-based design. Flash memory contains the VirtualNet firmware and the Card Information Structure (CIS) used by the host PCMCIA subsystem. SRAM memory accommodates the ARM core stack, VirtualNet firmware status variables, structures supporting host/firmware interface and network data buffers. When the host driver software passes network data to VirtualNet through the PCMCIA interface unit, the data is automatically rerouted to the external memory interface in order to reach the SRAM. Note that the VirtualNet firmware can be permanently kept in a slow Flash and loaded onto faster SRAM during initialization, so that instructions are fetched from the SRAM and the firmware performance is optimized.

External memory can be either 8-bit or 16-bit wide. External memory width is configured via BHWS pin. When 8-bit memory is used, VirtualNet supports 128K bytes SRAM and 128K bytes Flash memory. When 16-bit memory is used, VirtualNet supports 256K bytes SRAM and 256K bytes Flash memory.

Physical Attachment Interface (PAI)

The VirtualNet device can be connected to an IEEE 802.11 network via a flexible network interface. The physical layer network device is interconnected to VirtualNet via the physical attachment interface (PAI) module.

The Physical attachment interface (PAI) module has been designed to automatically handle many time-critical physical network management tasks and to provide primitives for efficient 802.11 MAC protocol implementation. The PAI contains a 64-byte transmit FIFO as well as a 64-byte receive FIFO and is capable of sophisticated DMA operations. Consequently, the DMA control imposes minimal overhead on the ARM core, while instant processor reaction to network events is not needed. This saves processing power for high-level MAC functions. The PAI also includes a 64-bit Time Synchronization Function (TSF) counter, as specified by the IEEE 802.11 protocol. Finally, the PAI provides automatic defer when the wireless medium is found occupied and a transmission is pending.

Data Enciphering/Deciphering Module

VirtualNet incorporates a data enciphering/deciphering module implementing the RC4 enciphering algorithm to offer secure wireless connections. The data enciphering/deciphering module is able to support the Wire Equivalence Privacy scheme as described by the IEEE 802.11 standard. This module acts on network data blocks stored in the SRAM to encipher or decipher the data blocks automatically, without loading the ARM core.

Timer Devices

VirtualNet includes two identical system timers. Each system timer is a completely independent device with adjustable prescale and preload, capable of producing interrupts in a periodic or one-shot fashion. System timers can be used to implement IEEE 802.11 protocol functions such as virtual medium allocation, power management or periodic beacon production.

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