FEDL63193-04

OKI Semiconductor

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ML63193

4-Bit Microcontroller with Built-in 1024-Dot Matrix LCD Driver and Melody Circuit.

GENERAL DESCRIPTION

The ML63193 is CMOS 4-bit microcontroller with built-in 1024-dot matrix LCD drivers (64 SEG. × 16 COM.), and operates at 0.9 V (Min). The ML63193 is suitable for applications as games, toys, watches, remote controller, etc. Which are provided with a LCD display.
The ML63193 is an M6318x series mask ROM-version product of OLMS-63K family, which employs Oki's original CPU core nX-4/250.

FEATURES

• Extensive instruction set
  408 instructions:
    Transfer, rotate, increment/decrement, arithmetic operations, compare, logic operations, mask operations, bit operations, ROM table reference, stack operations, flag operations, jump, conditional branch, call/return, control

• Wide variety of addressing modes
  Indirect addressing mode for 4 types of data memory with current bank register, extra bank register, HL register and XY register
  Data memory bank internal direct addressing mode

• Processing speed
  2 clocks per machine cycle, with most instructions executed in 1 machine cycle
  Minimum instruction execution time : 61 μs (@ 32.768 kHz system clock)
  : 1 μs (@ 2 MHz system clock)

• Clock generation circuit
  Low-speed clock : Crystal oscillation or RC oscillation selected with mask option (30 kHz to 80 kHz)
  High-speed clock : Ceramic oscillation or RC oscillation selected with software (2 MHz max)

• Program memory space
  64 K words
  Basic instruction length is 16 bits/1word.

• Data memory space
  2048 nibbles

• Stack level
  Call stack level : 16 levels
  Register stack level : 16 levels

• I/O Ports

Input ports:

Selectable as input pull-up resistor/input pull-down resistor/high impedance input.

I/O ports:

Selectable as input pull-up resistor/input pull-down resistor/high impedance input.
Selectable as P-channel open drain output/N-channel open drain output/high-impedance output/
CMOS output.

Can be interfaced with external peripherals that use a different power supply than this device uses.V_{DDI} is the power supply pin for ports.

Number of ports:

Input port	: 1 port × 4 bits
Input-output port	: 5 ports × 4 bits

• Melody output

Melody frequency	: 529 Hz to 2979 Hz
Tone length	: 63 varieties
Tempo	: 15 varieties
Melody data	: Stored in program memory
Buzzer driver signal output	: 4 kHz

• LCD driver

Number of segments	: 1024 Max. (64 SEG. × 16 COM.)
Duty	: Selectable as 1/1 to 1/16 duty
Bias	: Selectable as 1/4 or 1/5 bias (regulator built-in)
Frame frequency	: ex. 64 Hz (at 1/16 duty), 128 Hz (at 1/8 duty), 256 Hz (at 1/4 duty), 512 Hz (at 1/2 duty), 1024 Hz (at 1/1 duty)
Contrast	: 16 levels adjustable
Display modes	: Selectable as all-ON mode/all-OFF mode/power down mode/ normal display mode

• Multiplier/divider circuit

Multiplier	: (8 bits)×(8 bits) → Product (16 bits)
Divider	: (16 bits)/(8 bits) → Quotient (16 bits), Remainder (8 bits)

• System reset function

System reset through RESET pin (selectable as built-in 2 kHz RESET-Sampling circuit by mask option)
System reset by power-on detection (When not using 2 kHz RESET-Sampling circuit)
System reset by low-speed oscillation halt

• Battery check

Low-voltage supply check

The value of the judgment voltage is selected by the software (by setting the LD1 and LD0 bits of BLDCON).

LD1	LD0	Judgment Voltage (V)	Remarks
0	0	1.05 ± 0.10	Ta = 25°C
0	1	1.20 ± 0.10	Ta = 25°C
1	0	1.80 ± 0.10	Ta = 25°C
1	1	2.40 ± 0.10	Ta = 25°C

• Timers and Counter

8-bit timer	: 4 Selectable as auto-reload mode/capture mode/ clock frequency measurement mode
Watchdog timer	: 1
100 Hz timer	: 1 Measurable in steps of 1/100 sec.
15-bit time-base counter	: 1 1, 2, 4, 8, 16, 32, 64, and 128 Hz signals can be read

• Serial port

Mode	: Selectable as UART mode, synchronous mode
UART communication speed	: 1200 bps, 2400 bps, 4800 bps, 9600 bps
Clock frequency in synchronous mode	: Internal clock mode (32.768 kHz), External clock frequency
Data length	: 5 to 8 bits

• Shift register

Shift clock	: 1× or 1/2 × system clock, timer 1 overflow, external clock
Data length	: 8 bits

• Interrupt factors

External interrupt	: 4
Internal interrupt	: 14 (watchdog timer interrupt is a nonmaskable interrupt)

• Operating temperature	: –20 to +70 °C

• Power supply backup

Backup circuit (voltage multiplier) enables operation at 0.9 V minimum.

• Power supply voltage

When backup used	: 0.9 V to 2.7 V (Operating frequency: 30 k to 80 kHz) 1.2 V to 2.7 V (Operating frequency: 300 k to 500 kHz) 1.5 V to 2.7 V (Operating frequency: 200 k to 1 MHz)
When backup not used	: 1.8 V to 5.5 V (Operating frequency: 200 k to 2 MHz)

• Package:

Chip (128 pads)	: (Product name: ML63193-xxxWA)
144-pin plastic LQFP (LQFP144-P-2020-0.50-K)	: (Product name: ML63193-xxxTC) xxx indicates a code number.

MASK OPTION

In the ML63193 uses the mask option to specify the following functions:

- Low-Speeed clock oscillation circuit
  Specify the crystal oscillation circuit or the RC oscillation circuit for the low-speed clock oscillation circuit.
- Reset signal sampling
  Specify whether or not the reset signal will be sampled at 2 kHz.
  When specifying “will carry out 2 kHz sampling,” hold the RESET pin at a “H” level for 1 ms or more.

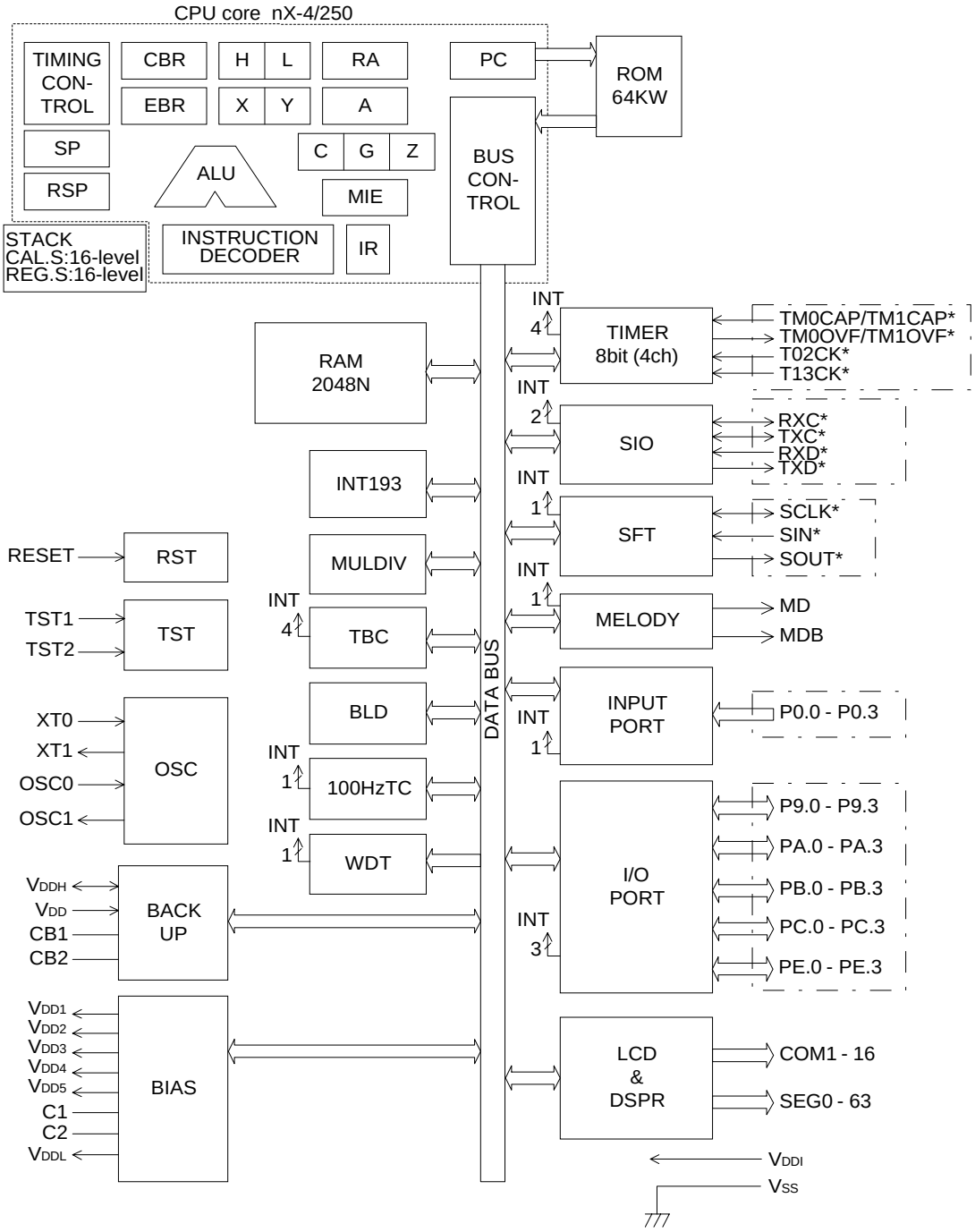
To use the mask option, assign mask option data in the application program in accordance with the formats below. The mask option area is an application program execution disabled area.

Mask Option Data Assignment Format

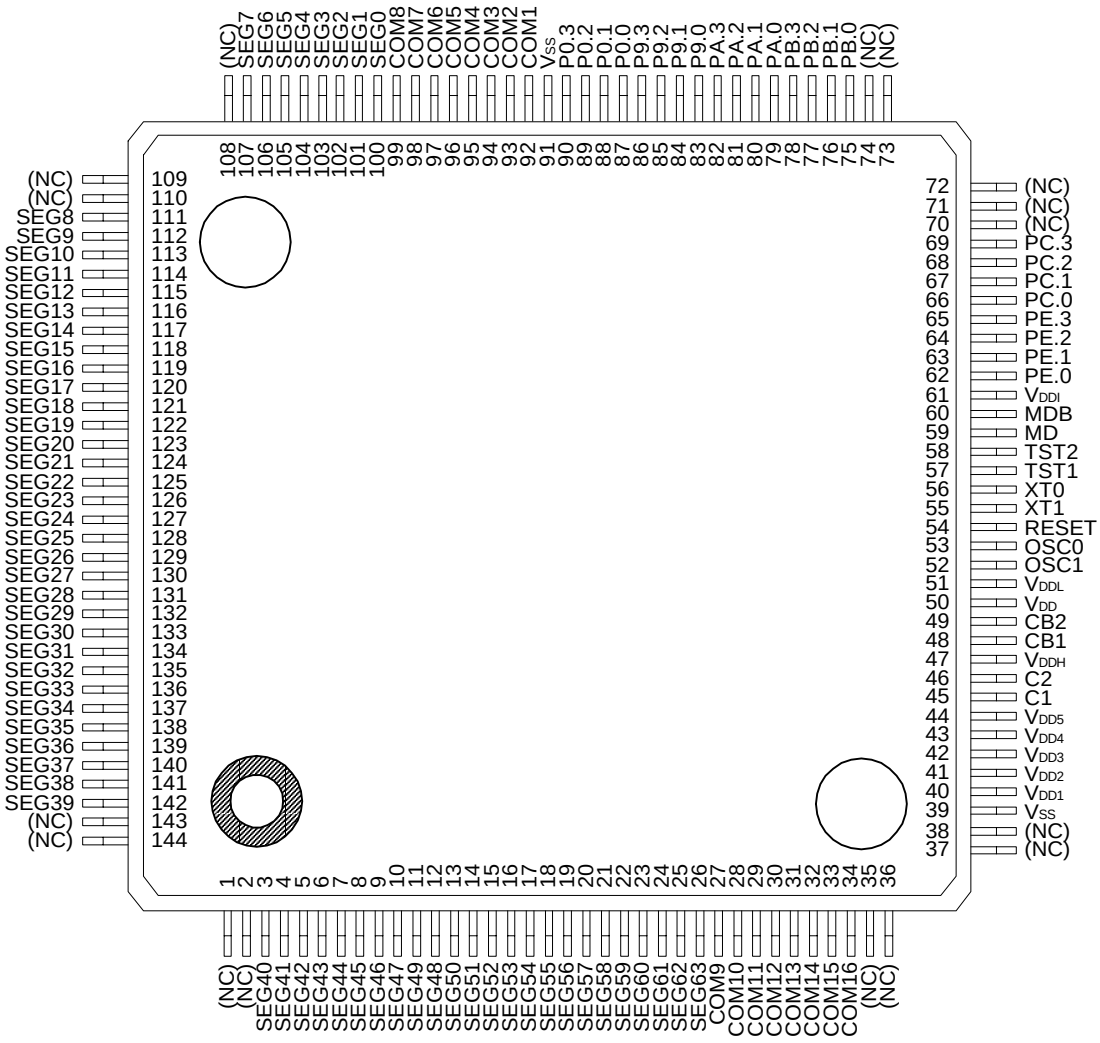
Function	Mask option area	bit	data	Option to be selected
Low-speed clock oscillation circuit (crystal oscillation circuit/RC oscillation circuit)	0FFE0H	bit 0	0	Crystal oscillation circuit
			1	RC oscillation circuit
Reset signal sampling (will/will not carry out 2 kHz sampling)		bit 1	0	Will carry out 2 kHz sampling
			1	Will not carry out 2 kHz sampling

BLOCK DIAGRAM

Asterisks (*) indicate the secondary function of each port. Signal names enclosed by chain lines (┈┈) Indicate interface signals of the V_{DDI} power supply system.



PIN CONFIGURATION (TOP VIEW)

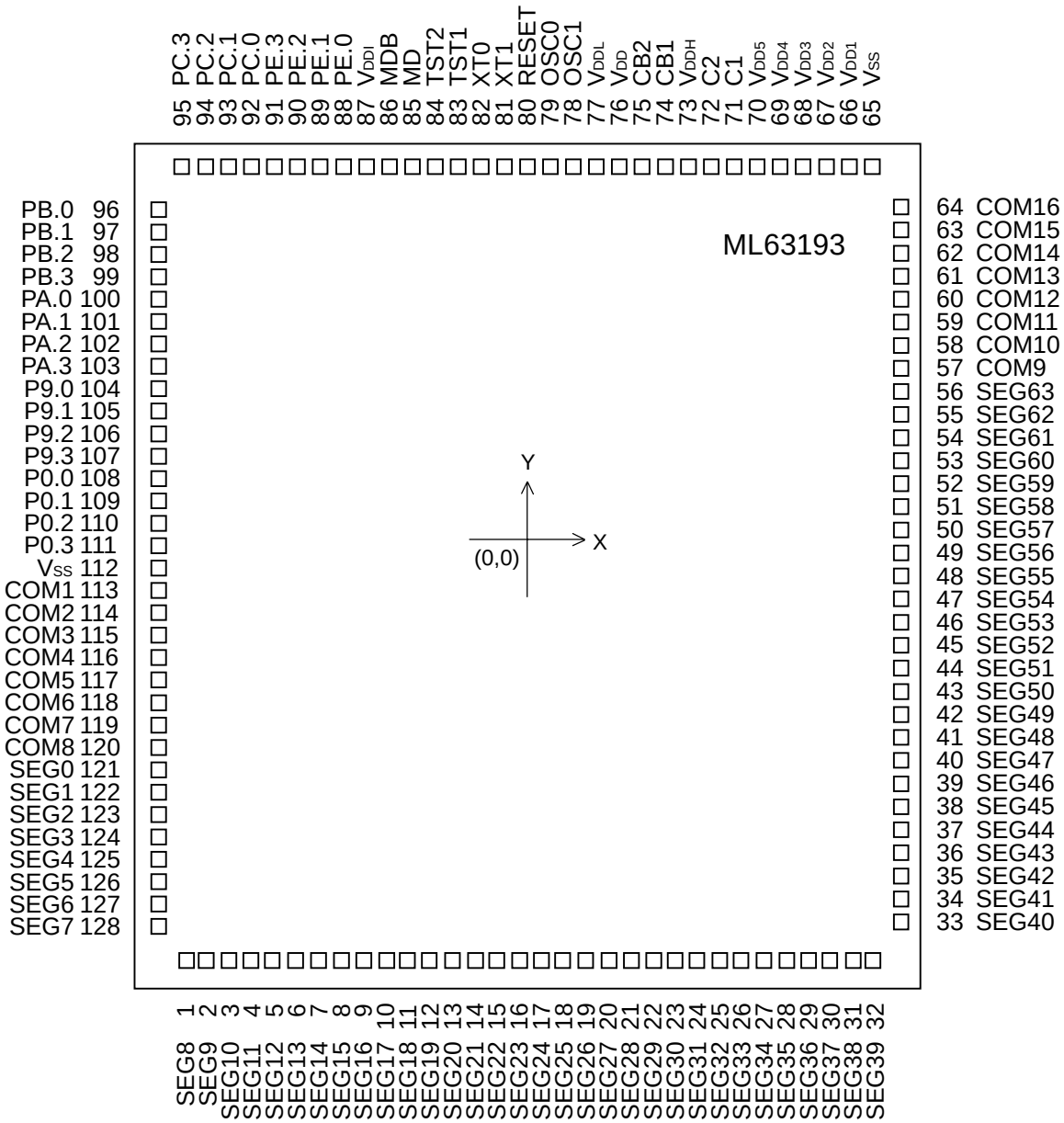


144-Pin Plastic LQFP
(TC: LQFP144-P-2020-0.50-K)

Note: Pins marked as (NC) are no-connection pins which are left open.

PAD CONFIGURATION

Pad Layout



Chip size	: 5.72 mm × 5.72 mm
Chip thickness	: 350 µm (280 µm: available as required)
Coordinate origin	: center of chip
Pad hole size	: 100 µm × 100 µm
Pad size	: 110 µm × 110 µm
Minimum pad pitch	: 140 µm

Note: The chip substrate voltage is V_{SS}.

Pad Coordinates

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)
1	SEG8	–2204	–2714
2	SEG9	–2063	–2714
3	SEG10	–1923	–2714
4	SEG11	–1783	–2714
5	SEG12	–1642	–2714
6	SEG13	–1502	–2714
7	SEG14	–1361	–2714
8	SEG15	–1221	–2714
9	SEG16	–1081	–2714
10	SEG17	–940	–2714
11	SEG18	–800	–2714
12	SEG19	–659	–2714
13	SEG20	–519	–2714
14	SEG21	–379	–2714
15	SEG22	–238	–2714
16	SEG23	–98	–2714
17	SEG24	43	–2714
18	SEG25	183	–2714
19	SEG26	323	–2714
20	SEG27	464	–2714
21	SEG28	604	–2714
22	SEG29	745	–2714
23	SEG30	885	–2714
24	SEG31	1025	–2714
25	SEG32	1166	–2714
26	SEG33	1306	–2714
27	SEG34	1447	–2714
28	SEG35	1587	–2714
29	SEG36	1727	–2714
30	SEG37	1868	–2714
31	SEG38	2008	–2714
32	SEG39	2149	–2714
33	SEG40	2714	–2149
34	SEG41	2714	–2008
35	SEG42	2714	–1868
36	SEG43	2714	–1727
37	SEG44	2714	–1587
38	SEG45	2714	–1447
39	SEG46	2714	–1306
40	SEG47	2714	–1166
41	SEG48	2714	–1025
42	SEG49	2714	–885
43	SEG50	2714	–745
44	SEG51	2714	–604
45	SEG52	2714	–464
46	SEG53	2714	–323
47	SEG54	2714	–183
48	SEG55	2714	–43
49	SEG56	2714	98
50	SEG57	2714	238
51	SEG58	2714	379
52	SEG59	2714	519
53	SEG60	2714	659
54	SEG61	2714	800
55	SEG62	2714	940
56	SEG63	2714	1081
57	COM9	2714	1221
58	COM10	2714	1361
59	COM11	2714	1502
60	COM12	2714	1642
61	COM13	2714	1783
62	COM14	2714	1923
63	COM15	2714	2063
64	COM16	2714	2204
65	V_{SS}	2152	2714
66	V_{DD1}	2011	2714
67	V_{DD2}	1871	2714
68	V_{DD3}	1730	2714
69	V_{DD4}	1590	2714
70	V_{DD5}	1450	2714
71	C1	1309	2714
72	C2	1169	2714
73	V_{DDH}	1028	2714
74	CB1	888	2714
75	CB2	748	2714
76	V_{DD}	607	2714
77	V_{DDL}	467	2714
78	OSC1	326	2714
79	OSC0	186	2714
80	RESET	46	2714
81	XT1	–95	2714
82	XT0	–235	2714
83	TST1	–376	2714
84	TST2	–516	2714
85	MD	–656	2714
86	MDB	–797	2714

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (µm)	Y (µm)
87	V_{DDI}	–937	2714
88	PE.0	–1078	2714
89	PE.1	–1218	2714
90	PE.2	–1358	2714
91	PE.3	–1499	2714
92	PC.0	–1639	2714
93	PC.1	–1780	2714
94	PC.2	–1920	2714
95	PC.3	–2060	2714
96	PB.0	–2714	2246
97	PB.1	–2714	2106
98	PB.2	–2714	1966
99	PB.3	–2714	1825
100	PA.0	–2714	1685
101	PA.1	–2714	1544
102	PA.2	–2714	1404
103	PA.3	–2714	1264
104	P9.0	–2714	1123
105	P9.1	–2714	983
106	P9.2	–2714	842
107	P9.3	–2714	702

Pad No.	Pad Name	X (µm)	Y (µm)
108	P0.0	–2714	562
109	P0.1	–2714	421
110	P0.2	–2714	281
111	P0.3	–2714	140
112	V_{SS}	–2714	0
113	COM1	–2714	–140
114	COM2	–2714	–281
115	COM3	–2714	–421
116	COM4	–2714	–562
117	COM5	–2714	–702
118	COM6	–2714	–842
119	COM7	–2714	–983
120	COM8	–2714	–1123
121	SEG0	–2714	–1264
122	SEG1	–2714	–1404
123	SEG2	–2714	–1544
124	SEG3	–2714	–1685
125	SEG4	–2714	–1825
126	SEG5	–2714	–1966
127	SEG6	–2714	–2106
128	SEG7	–2714	–2246

PIN DESCRIPTIONS

The basic functions of each pin of the ML63193 are described in Table 1.
A symbol with a slash "/" denotes a pin that has a secondary function. Refer to Table 2 for secondary functions.
For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.

Table 1 Pin Descriptions (Basic Functions)

Function	Symbol	Pin No.	Pad No.	Type	Description
Power Supply	V_{DD}	50	76	—	Positive power supply pin
	V_{SS}	39,91	65,112	—	Negative power supply pin
	V_{DD1}	40	66	—	Power supply pins for LCD bias (internally generated): Capacitors (0.1 μF) should be connected between these pins and V_{SS}.
	V_{DD2}	41	67		
	V_{DD3}	42	68		
	V_{DD4}	43	69		
	V_{DD5}	44	70		
	C1	45	71	—	Capacitor connection pins for LCD bias generation: A capacitor (0.1 μF) should be connected between C1 and C2.
	C2	46	72		
	V_{DDI}	61	87	—	Positive power supply pin for external interface (Power supply for input, and input-output ports)
	V_{DDL}	51	77	—	Positive power supply pin for internal logic (internally generated): A capacitor (0.1 μF) should be connected between this pin and V_{SS}.
	V_{DDH}	47	73	—	Voltage multiplier pin for power supply backup (internally generated): A capacitor (1.0 μF) should be connected between this pin and V_{SS}.
	CB1	48	74	—	Pins to connect a capacitor for voltage multiplier. A capacitor (1.0 μF) should be connected between CB1 and CB2.
	CB2	49	75		
Oscillation	XT0	56	82	I	Low-speed clock oscillation pins: An option for using crystal oscillation or RC oscillation is chosen by the mask option. If the crystal oscillation is chosen, a crystal should be connected between XT0 and XT1, and capacitor (C_G) should be connected between XT0 and V_{SS}. If the RC oscillation is chosen, external oscillation resistor (R_{OSL}) should be connected between XT0 and XT1.
	XT1	55	81	O	
	OSC0	53	79	I	High-speed clock oscillation pins: A ceramic resonator and capacitors (C_{L0}, C_{L1}) or external oscillation resistor (R_{OSH}) should be connected to these pins.
	OSC1	52	78	O	

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
Test	TST1	57	83	I	Input pins for testing. A pull-down resistor is internally connected to these pins. The user cannot use these pins.
	TST2	58	84	I	
Reset	RESET	54	80	I	System reset input pin. Setting this pin to “H“ level puts this device into a reset state. Then, setting this pin to “ L” level starts executing an instruction from address 0000H. An option for using RESET sampling circuit or not using is chosen by the mask option. When using RESET sampling circuit, the system reset mode is entered by holding the RESET pin at a “ H” level for 1ms or more. A pull-down resistor is internally connected to this pin.
Melody	MD	59	85	O	Melody output pin (non-inverted output)
	MDB	60	86	O	Melody output pin (inverted output)

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
Port	P0.0/INT5	87	108	I	4-bit input port: Pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.
	P0.1/INT5	88	109		
	P0.2/INT5	89	110		
	P0.3/INT5	90	111		
	P9.0	83	104	I/O	4-bit input output ports: In input mode, pull-up resister input, pull-down resister input, or high-impedance input is selectable for each bit. In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P9.1	84	105		
	P9.2	85	106		
	P9.3	86	107		
	PA.0	79	100	I/O	
	PA.1	80	101		
	PA.2	81	102		
	PA.3	82	103		
	PB.0/INT0/ TM0CAP/ TM0OVF	75	96	I/O	
	PB.1/INT0/ TM1CAP/ TM1OVF	76	97		
	PB.2/INT0/ T02CK	77	98		
	PB.3/INT0/ T13CK	78	99		
	PC.0/INT1/ RXD	66	92	I/O	
	PC.1/INT1/ TXC	67	93		
	PC.2/INT1/ RXC	68	94		
	PC.3/INT1/ TXD	69	95		
	PE.0/SIN	62	88	I/O	
	PE.1/SOUT	63	89		
	PE.2/SCLK	64	90		
	PE.3/INT2	65	91		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
LCD	COM1	92	113	O	LCD common signal output pins
	COM2	93	114		
	COM3	94	115		
	COM4	95	116		
	COM5	96	117		
	COM6	97	118		
	COM7	98	119		
	COM8	99	120		
	COM9	27	57		
	COM10	28	58		
	COM11	29	59		
	COM12	30	60		
	COM13	31	61		
	COM14	32	62		
	COM15	33	63		
	COM16	34	64		
	SEG0	100	121	O	LCD segment signal output pins
	SEG1	101	122		
	SEG2	102	123		
	SEG3	103	124		
	SEG4	104	125		
	SEG5	105	126		
	SEG6	106	127		
	SEG7	107	128		
	SEG8	111	1		
	SEG9	112	2		
	SEG10	113	3		
	SEG11	114	4		
	SEG12	115	5		
	SEG13	116	6		
	SEG14	117	7		
	SEG15	118	8		
	SEG16	119	9		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
LCD	SEG17	120	10	O	LCD segment signal output pins
	SEG18	121	11		
	SEG19	122	12		
	SEG20	123	13		
	SEG21	124	14		
	SEG22	125	15		
	SEG23	126	16		
	SEG24	127	17		
	SEG25	128	18		
	SEG26	129	19		
	SEG27	130	20		
	SEG28	131	21		
	SEG29	132	22		
	SEG30	133	23		
	SEG31	134	24		
	SEG32	135	25		
	SEG33	136	26		
	SEG34	137	27		
	SEG35	138	28		
	SEG36	139	29		
	SEG37	140	30		
	SEG38	141	31		
	SEG39	142	32		
	SEG40	3	33		
	SEG41	4	34		
	SEG42	5	35		
	SEG43	6	36		
	SEG44	7	37		
	SEG45	8	38		
	SEG46	9	39		
	SEG47	10	40		
	SEG48	11	41		
	SEG49	12	42		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
LCD	SEG50	13	43	O	LCD segment signal output pins
	SEG51	14	44		
	SEG52	15	45		
	SEG53	16	46		
	SEG54	17	47		
	SEG55	18	48		
	SEG56	19	49		
	SEG57	20	50		
	SEG58	21	51		
	SEG59	22	52		
	SEG60	23	53		
	SEG61	24	54		
	SEG62	25	55		
	SEG63	26	56		

Table 2 shows the secondary functions of each pin of the ML63193.

Table 2 Pin Descriptions (Secondary Functions)

Function	Symbol	Pin No.	Pad No.	Type	Description
External Interrupt	PB.0/INT0	75	96	I	External 0 interrupt input pins The change of input signal level causes an interrupt to occur. The Port B Interrupt Enable register (PBIE) enables or disables an interrupt for each bit.
	PB.1/INT0	76	97		
	PB.2/INT0	77	98		
	PB.3/INT0	78	99		
	PC.0/INT1	66	92	I	External 1 interrupt input pins The change of input signal level causes an interrupt to occur. The Port C Interrupt Enable register (PCIE) enables or disables an interrupt for each bit.
	PC.1/INT1	67	93		
	PC.2/INT1	68	94		
	PC.3/INT1	69	95		
	PE.3/INT2	65	91	I	External 2 interrupt input pin The change of input signal level causes an interrupt to occur.
	P0.0/INT5	87	108	I	External 5 interrupt input pins The change of input signal level causes an interrupt to occur. The Port 0 Interrupt Enable register (P0IE) enables or disables an interrupt for each bit.
	P0.1/INT5	88	109		
	P0.2/INT5	89	110		
	P0.3/INT5	90	111		
Capture	PB.0/ TM0CAP	75	96	I	Timer 0 capture input pin
	PB.1/ TM1CAP	76	97	I	Timer 1 capture input pin
Timer	PB.0/ TM0OVF	75	96	O	Timer 0 overflow flag output pin
	PB.1/ TM1OVF	76	97	O	Timer 1 overflow flag output pin
	PB.2/T02CK	77	98	I	External clock input pin for timer 0 and timer 2.
	PB.3/T13CK	78	99	I	External clock input pin for timer 1 and timer 3

Table 2 Pin Descriptions (Secondary Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
Serial Port	PC.0/RXD	66	92	I	Serial port receive data input pin
	PC.1/TXC	67	93	I/O	Sync serial port clock input-output pin Transmit clock output when this device is used as a master processor. Transmit clock input when this device is used as a slave processor.
	PC.2/RXC	68	94	I/O	Sync serial port clock input-output pin Receive clock output when this device is used as a master processor. Receive clock input when this device is used as a slave processor.
	PC.3/TXD	69	95	O	Serial port transmit data output pin
Shift Register	PE.0/SIN	62	88	I	Shift register receive data input pin
	PE.1/SOUT	63	89	O	Shift register transmit data output pin
	PE.2/SCLK	64	90	I/O	Shift register clock input-output pin. Clock output when this device is used as a master processor. Clock input when this device is used as a slave processor.

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD1}	Ta = 25°C	–0.3 to +1.6	V
Power supply voltage 2	V_{DD2}	Ta = 25°C	–0.3 to +2.9	V
Power supply voltage 3	V_{DD3}	Ta = 25°C	–0.3 to +4.2	V
Power supply voltage 4	V_{DD4}	Ta = 25°C	–0.3 to +5.5	V
Power supply voltage 5	V_{DD5}	Ta = 25°C	–0.3 to +6.8	V
Power supply voltage 6	V_{DD}	Ta = 25°C	–0.3 to +6.0	V
Power supply voltage 7	V_{DDI}	Ta = 25°C	–0.3 to +6.0	V
Power supply voltage 8	V_{DDH}	Ta = 25°C	–0.3 to +6.0	V
Input voltage 1	V_{IN1}	V_{DD} input, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Input voltage 2	V_{IN2}	V_{DDI} input, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output voltage 1	V_{OUT1}	V_{DD1} output, Ta = 25°C	–0.3 to V_{DD1} + 0.3	V
Output voltage 2	V_{OUT2}	V_{DD2} output, Ta = 25°C	–0.3 to V_{DD2} + 0.3	V
Output voltage 3	V_{OUT3}	V_{DD3} output, Ta = 25°C	–0.3 to V_{DD3} + 0.3	V
Output voltage 4	V_{OUT4}	V_{DD4} output, Ta = 25°C	–0.3 to V_{DD4} + 0.3	V
Output voltage 5	V_{OUT5}	V_{DD5} output, Ta = 25°C	–0.3 to V_{DD5} + 0.3	V
Output voltage 6	V_{OUT6}	V_{DD} output, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Output voltage 7	V_{OUT7}	V_{DDI} output, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output voltage 8	V_{OUT8}	V_{DDH} output, Ta = 25°C	–0.3 to V_{DDH} + 0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

- When backup is used

(V_{SS} = 0 V)

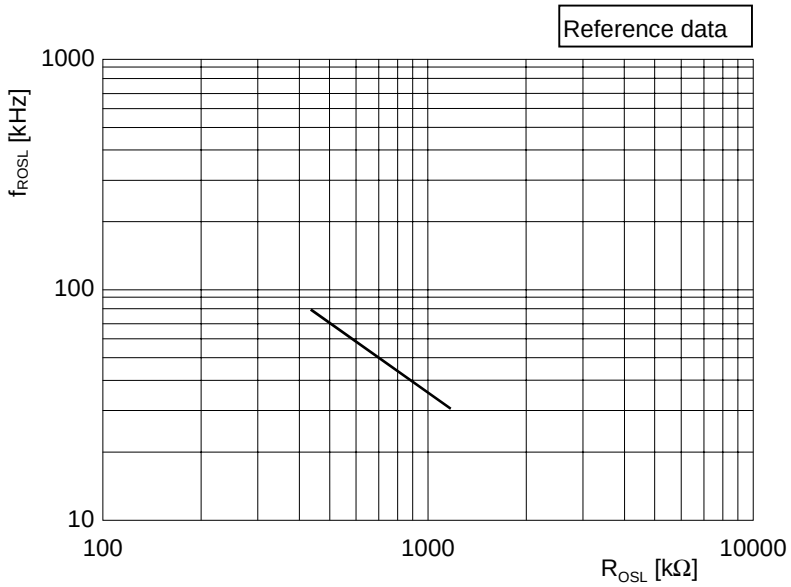
Parameter	Symbol	Condition		Rating	Unit
Operating Temperature	T_{op}	—		–20 to +70	°C
Operating Voltage	V_{DD}	—		0.9 to 2.7	V
	V_{DDI}	—		0.9 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	C_G = 5 to 25 pF		32.768 to 76.8	kHz
Low-speed RC Oscillation Frequency	f_{ROSL}	R_{OSL} = 1.0 MΩ		36 ± 30%	kHz
		R_{OSL} = 1.1 MΩ		33 ± 30%	
		R_{OSL} = 1.2 MΩ		30 ± 30%	
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 0.9 to 1.2 V		Not applied	Hz
		V_{DD} = 1.2 to 2.7 V		300 k to 500 k	
		V_{DD} = 1.5 to 2.7 V		200 k to 1 M	
High-speed RC Oscillation Frequency	f_{ROSH}	V_{DD} = 0.9 to 1.2 V		Not applied	Hz
		V_{DD} = 1.2 to 2.7 V	R_{OSH} = 400 kΩ	200 k ± 30%	
			R_{OSH} = 100 kΩ	700 k ± 30%	
			R_{OSH} = 75 kΩ	1 M ± 30%	

- When backup is not used

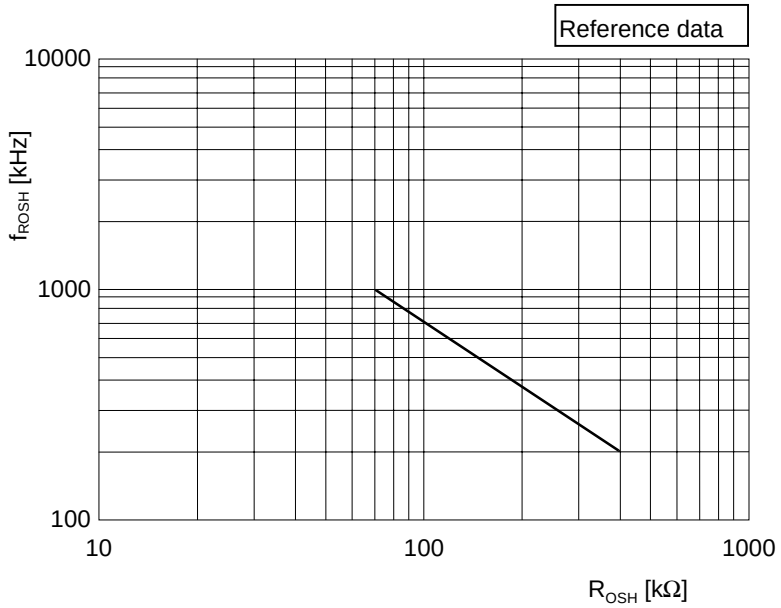
(V_{SS} = 0 V)

Parameter	Symbol	Condition		Rating	Unit
Operating Temperature	T_{op}	—		–20 to +70	°C
Operating Voltage	V_{DD}	—		1.8 to 5.5	V
	V_{DDI}	—		1.8 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	C_G = 5 to 25 pF		32.768 to 76.8	kHz
Low-speed RC Oscillation Frequency	f_{ROSL}	R_{OSL} = 1.0 MΩ		36 ± 30%	kHz
		R_{OSL} = 1.1 MΩ		33 ± 30%	
		R_{OSL} = 1.2 MΩ		30 ± 30%	
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 1.8 to 5.5 V		200 k to 2 M	Hz
High-speed RC Oscillation Frequency	f_{ROSH}	V_{DD} = 1.8 to 3.6 V	R_{OSH} = 100 kΩ	700 k ± 30%	Hz
			R_{OSH} = 75 kΩ	1 M ± 30%	
			R_{OSH} = 51 kΩ	1.35 M ± 30%	
		V_{DD} = 1.8 to 3.5 V, R_{OSH} = 30 kΩ		2 M ± 30%	

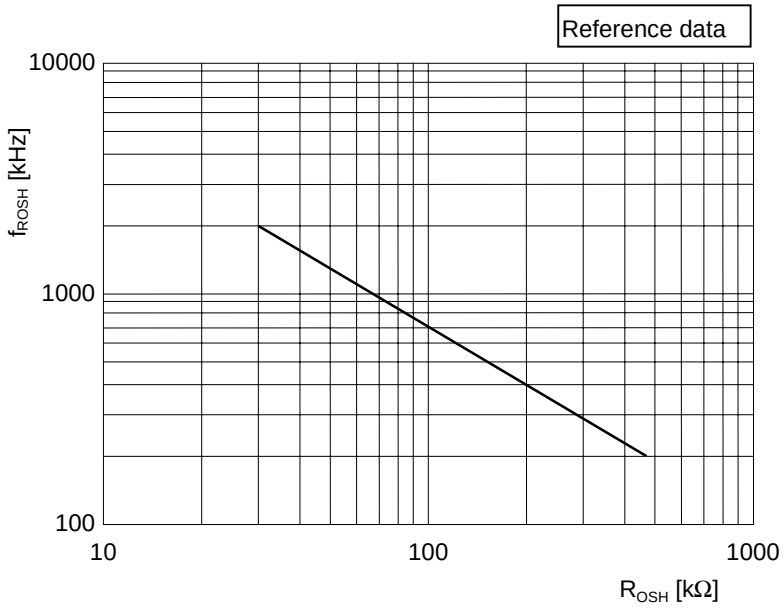
- Typical characteristics of low-speed RC oscillation
  When backup is used/backup is not used (V_{DD} = V_{DDI} = 1.5 V/V_{DD} = V_{DDI} = 3.0 V)



- Typical characteristics of high-speed RC oscillation
  When backup is used (V_{DD} = V_{DDI} = 1.5 V)



- Typical characteristics of high-speed RC oscillation
  When backup is not used (V_{DD} = V_{DDI} = 3.0 V)



ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD} = V_{DDI} = 0.9 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DD2} Voltage	V_{DD2}	1/5 bias, 1/4 bias (Ta = 25°C)	1.7	1.8	1.9	V	1
V_{DD2} Voltage Temperature Deviation	ΔV_{DD2}	—	—	–4.0	—	mV/°C	
V_{DD1} Voltage	V_{DD1}	1/5 bias, 1/4 bias	Typ.–0.1	1/2 × V_{DD2}	Typ.+0.1	V	
V_{DD3} Voltage	V_{DD3}	1/5 bias	Typ.–0.3	2/3 × V_{DD2}	Typ.+0.3		
		1/4 bias (connect V_{DD3} and V_{DD2})	Typ.–0.2	V_{DD2}	Typ.+0.2		
V_{DD4} Voltage	V_{DD4}	1/5 bias	Typ.–0.4	2 × V_{DD2}	Typ.+0.4		
		1/4 bias	Typ.–0.3	3/2 × V_{DD2}	Typ.+0.3		
V_{DD5} Voltage	V_{DD5}	1/5 bias	Typ.–0.5	5/2 × V_{DD2}	Typ.+0.5		
		1/4 bias	Typ.–0.4	2 × V_{DD2}	Typ.+0.4		
V_{DDH} Voltage (Backup used)	V_{DDH}	High-speed clock oscillation stopped V_{DD} = 1.5 V	2.8	—	3.0		
		High-speed clock oscillation (Ceramic oscillation, 1 MHz) V_{DD} = 1.5 V	2.0	—	2.7		
V_{DDL} Voltage	V_{DDL}	High-speed clock oscillation stopped	1.0	1.5	2.0		
		High-speed clock oscillation (Ceramic oscillation, 1 MHz) V_{DD} = 1.2 to 5.5 V	1.2	—	5.5		

Note: 1. "V_{DD2}" changes in the range from 1.8 to 2.4 V according to the valve of Display Contrast register (DSPCNT)

DC Characteristics (2)

(V_{DD} = V_{DDI} = 0.9 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	1.2	—	—	V	1
Crystal Oscillation Hold Voltage	V_{HOLD}	Backup used	0.9	—	—	V	
		Backup not used	1.7	—	—	V	
Crystal Oscillation Stop Detect Time	T_{STOP}	—	0.1	—	5.0	ms	
External RC Oscillator Capacitance	C_G	—	5	—	25	pF	
Internal RC Oscillator Capacitance	C_D	—	20	25	30	pF	
External Ceramic Oscillator Capacitance	C_{L0}, C_{L1}	CSA2.00 MG (Murata MFG.–make) used V_{DD} = 3.0 V	—	30	—	pF	
Internal RC Oscillator Capacitance	C_{OS}	—	8	12	16	pF	
POR Voltage	V_{POR1}	V_{DD} = 1.5 V	0	—	0.4	V	
		V_{DD} = 3.0 V	0	—	0.7	V	
Non-POR Voltage	V_{POR2}	V_{DD} = 1.5 V	1.2	—	1.5	V	
		V_{DD} = 3.0 V	2	—	3	V	
BLD Judgment Voltage	V_{BLDC}	LD1 = 1, LD0 = 1, Ta = 25°C	2.30	2.40	2.50	V	
		LD1 = 1, LD0 = 0, Ta = 25°C	1.70	1.80	1.90	V	
		LD1 = 0, LD0 = 1, Ta = 25°C	1.10	1.20	1.30	V	
		LD1 = 0, LD0 = 0, Ta = 25°C	0.95	1.05	1.15	V	
BLD Judgment Voltage Temperature Deviation	ΔV_{BLDC}	V_{BLDC} = 2.40 V (LD1 = 1, LD0 = 1)	—	–3.5	—	mV/°C	
		V_{BLDC} = 1.80 V (LD1 = 1, LD0 = 0)	—	–2.3	—	mV/°C	
		V_{BLDC} = 1.20 V (LD1 = 0, LD0 = 1)	—	–1.6	—	mV/°C	
		V_{BLDC} = 1.05 V (LD1 = 0, LD0 = 0)	—	–1.2	—	mV/°C	

Notes: 1. "T_{STOP}" indicates that if the crystal oscillator stops over the value of T_{STOP}, the system reset occurs.
2. "POR" denotes Power On Reset. (When not using RESET sampling circuit)
3. "V_{POR1}" indicates that POR occurs when V_{DD} falls from V_{DD} to V_{POR1} and again rises up to V_{DD}.
4. "V_{POR2}" indicates that POR dose not occur when V_{DD} falls from V_{DD} V_{POR2} and again rises up to V_{DD}.

DC Characteristics (3)

- When backup is used

(Low-speed clock = Crystal oscillation (32.768 kHz), $V_{DD} = V_{DDI} = 1.5$ V, $V_{SS} = 0$ V,
Display contrast register (DSPCNT) = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	5.6	6.5	μA	1
			Ta = –20 to +70°C	—	5.6	15.0		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	4.5	5.0		
			Ta = –20 to +70°C	—	4.5	13.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	23	26		
			Ta = –20 to +70°C	—	23	30		
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation. (approx. 700 kHz RC oscillation, $R_{OSH} = 100$ kΩ)		—	1100	1500		
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation. (1 MHz Ceramic oscillation)		—	950	1200		

DC Characteristics (4)

- When backup is not used

(Low-speed clock = Crystal oscillation (32.768 kHz), $V_{DD} = V_{DDI} = 3.0$ V, $V_{SS} = 0$ V,
Display contrast register (DSPCNT) = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	2.6	3.5	μA	1
			Ta = –20 to +70°C	—	2.6	7.0		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	2.0	2.8		
			Ta = –20 to +70°C	—	2.0	6.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	12	13		
			Ta = –20 to +70°C	—	12	16		
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation. (approx. 700 kHz RC oscillation, $R_{OSH} = 100$ kΩ)		—	1000	1200		
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation. (2 MHz Ceramic oscillation)		—	1100	1300		

DC Characteristics (5)

($V_{DD} = V_{DDI} = V_{DDH} = 3.0$ V, $V_{DD1} = 1.1$ V, $V_{DD2} = 2.2$ V, $V_{DD3} = 3.3$ V, $V_{DD4} = 4.4$ V, $V_{DD5} = 5.5$ V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	I_{OH1}	$V_{OH1} = V_{DDI} - 0.5$ V	$V_{DDI} = 1.5$ V	–2.5	–1.4	–0.4	mA	2
			$V_{DDI} = 3.0$ V	–6.0	–3.5	–1.0		
			$V_{DDI} = 5.0$ V	–8.5	–5.0	–1.5		
	I_{OL1}	$V_{OL1} = 0.5$ V	$V_{DDI} = 1.5$ V	0.4	1.4	2.5		
			$V_{DDI} = 3.0$ V	1.0	3.0	6.0		
			$V_{DDI} = 5.0$ V	1.5	3.7	8.5		
Output Current 2 (MD, MDB)	I_{OH2}	$V_{OH2} = V_{DD} - 0.7$ V	$V_{DD} = 1.5$ V	–4.0	–2.0	–0.5		
			$V_{DD} = 3.0$ V	–11.0	–6.0	–2.0		
			$V_{DD} = V_{DDH} = 5.0$ V	–14.0	–9.0	–4.0		
	I_{OL2}	$V_{OL2} = 0.7$ V	$V_{DD} = 1.5$ V	0.5	2.0	4.0		
			$V_{DD} = 3.0$ V	2.0	5.5	11.0		
			$V_{DD} = V_{DDH} = 5.0$ V	4.0	7.0	14.0		
Output Current 3 (SEG0 to SEG63) (COM1 to COM16)	I_{OH3}	$V_{OH3} = V_{DD5} - 0.2$ V (V_{DD5} level)		–	—	–4	µA	
	I_{OHM3}	$V_{OHM3} = V_{DD4} + 0.2$ V (V_{DD4} level)		4	—	—		
	I_{OHM3S}	$V_{OHM3S} = V_{DD4} - 0.2$ V (V_{DD4} level)		—	—	–4		
	I_{OMH3}	$V_{OMH3} = V_{DD3} + 0.2$ V (V_{DD3} level)		4	—	—		
	I_{OMH3S}	$V_{OMH3S} = V_{DD3} - 0.2$ V (V_{DD3} level)		—	—	–4		
	I_{OML3}	$V_{OML3} = V_{DD2} + 0.2$ V (V_{DD2} level)		4	—	—		
	I_{OML3S}	$V_{OML3S} = V_{DD2} - 0.2$ V (V_{DD2} level)		—	—	–4		
	I_{OLM3}	$V_{OLM3} = V_{DD1} + 0.2$ V (V_{DD1} level)		4	—	—		
	I_{OLM3S}	$V_{OLM3S} = V_{DD1} - 0.2$ V (V_{DD1} level)		—	—	–4		
	I_{OL3}	$V_{OL3} = V_{SS} + 0.2$ V (V_{SS} level)		4	—	—		
Output Current 4 (OSC1)	I_{OH4R}	$V_{OH4R} = V_{DDH} - 0.5$ V (RC oscillation)	$V_{DD} = V_{DDH} = 3.0$ V	–2.5	–1.3	–0.25	mA	
			$V_{DD} = V_{DDH} = 5.0$ V	–3.5	–1.7	–0.5		
	I_{OL4R}	$V_{OL4R} = 0.5$ V (RC oscillation)	$V_{DD} = V_{DDH} = 3.0$ V	0.25	1.5	2.5		
			$V_{DD} = V_{DDH} = 5.0$ V	0.5	1.8	3.5		
	I_{OH4C}	$V_{OH4C} = V_{DDH} - 0.5$ V (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0$ V	–500	–250	–100	µA	
			$V_{DD} = V_{DDH} = 5.0$ V	–800	–350	–200		
	I_{OL4C}	$V_{OL4c} = 0.5$ V (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0$ V	200	500	800		
			$V_{DD} = V_{DDH} = 5.0$ V	400	700	1000		
Output Leakage Current (P2.0 to P2.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	I_{OOH}	$V_{OH} = V_{DDI}$		—	—	0.3		
	I_{OOL}	$V_{OL} = V_{SS}$		–0.3	—	—		

DC Characteristics (6)

($V_{DD} = V_{DDI} = V_{DDH}$ = 3.0 V, V_{DD1} = 1.1 V, V_{DD2} = 2.2 V, V_{DD3} = 3.3 V, V_{DD4} = 4.4 V, V_{DD5} = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

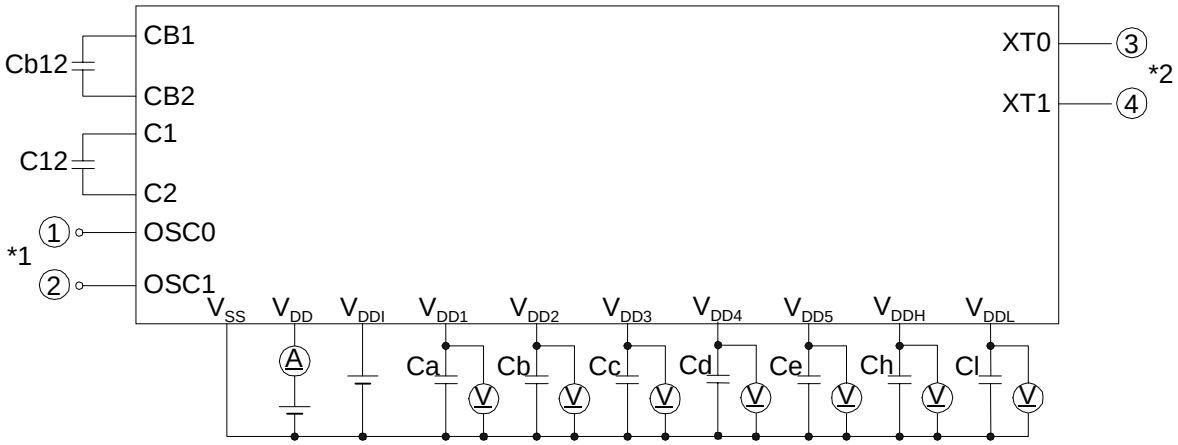
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	I_{IH1}	$V_{IH1} = V_{DDI}$ (when pulled down)	V_{DDI} = 1.5 V	2	20	45	µA	3
			V_{DDI} = 3.0 V	30	120	260		
			V_{DDI} = 5.0 V	70	350	650		
	I_{IL1}	$V_{IL1} = V_{SS}$ (when pulled up)	V_{DDI} = 1.5 V	–45	–20	–2		
			V_{DDI} = 3.0 V	–260	–120	–30		
			V_{DDI} = 5.0 V	–650	–350	–70		
	I_{IH1Z}	$V_{IH1} = V_{DDI}$ (in a high impedance state)		0	—	1		
	I_{IL1Z}	$V_{IL1} = V_{SS}$ (in a high impedance state)		–1	—	0		
Input Current 2 (OSC0)	I_{IL2}	$V_{IL2} = V_{SS}$ (when pulled up)	$V_{DD} = V_{DDH}$ = 3.0 V	–350	–170	–30		
			$V_{DD} = V_{DDH}$ = 5.0 V	–750	–450	–200		
	I_{IH2R}	$V_{IH2R} = V_{DDH}$ (RC oscillation)		0	—	1		
	I_{IL2R}	$V_{IL2R} = V_{SS}$ (RC oscillation)		–1	—	0		
	I_{IH2C}	$V_{IH2C} = V_{DDH}$ (ceramic oscillation)	$V_{DD} = V_{DDH}$ = 3.0 V	0.5	1.8	4.0		
			$V_{DD} = V_{DDH}$ = 5.0 V	3	6	10		
	I_{IL2C}	$V_{IL2C} = V_{SS}$ (ceramic oscillation)	$V_{DD} = V_{DDH}$ = 3.0 V	–4.0	–1.8	–0.5		
			$V_{DD} = V_{DDH}$ = 5.0 V	–10	–6	–3		
Input Current 3 (RESET)	I_{IH3}	$V_{IH3} = V_{DD}$	V_{DD} = 1.5 V	10	180	350		
			V_{DD} = 3.0 V	150	1100	2400		
			$V_{DD} = V_{DDH}$ = 5.0 V	0.5	2.7	5.0	mA	
	I_{IL3}	$V_{IL3} = V_{SS}$		–1	—	0	µA	
Input Current 4 (TST1, TST2)	I_{IH4}	$V_{IH4} = V_{DD}$	V_{DD} = 1.5 V	50	750	1500		
			V_{DD} = 3.0 V	0.5	3.0	5.5	mA	
			$V_{DD} = V_{DDH}$ = 5.0 V	2.0	6.5	11.0		
	I_{IL4}	$V_{IL4} = V_{SS}$		–1	—	0	µA	

DC Characteristics (7)

(V_{DD} = V_{DDI} = V_{DDH} = 3.0 V, V_{DD1} = 1.1 V, V_{DD2} = 2.2 V, V_{DD3} = 3.3 V, V_{DD4} = 4.4 V, V_{DD5} = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

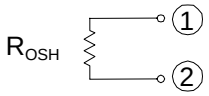
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	V_{IH1}	V_{DDI} = 1.5 V	1.2	—	1.5	V	4
		V_{DDI} = 3.0 V	2.4	—	3.0		
		V_{DDI} = 5.0 V	4.0	—	5.0		
	V_{IL1}	V_{DDI} = 1.5 V	0	—	0.3		
		V_{DDI} = 3.0 V	0	—	0.6		
		V_{DDI} = 5.0 V	0	—	1		
Input Voltage 2 (OSC0)	V_{IH2}	V_{DD} = V_{DDH} = 3.0 V	2.4	—	3.0		
		V_{DD} = V_{DDH} = 5.0 V	4.0	—	5.0		
	V_{IL2}	V_{DD} = V_{DDH} = 3.0 V	0	—	0.6		
		V_{DD} = V_{DDH} = 5.0 V	0	—	1		
Input Voltage 3 (RESET), (TST1), (TST2)	V_{IH3}	V_{DD} = 1.5 V	1.35	—	1.5		
		V_{DD} = 3.0 V	2.4	—	3.0		
		V_{DD} = 5.0 V	4.0	—	5.0		
	V_{IL3}	V_{DD} = 1.5 V	0	—	0.15		
		V_{DD} = 3.0 V	0	—	0.6		
		V_{DD} = 5.0 V	0	—	1		
Hysteresis Width 1 (P0.0 to P0.3) (P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	ΔV_{T1}	V_{DDI} = 1.5 V	0.05	0.1	0.3		
		V_{DDI} = 3.0 V	0.2	0.5	1.0		
		V_{DDI} = 5.0 V	0.25	1.0	1.5		
Hysteresis Width 2 (RESET), (TST1), (TST2)	ΔV_{T2}	V_{DD} = 1.5 V	0.05	0.1	0.3		
		V_{DD} = 3.0 V	0.2	0.5	1.0		
		V_{DD} = 5.0 V	0.25	1.0	1.5		
Input Pin Capacitance (P0.0 to P0.3) (P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PC.0 to PC.3) (PE.0 to PE.3)	C_{IN}	—	—	—	5	pF	1

Measuring circuit 1

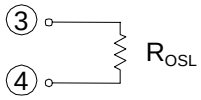


C_a, C_b, C_c, C_d, C_e, C_l, C_{12}	:	0.1 µF
C_h, C_{b12}	:	1 µF
C_G	:	15 pF
C_{L0}	:	30 pF
C_{L1}	:	30 pF
Ceramic Resonator	:	CSA2.00MG (2 MHz) CSB1000J (1 MHz) (Murata MFG.-make)

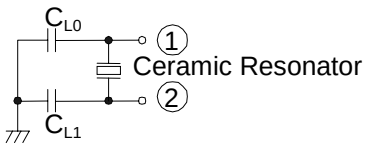
*1 RC Oscillator



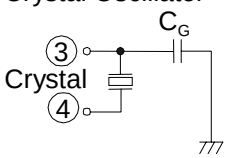
*2 RC Oscillator



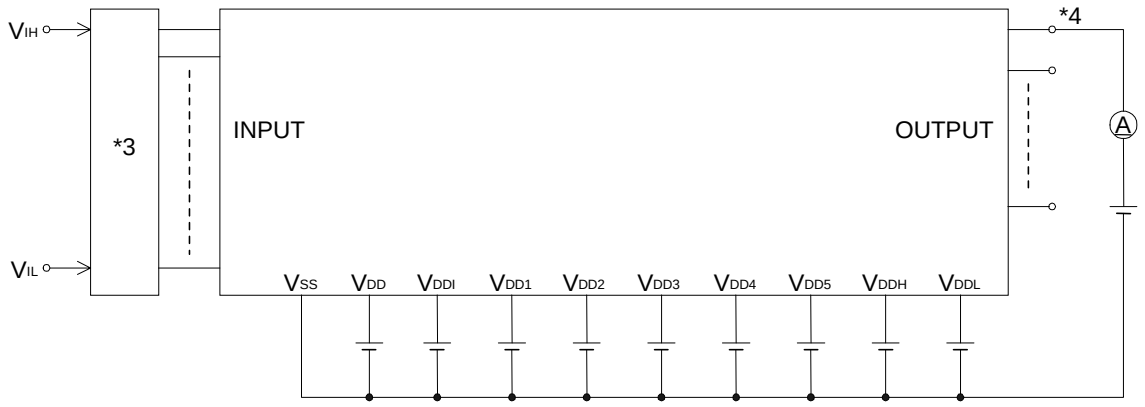
Ceramic Oscillator



Crystal Oscillator

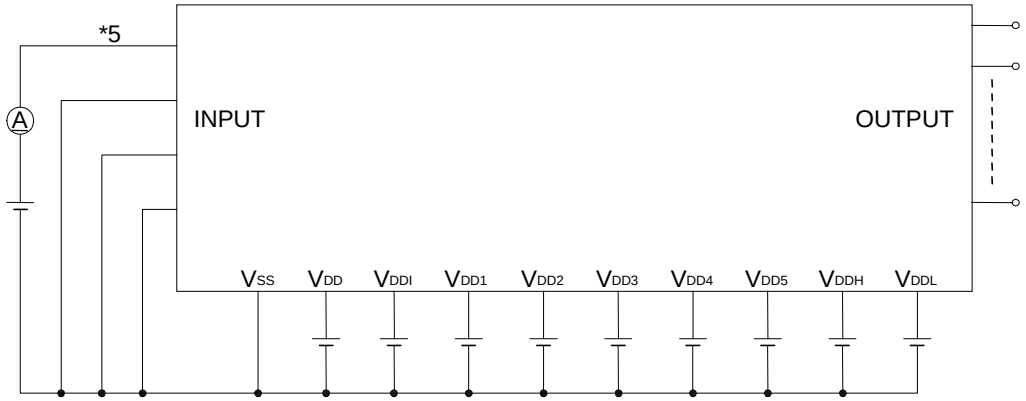


Measuring circuit 2

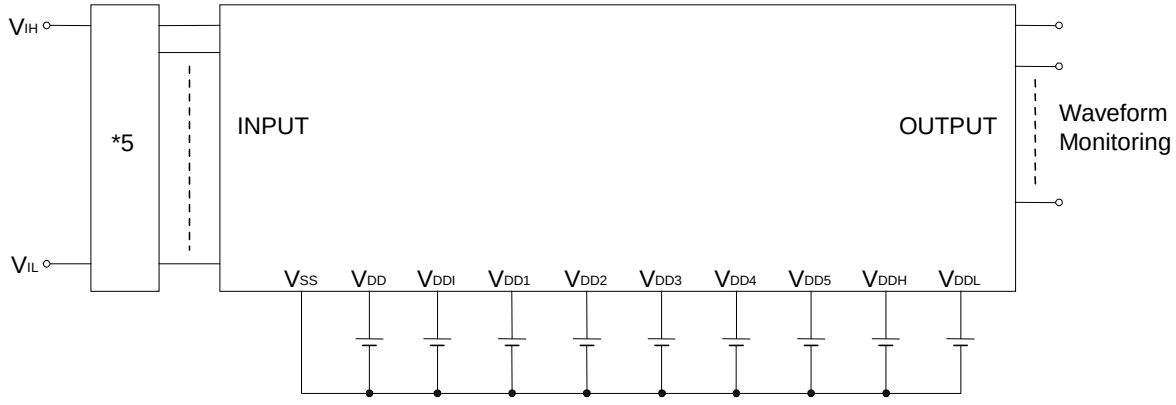


*3 Input logic circuit to determine the specified measuring conditions.
*4 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



*5 Measured at the specified input pins.

AC Characteristics (Serial Interface, Serial Port)

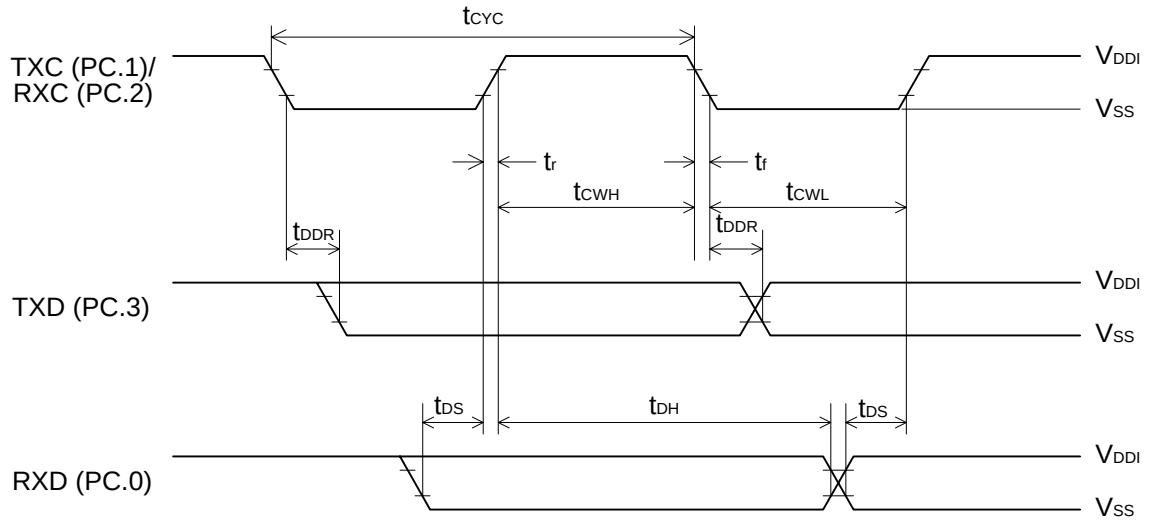
(1) Synchronous Communication

(V_{DD} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1.0	µs
TXC/RXC Input Rise Time	t_r	—	—	—	1.0	
TXC/RXC Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	
TXC/RXC Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	
TXC/RXC Input Cycle Time	t_{CYC}	—	2.0	—	—	
TXC/RXC Output Cycle Time	$t_{CYC\ (O)}$	CPU is in operating at 32.768 kHz	—	30.5	—	
TXD Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	
RXD Input Setup Time	t_{DS}	—	0.5	—	—	
RXD Input Hold Time	t_{DH}	—	0.8	—	—	

Synchronous communication timing

("H" level = 4.0 V, "L" level = 1.0 V)



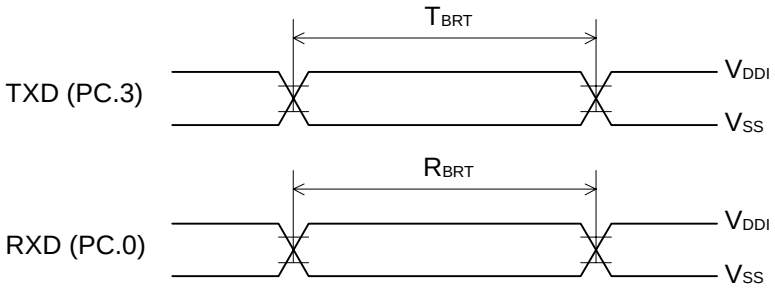
(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	T_{BRT}	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	R_{BRT}	$R_{BRT} \times 1.03$	

f_{BRT}: Baud rates (1200, 2400, 4800, 9600 bps)

UART communication timing

("H" level = 4.0 V, "L" level = 1.0 V)



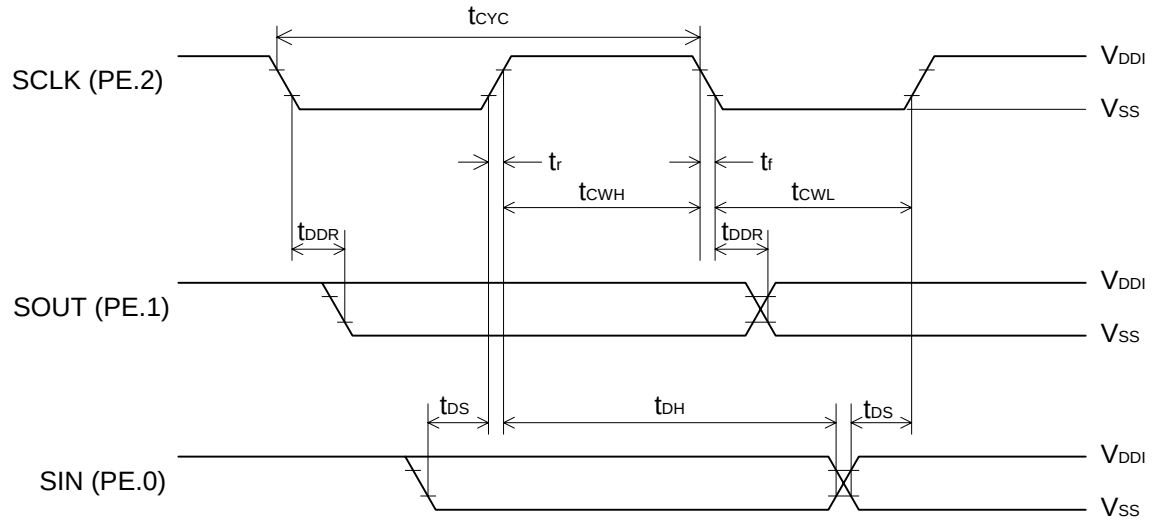
AC Characteristics (Serial Interface, Shift Register)

(V_{DD} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{DDI} = 5.0 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

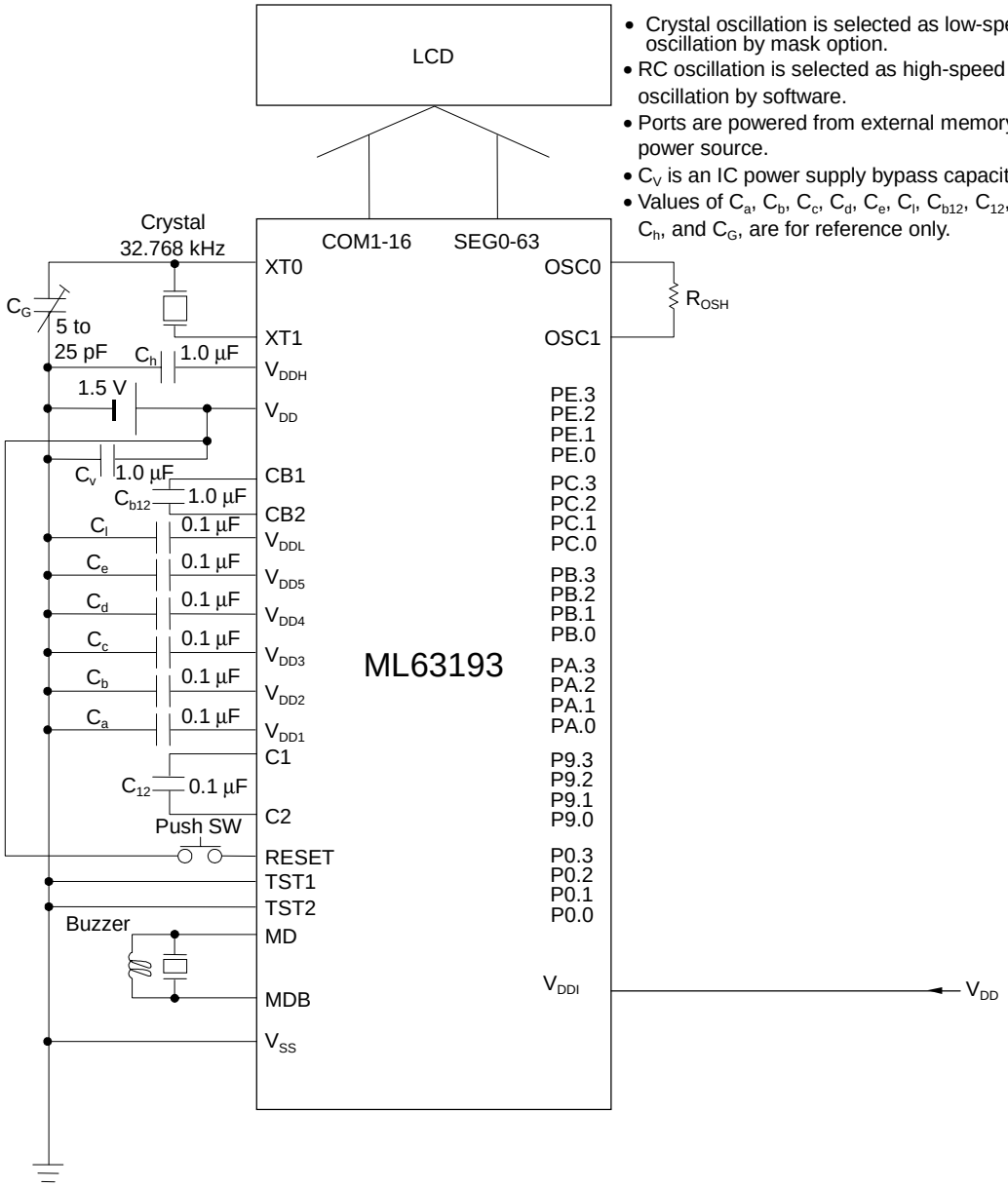
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Input Fall Time	t_f	—	—	—	1.0	µs
SCLK Input Rise Time	t_r	—	—	—	1.0	
SCLK Input “L” Level Pulse Width	t_{CWL}	—	0.8	—	—	
SCLK Input “H” Level Pulse Width	t_{CWH}	—	0.8	—	—	
SCLK Input Cycle Time	t_{CYC}		1.8	—	—	
SCLK Output Cycle Time	$t_{CYC1(O)}$	CPU is in operating at 32.768 kHz	—	30.5	—	
	$t_{CYC2(O)}$	CPU is in operating at 2 MHz V_{DD} = V_{DDH} = 1.8 to 3.5 V	—	0.5	—	
SOUT Output Delay Time	t_{DDR}	C_L = 10 pF	—	—	0.4	
SIN Input Setup Time	t_{DS}	—	0.5	—	—	
SIN Input Hold Time	t_{DH}	—	0.8	—	—	

AC characteristics timing

(“H” level = 4.0 V, “L” level = 1.0 V)

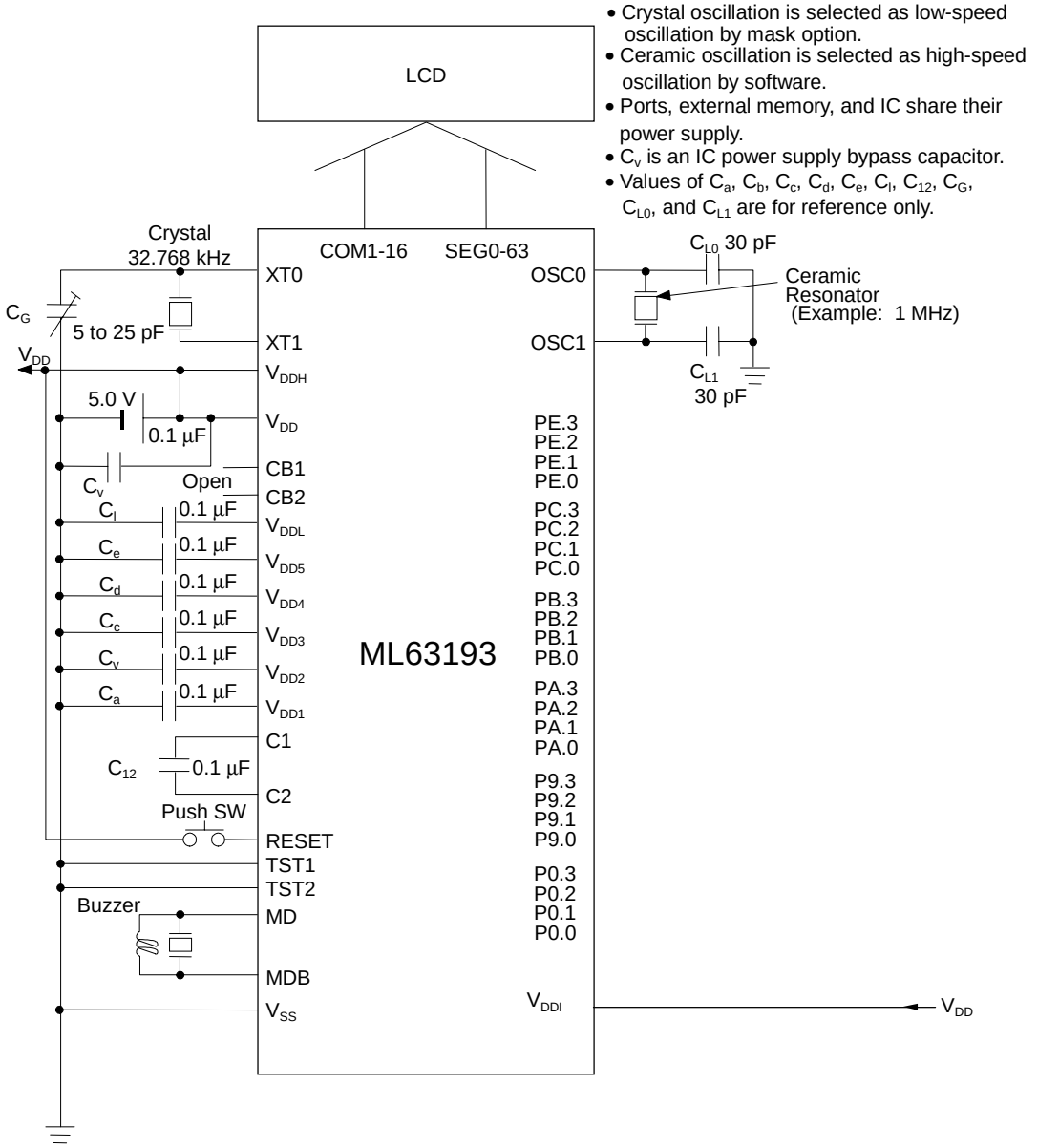


APPLICATION CIRCUITS



Note: V_{DDI} is the power supply pin for the input-output ports.
Be sure to connect the V_{DDI} pin either to the positive power supply pin (V_{DD}) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with Power Supply Backup



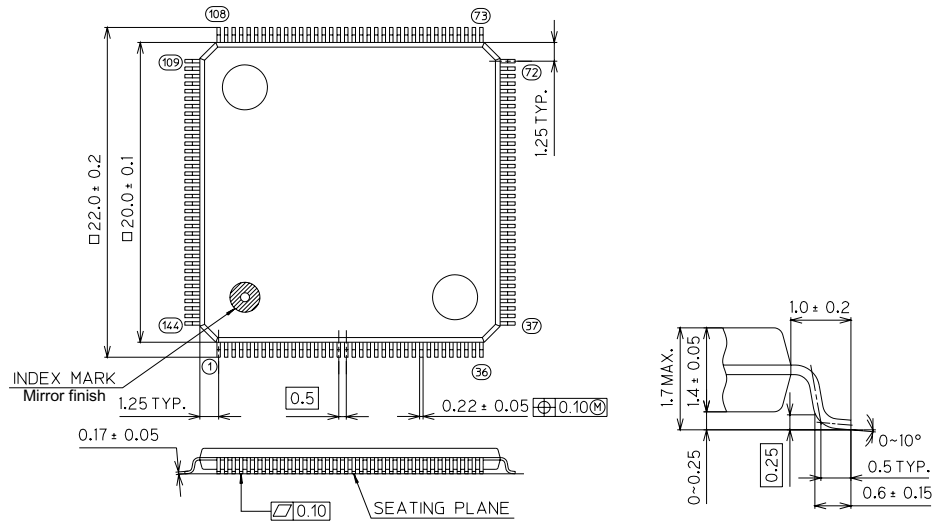
Note: V_{DDI} is the power supply pin for the input-output ports.
Be sure to connect the V_{DDI} pin either to the positive power supply pin (V_{DD}) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with No Power Supply Backup

PACKAGE DIMENSIONS

(Unit : mm)

LQFP144-P-2020-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.37 TYP.
Rev. No./Last Revised	5/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

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