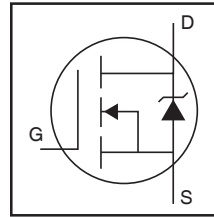


AUIRF1018ES

HEXFET® Power MOSFET

Features

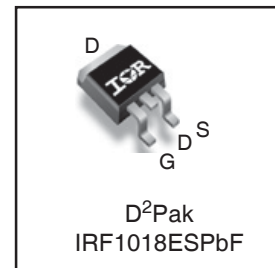
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}		60V
$R_{DS(on)}$	typ.	7.1mΩ
	max.	8.4mΩ
I_D		79A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	79	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	56	
I_{DM}	Pulsed Drain Current ①	315	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	110	W
	Linear Derating Factor	0.76	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally limited) ②	88	mJ
I_{AR}	Avalanche Current ①	47	A
E_{AR}	Repetitive Avalanche Energy ④	11	mJ
dv/dt	Peak Diode Recovery ③	21	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	1.32	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D ² Pak ⑦	—	40	

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*Qualification standards can be found at <http://www.irf.com/>

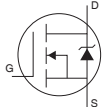
Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.073	—	V/°C	Reference to 25°C, I _D = 5mA ^①
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	7.1	8.4	mΩ	V _{GS} = 10V, I _D = 47A ^②
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 100μA
gfs	Forward Transconductance	110	—	—	S	V _{DS} = 50V, I _D = 47A
R _{G(int)}	Internal Gate Resistance	—	0.73	—	Ω	
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 60V, V _{GS} = 0V
		—	—	250		V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

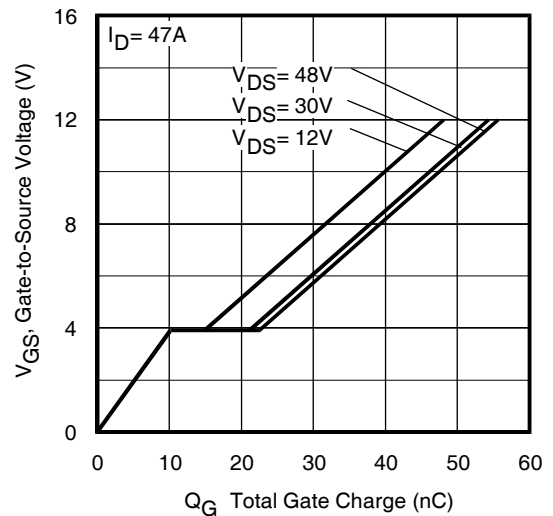
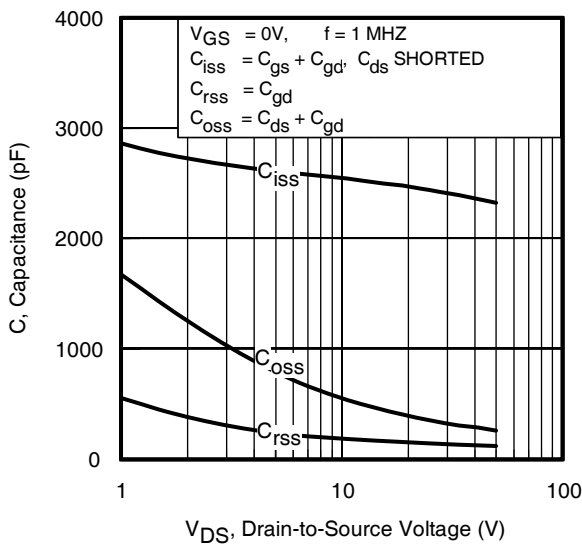
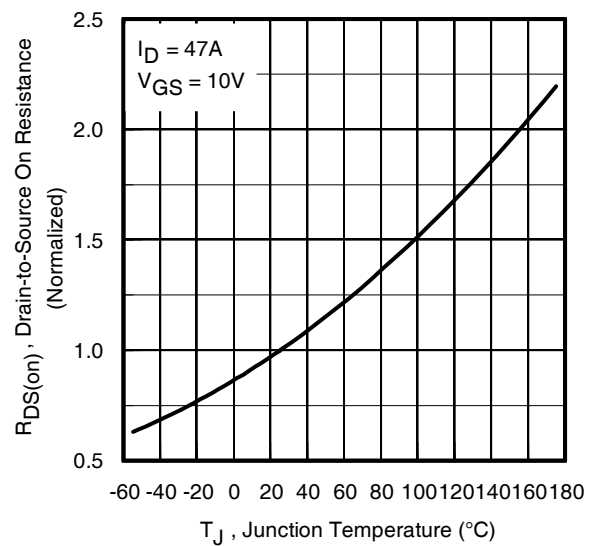
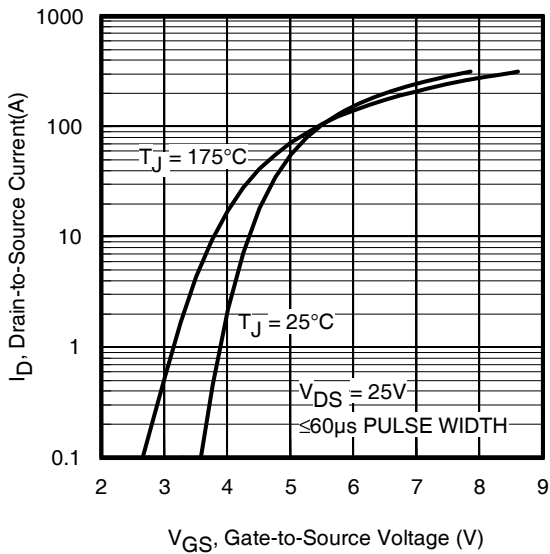
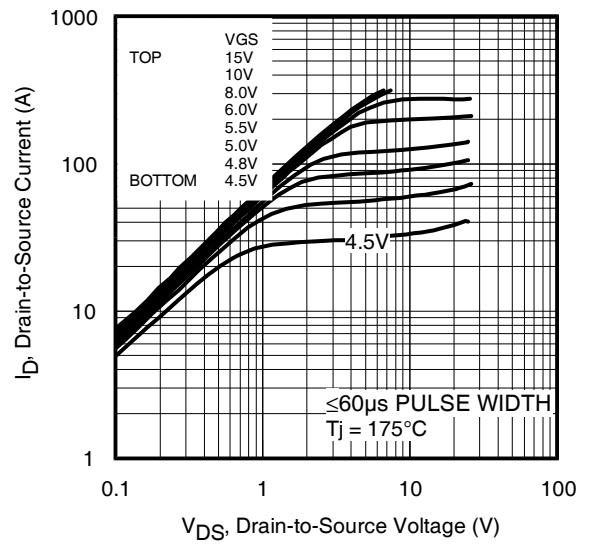
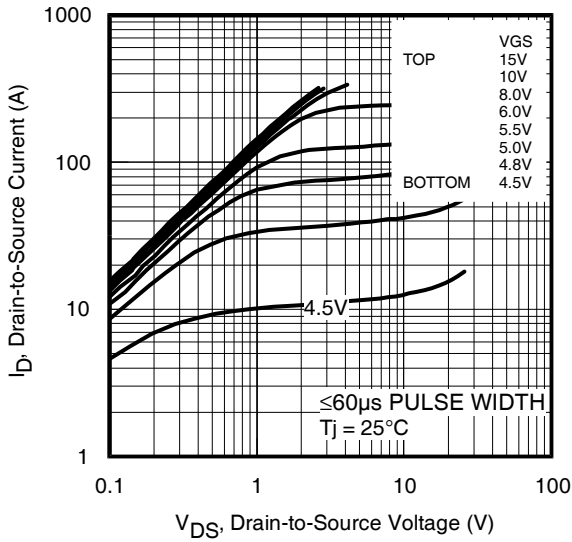
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q _g	Total Gate Charge	—	46	69	nC	I _D = 47A
Q _{gs}	Gate-to-Source Charge	—	10	—		V _{DS} = 30V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	12	—		V _{GS} = 10V ^④
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	34	—		I _D = 47A, V _{DS} = 0V, V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	13	—	ns	V _{DD} = 39V
t _r	Rise Time	—	35	—		I _D = 47A
t _{d(off)}	Turn-Off Delay Time	—	55	—		R _G = 10Ω
t _f	Fall Time	—	46	—		V _{GS} = 10V ^④
C _{iss}	Input Capacitance	—	2290	—		V _{GS} = 0V
C _{oss}	Output Capacitance	—	270	—		V _{DS} = 50V
C _{rss}	Reverse Transfer Capacitance	—	130	—	pF	f = 1.0MHz
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related) ^⑥	—	390	—		V _{GS} = 0V, V _{DS} = 0V to 60V ^⑥
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related) ^⑤	—	630	—		V _{GS} = 0V, V _{DS} = 0V to 60V ^⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	79	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	315		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 47A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	26	39	ns	T _J = 25°C V _R = 51V, T _J = 125°C I _F = 47A
Q _{rr}	Reverse Recovery Charge	—	24	36	nC	T _J = 25°C di/dt = 100A/μs ^④ T _J = 125°C
I _{RRM}	Reverse Recovery Current	—	1.8	—	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.08mH
R_G = 25Ω, I_{AS} = 47A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ I_{SD} ≤ 47A, di/dt ≤ 1668A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J approximately 90°C.
- ⑨ This is only applied to TO-220.



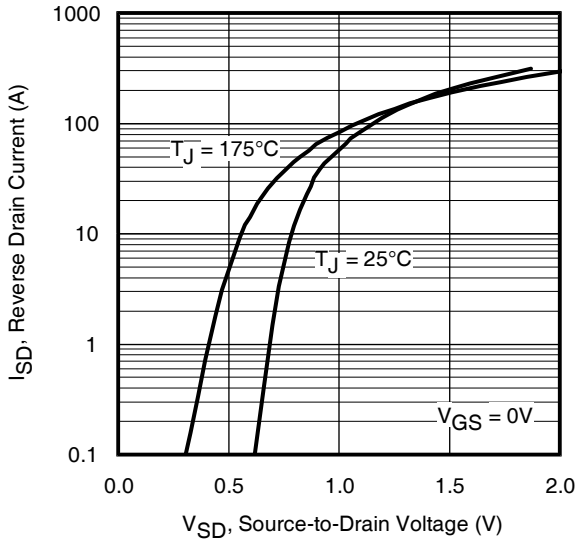


Fig 7. Typical Source-Drain Diode Forward Voltage

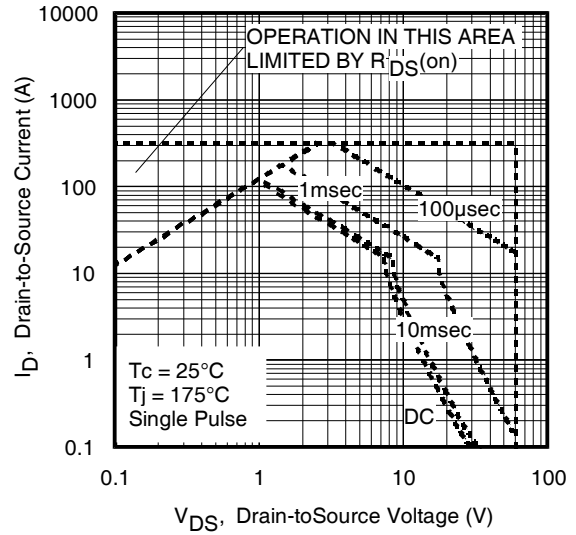


Fig 8. Maximum Safe Operating Area

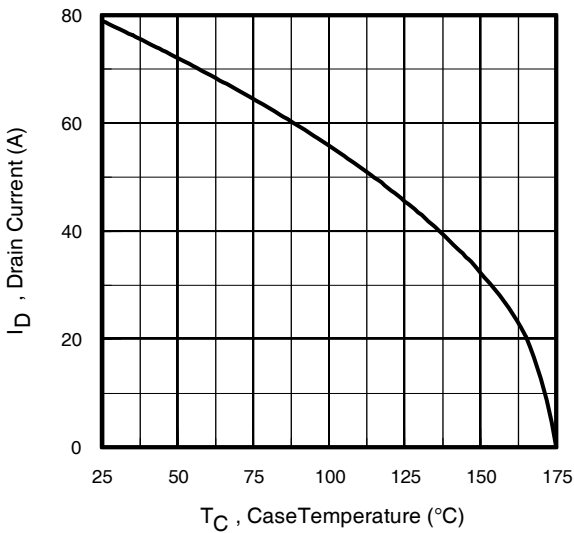


Fig 9. Maximum Drain Current vs. Case Temperature

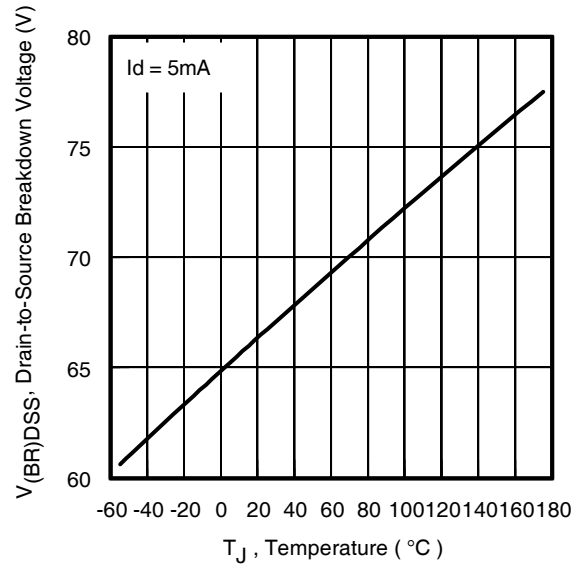


Fig 10. Drain-to-Source Breakdown Voltage

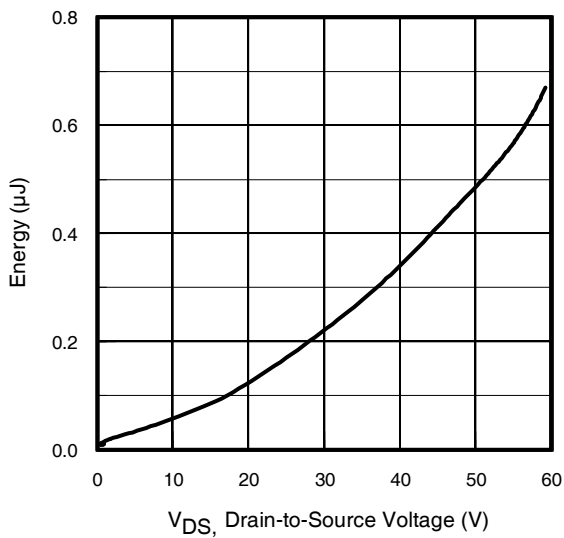


Fig 11. Typical C_{OSS} Stored Energy

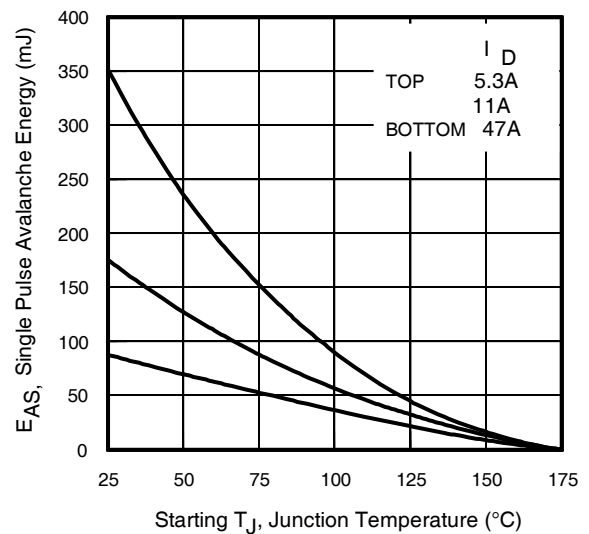


Fig 12. Maximum Avalanche Energy vs. Drain Current
www.irf.com

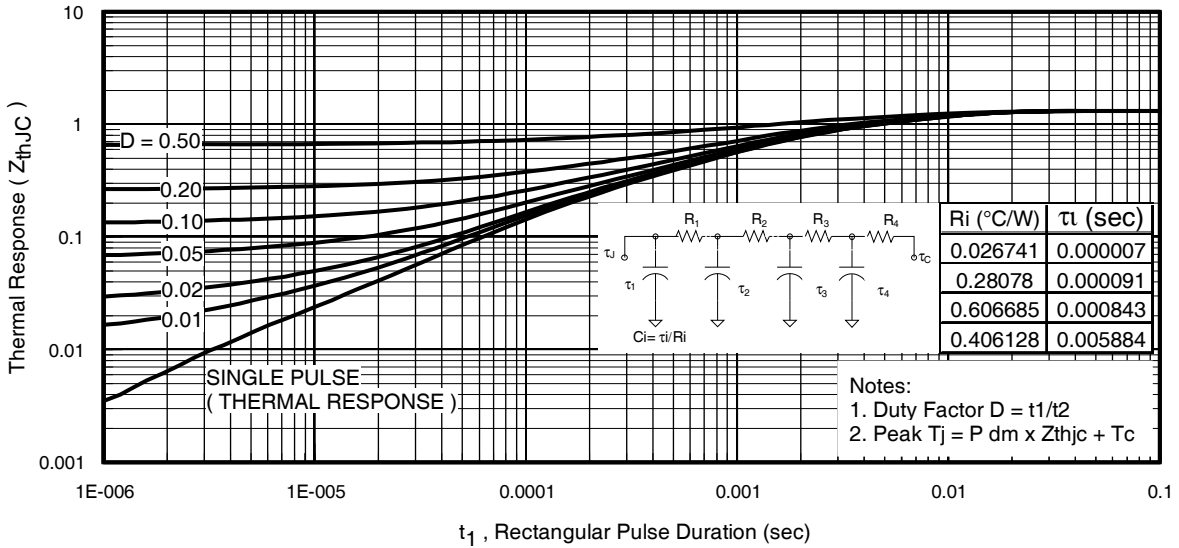


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

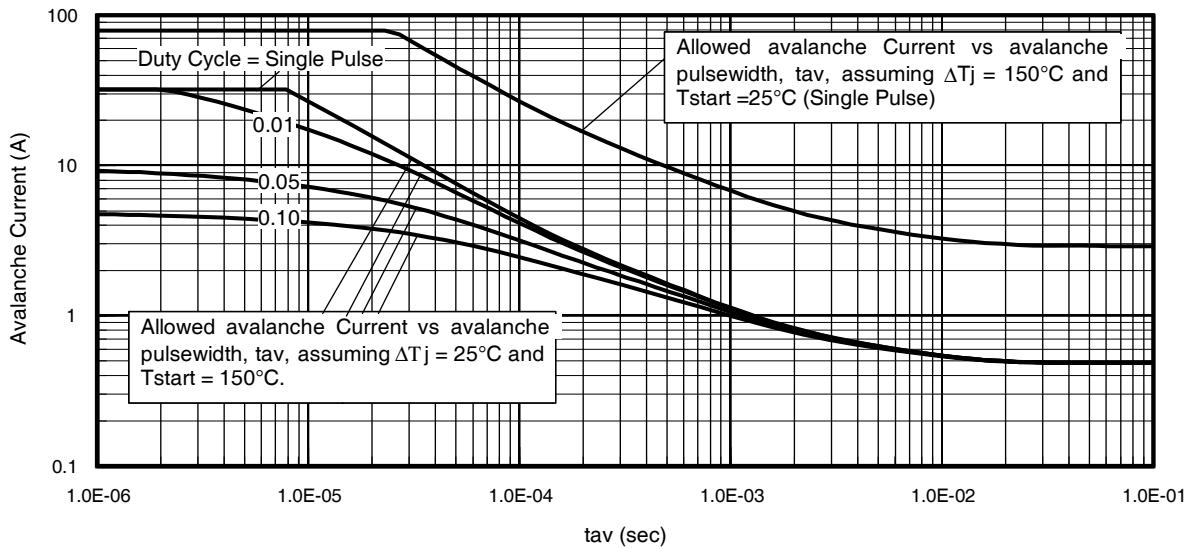
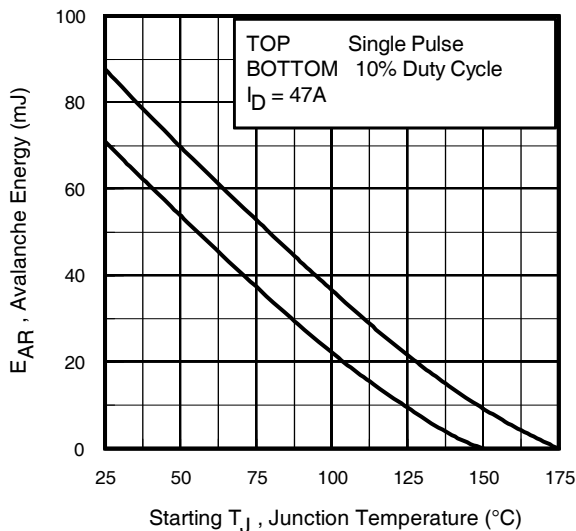


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

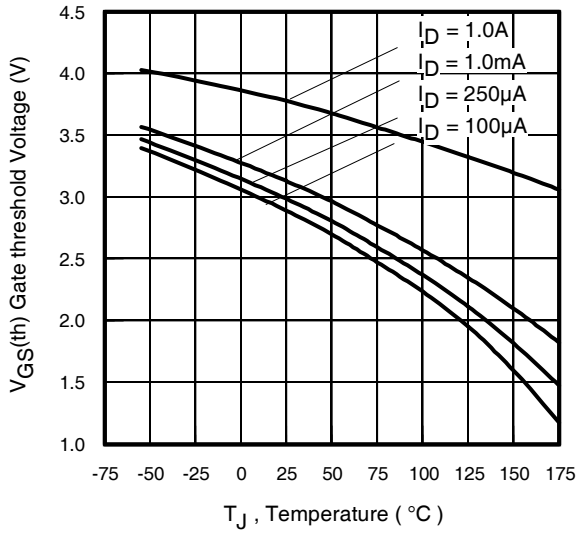


Fig 16. Threshold Voltage vs. Temperature

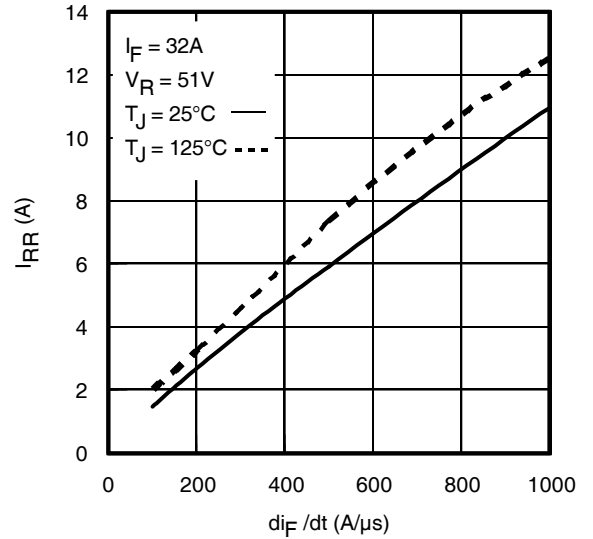


Fig. 17 - Typical Recovery Current vs. di_F/dt

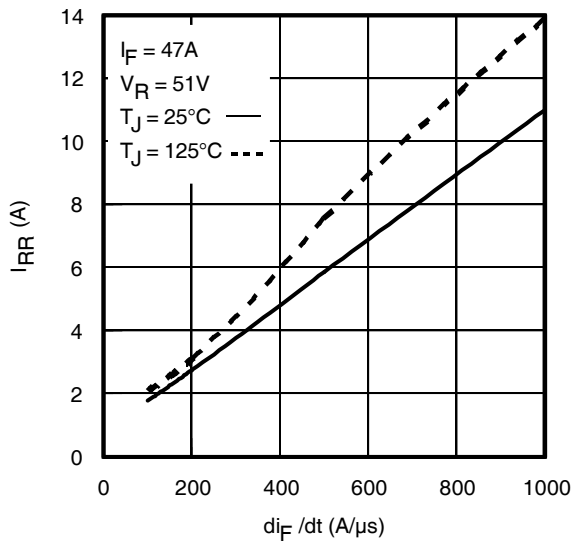


Fig. 18 - Typical Recovery Current vs. di_F/dt

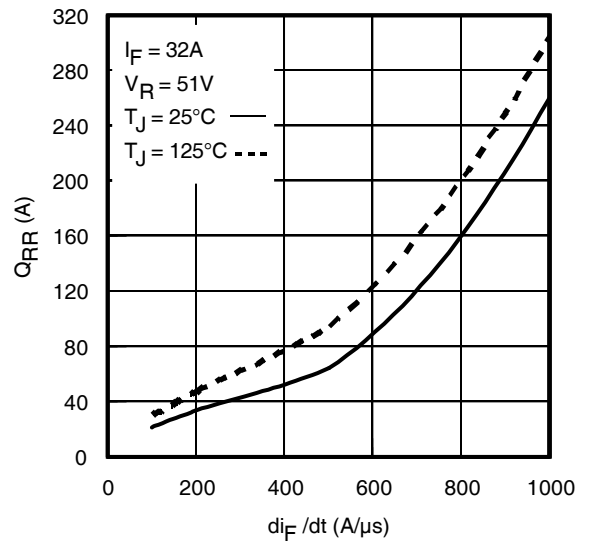


Fig. 19 - Typical Stored Charge vs. di_F/dt

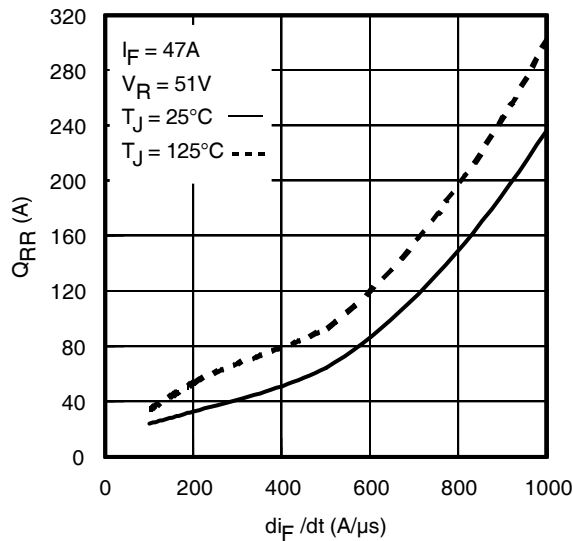


Fig. 20 - Typical Stored Charge vs. di_F/dt

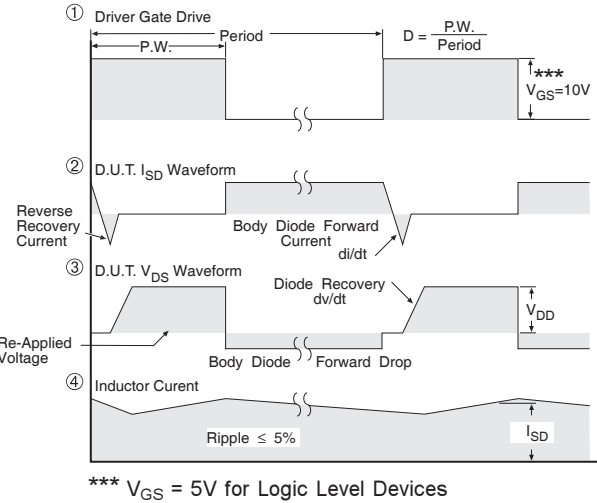
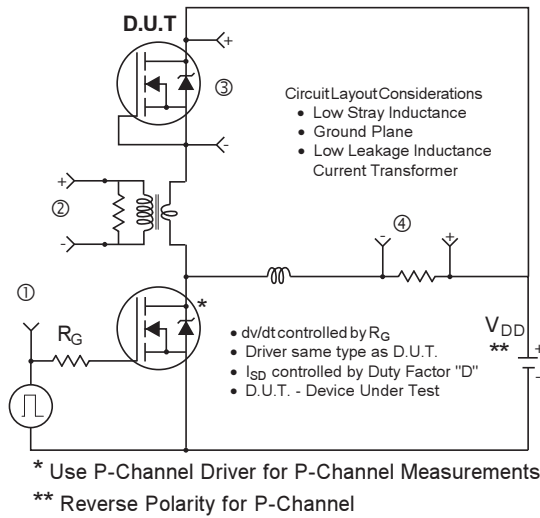


Fig 21. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

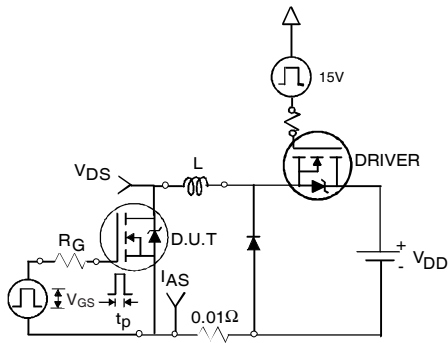


Fig 22a. Unclamped Inductive Test Circuit

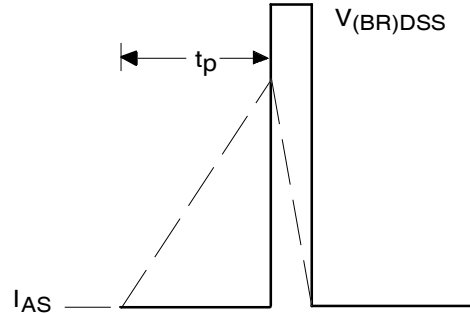


Fig 22b. Unclamped Inductive Waveforms

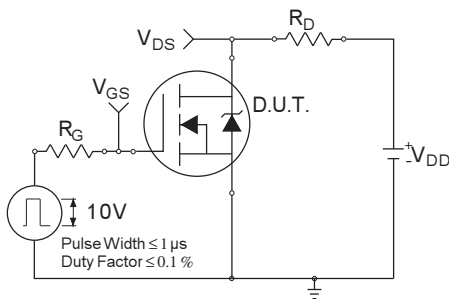


Fig 23a. Switching Time Test Circuit

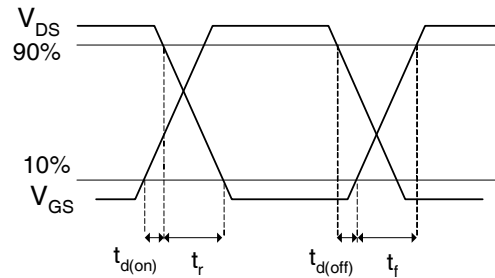


Fig 23b. Switching Time Waveforms

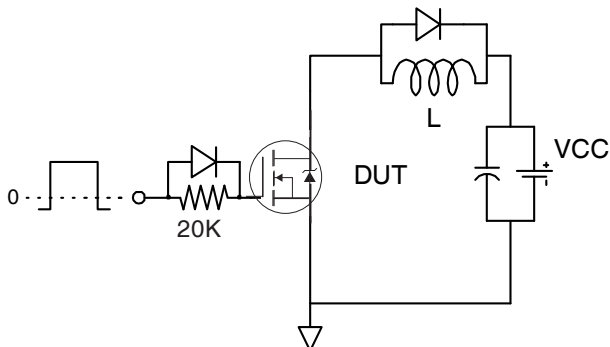


Fig 24a. Gate Charge Test Circuit

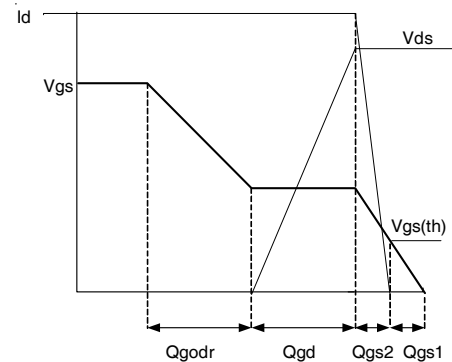
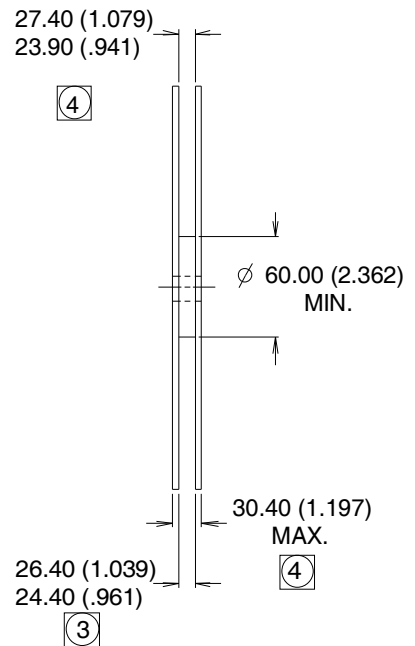
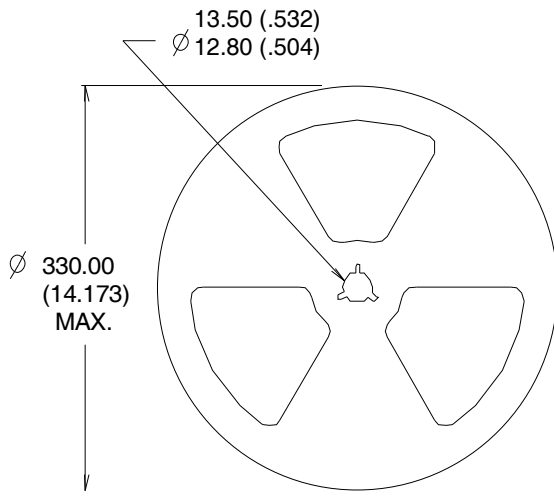
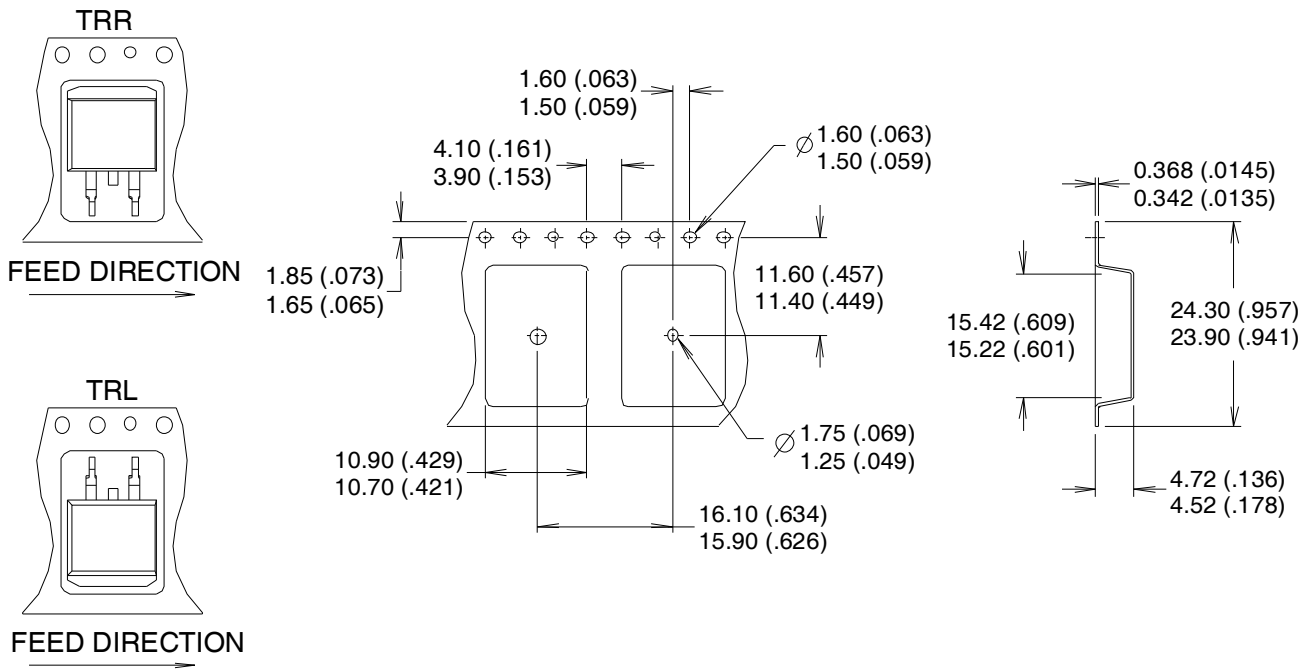


Fig 24b. Gate Charge Waveform

D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Ordering Information

Base part	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRF1018ES	D2Pak	Tube	50	AUIRF1018ES
		Tape and Reel Left	800	AUIRF1018ESTRL
		Tape and Reel Right	800	AUIRF1018ESTRR

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