19-2559; Rev 0; 7/02

PRELIMINARY

MAXIM

Dual-Phase, Quick-PWM Controllers for IMVP-IV CPU Core Power Supplies

CONFIDENTIAL INFORMATION—RESTRICTED TO INTEL IMVP LICENSEES

General Description

The MAX1987/MAX1988 are dual-phase, Quick-PWM™, step-down controllers for IMVP-IV™ CPU core supplies. Dual-phase operation reduces input ripple current requirements and output voltage ripple, while easing component selection and layout difficulties. The Quick-PWM control scheme provides instantaneous response to fast load-current steps. The MAX1987/MAX1988 include active voltage positioning with adjustable gain and offset, reducing power dissipation and bulk output capacitance requirements.

The MAX1987/MAX1988 are intended for two different notebook CPU core applications: stepping down the battery directly or stepping down the 5V system supply to create the core voltage. The single-stage conversion method allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the 5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size.

The MAX1987/MAX1988 meet the IMVP-IV specifications and can directly interface with the CPU power-good signals from the V_{CCP} and V_{CCMCH} rails within the system. The switching regulator features power-up sequencing, automatically ramping up to the Intel-specified boot voltage. The MAX1987/MAX1988 also feature independent four-level logic inputs for setting the boot voltage (B0 to B2) and the suspend voltage (S0 to S2).

The MAX1987/MAX1988 include output undervoltage protection, thermal protection, and system power-OK (SYSPOK) input. When any of these protection features detect a fault, the controller shuts down. Additionally, the MAX1987 includes overvoltage protection.

The MAX1987/MAX1988 are available in a low-profile 48-pin 7mm × 7mm Thin QFN package.

Applications

IMVP-IV Notebook Computers

Multiphase CPU Core Supply

Voltage-Positioned Step-Down Converters

Servers/Desktop Computers

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

IMVP-IV is a trademark of Intel Corp.

Typical Operating Circuit appears at end of data sheet.

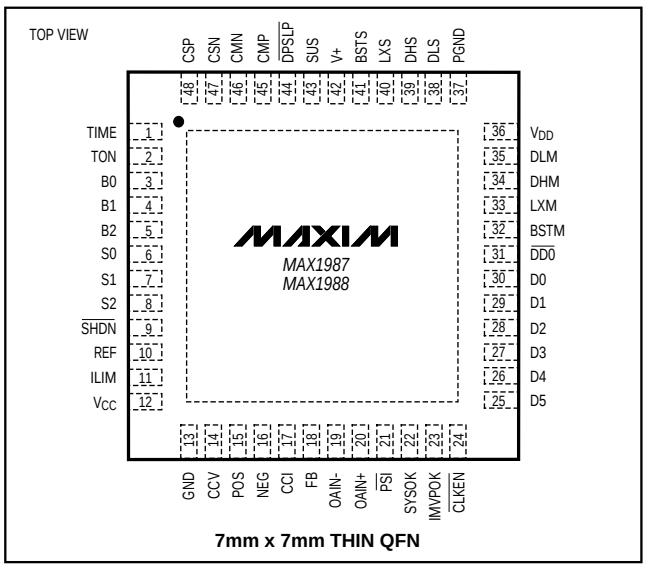
Features

- **Dual-Phase, Quick-PWM Controllers**
- **±0.75% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **Active Voltage Positioning with Adjustable Gain and Offset**
- **6-Bit On-Board DAC (16mV Increments)**
- **0.492V to 1.708V Output Adjust Range**
- **Selectable 200kHz/300kHz/550kHz Switching Frequency**
- **2V to 28V Battery Input Voltage Range**
- **Adjustable Slew Rate Control**
- **Drives Large Synchronous Rectifier MOSFETs**
- **Output Overvoltage Protection (MAX1987 Only)**
- **Undervoltage and Thermal Fault Protection**
- **IMVP-IV Power Sequencing and Timing**
- **Selectable Boot and Suspend Voltages**
- **Low-Profile 7mm × 7mm 48-Pin Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1987ETM	-40°C to +100°C	48 Thin QFN 7mm x 7mm
MAX1988ETM	-40°C to +100°C	48 Thin QFN 7mm x 7mm

Pin Configuration



7mm x 7mm THIN QFN

Dual-Phase, Quick-PWM Controllers for IMVP-IV CPU Core Power Supplies

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +30V
V_{CC} to GND .....-0.3V to +6V
V_{DD} to PGND .....-0.3V to +6V
$\overline{PSI}$, SUS, IMVPOK, $\overline{CLKEN}$, $\overline{DPSLP}$, SYSOK, D0–D5 to GND .....-0.3V to +6V
ILIM, FB, POS, NEG, CCV, CCI, REF, OAIN+, OAIN- to GND .....-0.3V to (V_{CC} + 0.3V)
CMP, CSP, CMN, CSN to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{DDO}$, TON, TIME, B0, B1, B2, S0, S1, S2 to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{SHDN}$ to GND (Note 1) .....-0.3V to +18V
DLM, DLS to PGND .....-0.3V to (V_{DD} + 0.3V)
BSTM, BSTS to GND .....-0.3V to +36V
DHM to LXM .....-0.3V to (V_{BSTM} + 0.3V)
LXM to BSTM .....-6V to +0.3V
DHS to LXS .....-0.3V to (V_{BSTS} + 0.3V)
LXS to BSTS .....-6V to +0.3V
GND to PGND .....-0.3V to +0.3V
REF Short-Circuit Duration (T_A = +70°C) .....Continuous
Continuous Power Dissipation
48-Pin QFN (derate 26.3mW/°C above +70°C) 2.105W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: $\overline{SHDN}$ may be forced to 12V, for the purpose of debugging prototype boards using the no-fault test mode, which disables fault protection and disables overlapping operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = $V_{\overline{PSI}}$ = V_{B1} = V_{OAIN-} = 5V, V_{B2} = 2V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, V_{D4} = V_{D3} = V_{D2} = 1.0V, V_{SUS} = V_{D5} = V_{D1} = V_{D0} = V_{S0} = V_{S1} = V_{S2} = V_{B0} = 0, **T_A = 0°C to +85°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input-Voltage Range		Battery voltage, V+		2		28	V
		V_{CC}, V_{DD}		4.5		5.5	
DC Output-Voltage Accuracy (Note 2)		V+ = 4.5V to 28V, includes load regulation error	DAC codes from 1.276V to 1.708V	-0.75		+0.75	%
			DAC codes from 0.844V to 1.260V	-1.25		+1.25	
			DAC codes from 0.492V to 0.828V	-3.00		+3.00	
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V+ = 4.5V to 28V			5		mV
Input Bias Current	I_{FB}	FB		-2		+2	µA
	I_{POS}, I_{NEG}	POS, NEG		-0.2		+0.2	
POS, NEG Common-Mode Range		$\overline{DPSLP}$ = GND		0		2	V
POS, NEG Differential Range		V_{POS} - V_{NEG} , $\overline{DPSLP}$ = GND		-200		+200	mV
POS, NEG Offset Gain	A_{OS}	$\Delta V_{FB}/(V_{POS} - V_{NEG})$, ($V_{POS}$ - V_{NEG}) = 100mV, $\overline{DPSLP}$ = GND		0.95	1.00	1.05	mV/mV
POS, NEG Enable Time	t_{OS}	Measured from the time $\overline{DPSLP}$ goes low to the time in which POS, NEG affect a change in the set point (V_{DAC})			0.1		µs
TIME Frequency Accuracy	f_{TIME}	640kHz nominal, R_{TIME} = 23.5kΩ		580	640	700	kHz
		320kHz nominal, R_{TIME} = 47kΩ		295	320	345	
		64kHz nominal, R_{TIME} = 235kΩ		58	64	70	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = $V_{\overline{PSI}}$ = V_{B1} = V_{OAIN-} = 5V, V_{B2} = 2V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, V_{D4} = V_{D3} = V_{D2} = 1.0V, V_{SUS} = V_{D5} = V_{D1} = V_{D0} = V_{S0} = V_{S1} = V_{S2} = V_{B0} = 0, **T_A = 0°C to +85°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time (Note 3)	t_{ON}	V+ = 12V, V_{FB} = V_{CCI} = 1.2V	TON = REF (550kHz)	155	180	205	ns
			TON = open (300kHz)	320	355	390	
			TON = V_{CC} (200kHz)	475	525	575	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	TON = REF (550kHz)			330	375	ns
		TON = V_{CC} or open (200kHz or 300kHz)			435	500	
$\overline{DDO}$ Delay Time	$t_{\overline{DDO}}$	Measured from the time FB reaches the voltage set by S0 to S2. Clock speed set by R_{TIME}.			32		clks
SKIP Delay Time	t_{SKIP}	Measured from the time when $\overline{DDO}$ is asserted to the time in which the controller begins pulse-skipping operation			30		clks
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point			1.70	2.70	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point			<1	5	µA
Quiescent Battery Supply Current (V+)	I_{V+}	Measured at V+			25	50	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND			2	5	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND			<1	5	µA
Shutdown Battery Supply Current (V+)		Measured at V+, $\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0 or 5V			<1	5	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.990	2.000	2.010	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = -10µA to +100µA		-10		+10	mV
FAULT PROTECTION							
Output Overvoltage Protection Threshold (MAX1987 Only)	V_{OVP}	Measured at FB		1.95	2.00	2.05	V
Output Overvoltage Propagation Delay (MAX1987 Only)	t_{OVP}	FB forced above 2.05V			10		µs
Output Undervoltage Protection Threshold	V_{UVLO}	Measured at FB with respect to unloaded output voltage		67	70	73	%
Output Undervoltage Propagation Delay	t_{UVP}	FB forced 2% below trip threshold			10		µs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = $V_{\overline{PSI}}$ = V_{B1} = V_{OAIN-} = 5V, V_{B2} = 2V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, V_{D4} = V_{D3} = V_{D2} = 1.0V, V_{SUS} = V_{D5} = V_{D1} = V_{D0} = V_{S0} = V_{S1} = V_{S2} = V_{B0} = 0, **T_A = 0°C to +85°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IMVPOK, $\overline{CLKEN}$ Threshold		V_{SYSPOK} = 5V; measured at FB with respect to unloaded output voltage	Lower threshold (undervoltage)	-13	-10	-7	%
			Upper threshold (overvoltage)	+7	+10	+13	
$\overline{CLKEN}$ Delay	$t_{\overline{CLKEN}}$	FB in regulation, measured from the rising edge of SYSPOK		30	50	90	µs
Output Fault, IMVPOK, and $\overline{CLKEN}$ Transition Blanking Time	t_{BLANK}	Measured from the time when FB reaches the voltage set by the DAC code, clock speed set by R_{TIME} (Note 4)			32		clks
IMVPOK Delay	t_{IMVPOK}	FB in regulation, measured from the falling edge of $\overline{CLKEN}$		3	5	7	ms
IMVPOK, $\overline{CLKEN}$ Output Low Voltage		I_{SINK} = 3mA				0.3	V
IMVPOK, $\overline{CLKEN}$ Leakage Current		High state, IMVPOK, $\overline{CLKEN}$ forced to 5.5V				1	µA
V_{CC} Undervoltage Lockout Threshold	V_{UVLO} (VCC)	Rising edge, hysteresis = 90mV, PWM disabled below this level		4.0	4.2	4.4	V
Thermal Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			160		°C
CURRENT LIMIT AND BALANCE							
Current-Limit Threshold Voltage (Positive, Default)	V_{LIMIT}	CMP - CMN, CSP - CSN; ILIM = V_{CC}		27	30	33	mV
Current-Limit Threshold Voltage (Positive, Adjustable)	V_{LIMIT}	CMP - CMN, CSP - CSN	V_{ILIM} = 1V	47	50	53	mV
			V_{ILIM} = 1.5V	72	75	78	
Current-Limit Threshold Voltage (Negative)	V_{LIMIT} (NEG)	CMP - CMN, CSP - CSN; ILIM = V_{CC}, SUS = GND, and $\overline{DPSLP}$ = $\overline{PSI}$ = V_{CC}		-30	-36	-42	mV
Current-Limit Threshold Voltage (Zero-Crossing)	V_{ZERO}	CMP - CMN, CSP - CSN; SUS = V_{CC} or $\overline{DPSLP}$ = GND or $\overline{PSI}$ = GND			1.5		mV
CMP, CMN, CSP, CSN Input Ranges				0		2	V
CMP, CMN, CSP, CSN Input Current		V_{CSP} = V_{CSN} = 0 to 5V		-2		+2	µA
ILIM Input Current	I_{ILIM}	V_{ILIM} = 0 to 5V			0.1	200	nA
Current-Limit Default Switchover Threshold		ILIM		3	V_{CC} - 1	V_{CC} - 0.4	V
Current-Balance Offset	$V_{OS(IBAL)}$	(V_{CMP} - V_{CMN}) - (V_{CSP} - V_{CSN}); I_{CCI} = 0, -20mV < (V_{CMP} - V_{CMN}) <+20mV, 0.5V < V_{CCI} < 2.8V		-2.0		+2.0	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = $V_{\overline{PSI}}$ = V_{B1} = V_{OAIN-} = 5V, V_{B2} = 2V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, V_{D4} = V_{D3} = V_{D2} = 1.0V, V_{SUS} = V_{D5} = V_{D1} = V_{D0} = V_{S0} = V_{S1} = V_{S2} = V_{B0} = 0, **T_A = 0°C to +85°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Balance Transconductance	$g_{M(IBAL)}$				400		µS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V			1.0	4.5	Ω
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			1.0	4.5	Ω
		Low state (pulldown)			0.4	2.0	
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			1.6		A
DL_ Gate-Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 5V			4		A
DL_ Gate-Driver Source Current	$I_{DL(SOURCE)}$	DL_ forced to 2.5V			1.6		A
Dead Time	t_{DEAD}	DL_ rising			35		ns
		DH_ rising			26		
VOLTAGE-POSITIONING AMPLIFIER							
Input Offset Voltage	V_{OS}			-1.5		+1.5	mV
Input Bias Current	I_{BIAS}	OAIN+, OAIN-			0.1	200	nA
Op Amp Disable Threshold		OAIN-		3	V_{CC} - 1	V_{CC} - 0.4	V
Common-Mode Input-Voltage Range	V_{CM}	Guaranteed by CMRR test		0		2.5	V
Common-Mode Rejection Ratio	CMRR	V_{OAIN+} = V_{OAIN-} = 0 to 2.5V		70	100		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.5V to 5.5V		75	100		dB
Large-Signal Voltage Gain	A_{OA}	R_L = 1kΩ to V_{CC}/2		70	112		dB
Output-Voltage Swing		(V_{OAIN+} - V_{OAIN-}) ≥ 10mV, R_L = 1kΩ to V_{CC}/2	V_{CC} - V_{FBH}		77	300	mV
			V_{FBL}		47	200	
Input Capacitance					11		pF
Gain-Bandwidth Product					3		MHz
Slew Rate					0.3		V/µs
Capacitive Load Stability		No sustained oscillations			400		pF
LOGIC AND I/O							
Logic-Input High Voltage	V_{IH}	SUS, $\overline{DPSLP}$, $\overline{SHDN}$, SYSPOK		2.4			V
Logic-Input Low Voltage	V_{IL}	SUS, $\overline{DPSLP}$, $\overline{SHDN}$, SYSPOK				0.8	V
Logic-Input Current		SUS, $\overline{DPSLP}$, $\overline{SHDN}$, SYSPOK		-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = $V_{\overline{PSI}}$ = V_{B1} = V_{OAIN-} = 5V, V_{B2} = 2V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, V_{D4} = V_{D3} = V_{D2} = 1.0V, V_{SUS} = V_{D5} = V_{D1} = V_{D0} = V_{S0} = V_{S1} = V_{S2} = V_{B0} = 0, **T_A = 0°C to +85°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ No-Fault Threshold		To enable no-fault mode		12		15	V
1V Logic-Input High Voltage		D0–D5, $\overline{PSI}$		0.7			V
1V Logic-Input Low Voltage		D0–D5, $\overline{PSI}$				0.3	V
DAC Input Current		D0–D5, $\overline{PSI}$		-1		+1	µA
Driver Disable Output High Voltage		$\overline{DDO}$, I_{LOAD} = 1mA		2.4			V
Driver Disable Output Low Voltage		$\overline{DDO}$, I_{LOAD} = 1mA				0.3	V
Four-Level Input Logic Levels		TON, S0 to S2, B0 to B2	High	V_{CC} - 0.4			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.5	
Four-Level Input Current		TON, S0 to S2, B0 to B2 forced to GND or V_{CC}		-4		+4	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = $V_{\overline{PSI}}$ = V_{B1} = V_{OAIN-} = 5V, V_{B2} = 2V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, V_{D4} = V_{D3} = V_{D2} = 1.0V, V_{SUS} = V_{D5} = V_{D1} = V_{D0} = V_{S0} = V_{S1} = V_{S2} = V_{B0} = 0, **T_A = -40°C to +100°C**, unless otherwise specified.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input-Voltage Range		Battery voltage, V+		2	28	V
		V_{CC}, V_{DD}		4.5	5.5	
DC Output-Voltage Accuracy (Note 2)		V+ = 4.5V to 28V, includes load regulation error	DAC codes from 1.276V to 1.708V	-1.00	+1.00	%
			DAC codes from 0.844V to 1.260V	-1.50	+1.50	
			DAC codes from 0.492V to 0.828V	-3.5	+3.5	
POS, NEG Offset Gain	A_{OFF}	$\Delta V_{FB}/(V_{POS} - V_{NEG})$, $(V_{POS} - V_{NEG})$ = 100mV, $\overline{DPSLP}$ = GND		0.95	1.05	mV/mV
TIME Frequency Accuracy	f_{TIME}	640kHz nominal, R_{TIME} = 23.5kΩ		580	700	kHz
		320kHz nominal, R_{TIME} = 47kΩ		295	345	
		64kHz nominal, R_{TIME} = 235kΩ		58	70	
On-Time (Note 3)	t_{ON}	V+ = 12V, V_{FB} = V_{CCI} = 1.2V	TON = REF (550kHz)	155	205	ns
			TON = open (300kHz)	320	390	
			TON = V_{CC} (200kHz)	475	575	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = $V_{\overline{PSI}}$ = V_{B1} = V_{OAIN-} = 5V, V_{B2} = 2V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, V_{D4} = V_{D3} = V_{D2} = 1.0V, V_{SUS} = V_{D5} = V_{D1} = V_{D0} = V_{S0} = V_{S1} = V_{S2} = V_{B0} = 0, **T_A = -40°C to +100°C**, unless otherwise specified.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	TON = REF (550kHz)			375	ns
		TON = V_{CC} or open (200kHz or 300kHz)			500	
BIAS AND REFERENCE						
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point			3.00	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point			30	µA
Quiescent Battery Supply Current (V+)	I_{V+}	Measured at V+			50	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND			20	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND			20	µA
Shutdown Battery Supply Current (V+)		Measured at V+, $\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0 or 5V			20	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.985	2.015	V
FAULT PROTECTION						
Output Overvoltage Protection Threshold (MAX1987 Only)		Measured at FB		1.95	2.05	V
Output Undervoltage Protection Threshold		Measured at FB with respect to unloaded output voltage		67	73	%
IMVPOK, $\overline{CLKEN}$ Threshold		V_{SYSPOK} = 5V; measured at FB with respect to unloaded output voltage	Lower threshold (undervoltage)	-13	-7	%
			Upper threshold (overvoltage)	7	13	
$\overline{CLKEN}$ Delay	$t_{\overline{CLKEN}}$	FB in regulation, measured from the rising edge of SYSPOK		30		µs
IMVPOK Delay	t_{IMVPOK}	FB in regulation, measured from the falling edge of $\overline{CLKEN}$		3		ms
V_{CC} Undervoltage Lockout Threshold	V_{UVLO} (VCC)	Rising edge, hysteresis = 90mV, PWM disabled below this level		3.95	4.45	V
CURRENT LIMIT AND BALANCE						
Current-Limit Threshold Voltage (Positive, Default)	V_{LIMIT}	CMP - CMN, CSP - CSN; ILIM = V_{CC}		25	35	mV
Current-Limit Threshold Voltage (Positive, Adjustable)	V_{LIMIT}	CMP - CMN, CSP - CSN	V_{ILIM} = 1V	45	55	mV
			V_{ILIM} = 1.5V	70	80	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{DPSLP}}$ = $V_{\overline{PSI}}$ = V_{B1} = V_{OAIN-} = 5V, V_{B2} = 2V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = V_{OAIN+} = V_{NEG} = V_{POS} = 1.26V, V_{D4} = V_{D3} = V_{D2} = 1.0V, V_{SUS} = V_{D5} = V_{D1} = V_{D0} = V_{S0} = V_{S1} = V_{S2} = V_{B0} = 0, **T_A = -40°C to +100°C**, unless otherwise specified.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Current-Limit Threshold Voltage (Negative)	V_{LIMIT} (NEG)	CMP - CMN, CSP - CSN; ILIM = V_{CC}, SUS = GND and $\overline{DPSLP}$ = V_{CC}		-27	-45	mV
Current-Balance Offset	$V_{OS(IBAL)}$	(V_{CMP} - V_{CMN}) - (V_{CSP} - V_{CSN}); I_{CCI} = 0, -20mV < (V_{CMP} - V_{CMN}) < 20mV, 0.5V < V_{CCI} < 2.8V		-3	+3	mV
GATE DRIVERS						
DH_Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V			4.5	Ω
DL_Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			4.5	Ω
		Low state (pulldown)			2.0	
VOLTAGE-POSITIONING AMPLIFIER						
Input Offset Voltage	V_{OS}			-2.5	+2.5	mV
Common-Mode Input Voltage Range	V_{CM}	Guaranteed by CMRR test		0	2.5	V
Output-Voltage Swing		(V_{OAIN+} - V_{OAIN-}) ≥ 10mV, R_L = 1kΩ to V_{CC}/2	V_{CC} - V_{FBH}		300	mV
			V_{FBL}		200	
LOGIC AND I/O						
Logic-Input High Voltage	V_{IH}	SUS, $\overline{DPSLP}$, $\overline{SHDN}$, SYSPOK		2.4		V
Logic-Input Low Voltage	V_{IL}	SUS, $\overline{DPSLP}$, $\overline{SHDN}$, SYSPOK			0.8	V
1V Logic-Input High Voltage		D0–D5, $\overline{PSI}$		0.7		V
1V Logic-Input Low Voltage		D0–D5, $\overline{PSI}$			0.3	V
Four-Level Input Logic Levels		TON, S0 to S2, B0 to B2	High	V_{CC} - 0.4		V
			Open	3.15	3.85	
			REF	1.65	2.35	
			Low		0.5	

Note 2: DC output accuracy specifications refer to the trip level of the error amplifier. The output voltage has a DC regulation higher than the trip level by 50% of the output ripple. When pulse-skipping, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

Note 3: On-time and minimum off-time specifications are measured from 50% to 50% at the DHM and DHS pins, with LX_ forced to GND, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times can be different due to MOSFET switching speeds.

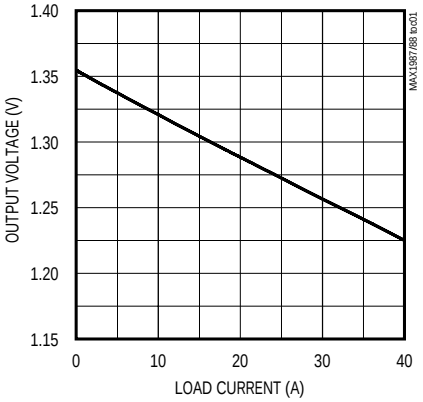
Note 4: The output fault-blanking time is measured from the time when FB reaches the regulation voltage set by the DAC code. During power-up, the regulation voltage is set by the boot DAC code (B0 to B2). During normal operation (SUS = GND), the regulation voltage is set by the VID DAC inputs (D0–D5). During suspend mode (SUS = V_{CC}), the regulation voltage is set by the suspend DAC inputs (S0 to S2).

Note 5: Specifications to T_A = -40°C to +100°C are guaranteed by design and are not production tested.

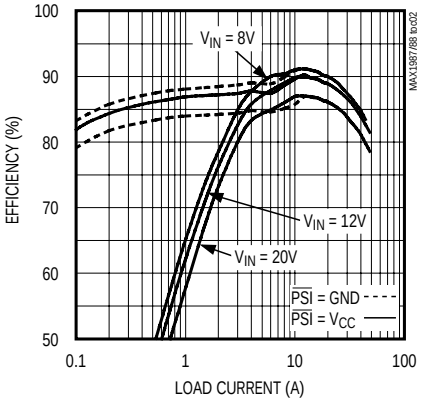
Typical Operating Characteristics

(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, SUS = GND, $\overline{SHDN}$ = $\overline{DPSLP}$ = $\overline{PSI}$ = V_{CC}, B0 to B2 set for 1.372V, S0 to S2 set for 0.748V, T_A = +25°C, unless otherwise specified.)

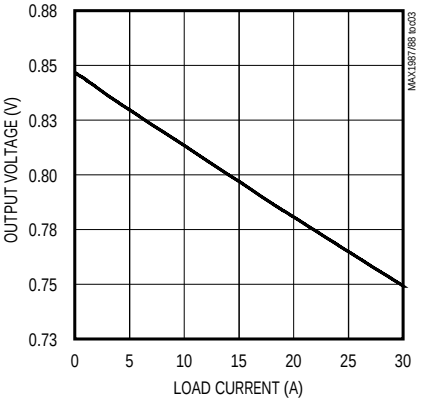
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.356V)



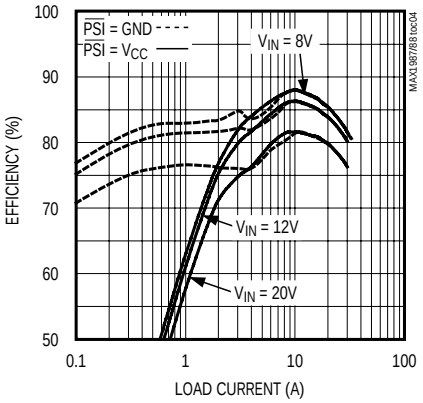
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.356V)



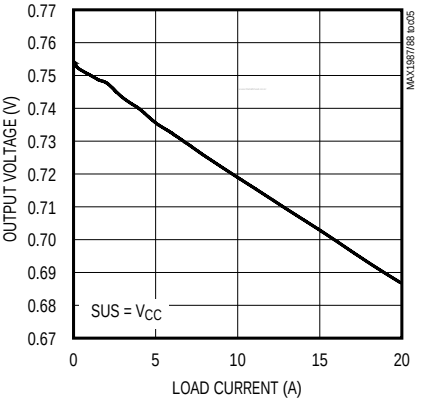
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 0.844V)



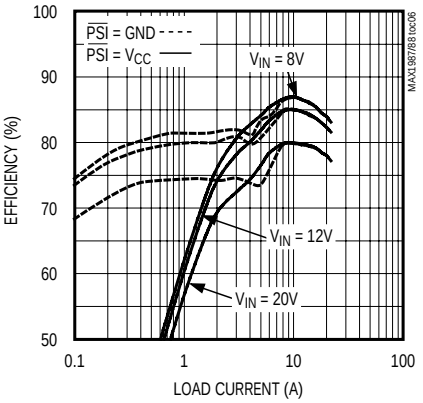
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.844V)



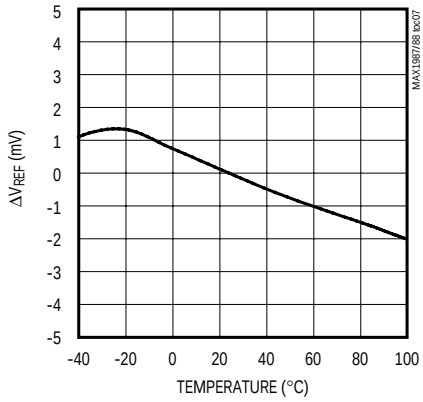
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 0.748V)



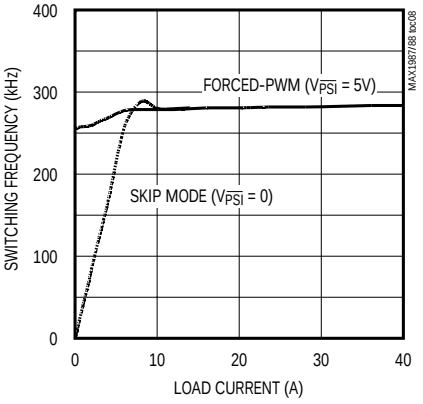
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.748V)



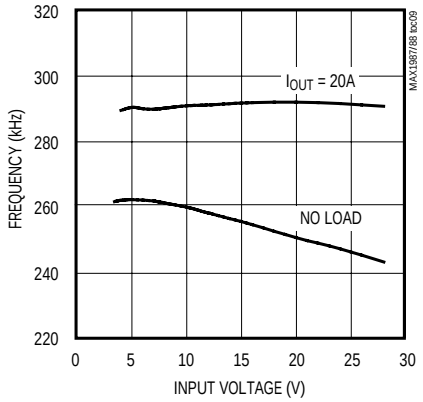
REFERENCE VOLTAGE SHIFT vs. TEMPERATURE



SWITCHING FREQUENCY vs. LOAD CURRENT



SWITCHING FREQUENCY vs. INPUT VOLTAGE

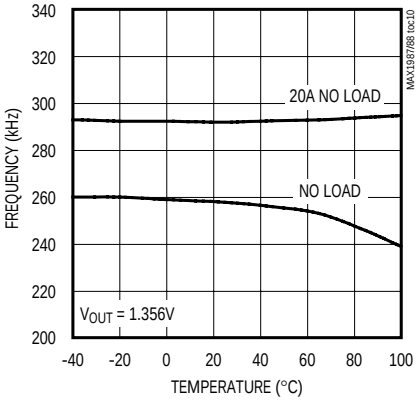


Dual-Phase, Quick-PWM Controllers for IMVP-IV CPU Core Power Supplies

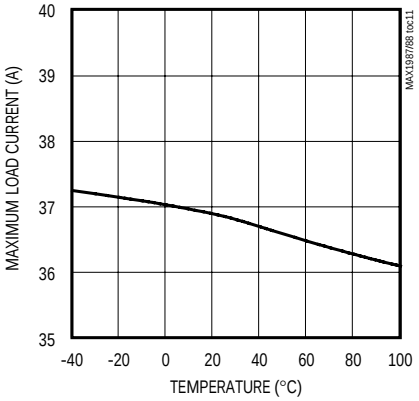
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, SUS = GND, $\overline{SHDN}$ = $\overline{DPSLP}$ = $\overline{PSI}$ = V_{CC}, B0 to B2 set for 1.372V, S0 to S2 set for 0.748V, T_A = +25°C, unless otherwise specified.)

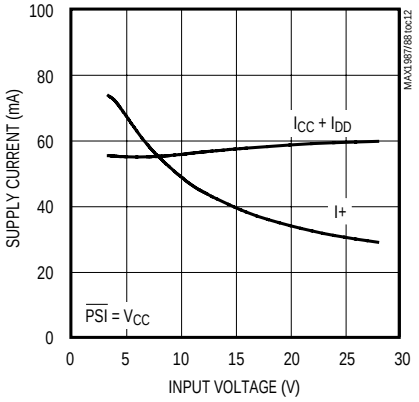
SWITCHING FREQUENCY vs. TEMPERATURE



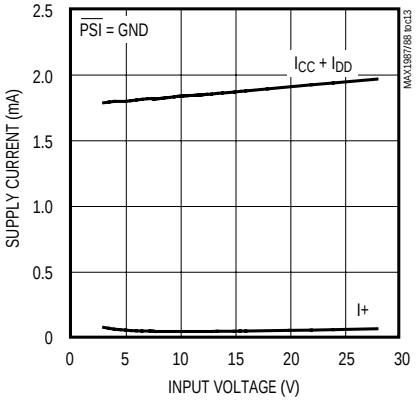
OUTPUT CURRENT AT CURRENT LIMIT vs. TEMPERATURE



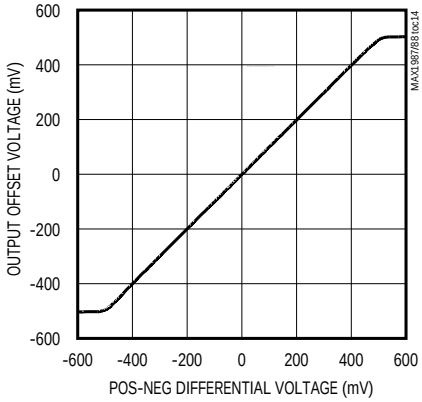
NO LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (FORCED-PWM MODE)



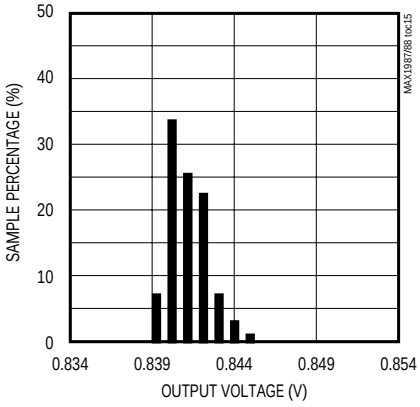
NO LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (PULSE SKIPPING)



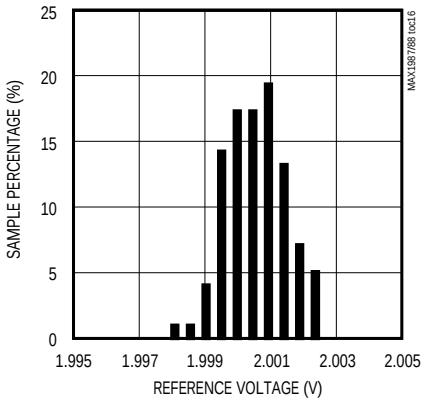
OUTPUT OFFSET VOLTAGE vs. POS-NEG DIFFERENTIAL VOLTAGE



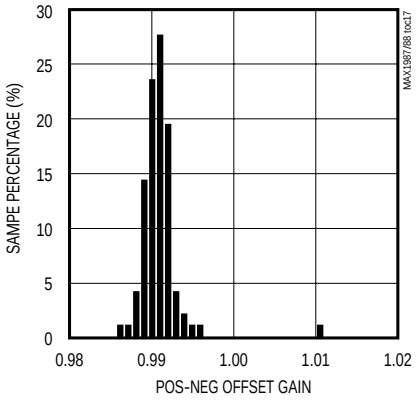
0.844V OUTPUT-VOLTAGE DISTRIBUTION



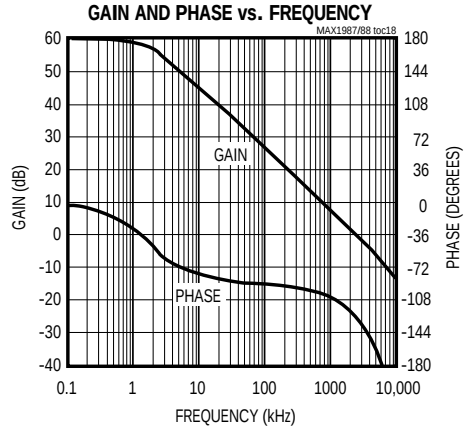
REFERENCE VOLTAGE DISTRIBUTION



POS-NEG OFFSET GAIN DISTRIBUTION



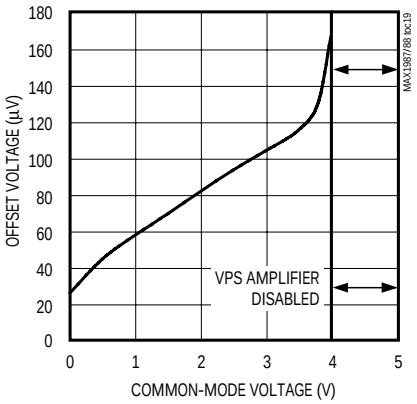
VOLTAGE-POSITIONING AMPLIFIER GAIN AND PHASE vs. FREQUENCY



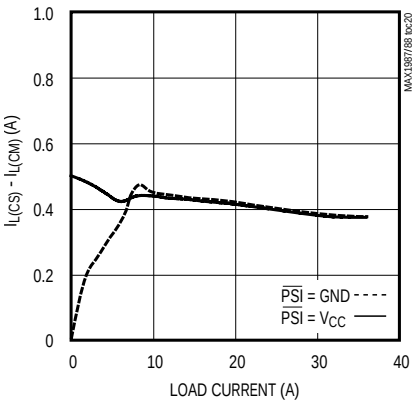
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, SUS = GND, $\overline{SHDN}$ = $\overline{DPSLP}$ = $\overline{PSI}$ = V_{CC}, B0 to B2 set for 1.372V, S0 to S2 set for 0.748V, T_A = +25°C, unless otherwise specified.)

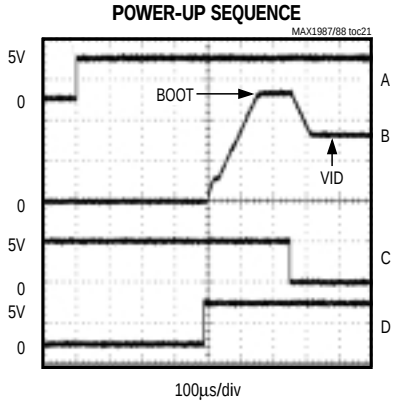
VPS AMPLIFIER OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



INDUCTOR CURRENT DIFFERENCE vs. LOAD CURRENT

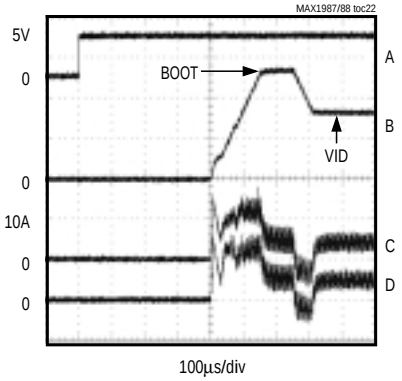


POWER-UP SEQUENCE



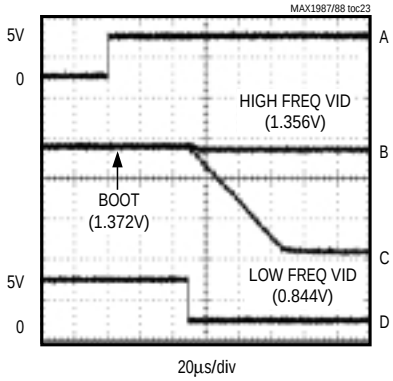
A. $V_{\overline{SHDN}}$ = 0 TO 5V, 5V/div
B. $V_{\overline{OUT}}$ = 0 TO 1.372V TO 0.844V, 500mV/div
C. $\overline{CLKEN}$, 5V/div
D. $\overline{DDO}$, 5V/div
R_{LOAD} = 80mΩ

SOFT-START



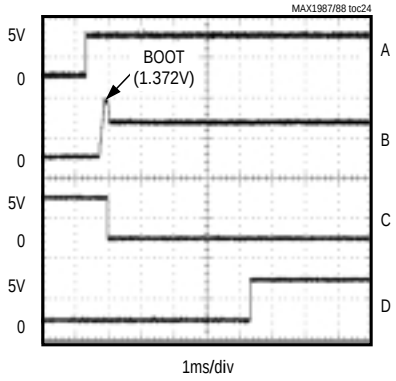
A. $V_{\overline{SHDN}}$ = 0 TO 5V, 5V/div
B. $V_{\overline{OUT}}$ = 0 TO 1.372V TO 0.844V, 500mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div
R_{LOAD} = 80mΩ

SYSTEM POWER-OK



A. V_{SYSPOK} = 0 TO 5V, 5V/div
B. HIGH FREQ: V_{OUT} = 1.356V, 200mV/div
C. LOW FREQ: V_{OUT} = 0.844V, 200mV/div
D. $\overline{CLKEN}$, 5V/div

IMVPOK DELAY

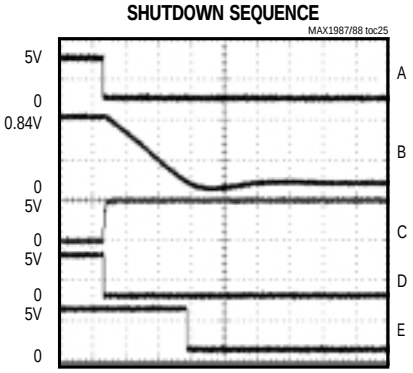


A. $V_{\overline{SHDN}}$ = 0 TO 5V, 5V/div
B. $V_{\overline{OUT}}$ = 0 TO 0.844V, 1V/div
C. $\overline{CLKEN}$, 5V/div
D. IMVPOK, 5V/div

Typical Operating Characteristics (continued)

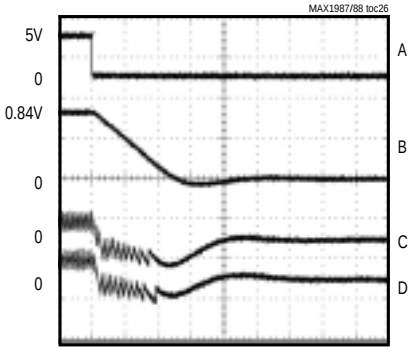
(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, SUS = GND, $\overline{SHDN}$ = $\overline{DPSLP}$ = $\overline{PSI}$ = V_{CC}, B0 to B2 set for 1.372V, S0 to S2 set for 0.748V, T_A = +25°C, unless otherwise specified.)

SHUTDOWN SEQUENCE



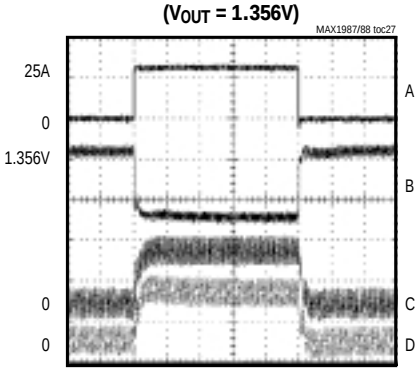
A. $V_{\overline{SHDN}}$ = 5V TO 0, 5V/div
B. V_{OUT} = 0.844V TO 0, 500mV/div
C. $\overline{CLKEN}$, 5V/div
D. $\overline{IMVPOK}$, 5V/div
E. $\overline{DDO}$, 5V/div
R_{LOAD} = 80mΩ

SOFT SHUTDOWN



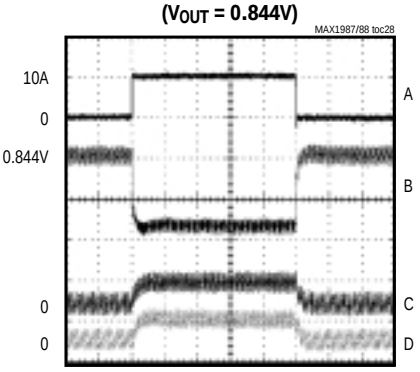
A. $V_{\overline{SHDN}}$ = 5V TO 0, 5V/div
B. V_{OUT} = 0.844V TO 0, 500mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div
R_{LOAD} = 80mΩ

LOAD TRANSIENT (V_{OUT} = 1.356V)



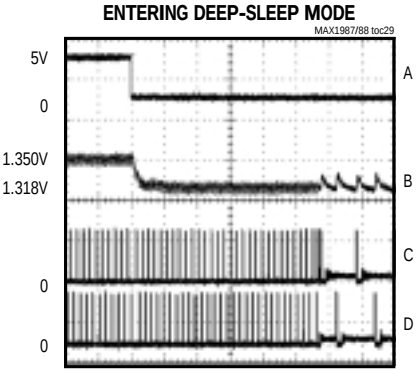
A. I_{OUT} = 0 TO 25A, 20A/div
B. V_{OUT} = 1.356V TO 1.281V, 50mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div

LOAD TRANSIENT (V_{OUT} = 0.844V)



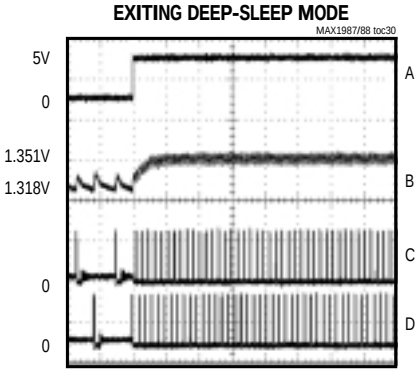
A. I_{OUT} = 0 TO 10A, 10A/div
B. V_{OUT} = 0.844V TO 0.814V, 20mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div

ENTERING DEEP-SLEEP MODE



A. $V_{\overline{DPSLP}}$ = 5V TO 0, 5V/div
B. V_{OUT} = 1.350V TO 1.318V, 50mV/div
C. LXM, 10V/div
D. LXS, 10V/div
SUS = GND, I_{OUT} = 1A

EXITING DEEP-SLEEP MODE

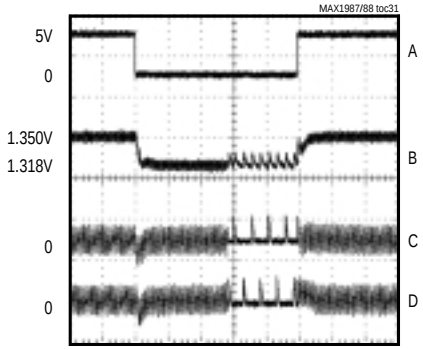


A. $V_{\overline{DPSLP}}$ = 0 TO 5V, 5V/div
B. V_{OUT} = 1.318V TO 1.351V, 50mV/div
C. LXM, 10V/div
D. LXS, 10V/div
SUS = GND, I_{OUT} = 1A

Typical Operating Characteristics (continued)

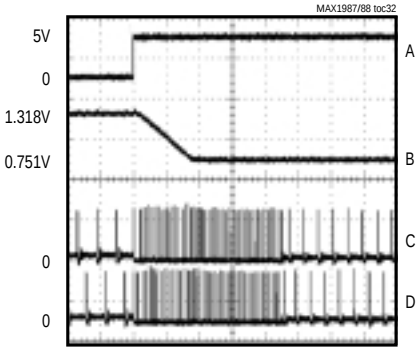
(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, SUS = GND, $\overline{SHDN}$ = $\overline{DPSLP}$ = $\overline{PSI}$ = V_{CC}, B0 to B2 set for 1.372V, S0 to S2 set for 0.748V, T_A = +25°C, unless otherwise specified.)

DEEP-SLEEP TRANSITION



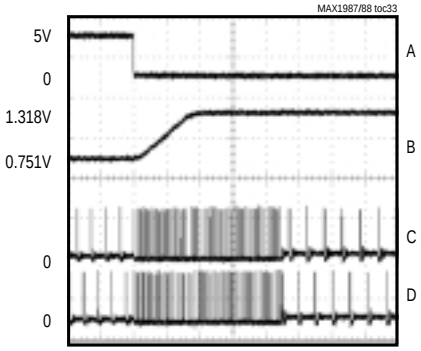
A. $V_{\overline{DPSLP}}$ = 5V TO 0, 5V/div
B. V_{OUT} = 1.350V TO 1.318V, 50mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div
SUS = GND, I_{OUT} = 1A

ENTERING SUSPEND MODE



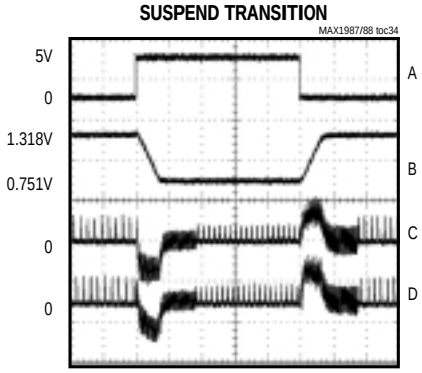
A. V_{SUS} = 0 TO 5V, 5V/div
B. V_{OUT} = 1.318V TO 0.751V, 500mV/div
C. LXM, 10V/div
D. LXS, 10V/div
$\overline{DPSLP}$ = GND, I_{OUT} = 1.0A

EXITING SUSPEND MODE



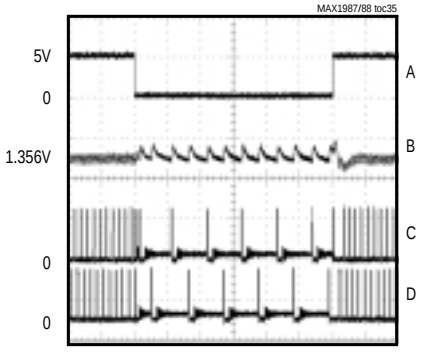
A. V_{SUS} = 5V TO 0, 5V/div
B. V_{OUT} = 0.751V TO 1.318V, 500mV/div
C. LXM, 10V/div
D. LXS, 10V/div
$\overline{DPSLP}$ = GND, I_{OUT} = 1A

SUSPEND TRANSITION



A. V_{SUS} = 0 TO 5V, 5V/div
B. V_{OUT} = 1.318V TO 0.751V, 500mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div
$\overline{DPSLP}$ = GND, I_{OUT} = 1A

$\overline{PSI}$ TRANSITION



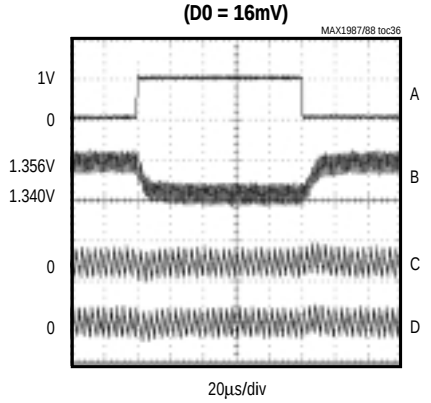
A. $V_{\overline{PSI}}$ = 5V TO 0, 5V/div
B. V_{OUT} = 1.356V, 50mV/div
C. LXM, 10V/div
D. LXS, 10V/div
I_{OUT} = 1A

Dual-Phase, Quick-PWM Controllers for IMVP-IV CPU Core Power Supplies

Typical Operating Characteristics (continued)

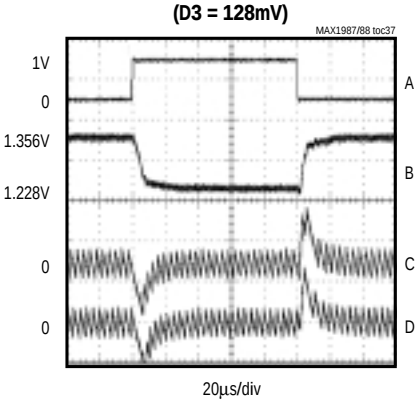
(Circuit of Figure 1, V+ = 12V, V_{CC} = V_{DD} = 5V, SUS = GND, $\overline{SHDN}$ = $\overline{DPSLP}$ = $\overline{PSI}$ = V_{CC}, B0 to B2 set for 1.372V, S0 to S2 set for 0.748V, T_A = +25°C, unless otherwise specified.)

DYNAMIC VID TRANSITION (D0 = 16mV)



A. V_{D0} = 0 TO 1V, 1V/div
B. V_{OUT} = 1.356V TO 1.340V, 20mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div

DYNAMIC VID TRANSITION (D3 = 128mV)



A. V_{D3} = 0 TO 1V, 1V/div
B. V_{OUT} = 1.356V TO 1.228V, 100mV/div
C. I_{LM}, 10A/div
D. I_{LS}, 10A/div

Pin Description

PIN	NAME	FUNCTION
1	TIME	Slew-Rate Adjustment Pin. Connect a resistor from TIME to GND to set the internal slew-rate clock. A 235kΩ to 23.5kΩ resistor sets the clock from 64kHz to 640kHz, f_{SLEW} = 320kHz × 47kΩ/R_{TIME}.
2	TON	On-Time Selection Control Input. This four-level input sets the K-factor value (Table 3) used to determine the DH on-time (see the *On-Time One-Shot* section): GND = 1000kHz (untested), REF = 550kHz, open = 300kHz, V_{CC} = 200kHz per phase
3, 4, 5	B0, B1, B2	Boot-Mode Voltage Select Inputs. B0 to B2 are four-level digital inputs that select the boot-mode VID code (Table 6) for the boot-mode multiplexer inputs. During power-up, the boot-mode VID code is delivered to the DAC (see the *Internal Multiplexers* section).
6, 7, 8	S0, S1, S2	Suspend-Mode Voltage Select Inputs. S0 to S2 are four-level digital inputs that select the suspend-mode VID code (Table 5) for the suspend-mode multiplexer inputs. If SUS is high, the suspend-mode VID code is delivered to the DAC (see the *Internal Multiplexers* section), overriding any other voltage setting (Figure 9).
9	$\overline{SHDN}$	Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the IC into its 1µA shutdown state. During the transition from normal operation to shutdown, the output voltage is ramped down at the output voltage slew rate programmed by the TIME pin. In shutdown mode, DLM and DLS are forced to V_{DD} to clamp the output to ground. Forcing $\overline{SHDN}$ to 12V~15V disables both overvoltage protection and undervoltage protection circuits, disables overlap operation, and clears the fault latch. Do not connect $\overline{SHDN}$ to >15V.
10	REF	2V Reference Output. Bypass to GND with a 0.22µF or greater ceramic capacitor. The reference can source 100µA for external loads. Loading REF degrades output-voltage accuracy according to the REF load regulation error.
11	ILIM	Current-Limit Adjustment. The current-limit threshold defaults to 30mV if ILIM is connected to V_{CC}. In adjustable mode, the current-limit threshold voltage is precisely 1/20th the voltage seen at ILIM over a 200mV to 1.5V range. The logic threshold for switchover to the 30mV default value is approximately V_{CC} - 1V.

Pin Description (continued)

PIN	NAME	FUNCTION
12	V_{CC}	Analog Supply Voltage Input for PWM Core. Connect V_{CC} to the system supply voltage (4.5V to 5.5V) with a series 10Ω resistor. Bypass to GND with a 1µF or greater ceramic capacitor, as close to the IC as possible.
13	GND	Analog Ground. Connect the MAX1987/MAX1988s' exposed pad to analog ground.
14	CCV	Voltage Integrator Capacitor Connection. Connect a 47pF to 1000pF (270pF typ) capacitor from CCV to analog ground (GND) to set the integration time constant.
15	POS	Feedback Offset Adjust Positive Input. The output shifts by 100% (typ) of the differential input voltage appearing between POS and NEG when $\overline{DPSLP}$ is low. The common-mode range of POS and NEG is 0 to 2V. POS and NEG should be generated from resistor-dividers from the output.
16	NEG	Feedback Offset Adjust Negative Input. The output shifts by 100% (typ) of differential input voltage appearing between POS and NEG when $\overline{DPSLP}$ is low. The common-mode range of POS and NEG is 0 to 2V. POS and NEG should be generated from resistor-dividers from the output.
17	CCI	Current Balance Compensation. Connect a 470pF capacitor between CCI and FB (see the *Current Balance Compensation* section). An additional 470kΩ to 1MΩ resistor between CCI and FB for low-frequency operation.
18	FB	Feedback Input. FB is internally connected to both the feedback input and the output of the voltage-positioning op amp (Figure 2). Connect a resistor between FB and OAIN- (Figure 1) to set the voltage-positioning gain (see the *Setting Voltage Positioning* section).
19	OAIN-	Dual-Mode Op Amp Inverting Input and Op Amp Disable Input. When using the internal op amp for additional voltage-positioning gain (Figure 1), connect to the negative terminal of the current-sense resistor through a 1.0kΩ ±1% resistor as described in the *Setting Voltage Positioning* section. Connect OAIN- to V_{CC} to disable the op amp. The logic threshold to disable the op amp is approximately V_{CC} - 1V.
20	OAIN+	Op Amp Noninverting Input. When using the internal op amp for additional voltage-positioning gain (Figure 1), connect to the positive terminal of the current-sense resistor through a resistor as described in the *Setting Voltage Positioning* section.
21	$\overline{PSI}$	Power-Status Indicator Input. When $\overline{PSI}$ is pulled low, the MAX1987/MAX1988 immediately enter pulse-skipping operation, blank the IMVPOK output high, and blank the $\overline{CLKEN}$ output low.
22	SYSPOK	System Power-Good Input. Primarily, SYSPOK serves as the wired NOR junction of the open-drain power-good signals for the V_{CCP} and V_{CCMCH} supplies. A falling edge on SYSPOK shuts down the MAX1987/MAX1988 and sets the fault latch. Toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V to restart the controller.
23	IMVPOK	Open-Drain Power-Good Output. After output voltage transitions, except during power-up and power-down, if OUT is in regulation, then IMVPOK is high impedance. IMVPOK is high impedance whenever the slew rate control is active (output voltage transitions). IMVPOK is forced low in shutdown. A pullup resistor on IMVPOK causes additional finite shutdown current. IMVPOK also reflects the state of SYSPOK and includes a 3ms (min) delay for power-up.
24	$\overline{CLKEN}$	Clock Enable Logic Output. This inverted logic output indicates when SYSPOK is high and the output voltage sensed at FB is in regulation. $\overline{CLKEN}$ is forced low during VID transitions.
25–30	D5–D0	Low-Voltage VID DAC Code Inputs. D0 is the LSB, and D5 is the MSB of the internal 6-bit VID DAC (Table 4). The D0–D5 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. In all normal active modes (modes other than suspend mode and boot mode), the output voltage is set by the VID code indicated by the D0–D5 logic-level voltages on D0–D5. In suspend mode (SUS = high), the decoded state of the four-level S0 to S2 inputs sets the output voltage. In boot mode (see the *Power-Up Sequence* section), the decoded state of the four-level B0 to B2 inputs set the output voltage.

Pin Description (continued)

PIN	NAME	FUNCTION
31	$\overline{DDO}$	Driver-Disable Output. This TTL logic output can be used to disable the driver outputs on slave-switching regulator controllers, such as the MAX1980—forcing a high-impedance condition and making it possible for the MAX1987/MAX1988 master controller to operate in low-current SKIP mode. $\overline{DDO}$ goes low 32 R_{TIME} clock cycles after the MAX1987/MAX1988 complete a transition to the suspend mode or deep-sleep voltage (see the *Low-Power Pulse Skipping* section). Another 32 clock cycles later, the MAX1987/MAX1988 enter automatic pulse-skipping operation.
32	BSTM	Main Boost Flying Capacitor Connection. An optional resistor in series with BSTM allows the DHM pullup current to be adjusted.
33	LXM	Main Inductor Connection. LXM is the internal lower supply rail for the DHM high-side gate driver.
34	DHM	Main High-Side Gate-Driver Output Swings LXM to BSTM
35	DLM	Main Low-Side Gate Driver Output. DLM swings from PGND to V_{DD}. DLM is forced high after the MAX1987/MAX1988 power down ($\overline{SHDN}$ = GND) or when the MAX1987 detects an overvoltage fault. The MAX1988 does not include overvoltage protection.
36	V_{DD}	Supply Voltage Input for the DLM and DLS Gate Drivers. Connect to the system supply voltage (4.5V to 5.5V). Bypass V_{DD} to PGND with a 2.2µF or greater ceramic capacitor, as close to the IC as possible.
37	PGND	Power Ground. Ground connection for the low-side gate drivers DLM and DLS.
38	DLS	Secondary Low-Side Gate Driver Output. DLS swings from PGND to V_{DD}. DLS is forced high after the MAX1987/MAX1988 power down ($\overline{SHDN}$ = GND) or when the MAX1987 detects an overvoltage fault. The MAX1988 does not include overvoltage protection.
39	DHS	Secondary High-Side Gate-Driver Output Swings LXS to BSTS
40	LXS	Secondary Inductor Connection. LXS is the internal lower supply rail for the DHS high-side gate driver.
41	BSTS	Secondary Boost Flying Capacitor Connection. An optional resistor in series with BSTS allows the DHS pullup current to be adjusted.
42	V+	Battery Voltage Sense Connection. Used only for PWM one-shot timing. DH_ on-time is inversely proportional to input voltage over a range of 2V to 28V.
43	SUS	Suspend-Mode Control Input. When SUS is high, the regulator slews to the suspend voltage level. This level is set with four-level logic signals at the S0 to S2 inputs. 32 clock cycles after the transition to the suspend-mode voltage is completed, $\overline{DDO}$ goes low (see the *Low-Power Pulse Skipping* section). Another 32 clock cycles later, the MAX1987/MAX1988 are allowed to enter pulse-skipping operation.
44	$\overline{DPSLP}$	Deep-Sleep Control Input. When $\overline{DPSLP}$ is low, the system enters the deep-sleep state and the regulator applies the appropriate deep-sleep offset. The MAX1987/MAX1988 add the offset measured at the POS and NEG pins to the output. 32 clock cycles after the deep-sleep transition is completed, $\overline{DDO}$ goes low (see the *Low-Power Pulse Skipping* section). Another 32 clock cycles later, the MAX1987/MAX1988 are allowed to enter pulse-skipping operation.
45	CMP	Main Inductor Positive Current-Sense Input
46	CMN	Main Inductor Negative Current-Sense Input
47	CSN	Secondary Inductor Negative Current-Sense Input
48	CSP	Secondary Inductor Positive Current-Sense Input

Table 1. Component Selection for Standard Multiphase Applications (Figure 1)

DESIGNATION	COMPONENT
Input Voltage Range*	7V to 24V
VID Output Voltage (D5–D0)	1.356V (D5–D0 = 010110)
Boot Voltage (B0 to B2)	1.372V (B2 = REF, B1 = REF, B0 = REF)
Suspend Voltage (S0 to S2)	0.748V (S2 = V_{CC}, S1 = V_{CC}, S0 = GND)
Deep-Sleep Offset Voltage (POS, NEG)	2.7%
Maximum Load Current (typ)	40A
Inductor (L_M, L_S)	0.6µH Panasonic ETQP1H0R6BFA or Sumida CDEP134H-0R6
Switching Frequency	300kHz (TON = float)
High-Side MOSFET (N_H, per phase)	Fairchild (2) FDS6694 or Siliconix (2) Si4860DY
Low-Side MOSFET (N_L, per phase)	Fairchild (2) FDS6688 or Siliconix (2) Si4362DY
Input Capacitance (C_{IN})	(6) 10µF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M
Output Capacitance (C_{OUT})	(3) 470µF, 2.5V Sanyo 2R5TPD470M or (4) 330µF, 2.5V Panasonic EEFUEOD33IXR
Current-Sense Resistor (R_{SENSE}, per phase)	1.5mΩ Panasonic ERJM1WTJ1M5U

**Input voltages less than 7V require additional input capacitance.*

Table 2. Component Suppliers

MANUFACTURER	PHONE	WEBSITE
BI Technologies	714-447-2345 (USA)	www.bitechnologies.com
Central Semiconductor	631-435-1110 (USA)	www.centralsemi.com
Coilcraft	800-322-2645 (USA)	www.coilcraft.com
Coiltronics	561-752-5000 (USA)	www.coiltronics.com
Fairchild Semiconductor	888-522-5372 (USA)	www.fairchildsemi.com
International Rectifier	310-322-3331 (USA)	www.irf.com
Kemet	408-986-0424 (USA)	www.kemet.com
Panasonic	847-468-5624 (USA)	www.panasonic.com
Sanyo	65-281-3226 (Singapore) 408-749-9714 (USA)	www.secc.co.jp
Siliconix (Vishay)	203-268-6261 (USA)	www.vishay.com
Sumida	408-982-9660 (USA)	www.sumida.com
Taiyo Yuden	03-3667-3408 (Japan) 408-573-4150 (USA)	www.t-yuden.com
TDK	847-803-6100 (USA) 81-3-5201-7241 (Japan)	www.component.tdk.com
Toko	858-675-8013 (USA)	www.tokoam.com

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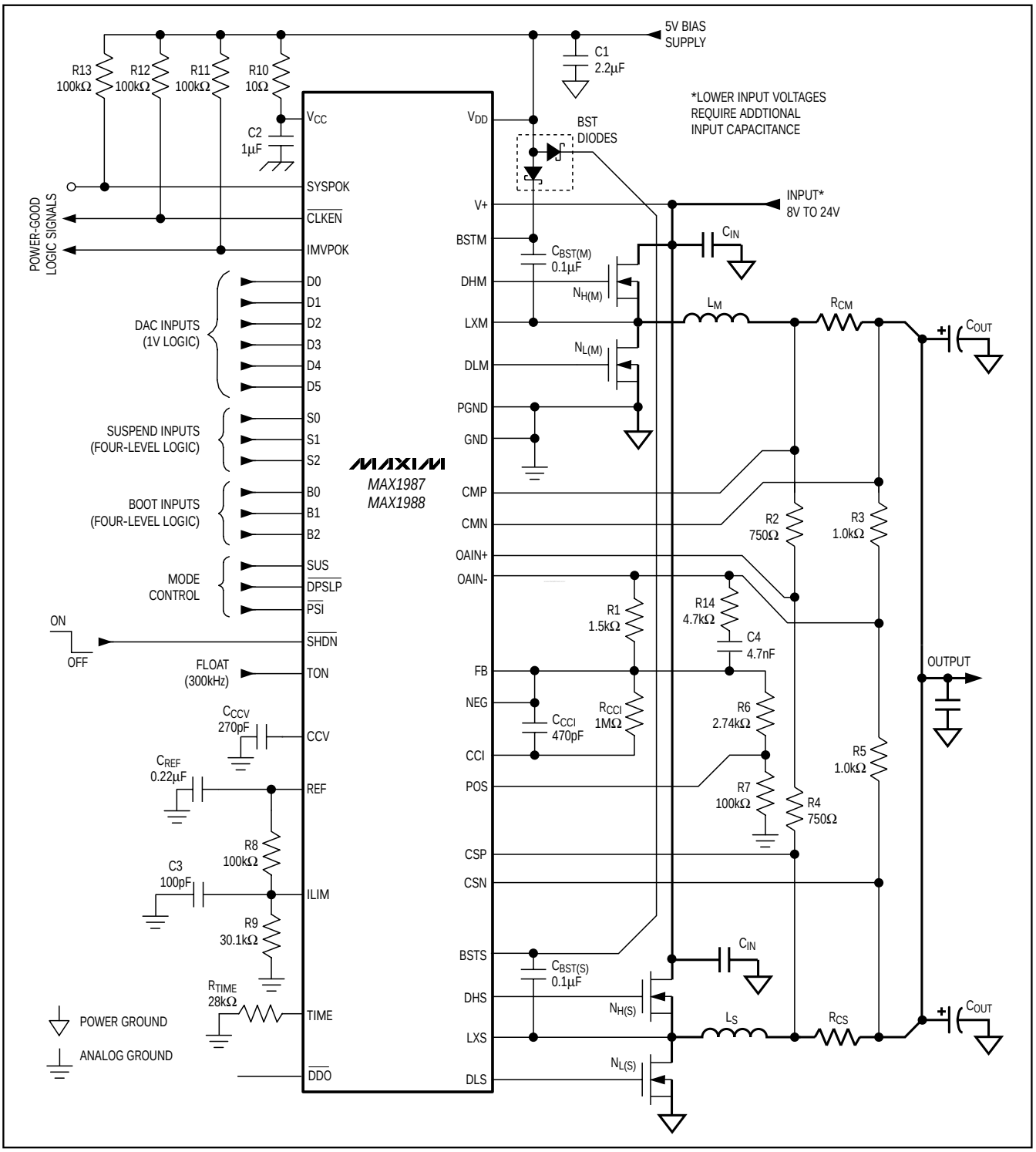

Figure 1. Standard Application Circuit (Master)

Detailed Description

5V Bias Supply (VCC and VDD)

The MAX1987/MAX1988 require an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95% efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If standalone capability is needed, the +5V bias supply can be generated with an external linear regulator.

The 5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$
$$= 10mA \text{ to } 100mA \text{ (typ)}$$

where I_{CC} is 1.7mA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V+ and V_{DD} can be connected together if the input power source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Free-Running, Constant On-Time PWM Controller with Input Feedforward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feedforward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage, and directly proportional to output voltage and the difference between the main and secondary inductor currents (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot is triggered if the error comparator is low, the low-side switch currents are below the current-limit threshold, and the minimum off-time one-shot has timed out. The controller maintains 180° out-of-phase operation by alternately triggering the main and secondary phases after the error comparator drops below the output voltage set point.

On-Time One-Shot (TON)

The core of each phase contains a fast, low-jitter, adjustable one-shot that sets the high-side MOSFET's on-time. The one-shot for the main phase simply varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the V+ input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON(MAIN)} = \frac{K(V_{FB} + 0.075V)}{V_{IN}}$$

where K is set by the TON pin-strap connection (Table 3) and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch.

The one-shot for the secondary phase varies the on-time in response to the input voltage and the difference between the main and secondary inductor currents. Two identical transconductance amplifiers integrate the difference between the master and slave current-sense signals. The summed output is internally connected to CCI, allowing adjustment of the integration time constant with a compensation network connected between CCI and FB. The resulting compensation current and voltage are determined by the following equations:

$$I_{CCI} = g_M(V_{CMP} - V_{CMN}) - g_M(V_{CSP} - V_{CSN})$$
$$V_{CCI} = V_{FB} + I_{CCI}Z_{CCI}$$

where Z_{CCI} is the impedance at the CCI output.

The secondary on-time one-shot uses this integrated signal (V_{CCI}) to set the secondary high-side MOSFETs on-time. When the main and secondary current-sense signals (V_{CM} = V_{CMP} - V_{CMN} and V_{CS} = V_{CSP} - V_{CSM}) become unbalanced, the transconductance amplifiers adjust the secondary on time, which increases or decreases the secondary inductor current until the current-sense signals are properly balanced:

$$t_{ON(2ND)} = K\left(\frac{V_{CCI} + 0.075V}{V_{IN}}\right)$$
$$= K\left(\frac{V_{FB} + 0.075V}{V_{IN}}\right) + K\left(\frac{I_{CCI}Z_{CCI}}{V_{IN}}\right)$$
$$= (\text{Main On-time}) + (\text{Secondary Current Balance Correction})$$

This algorithm results in a nearly constant switching frequency and balanced inductor currents, despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the

frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output-voltage ripple. The on-time one-shots have good accuracy at the operating points specified in the *Electrical Characteristics* (±10% at 200kHz and 300kHz, ±12% at 550kHz). On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* can vary over a wider range. For example, the 550kHz setting typically runs about 10% slower with inputs much greater than 12V due to the very short on-times required.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PC board copper losses in the output and ground tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in PWM mode (SUS = low, $\overline{DPSLP}$ = low) and during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{(V_{OUT} + V_{DROP1})}{t_{ON}(V_{IN} + V_{DROP1} - V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PC board resistances; and t_{ON} is the on-time as determined above.

Table 3. Approximate K-Factor Errors

TON CONNECTION	FREQUENCY SETTING (kHz)	K-FACTOR (µs)	MAX K-FACTOR ERROR (%)
V_{CC}	200	5	±10
Float	300	3.3	±10
REF	550	1.8	±12.5
GND	1000	1.0	±12.5

Current Balance

Without active current-balance circuitry, the current matching between phases depends on the MOSFETs' on-resistance ($R_{DS(ON)}$), thermal ballasting, on-/off-time matching, and inductance matching. For example, variation in the low-side MOSFET on-resistance (ignoring thermal effects) results in a current mismatch that is proportional to the on-resistance difference:

$$I_{MAIN} - I_{2ND} = I_{MAIN}\left[1 - \left(\frac{R_{MAIN}}{R_{2ND}}\right)\right]$$

Thermal ballasting as the loaded MOSFETs heat up actually improves the current balance. The stronger MOSFET (the phase with the lower $R_{DS(ON)}$) pulls more current, which heats up the MOSFET more than the other phase, increasing the thereby reducing the current mismatch. Taking thermal effects into account, the on-resistance of the switching MOSFETs can be determined by the following equation:

$$R_{DS(ON)} = \frac{R_{TA(25)}}{1 - (R_{TA(25)} I_L^2 R_{\theta JA} \Delta R_{TEMPCO}}$$

where $R_{TA(25)}$ is the on-resistance at room temperature, I_L is the inductor current through the MOSFET, $R_{\theta JA}$ (°C/W) is the junction-to-ambient thermal resistance of the MOSFET package, and ΔR_{TEMPCO} (0.5%/°C) is the temperature coefficient of the MOSFET. Thermal ballasting can typically reduce the current mismatch by as much as a third. Unfortunately, mismatches between on-times, off-times, and inductor values increase the worst-case current imbalance making it impossible to passively guarantee accurate current balancing.

The MAX1987/MAX1988 integrate the difference between the current-sense voltages and adjusts the on-time of the secondary phase to maintain current balance. The current balance now relies on the accuracy of the current-sense resistors instead of the inaccurate, thermally sensitive on-resistance of the low-side tracking MOSFETs. With active current balancing, the current mismatch is simply determined by the current-sense resistor values and the offset voltage of the transconductance amplifiers:

$$I_{OS(BAL)} = I_{LM} - I_{LS} = \frac{V_{OS(IBAL)}}{R_{SENSE}}$$

where $R_{SENSE} = R_{CM} = R_{CS}$ and $V_{OS(IBAL)}$ is the current-balance offset specification in the *Electrical Characteristics*.

The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches resulting in different dI/dt for the two phases. The time it takes the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Dual 180° Out-of-Phase Operation

The two phases in the MAX1987/MAX1988 operate 180° out-of-phase to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making the MAX1987/MAX1988 ideal for high-power, cost-sensitive applications.

Typically, switching regulators provide transfer power using only one phase instead of dividing the power among several phases. In these applications, the input capacitors must support high-instantaneous current requirements. The high RMS ripple current can lower efficiency due to I^2R power loss associated with the input capacitor's effective series resistance (ESR). Therefore, the system typically requires several low-ESR input capacitors in parallel to minimize input voltage ripple, to reduce ESR-related power losses, and to meet the necessary RMS ripple-current rating.

With the MAX1987/MAX1988, the controller shares the current between two phases that operate 180° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of either phase is effectively halved, resulting in reduced input-voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance can be achieved with fewer or less expensive input capacitors.

Transient Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 180° out-of-phase when a transient occurs actually respond slower than an equivalent single-phase controller. In order to provide fast transient response, the MAX1987/MAX1988 support a phase overlap mode that allows the individual phases to operate simultaneously when heavy load transients are detected, effectively reducing the response time. After either high-side MOSFET turns off, if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on both high-side MOSFETs during the next on-time cycle. This maximizes the total inductor current slew rate. The phases remain overlapped until the output voltage exceeds the regulation voltage after the minimum off-time expires.

After the phase overlap mode ends, the controller automatically begins with the opposite phase. For example, if the secondary phase provided the last on-time pulse before overlap operation began, the controller starts switching with the main phase when overlap operation ends.

Integrator Amplifiers/Output Voltage Offsets

Two transconductance amplifiers provide a fine adjustment to the output regulation point (Figure 2). One amplifier forces the DC average of the feedback voltage to equal the VID DAC setting. The second amplifier is used to create small positive or negative offsets from the VID DAC setting, using the POS and NEG pins.

The feedback amplifier integrates the feedback voltage, allowing accurate DC output voltage regulation regardless of the output ripple voltage. The feedback amplifier has the ability to shift the output voltage by ±8%. The differential input voltage range is at least ±80mV total, including DC offset and AC ripple. The integration time constant can be set easily with one capacitor at the CCV pin. Use a capacitor value of 47pF to 1000pF (270pF typ).

The POS/NEG amplifier is used to add small offsets to the VID DAC setting in deep-sleep mode ($\overline{DPSLP}$ = low). The offset amplifier is summed directly with the feedback voltage, making the offset gain independent of the DAC code. This amplifier has the ability to offset the output by ±200mV. To create an output offset, bias POS and NEG to a voltage (typically V_{OUT} or REF) within their 0 to 2V common-mode range, and offset them from one another with a resistive divider (Figure 1). If V_{POS} is higher than V_{NEG}, then the output is shifted in the positive direction. If V_{NEG} is higher than V_{POS}, then the output is shifted in the negative direction. The output offset equals the voltage difference from POS to NEG.

Forced-PWM Operation (Normal Mode)

During normal mode, when the CPU is actively running (SUS = low, $\overline{DPSLP}$ = high, $\overline{PSI}$ = high), the MAX1987/MAX1988 operate with the low-noise forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparator, forcing the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform. The benefit of forced-PWM mode is to keep the switching frequency fairly constant.

Forced-PWM operation comes at a cost: the no-load 5V bias supply current remains between 10mA to 100mA, depending on the external MOSFETs and switching

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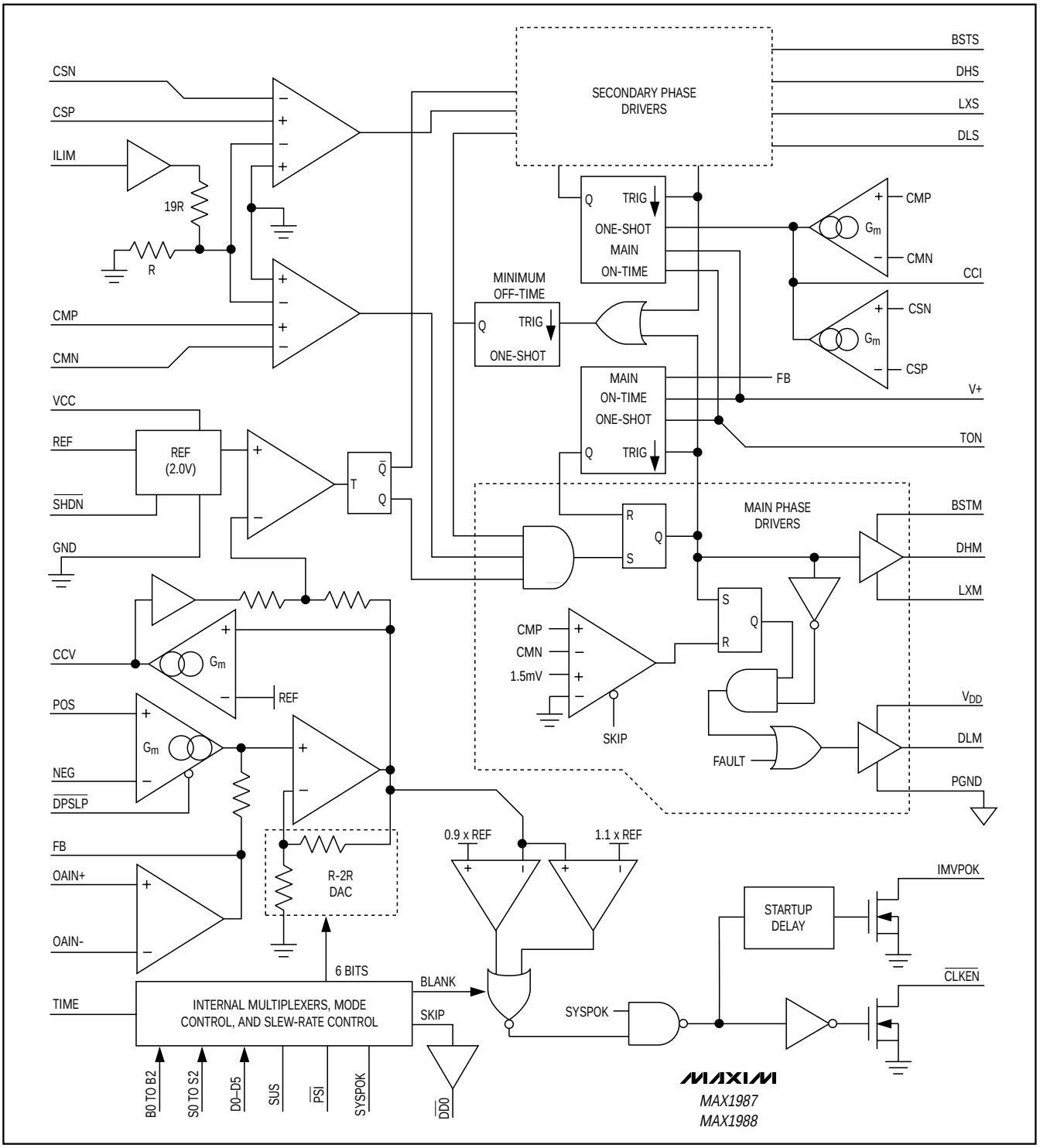

Figure 2. MAX1987/MAX1988 Functional Diagram

frequency. To maintain high efficiency under light-load conditions, the MAX1987/MAX1988 automatically switch to the low-power pulse-skipping control scheme after entering suspend or deep-sleep mode.

During output voltage and mode transitions ($\overline{PSI}$ = high), the MAX1987/MAX1988 use forced-PWM operation to ensure fast, accurate transitions. Since forced-PWM operation disables the zero-crossing comparator, the inductor current reverses under light loads, quickly discharging the output capacitors. The controller maintains forced-PWM operation for 32 clock cycles (set by R_{TIME}) after the controller sets the last DAC code value to guarantee the output voltage settles properly before entering pulse-skipping operation.

Low-Power Pulse Skipping

During deep-sleep mode ($\overline{DPSLP}$ = low), low-power suspend (SUS = high), or pulse-skipping override mode ($\overline{PSI}$ = low), the MAX1987/MAX1988 use an automatic pulse-skipping control scheme, alternately switching both phases in order to maintain the current balance.

For deep-sleep mode, when the CPU pulls $\overline{DPSLP}$ low, the MAX1987/MAX1988 shift the output voltage to incorporate the offset voltage set by the POS and NEG inputs (Figure 3). 32 R_{TIME} clock cycles after $\overline{DPSLP}$ goes low, the controller pulls the driver-disable output ($\overline{DDO}$) low. An additional 30 R_{TIME} clock cycles later, the MAX1987/MAX1988 enter low-power operation, allowing automatic pulse skipping under light loads. When the CPU drives $\overline{DPSLP}$ high, the MAX1987/MAX1988 immediately enter forced-PWM operation, force $\overline{DDO}$ high, and eliminate the output offset, slewing the output to the operating voltage set by the D0–D5 inputs. When either $\overline{DPSLP}$ transition occurs, the MAX1987/MAX1988 force IMVPOK high and CLKEN low for 32 R_{TIME} clock cycles.

When entering suspend mode (SUS driven high), the MAX1987/MAX1988 slew the output down to the suspend output voltage set by S0 to S2 inputs (Figure 4). 32 R_{TIME} clock cycles after the slew-rate controller reaches the last DAC code (see the *Output Voltage Transition Timing* section), the $\overline{DDO}$ is asserted low. After an additional 30 R_{TIME} clock cycles, the MAX1987/MAX1988 enter low-power operation, allowing pulse skipping under light loads. When the CPU pulls SUS low, the MAX1987/MAX1988 immediately enter forced-PWM operation, force $\overline{DDO}$ high, and slew the output up to the operating voltage set by the D0–D5 inputs. When either SUS transition occurs, the MAX1987/MAX1988 blank IMVPOK and $\overline{CLKEN}$, preventing IMVPOK from going low and $\overline{CLKEN}$ from going high. The blanking remains active until the slew rate controller has reached the last DAC code and 32 additional R_{TIME} clock pulses have passed.

When $\overline{PSI}$ is pulled low, the MAX1987/MAX1988 override forced-PWM operation and use the automatic pulse-skipping control scheme regardless of the state of the SUS and $\overline{DPSLP}$ control inputs. Once $\overline{PSI}$ is pulled low, the controller asserts the driver-disable output ($\overline{DDO}$ = low), forces IMVPOK high, and forces $\overline{CLKEN}$ low. When $\overline{PSI}$ is used during mode transitions, the constant IMVPOK and $\overline{CLKEN}$ blanking allows indefinite settling times.

In applications with more than two phases, the driver-disable signal is used to force one or more slave regulators into a high-impedance state. When the master's $\overline{DDO}$ output is driven low, the slave controller with driver disable (MAX1980) forces its $DL_{(SLAVE)}$ and $DH_{(SLAVE)}$ gate drivers low, effectively disabling the slave controller. Disabling the slave controller allows the MAX1987/MAX1988 to enter low-power pulse skipping operation under low-power conditions, improving light-load efficiency. When $\overline{DDO}$ is driven high, the slave controller (MAX1980) enables the drivers, allowing normal forced-PWM operation. For detailed operation with slave controllers, refer to the MAX1980 data sheet.

Automatic Pulse-Skipping Switchover

In skip mode ($\overline{PSI}$ = low, SUS = high, or $\overline{DPSLP}$ = low), an inherent automatic switchover to PFM takes place at light loads (Figure 5). This switchover is affected by a comparator that truncates the low-side switch on time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across the current-sense resistors. Once V_{C_P} - V_{C_N} drops below 1.5mV (typ), the comparator forces DL_ low (Figure 2). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 6). For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles.

The total load current at the PFM/PWM crossover threshold ($I_{LOAD(SKIP)}$) is approximately:

$$I_{LOAD(SKIP)} = \left(\frac{V_{OUT}K}{L}\right)\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

where K is the on-time scale factor (Table 3).

Dual-Phase, Quick-PWM Controllers for IMVP-IV CPU Core Power Supplies

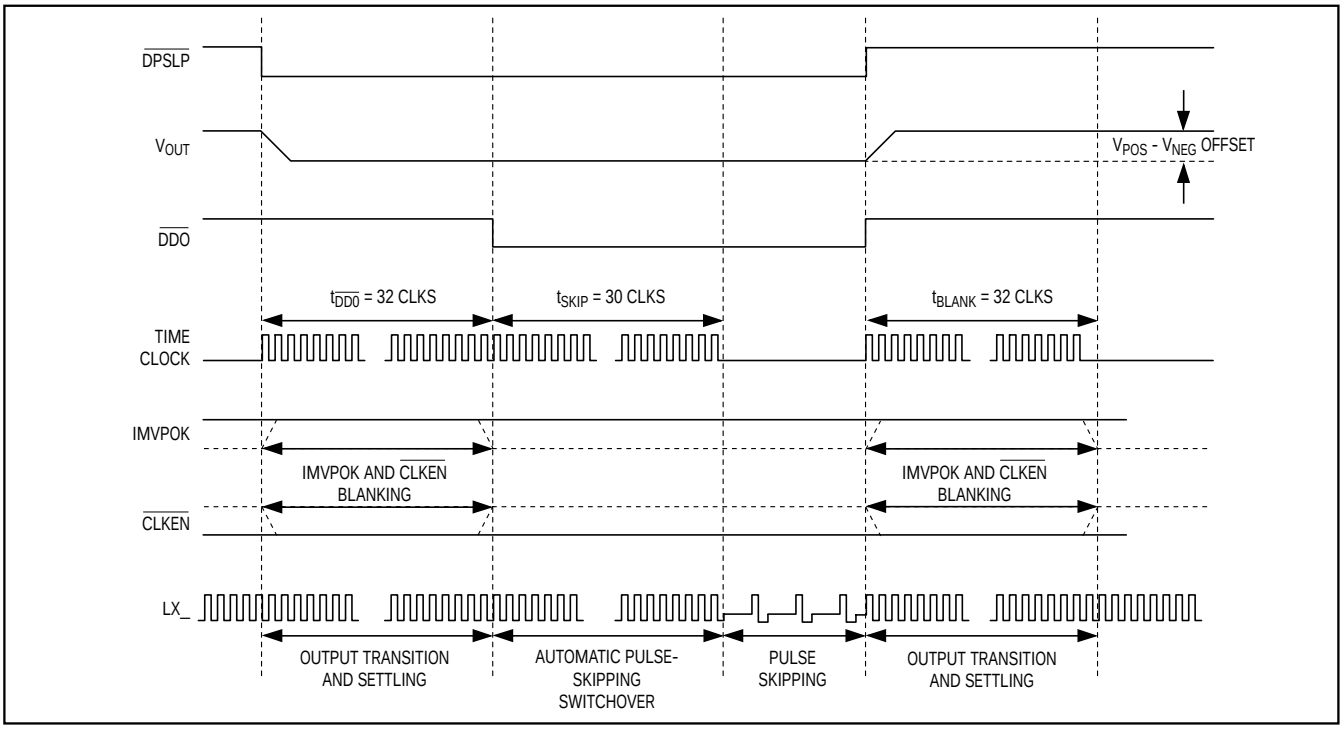

Figure 3. MAX1987/MAX1988 Deep Sleep Transition

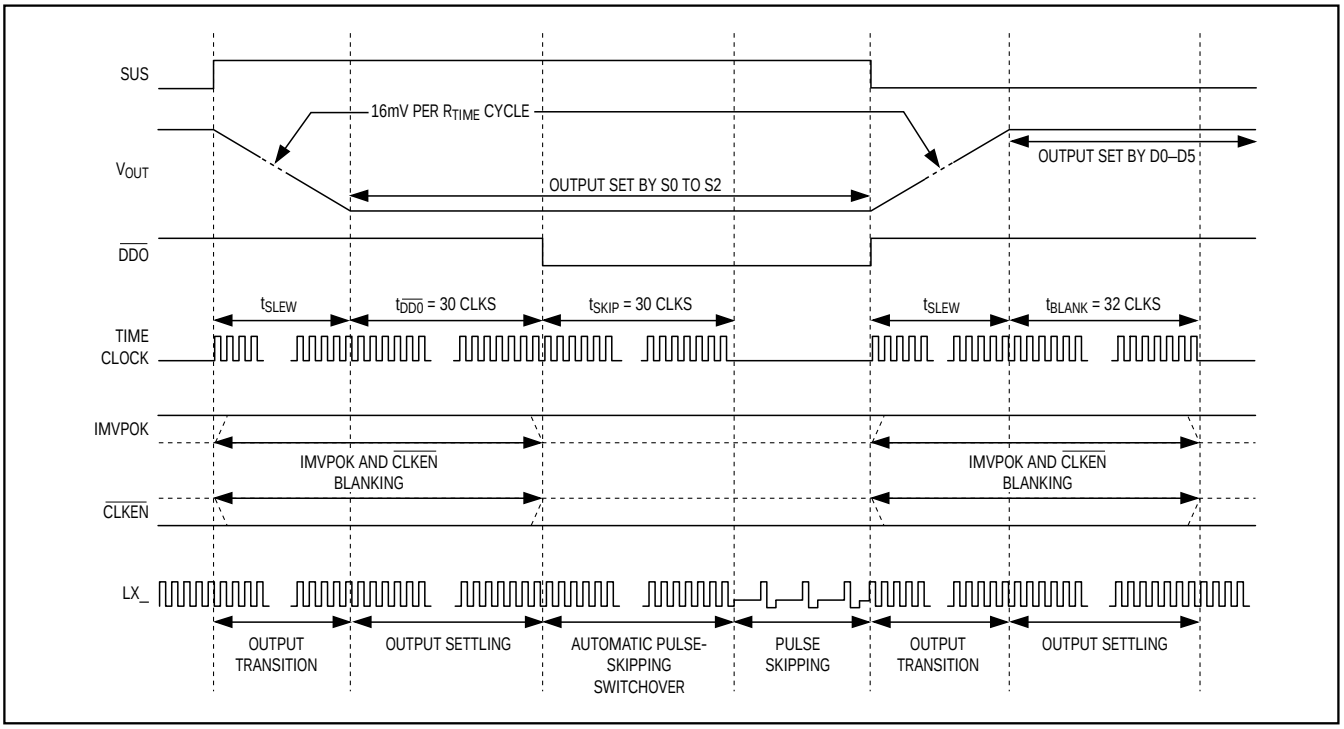

Figure 4. MAX1987/MAX1988 Suspend Transition

For example, in the standard application circuit this becomes:

$$\left(\frac{1.3V \times 3.3\mu s}{0.6\mu H}\right)\left(\frac{12V - 1.3V}{12V}\right) = 6.4A$$

The switching waveforms can appear noisy and asynchronous when light loading activates pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs between PFM noise and light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low-input voltage levels.

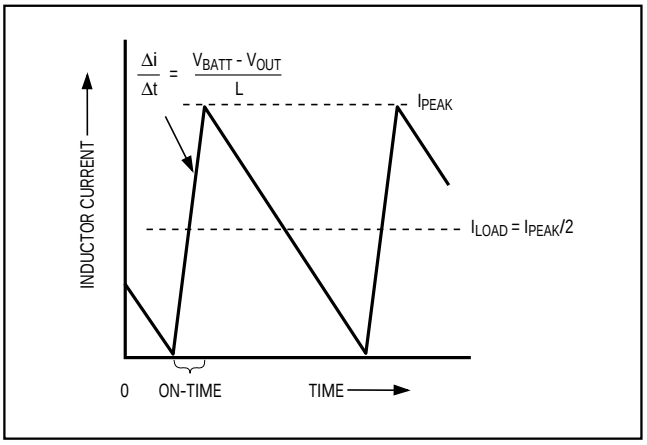

Figure 5. Pulse-Skipping/Discontinuous Crossover Point

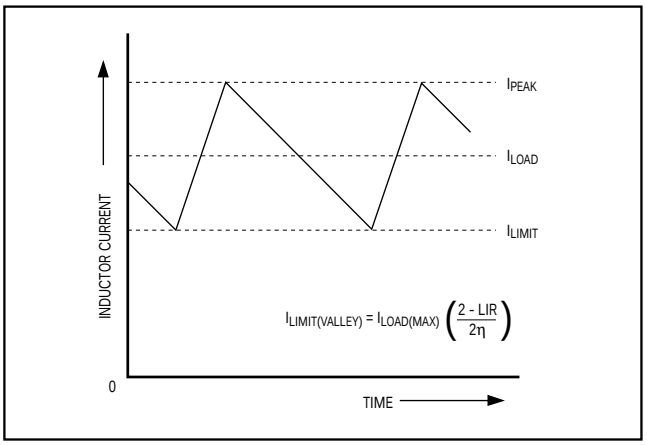

Figure 6. "Valley" Current-Limit Threshold Point

Current-Limit Circuit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses current-sense resistors from CMP to CMN and from CSP to CSN as the current-sensing elements (Figure 1). If the current-sense signal of the selected phase is above the current-limit threshold, the PWM controller does not initiate a new cycle (Figure 2) until the inductor current of the selected phase drops below the valley current-limit threshold. When either phase trips the current limit, both phases are effectively current limited since the interleaved controller does not initiate a cycle with either phase.

Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit, and therefore tracks the positive current limit when ILIM is adjusted. When a phase drops below the negative current limit, the controller immediately activates an on-time pulse—DL_ turns off, and DH_ turns on—allowing the inductor current to remain above the negative current threshold.

The current-limit threshold is adjusted with an external resistive voltage-divider at ILIM. The current-limit threshold voltage adjustment range is from 10mV to 75mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/20th the voltage seen at ILIM. The threshold defaults to 30mV when ILIM is connected to V_{CC}. The logic threshold for switchover to the 30mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CMP, CMN, CSP, CSN).

MOSFET Gate Drivers (DH, DL)

The DH_ and DL_ drivers are optimized for driving moderately sized, high-side and larger, low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{IN} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL_ output and prevents the high-side FET from turning on until DL_ is fully off. There must

be a low-resistance, low-inductance path from the DL_ driver to the MOSFET gate in order for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1987/MAX1988 interprets the MOSFET gate as "off" while there is actually charge still left on the gate. Use very short, wide traces (50mils to 100mils wide if the MOSFET is 1in from the device). The dead time at the other edge (DH_ turning off) is determined by a fixed 35ns internal delay.

The internal pulldown transistor that drives DL_ low is robust, with a 0.4Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when LX_ switches from ground to V_{IN}. Applications with high input voltages and long, inductive DL_ traces can require additional gate-to-source capacitance to ensure fast rising LX_ edges do not pull up the low-side MOSFETs' gate voltage, causing shoot-through currents. The capacitive coupling between LX_ and DL_ created by the MOSFETs' gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the minimum threshold voltage:

$$V_{GS(TH)} < V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage can cause problems in marginal designs. Typically, adding a 4700pF between DL_ and power ground (C_{NL} in Figure 7), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternatively, shoot-through currents can be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST_ slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 7). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

Voltage-Positioning Amplifier

The MAX1987/MAX1988 include an independent op amp for adding gain to the voltage positioning sense path. The voltage-positioning gain allows the use of low-value, current-sense resistors in order to minimize power dissipation. This 3MHz gain-bandwidth amplifier

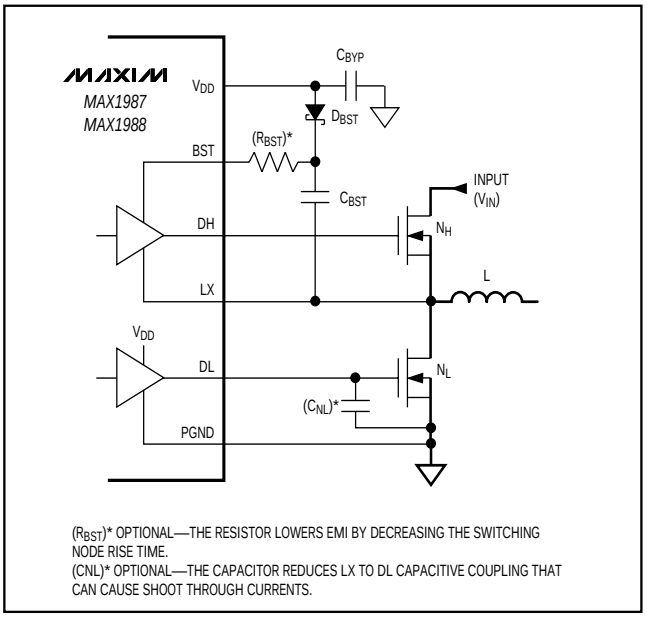

Figure 7. Optional Gate Driver Circuitry

was designed with low offset voltage (70µV typ) to meet the IMVP-IV output accuracy requirements.

The inverting (OAIN-) and noninverting (OAIN+) inputs are used to differentially sense the voltage across the voltage-positioning sense resistor. The op amp's output is internally connected to the regulator's feedback input (FB). The op amp should be configured as a noninverting, differential amplifier as shown in Figures 1 and 10. The voltage-positioning slope is set by properly selecting the feedback resistor connected from FB to OAIN- (see the *Setting Voltage Positioning* section). For applications using a slave controller, additional differential input resistors (summing configuration) should be connected to the slave's voltage-positioning sense resistor (Figures 1 and 10). Summing together both the master and slave current-sense signals ensures that the voltage-positioning slope remains constant when the slave controller is disabled.

In applications that do not require voltage positioning gain, the amplifier can be disabled by connecting the OAIN- pin directly to V_{CC}. The disabled amplifier's output becomes high impedance, guaranteeing that the unused amplifier does not corrupt the FB input signal. The logic threshold to disable the op amp is approximately V_{CC} - 1V.

Power-Up Sequence

The MAX1987/MAX1988 are enabled when $\overline{SHDN}$ is driven high (Figure 8). First, the reference powers up. Once

the reference exceeds its undervoltage lockout threshold, the PWM regulator becomes active. The slew-rate controller ramps up the output voltage in 16mV increments to the selected boot code value (B0 to B2, Table 7). The ramp rate is set with the R_{TIME} resistor (see the *Output Voltage Transition Timing* section).

SYSPOK serves as the combined power-good input for V_{CCP} and V_{CCMCH}. Once these supplies are within ±10% of their output voltage, their power-good outputs become high impedance, allowing SYSPOK to be pulled high. Approximately 50µs after the MAX1987/MAX1988 detect both a logic high voltage on SYSPOK and the slew-rate controller reaches the DAC code set by B0 to B2, the controller pulls $\overline{CLKEN}$ low and slews the output to the proper operating voltage (Table 4).

When $\overline{CLKEN}$ goes low, the MAX1987/MAX1988 keep IMVPOK low for an additional 3ms (min), guaranteeing that the CPU has time to start properly. If the MAX1987/MAX1988 do not detect a fault, then IMVPOK is pulled high once the 3ms timer expires.

Power-On Reset

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch, activating boot mode, and preparing the PWM for operation. V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching, and forces the DL gate driver high (to enforce output overvoltage protection). When V_{CC} rises above 4.25V, the DAC inputs are sampled and the output voltage begins to slew to the boot voltage (Table 7).

For automatic startup, the battery voltage should be present before V_{CC}. If the MAX1987/MAX1988 attempt to bring the output into regulation without the battery voltage present, the fault latch trips. The $\overline{SHDN}$ pin can be toggled to reset the fault latch.

Input Undervoltage Lockout

During startup, the V_{CC} UVLO circuitry forces the DL gate driver high and the DH gate driver low, inhibiting switching until an adequate supply voltage is reached. Once V_{CC} rises above 4.25V, valid transitions detected at the trigger input initiate a corresponding on-time pulse (see the *On-Time One-Shot* section).

If the V_{CC} voltage drops below 4.25V, it is assumed that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, DL is forced high in this mode, to force the output to ground. This results in large negative inductor current and possibly small negative output voltages. If V_{CC} is likely to drop in this fashion, the output can be clamped with a Schottky diode to PGND to reduce the negative excursion.

Shutdown

When $\overline{SHDN}$ or SYSPOK goes low, the MAX1987/MAX1988 enter low-power shutdown mode. IMVPOK is pulled low and $\overline{CLKEN}$ is driven high immediately. The

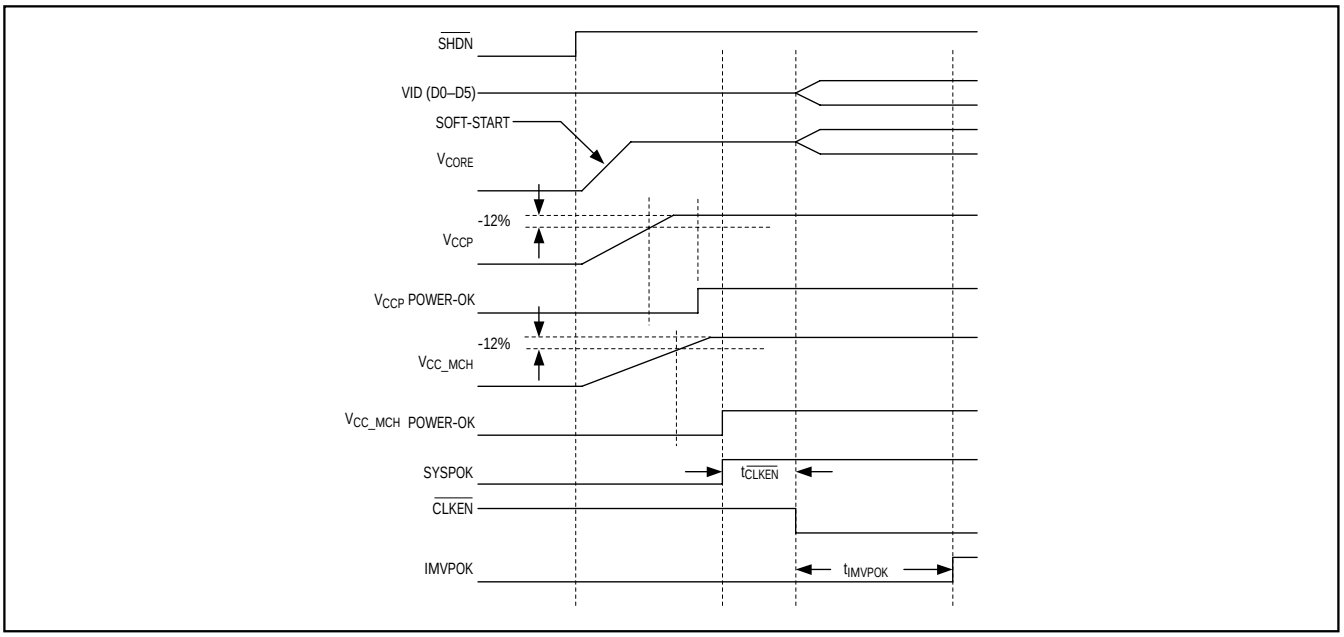

Figure 8. Power-Up Sequence Timing Diagram

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output voltage ramps down to 0V in 16mV steps at the clock rate set by R_{TIME}. When the DAC reaches the 0V setting, DL goes high, DH goes low, the reference is turned off, the boot mode latch is cleared, and the supply current drops to about 1µA. When a fault condition (output undervoltage lockout, thermal shutdown, or a falling edge on SYSPOK) activates the shutdown sequence, the controller sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the MAX1987/MAX1988, toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V.

When $\overline{SHDN}$ goes high, the reference powers up, and after the reference UVLO is passed, the DAC target is evaluated and switching begins. The slew-rate controller ramps up from 0V in 16mV steps to the currently selected boot-code value (see the *Power-Up Sequence* section). There is no traditional soft-start (variable current limit) circuitry, so full output current is available immediately.

Internal Multiplexers

The MAX1987/MAX1988 have two unique internal DAC input multiplexers (muxes) that can select one of three different DAC code settings for different processor states, depending on the power-up sequence and SUS state. On startup, the controller selects the DAC code from the B0 to B2 (SUS = low) or S0 to S2 (SUS = high) input decoder (Figure 9). Once SYSPOK goes high and the MAX1987/MAX1988 properly regulate to the boot voltage, a second multiplexer selects the DAC code from either D0–D5 (SUS = low) or S0 to S2 (SUS = high).

DAC Inputs (D0–D5)

During normal operation (SUS = low), the digital-to-analog converter (DAC) programs the output voltage using the D0–D5 inputs. D0–D5 are low-voltage (1V) logic inputs, designed to interface directly with the IMVP-IV CPU. Do not leave D0–D5 unconnected. D0–D5 can be changed while the MAX1987/MAX1988 are active, initiating a transition to a new output voltage level. Change D0–D5 together, avoiding greater than 1µs skew between bits. Otherwise, incorrect DAC readings can cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages (Table 5) are compatible with IMVP-IV specification.

Four-Level Logic Inputs

TON, B0 to B2, and S0 to S2 are four-level logic inputs. These inputs help expand the functionality of the controller without adding an excessive number of pins. The four-level inputs are intended to be static inputs. When left open, an internal resistive voltage-divider sets the input voltage to approximately 3.5V. Therefore, connect the four-level logic inputs directly to VCC, REF, or GND when selecting one of the other logic levels. See the *Electrical Characteristics* for exact logic-level voltages.

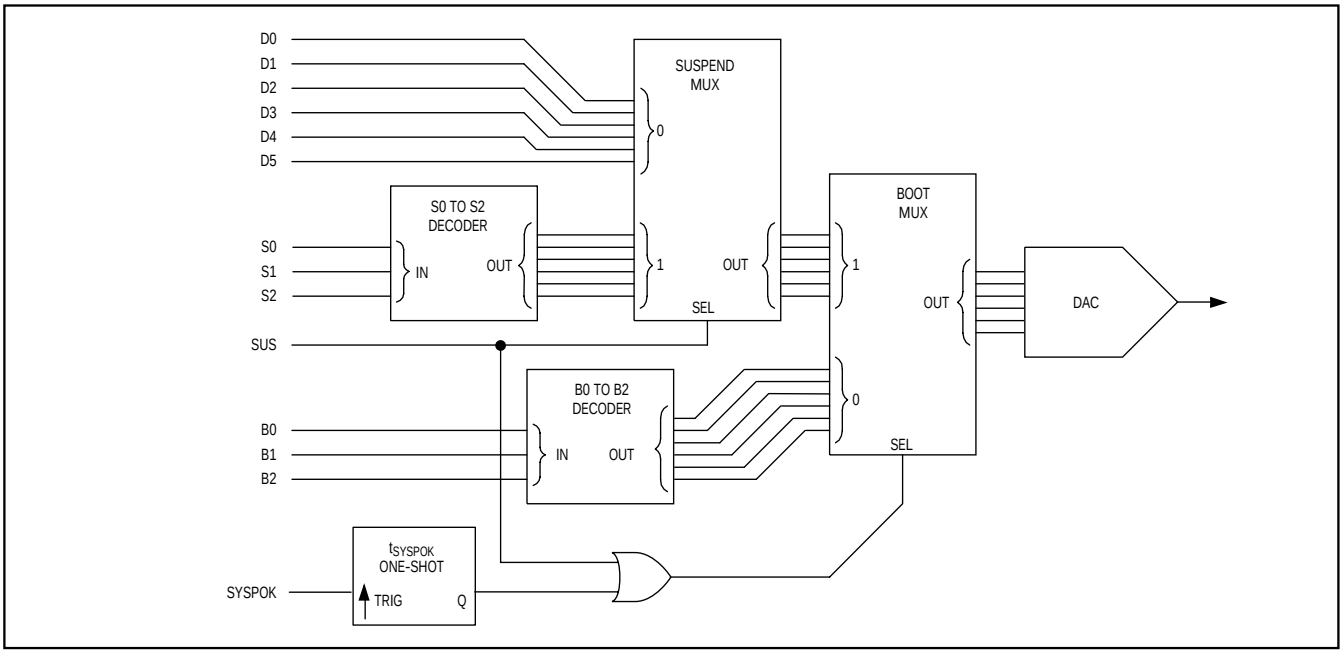


Figure 9. Internal Multiplexers Block Diagram

Table 4. Operating Mode Truth Table

$\overline{SHDN}$	SYSPOK	SUS	$\overline{DPSLP}$	$\overline{DDO}$	$\overline{PSI}$	OUTPUT VOLTAGE	OPERATING MODE
0	x	x	x	0	x	GND	Low-Power Shutdown Mode. DL is forced high, DH is forced low, and the PWM controller is disabled. The supply current drops to 1µA.
1	0	0	x	1	x	B0 to B2 (No offset)	Power-Up Mode. When enabled, the MAX1987/ MAX1988 softly ramp up the output voltage to the selected boot voltage (B0 to B2, Table 7). The controller remains at the boot voltage until SYSPOK is driven high (see the *Power-Up Sequence* section).
1	1	0	1	1	1	D0–D5 (No offset)	Normal Operation. The no-load output voltage is determined by the selected VID DAC code (D0–D5, Table 5).
1	1	0	1	0	0	D0–D5 (No offset)	Pulse-Skipping Override. When $\overline{PSI}$ is pulled low, the MAX1987/MAX1988 immediately enter pulse-skipping operation allowing automatic PWM/PFM switchover under light loads. The IMVPOK output is forced high, and the $\overline{CLKEN}$ output is forced low as long as $\overline{PSI}$ is pulled low.
1	1	0	0	0	x	D0–D5 (Plus offset)	Deep-Sleep Mode. The no-load output voltage is determined by the selected VID DAC code (D0–D5, Table 5) plus the offset voltage set by POS and NEG. Operation with automatic PWM/PFM switchover for pulse-skipping under light loads.
1	x	1	x	0	x	S0 to S2 (No offset)	Suspend Mode. The no-load output voltage is determined by the selected suspend code (S0 to S2, Table 6), overriding all other active modes of operation. Operation with automatic PWM/PFM switchover for pulse-skipping under light loads.
1	0	x	x	0	x	GND	Fault Mode. The fault latch has been set by either UVP, OVP (MAX1987 only), thermal shutdown, or a falling edge on SYSPOK. The controller remains in FAULT mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

Table 5. Output Voltage VID DAC Codes (SUS = Low)

D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	0	1.708
0	0	0	0	0	1	1.692
0	0	0	0	1	0	1.676
0	0	0	0	1	1	1.660
0	0	0	1	0	0	1.644
0	0	0	1	0	1	1.628
0	0	0	1	1	0	1.612
0	0	0	1	1	1	1.596
0	0	1	0	0	0	1.580
0	0	1	0	0	1	1.564
0	0	1	0	1	0	1.548
0	0	1	0	1	1	1.532
0	0	1	1	0	0	1.516
0	0	1	1	0	1	1.500
0	0	1	1	1	0	1.484
0	0	1	1	1	1	1.468
0	1	0	0	0	0	1.452
0	1	0	0	0	1	1.436
0	1	0	0	1	0	1.420
0	1	0	0	1	1	1.404
0	1	0	1	0	0	1.388
0	1	0	1	0	1	1.372
0	1	0	1	1	0	1.356
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	0	1	1.308
0	1	1	0	1	0	1.292
0	1	1	0	1	1	1.276
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	0	1.228
0	1	1	1	1	1	1.212

D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
1	0	0	0	0	0	1.196
1	0	0	0	0	1	1.180
1	0	0	0	1	0	1.164
1	0	0	0	1	1	1.148
1	0	0	1	0	0	1.132
1	0	0	1	0	1	1.116
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.084
1	0	1	0	0	0	1.068
1	0	1	0	0	1	1.052
1	0	1	0	1	0	1.036
1	0	1	0	1	1	1.020
1	0	1	1	0	0	1.004
1	0	1	1	0	1	0.988
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
1	1	0	0	0	0	0.940
1	1	0	0	0	1	0.924
1	1	0	0	1	0	0.908
1	1	0	0	1	1	0.892
1	1	0	1	0	0	0.876
1	1	0	1	0	1	0.860
1	1	0	1	1	0	0.844
1	1	0	1	1	1	0.828
1	1	1	0	0	0	0.812
1	1	1	0	0	1	0.796
1	1	1	0	1	0	0.780
1	1	1	0	1	1	0.764
1	1	1	1	0	0	0.748
1	1	1	1	0	1	0.732
1	1	1	1	1	0	0.716
1	1	1	1	1	1	0.700

Table 6. Suspend Mode DAC Codes (SUS = High)

S2	S1	S0	OUTPUT VOLTAGE (V)
GND	GND	GND	1.452
GND	GND	REF	1.436
GND	GND	OPEN	1.420
GND	GND	V_{CC}	1.404
GND	REF	GND	1388
GND	REF	REF	1.372
GND	REF	OPEN	1.356
GND	REF	V_{CC}	1.340
GND	OPEN	GND	1.324
GND	OPEN	REF	1.308
GND	OPEN	OPEN	1.292
GND	OPEN	V_{CC}	1.276
GND	V_{CC}	GND	1.260
GND	V_{CC}	REF	1.244
GND	V_{CC}	OPEN	1.228
GND	V_{CC}	V_{CC}	1.212
REF	GND	GND	1.196
REF	GND	REF	1.180
REF	GND	OPEN	1.164
REF	GND	V_{CC}	1.148
REF	REF	GND	1.132
REF	REF	REF	1.116
REF	REF	OPEN	1.100
REF	REF	V_{CC}	1.084
REF	OPEN	GND	1.068
REF	OPEN	REF	1.052
REF	OPEN	OPEN	1.036
REF	OPEN	V_{CC}	1.020
REF	V_{CC}	GND	1.004
REF	V_{CC}	REF	0.988
REF	V_{CC}	OPEN	0.972
REF	V_{CC}	V_{CC}	0.956

S2	S1	S0	OUTPUT VOLTAGE (V)
OPEN	GND	GND	0.940
OPEN	GND	REF	0.924
OPEN	GND	OPEN	0.908
OPEN	GND	V_{CC}	0.892
OPEN	REF	GND	0.876
OPEN	REF	REF	0.860
OPEN	REF	OPEN	0.844
OPEN	REF	V_{CC}	0.828
OPEN	OPEN	GND	0.812
OPEN	OPEN	REF	0.796
OPEN	OPEN	OPEN	0.780
OPEN	OPEN	V_{CC}	0.764
OPEN	V_{CC}	GND	0.748
OPEN	V_{CC}	REF	0.732
OPEN	V_{CC}	OPEN	0.716
OPEN	V_{CC}	V_{CC}	0.700
V_{CC}	GND	GND	0.684
V_{CC}	GND	REF	0.668
V_{CC}	GND	OPEN	0.652
V_{CC}	GND	V_{CC}	0.636
V_{CC}	REF	GND	0.620
V_{CC}	REF	REF	0.604
V_{CC}	REF	OPEN	0.588
V_{CC}	REF	V_{CC}	0.572
V_{CC}	OPEN	GND	0.556
V_{CC}	OPEN	REF	0.540
V_{CC}	OPEN	OPEN	0.524
V_{CC}	OPEN	V_{CC}	0.508
V_{CC}	V_{CC}	GND	0.492
V_{CC}	V_{CC}	REF	0.476
V_{CC}	V_{CC}	OPEN	0.460
V_{CC}	V_{CC}	V_{CC}	0.444

Table 7. Boot Mode DAC Codes (Power-Up)

B2	B1	B0	OUTPUT VOLTAGE (V)
GND	GND	GND	1.708
GND	GND	REF	1.692
GND	GND	OPEN	1.676
GND	GND	V_{CC}	1.660
GND	REF	GND	1.644
GND	REF	REF	1.628
GND	REF	OPEN	1.612
GND	REF	V_{CC}	1.596
GND	OPEN	GND	1.580
GND	OPEN	REF	1.564
GND	OPEN	OPEN	1.548
GND	OPEN	V_{CC}	1.532
GND	V_{CC}	GND	1.516
GND	V_{CC}	REF	1.500
GND	V_{CC}	OPEN	1.484
GND	V_{CC}	V_{CC}	1.468
REF	GND	GND	1.452
REF	GND	REF	1.436
REF	GND	OPEN	1.420
REF	GND	V_{CC}	1.404
REF	REF	GND	1.388
REF	REF	REF	1.372
REF	REF	OPEN	1.356
REF	REF	V_{CC}	1.340
REF	OPEN	GND	1.324
REF	OPEN	REF	1.308
REF	OPEN	OPEN	1.292
REF	OPEN	V_{CC}	1.276
REF	V_{CC}	GND	1.260
REF	V_{CC}	REF	1.244
REF	V_{CC}	OPEN	1.228
REF	V_{CC}	V_{CC}	1.212

B2	B1	B0	OUTPUT VOLTAGE (V)
OPEN	GND	GND	1.196
OPEN	GND	REF	1.180
OPEN	GND	OPEN	1.164
OPEN	GND	V_{CC}	1.148
OPEN	REF	GND	1.132
OPEN	REF	REF	1.116
OPEN	REF	OPEN	1.100
OPEN	REF	V_{CC}	1.084
OPEN	OPEN	GND	1.068
OPEN	OPEN	REF	1.052
OPEN	OPEN	OPEN	1.036
OPEN	OPEN	V_{CC}	1.020
OPEN	V_{CC}	GND	1.004
OPEN	V_{CC}	REF	0.988
OPEN	V_{CC}	OPEN	0.972
OPEN	V_{CC}	V_{CC}	0.956
V_{CC}	GND	GND	0.940
V_{CC}	GND	REF	0.924
V_{CC}	GND	OPEN	0.908
V_{CC}	GND	V_{CC}	0.892
V_{CC}	REF	GND	0.876
V_{CC}	REF	REF	0.860
V_{CC}	REF	OPEN	0.844
V_{CC}	REF	V_{CC}	0.828
V_{CC}	OPEN	GND	0.812
V_{CC}	OPEN	REF	0.796
V_{CC}	OPEN	OPEN	0.780
V_{CC}	OPEN	V_{CC}	0.764
V_{CC}	V_{CC}	GND	0.748
V_{CC}	V_{CC}	REF	0.732
V_{CC}	V_{CC}	OPEN	0.716
V_{CC}	V_{CC}	V_{CC}	0.700

Suspend Mode

When the processor enters low-power suspend mode, the processor sets the regulator to a lower output voltage to reduce power consumption. The MAX1987/MAX1988 include independent suspend mode output voltage codes set by the four-level inputs S0 to S2. When the CPU suspends operation, SUS is driven high, overriding the 6-bit VID DAC code set by either D0–D5 (normal operation) or B0 to B2 (power-up). The master controller slews the output to the selected suspend mode voltage. During the transition, the MAX1987/MAX1988 assert forced-PWM operation until 62 R_{TIME} clock cycles ($t_{\overline{DDO}}$ + t_{SKIP}) after the slew-rate controller reaches the suspend mode voltage.

When SUS is low during normal operation (SYSPOK = high), the output voltage is dynamically controlled by the 6-bit VID DAC inputs (D0–D5).

Output Voltage Transition Timing

The MAX1987/MAX1988 are designed to perform mode transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance. This makes the IC ideal for IMVP-IV CPUs.

At the beginning of an output voltage transition, the MAX1987/MAX1988 blank the IMVPOK and $\overline{CLKEN}$ outputs, preventing them from changing states. IMVPOK and $\overline{CLKEN}$ remain blanked during the transition and are re-enabled 32 clock cycles after the slew-rate controller has set the final DAC code value. The slew-rate clock frequency (set by the resistor R_{TIME}) must be set fast enough to ensure that the transition is completed within the maximum allotted time.

The slew-rate controller transitions the output voltage in 16mV increments during soft-start, soft shutdown, and suspend mode transitions. The total time for a transition depends on R_{TIME}, the voltage difference, and the accuracy of the MAX1987/MAX1988s' slew-rate clock, and is not dependent on the total output capacitance. The greater the output capacitance, the higher the surge current required for the transition. The MAX1987/MAX1988 automatically control the current to the minimum level required to complete the transition in the calculated time, as long as the surge current is less than the current limit set by ILIM. The transition time is given by:

$$t_{SLEW} \approx \frac{1}{f_{SLEW}}\left(\frac{V_{NEW} - V_{OLD}}{16mV}\right) \text{ for } V_{OUT} \text{ rising}$$

$$t_{SLEW} \approx \frac{1}{f_{SLEW}}\left[\left(\frac{V_{OLD} - V_{NEW}}{16mV}\right) + 2\right] \text{ for } V_{OUT} \text{ falling}$$

where f_{SLEW} = 320kHz x 47kΩ / R_{TIME}, V_{OLD} is the original DAC setting, and V_{NEW} is the new DAC setting. The additional 2 clock cycles on the falling edge time are due to internal synchronization delays. See TIME Frequency Accuracy in the *Electrical Characteristics* for f_{SLEW} limits.

The practical range of R_{TIME} is 23.5kΩ to 235kΩ corresponding with 1.6µs to 15.6µs per 16mV step. Although the DAC takes discrete 16mV steps, the output filter makes the transitions relatively smooth. The average inductor current required to make an output-voltage transition is:

$$I_L \cong C_{OUT} \times 16mV \times f_{SLEW}$$

Output Overvoltage Protection (MAX1987 Only)

The overvoltage protection (OVP) circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The output voltage is continuously monitored for overvoltage. If the actual FB voltage exceeds 2V, the OVP circuit immediately forces the DL low-side gate-driver high, pulls the DH high-side gate-driver low, sets the fault latch, and shuts down the PWM controller. This action turns on the synchronous-rectifier MOSFET with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output to ground. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows. When the fault latch is activated, the controller pulls IMVPOK low and drives $\overline{CLKEN}$ high. The controller remains shut down until the fault latch is cleared by toggling $\overline{SHDN}$ or cycling the V_{CC} power supply below 1V.

Overvoltage protection can be disabled through the NO FAULT test mode (see the *NO FAULT Test Mode* section).

Output Undervoltage Shutdown

The output UVP function is similar to foldback-current-limiting, but employs a timer rather than a variable current limit. If the MAX1987/MAX1988 output voltage is under 70% of the nominal value, the controller activates the shutdown sequence and sets the fault latch. Once the controller ramps down to the 0V DAC code setting, it forces the DL low-side gate-driver high, and pulls the

DH high-side gate-driver low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 1V to clear the fault latch and reactivate the controller. UVP is ignored during output voltage transitions and remains blanked for an additional 32 clock cycles after the controller reaches the final DAC code value.

UVP can be disabled through the NO FAULT test mode (see the *NO FAULT Test Mode* section).

Thermal Fault Protection

The MAX1987/MAX1988 feature a thermal fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch and activates the soft shutdown sequence. Once the controller ramps down to the 0V DAC code setting, it forces the DL low-side gate-driver high, and pulls the DH high-side gate-driver low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 1V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C.

Thermal shutdown can be disabled through the NO FAULT test mode (see the *NO FAULT Test Mode* section).

NO FAULT Test Mode

The latched fault protection features and overlap mode can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a "No Fault" test mode is provided to disable the overvoltage protection (MAX1987), undervoltage protection, thermal shutdown, and overlap mode. Additionally, the test mode clears the fault latch if it has been set. The NO FAULT test mode is entered by forcing 12V to 15V on $\overline{SHDN}$.

Design Procedure

Firmly establish the input-voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

Input-Voltage Range: The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.

Maximum Load Current: There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

$$I_{LOAD(MAIN)} = I_{LOAD(2ND)} = \frac{I_{LOAD}}{2}$$

Switching Frequency: This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

Inductor Operating Point: This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = 2\left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

Example: $I_{LOAD(MAX)}$ = 40A, V_{IN} = 12V, V_{OUT} = 1.3V, f_{SW} = 300kHz, 30% ripple current or LIR = 0.3.

$$L = \frac{2 \times 1.3V \times (12V - 1.3V)}{12V \times 300kHz \times 40A \times 0.3} = 0.64\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The

core must be large enough not to saturate at the peak inductor current (I_{PEAK}).

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{2}\right)\left(1+\frac{LIR}{2}\right)$$

Transient Response

The inductor ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on time and minimum off-time:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2\left[\left(\frac{V_{OUT}K}{V_{IN}}\right)+t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{(V_{IN}-2V_{OUT})K}{V_{IN}}\right)-2t_{OFF(MIN)}\right]} + \frac{\Delta I_{LOAD(MAX)}}{2C_{OUT}}\left[\left(\frac{V_{OUT}K}{V_{IN}}\right)+t_{OFF(MIN)}\right]$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* section) and K is from Table 3.

The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2C_{OUT}V_{OUT}}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{LIMIT(LOW)} > \left(\frac{I_{LOAD(MAX)}}{2}\right)\left(1-\frac{LIR}{2}\right)$$

where $I_{LIMIT(LOW)}$ equals the minimum current-limit threshold voltage divided by the current-sense resistor (R_{SENSE}). For the 30mV default setting, the minimum current-limit threshold is 27mV.

Connect ILIM to V_{CC} for a default 30mV current-limit threshold. In adjustable mode, the current-limit threshold is precisely 1/20th the voltage seen at ILIM. For an adjustable threshold, connect a resistive divider from REF to GND with ILIM connected to the center tap. The external 200mV to 1.5V adjustment range corresponds to a 10mV to 75mV current-limit threshold. When adjusting the current limit, use 1% tolerance resistors with approximately 10µA of divider current to prevent a significant increase of errors in the current-limit tolerance.

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase systems out-of-phase, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage by reducing the total inductor ripple current. For 180° out-of-phase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{\left(\frac{V_{IN}-2V_{OUT}}{f_{SW}L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)}$$

where f_{SW} is the switching frequency per phase. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Dual-Phase, Quick-PWM Controllers for IMVP-IV CPU Core Power Supplies

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where $f_{ESR} = \frac{1}{2\pi R_{EFF} C_{OUT}}$

and $R_{EFF} = R_{ESR} + A_{VPS} R_{SENSE} + R_{PCB}$

where C_{OUT} is the total output capacitance, R_{ESR} is the total equivalent-series-resistance, R_{SENSE} is the current-sense resistance ($R_{CM} = R_{CS}$), A_{VPS} is the voltage positioning gain, and R_{PCB} is the parasitic board resistance between the output capacitors and sense resistors.

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, Sanyo POSCAP, and Panasonic SP capacitors, in wide-spread use at the time of publication, have typical ESR zero frequencies below 50kHz. In the standard application circuit, the ESR needed to support a $30mV_{P-P}$ ripple is 30mV/(40A x 0.3) = 2.5mΩ. Four 330µF/2.5V Panasonic SP (type XR) capacitors in parallel provide 2.5mΩ (max) ESR. Their typical combined ESR results in a zero at 40kHz.

Ceramic capacitors have a high ESR zero frequency, but applications with significant voltage positioning can take advantage of their size and low ESR. Don't put high-value ceramic capacitors directly across the output without verifying that the circuit contains enough voltage positioning and series PC board resistance to ensure stability. When only using ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output capacitance requirement. Their relatively low capacitance value can cause output overshoot when stepping from full-load to no-load conditions, unless a small inductor value is used (high switching frequency) to minimize the energy transferred from inductor to capacitor during load-step recovery. The efficiency penalty for operating at 550kHz is about 3% when compared to the 300kHz circuit, primarily due to the high-side MOSFET switching losses.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and feedback-loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The MAX1987/MAX1988 operate 180° out-of-phase, alternating the turn-on times of each phase. This minimizes the input ripple current by dividing the load current between the two phases. The I_{RMS} requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{2V_{IN}} \right) \sqrt{2V_{OUT}(V_{IN} - 2V_{OUT})}$$

The worst-case RMS current requirement occurs when operating with a 25% duty cycle ($V_{IN} = 4V_{OUT}$). At this point, the above equation simplifies to $I_{RMS} = 0.25 \times I_{LOAD}$. When compared to a single-phase regulator, the multiphase converter reduces the RMS input current by at least 30%.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX1987/MAX1988 are operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums.

Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or D^2PAK), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD\ (N_H\ Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{2}\right)^2 R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in the high-side MOSFET (N_H), due to switching losses, is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (N_H\ Switching) = \frac{(V_{IN(MAX)})^2 C_{RSS} f_{SW} I_{LOAD}}{2 I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of N_H and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the $C \times V_{IN}^2 \times f_{SW}$ switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low-battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD\ (N_H\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{2}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can “over design” the circuit to tolerate:

$$I_{LOAD} = 2 I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum single-phase valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good size heatsink to handle the overload power dissipation.

Choose a Schottky diode (D1) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/6th of the total load current. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs’ gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified

in the MOSFET's data sheet. For example, assume (2) FDS6694 N-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single FDS6694 has a typical gate charge of 13nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{2 \times 13nC}{200mV} = 0.13\mu F$$

Selecting the closest standard value, this example requires a 0.1µF ceramic capacitor.

Current Balance Compensation (CCI)

The current-balance compensation capacitor (C_{CCI}) integrates the difference between the main and secondary current-sense voltages. This capacitor allows the user to optimize the dynamics of the current-balance loop. Large capacitor values increase the integration time constant, resulting in larger current differences between the phases during transients. Small capacitor values allow the current loop to respond cycle-by-cycle, but can result in small DC current variations between the phases. For most applications, a 470pF capacitor from CCI to FB works well.

In pulse-skipping operation, the integration time becomes much smaller than the off-time. This allows the offset current to charge up the CCI compensation capacitor, extending the secondary on-time so that a current imbalance occurs. Add a 470kΩ to 1MΩ resistor between CCI and FB (R_{CCI}) to cancel the offset current.

Setting Voltage Positioning

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the processor's power dissipation. When the output is loaded, an internal op amp (Figures 2 and 10) increases the signal fed back to the MAX1987/MAX1988s' feedback input. The adjustable amplification allows the use of standard, low-value, current-sense resistors, significantly reducing the power dissipated in the current-sense resistors when compared to connecting the feedback voltage directly to the current-sense resistor. The load transient response of this control loop is extremely fast yet well controlled, so the amount of voltage change can be accurately confined within the limits stipulated in the microprocessor power-supply guidelines. To understand the benefits of dynamically adjusting the output voltage, see the *Voltage Positioning and Effective Efficiency* section.

The voltage-positioned circuit determines the load current from the voltage across the current-sense resistors (R_{SENSE} = R_{CM} = R_{CS}) connected between the inductors and output capacitors, as shown in Figure 10. The voltage drop can be determined by the following equation:

$$V_{VPS} = \left(1 + \frac{2R_F}{R_B}\right)\left(\frac{I_{LOAD}}{2}\right)R_{SENSE}$$

$$V_{VPS} = \left(\frac{1}{2} + \frac{R_F}{R_B}\right)I_{LOAD}R_{SENSE}$$

$$V_{VPS} = A_{VPS}I_{LOAD}R_{SENSE}$$

The current-sense summation maintains the proper 180° out-of-phase operation. Select the positive input summing resistors using the following equation:

$$R_A = R_B \,//\, (2R_F)$$

Minimum Input Voltage Requirements and Dropout Performance

The output voltage adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot and the number of phases. For best dropout performance, use the slower (200kHz) on-time settings. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 3). Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ is an indicator of the ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows tradeoffs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

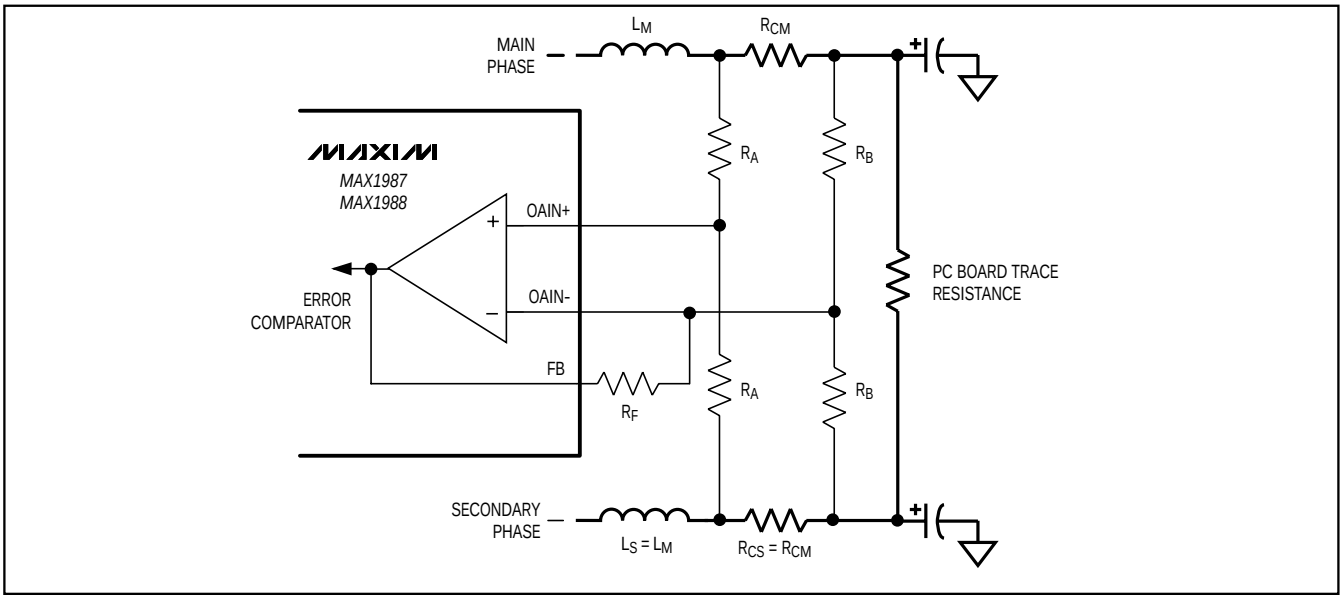


Figure 10. Voltage Positioning Gain

$$V_{IN(MIN)} = \eta \left[\frac{V_{FB} - V_{VPS} + V_{DROP1}}{1 - \eta\left(\frac{h \times t_{OFF(MIN)}}{K}\right)} \right] + V_{DROP2} - V_{DROP1} + V_{VPS}$$

where η is the number of phases, V_{VPS} is the voltage-positioning droop, V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths (see the *On-Time One-Shot* section), $t_{OFF(MIN)}$ is from the *Electrical Characteristics*, and K is taken from Table 3. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then reduce the operating frequency or add output capacitance to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example:

V_{FB} = 1.4V

K_{MIN} = 3.0µs for f_{SW} = 300kHz

$t_{OFF(MIN)}$ = 400ns

V_{VPS} = 3mV/A x 30A = 90mV

$V_{DROP1} = V_{DROP2}$ = 150mV (30A load)

h = 1.5 and η = 2

$$V_{IN(MIN)} = 2 \times \left[\frac{1.4V - 90mV + 150mV}{1 - 2 \times (0.4\mu s \times 1.5 / 3.0\mu s)} \right] + 150mV - 150mV + 90mV = 4.96V$$

Calculating again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = 2 \times \left[\frac{1.4V - 90mV + 150mV}{1 - 2 \times (0.4\mu s \times 1.0 / 3.0\mu s)} \right] + 150mV - 150mV + 90mV = 4.07V$$

Therefore, V_{IN} must be greater than 4.1V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 5V.

Dual-Phase, Quick-PWM Controllers for IMVP-IV CPU Core Power Supplies

Applications Information

Voltage Positioning and Effective Efficiency

Powering new mobile processors requires careful attention to detail to reduce cost, size, and power dissipation. As CPUs became more power hungry, it was recognized that even the fastest DC-DC converters were inadequate to handle the transient power requirements. After a load transient, the output instantly changes by $ESR_{COUT} \times \Delta I_{LOAD}$. Conventional DC-DC converters respond by regulating the output voltage back to its nominal state after the load transient occurs (Figure 11). However, the CPU only requires that the output voltage remain above a specified minimum value. Dynamically positioning the output voltage to this lower limit allows the use of fewer output capacitors and reduces power consumption under load.

For a conventional (nonvoltage-positioned) circuit, the total voltage change is:

$$V_{P-P1} = (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in Figure 12. Setting the converter to regulate at a lower voltage when under load allows a larger voltage step when the output current suddenly decreases (Figure 11). So the total voltage change for a voltage-positioned circuit is:

$$V_{P-P2} = (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in the *Design Procedure* section. Since the amplitudes are the same for both circuits ($V_{P-P1} = V_{P-P2}$), the voltage-positioned circuit tolerates twice the ESR. Since the ESR specification is achieved by paralleling several capacitors, fewer units are needed for the voltage-positioned circuit.

An additional benefit of voltage positioning is reduced power consumption at high load currents. Since the output voltage is lower under load, the CPU draws less current. The result is lower power dissipation in the CPU, although some extra power is dissipated in R_{SENSE}. For a nominal 1.4V, 30A output (R_{LOAD} = 46.7mΩ), reducing the output voltage 7.1% gives an output voltage of 1.3V and an output current of 27.8A.

Given these values, CPU power consumption is reduced from 42W to 36.1W. The additional power consumption of R_{SENSE} is:

$$1.5m\Omega \times (27.8A)^2 = 1.16W$$

which results in an overall power savings of:

$$42W - (36.1W + 1.16W) = 4.7W$$

In effect, 5.9W of CPU dissipation is saved and the power supply dissipates much of the savings, but both the net savings and the transfer of dissipation away from the hot CPU are beneficial. Effective efficiency is defined as the efficiency required of a nonvoltage-positioned circuit to equal the total dissipation of a voltage-positioned circuit for a given CPU operating condition.

Calculate effective efficiency as follows:

1) Start with the efficiency data for the positioned circuit (V_{IN}, I_{IN}, V_{OUT}, I_{OUT}).
2) Model the load resistance for each data point:
   $R_{LOAD} = V_{OUT} / I_{OUT}$
3) Calculate the output current that would exist for each R_{LOAD} data point in a nonpositioned application:
   $I_{NP} = V_{NP} / R_{LOAD}$
   where V_{NP} = 1.6V (in this example).
4) Calculate effective efficiency as:
   Effective efficiency = $(V_{NP} \times I_{NP}) / (V_{IN} \times I_{IN})$ = calculated nonpositioned power output divided by the measured voltage-positioned power input.
5) Plot the efficiency data point at the nonpositioned current, I_{NP}.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 13). If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.

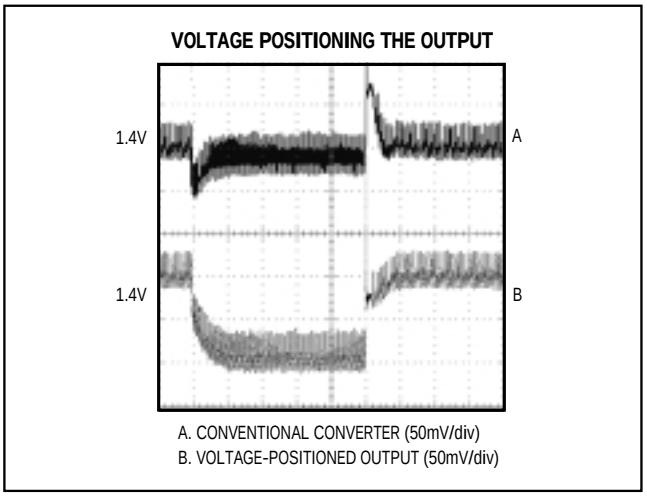


Figure 11. Voltage Positioning the Output

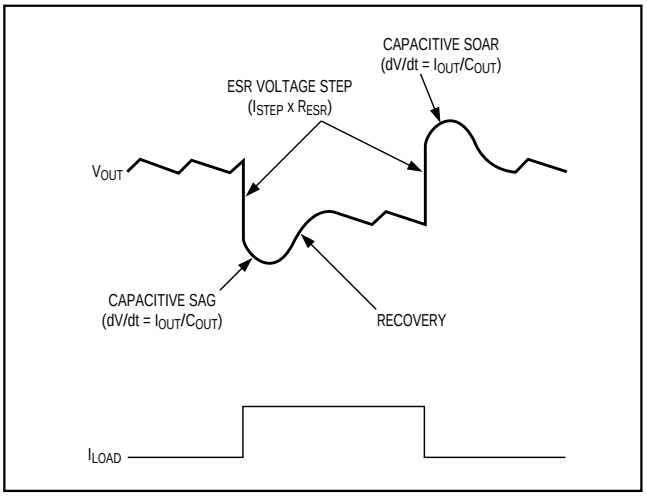


Figure 12. Transient Response Regions

2) Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the MAX1987/MAX1988. This includes the V_{CC} bypass capacitor, REF bypass capacitor, compensation (CCV) components, and the resistive-dividers connected to ILIM and POS/NEG.

3) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.

4) Keep the high-current gate-driver traces (DL_, DH_, LX_, and BST_) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.

5) C_P, C_N, OAIN+, and OAIN- connections for current limiting and voltage positioning must be made using Kelvin sense connections to guarantee the current-sense accuracy.

6) When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.

7) Route high-speed switching nodes away from sensitive analog areas (REF, CCV, CCI, FB, C_P, C_N, etc.). Make all pin-strap control input connections ($\overline{SHDN}$, ILIM, B0 to B2, S0 to S2, TON) to analog ground or V_{CC} rather than power ground or V_{DD}.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.

2) Mount the controller IC adjacent to the low-side MOSFET. The DLM and DLS gate traces must be short and wide (50mils to 100mils wide if the MOSFET is 1in from the controller IC).

3) Group the gate-drive components (BST_ diodes and capacitors, V_{DD} bypass capacitor) together near the controller IC.

4) Make the DC-DC controller ground connections as shown in Figures 1 and 13. This diagram can be viewed as having three separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND pin and V_{DD} bypass capacitor go; and the analog ground plane where sensitive analog components, the GND pin, and V_{CC} bypass capacitor go. The GND plane must meet the PGND plane only at a single point directly beneath the IC. The respective ground planes should connect to the high-power output ground with a short metal trace from PGND to the source of the low-side MOSFET (the

middle of the star ground). This point must also be very close to the output capacitor ground terminal.

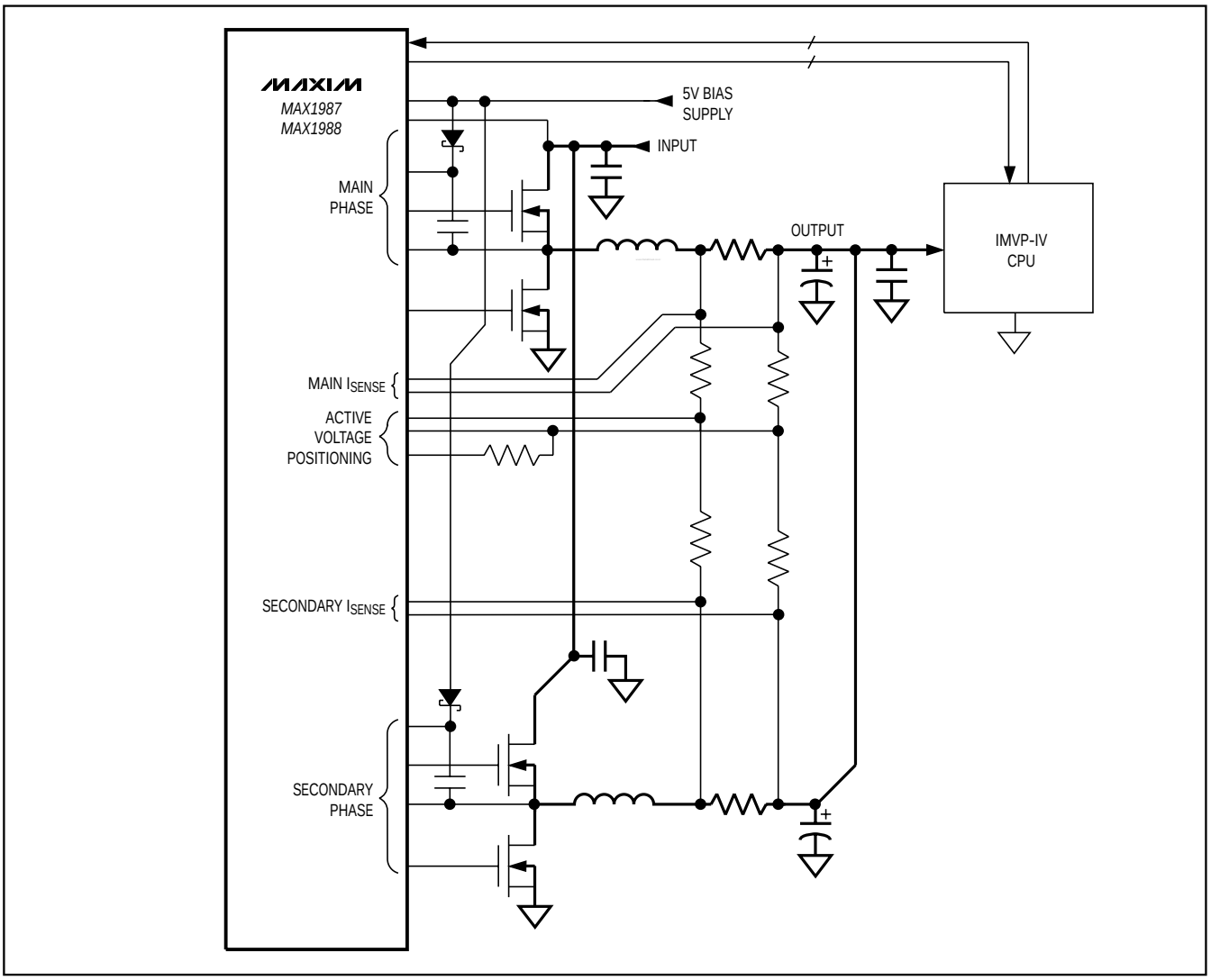
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

Chip Information

TRANSISTOR COUNT: 9559

PROCESS: BiCMOS

Typical Operating Circuit



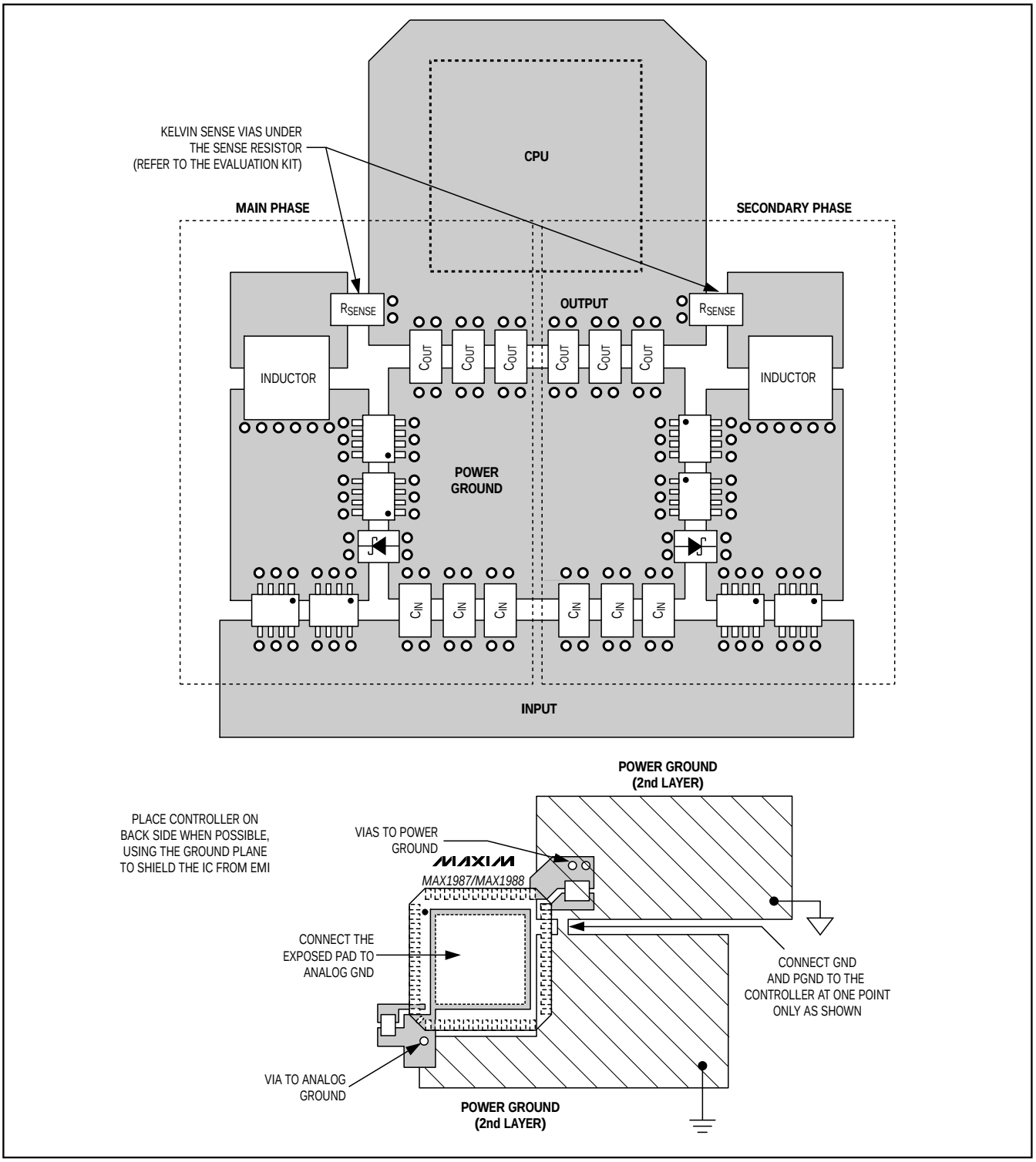
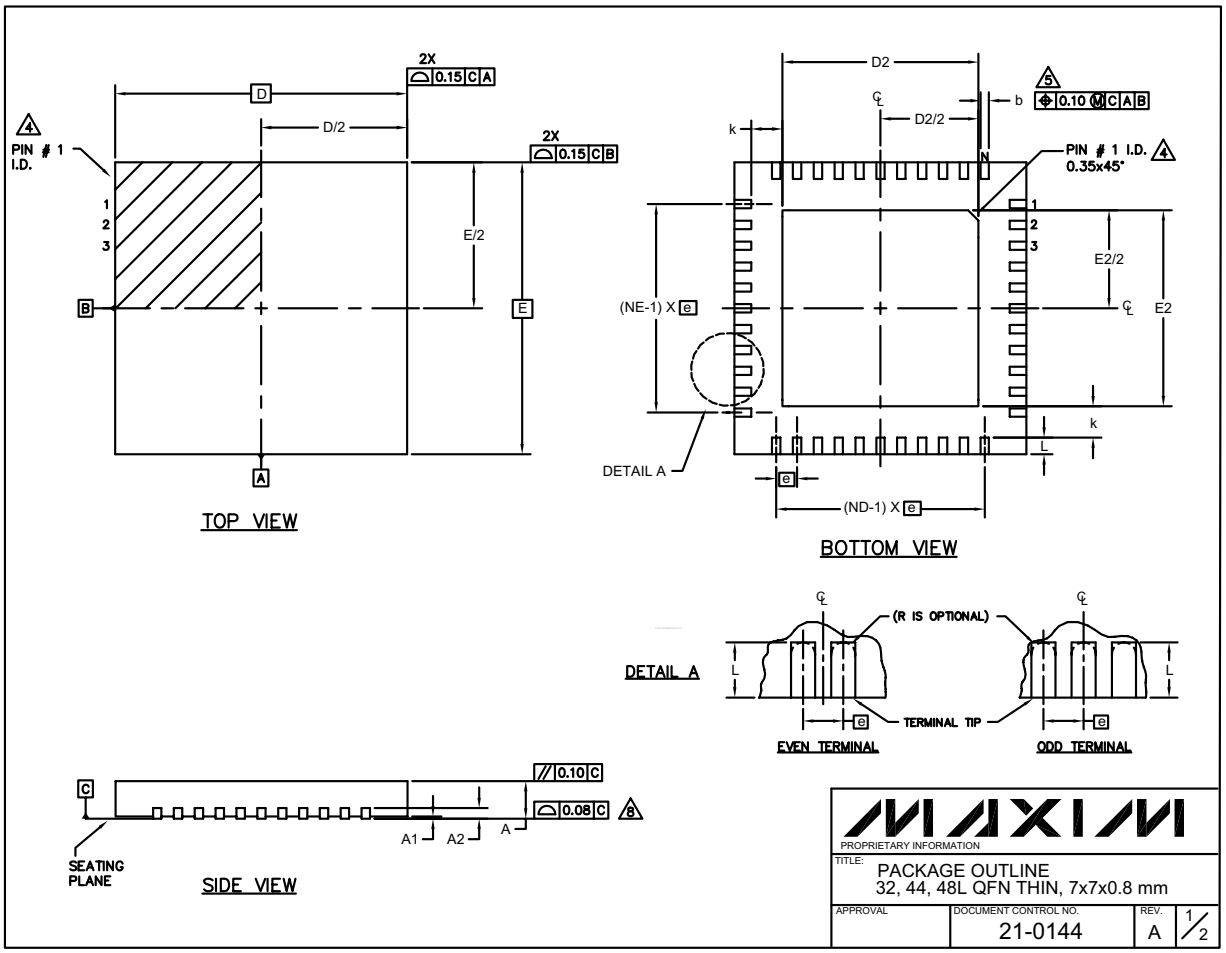


Figure 13. PC Board Layout Example

Dual-Phase, Quick-PWM Controllers for IMVP-IV CPU Core Power Supplies

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65
N	32			44			48			44		
ND	8			11			12			10		
NE	8			11			12			12		

EXPOSED PAD VARIATIONS								
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-1	-	4.55	4.70	4.85	4.55	4.70	4.85	-
T4477-1	-	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13, 24, 37, 48	4.20	4.30	4.40	4.20	4.30	4.40	-
T4877-2	-	5.45	5.60	5.75	5.45	5.60	5.75	WKKD-2

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 32, 44, 48L QFN THIN, 7x7x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	A	2/2