Micro Power Systems

MP8791

CMOS 12-Bit High Speed Analog-to-Digital Converter with Parallel Logic Interface Port

FEATURES

- 12-Bit ADC with DNL = ±1 LSB, INL = ±2 LSB
- SNR > 60 dB
- Sampling Frequency ≤ 2 MHz
- 28-Pin Package
- Internal Track and Hold: Input –3 dB Frequency = 10 MHz
- Single 5 V Supply
- Rail-to-Rail Input Range
- V_{REF} Range: 1.5 V to V_{DD}
- CMOS Low Power: 175 mW (typ)
- 1/4, 1/2 and 3/4 Scale Reference Resistor Taps
- TTL Compatible
- Three-State Outputs
- Binary and Two's Complement Digital Output Mode
- Latch-Up Proof

APPLICATIONS

- Instrumentation
- DAS
- Radar
- Medical Imaging
- Ultrasound
- Broadcast and Studio Video
- Magnetic Resonance Signal Acquisition
- Digital Oscilloscopes
- Spectrum Analysis

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GENERAL DESCRIPTION

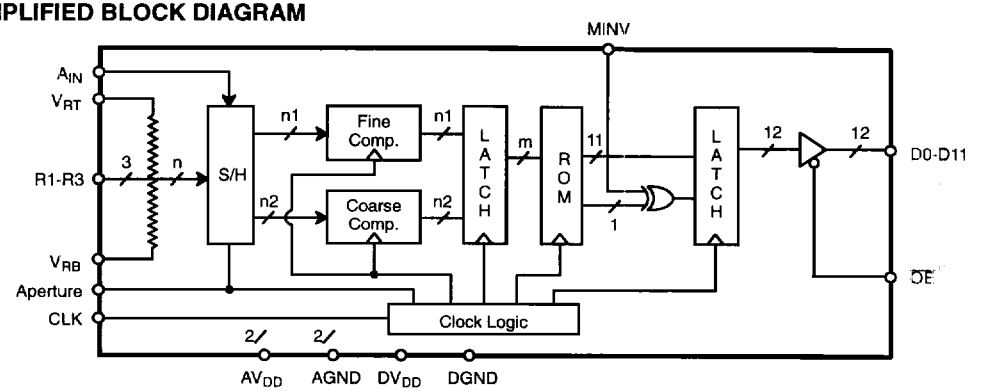
The MP8791 is a 2 MSPS 12-bit subranging analog to digital converter with DNL = ±1 LSB and INL = ±2 LSB. The MP8791 contains an internal track and hold and an analog input bandwidth of 10 MHz.

The MP8791 operates with a single 5 V supply while consuming less than 200 mW of power (typical). Separate pins for reference ladder terminals and power supplies allow flexibility for various A_{IN}, ΔV_{REF}, and power supply ranges.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay from sample edge. The digital output port is also equipped with a tri-state function. MINV enables binary and 2's complement data formatting. Through pins R1-R3, transfer function adjustment, linearity, and speed enhancement can be accommodated.

Specified for operation over the commerical / industrial (–40 to +85°C) temperature range, the MP8791 is available in Plastic dual-in-line (PDIP) and Surface Mount (SOIC) packages.

SIMPLIFIED BLOCK DIAGRAM



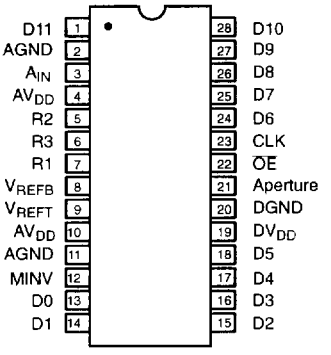
MP8791

ORDERING INFORMATION

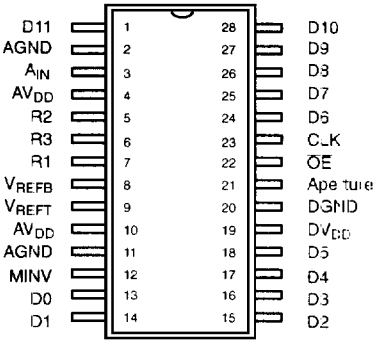
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	–40 to +85°C	MP8791AN*	±1	±2 1/2
SOIC	–40 to +85°C	MP8791AS	±1	±2 1/2

*Contact factory for availability.

PIN CONFIGURATIONS



28 Pin PDIP (0.600")
N28
Contact Factory for Availability of Smaller PDIP Packages



28 Pin SOIC (EIAJ, 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	D11	Data Bit 11 (MSB)
2	AGND	Analog Ground
3	A_{IN}	Analog Input
4	AV_{DD}	Analog Positive Supply
5	R2	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R3	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R1	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{REFB}	Negative Reference
9	V_{REFT}	Positive Reference
10	AV_{DD}	Analog Positive Supply
11	AGND	Analog Ground
12	MINV	Invert MSB (Active High)
13	D0	Data Bit 0 (LSB)
14	D1	Data Bit 1

PIN NO.	NAME	DESCRIPTION
15	D2	Data Bit 2
16	D3	Data Bit 3
17	D4	Data Bit 4
18	D5	Data Bit 5
19	DV_{DD}	Digital Positive Supply
20	DGND	Digital Negative Supply
21	Aperture	Delayed Clock, indicates sample point
22	$\overline{OE}$	Output Enable (Active Low)
23	CLK	Clock
24	D6	Data Bit 6
25	D7	Data Bit 7
26	D8	Data Bit 8
27	D9	Data Bit 9
28	D10	Data Bit 10

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 2 MHz (50% Duty Cycle), $V_{REF(+)}$ = 5.0 V, $V_{REF(-)}$ = AGND, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution			12				Bits	
Sampling Rate	FS			2			MHz	
ACCURACY[1]								
Differential Non-Linearity	DNL			±1			LSB	
Integral Non-Linearity	INL			±2 1/2			LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20				LSB	
Full Scale Error	EFS		–20				LSB	
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$	0.5		AV_{DD}			V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND					V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}			V	
Ladder Resistance	R_L		550				Ω	
ANALOG INPUT								
Input Bandwidth (–3 dB)[4]	BW		10				MHz	
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50				pF	
Input Capacitance Convert[5]			8				pF	
Aperture Delay from Clock	t_{AP}		20				ns	
Aperture Delay from Aperture Signal	t_{AP}		0				ns	Aperture pin load 5 pF. Measured at 50% point.
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}		2.4				V	
Logical "0" Voltage	V_{IL}		0.8				V	
Leakage Currents [6]	I_{IN}							V_{IN}=DGND to DV_{DD}
CLK, $\overline{OE}$, MINV			10				µA	
Input Capacitance			5				pF	
Clock Timing								
Clock Period	t_S	100	500				ns	
Rise & Fall Time[7]	t_R, t_F		15				ns	
"High" Time	t_{PWH}	50	220				ns	
"Low" Time	t_{PWL}	50	220				ns	
Duty Cycle			50				%	
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	V_{DD}-0.5					V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.5			V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}		1				µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}		30				ns	
Data Enable Delay	t_{DEN}		20				ns	
Data Tristate Delay	t_{DHZ}		20				ns	

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ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLIES[8] (Tmin to Tmax)								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}		5				V	
Current (AV_{DD} + DV_{DD})	I_{DD}			40			mA	
AC PARAMETERS								
Signal Noise Ratio	SNR		66				dB	

NOTES
1. Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).
2. Guaranteed. Not tested.
3. Specified values guarantee functionality. Refer to other parameters for accuracy.
4. –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
5. Switched capacitor analog input requires driver with low output resistance.
6. All inputs have diodes to DV_{DD} and DGND. Input(s) $\overline{OE}$ and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
7. Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
8. AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2, 3) (T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... 7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PQFP 450mW
Derates above 75°C ..... 6mW/°C

NOTES:
(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
(3) V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

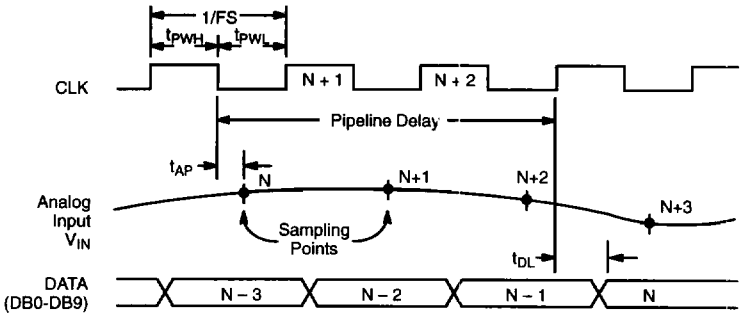


Figure 1. Timing Diagram

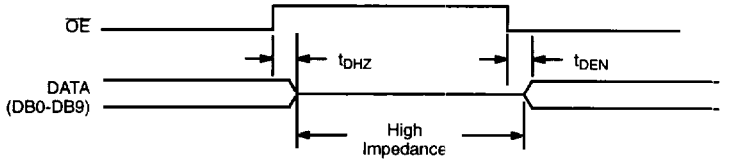


Figure 2. Tri-State Timing Diagram

OVERVIEW OF THE 8791 PINS & OPERATION NOTES :

$\overline{OE}$: Output Enable (input).

This signal controls the tri-state drivers on the digital outputs D0 - D11. During normal operation $\overline{OE}$ should be held low so that all outputs are enabled (NOTE: an internal resistor will pull $\overline{OE}$ to this level if it is not connected). When $\overline{OE}$ is driven high D0 - D11 go into high impedances mode. This control operates asynchronously to the clock and only controls the output drivers. The internal output register will get updated if the clock is running while the outputs are in tri-state mode. If possible, $\overline{OE}$ should be in tristate during Clock = 1 to reduce digital noise coupling into A_{IN} during the sample time. Aperture provides a convenient control for this purpose since it guarantees that the A_{IN} sample period is complete when the outputs are enabled.

APERTURE: Aperture Delay Sync (output).

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event. The Aperture pin may also be used to control the $\overline{OE}$ (outputs between tristate and active mode). This will reduce the errors introduced by digital output coupling during the A_{IN} sample time.

MINV: Digital Output Format (input).

This signal controls the format of the digital output data bits D0 – D11. Normally it is held low so the data is in straight binary format (all 0's when $V_{IN} = V_{RB}$; all 1's when $V_{IN} = V_{RT}$). If MINV is pulled high then the MSB (D11) will be inverted.

MINV is meant to be a static digital signal. If it is to change during operation it should only change when the CLK is low. Changing MINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV has a internal pull down device. This function is not available in the engineering sidebraze samples. For these samples, this pin must be tied to GND.

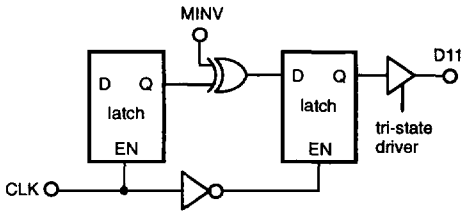


Figure 3. MINV Simplified Logic Circuit

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. The diagram *Figure 9.* shows an equivalent input circuit.

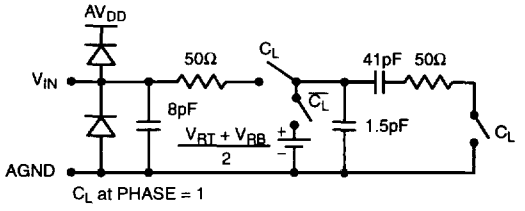


Figure 4. Equivalent Input Circuit

R1, R2, R3: Reference Ladder Taps.

These taps connect to every 1/4 point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to V_{SS}, this helps reduce the INL errors by stabilizing the reference ladder voltages.

These taps can also be used to alter the transfer curve of the ADC. A 4 segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

This may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

The internal interconnect resistance from each of the t_{AP} pins to the ladder is less than 3Ω.

1.6V maximum per tap is recommended for applications above 85°C. Up to 3.2V is allowed for applications under 85°C.

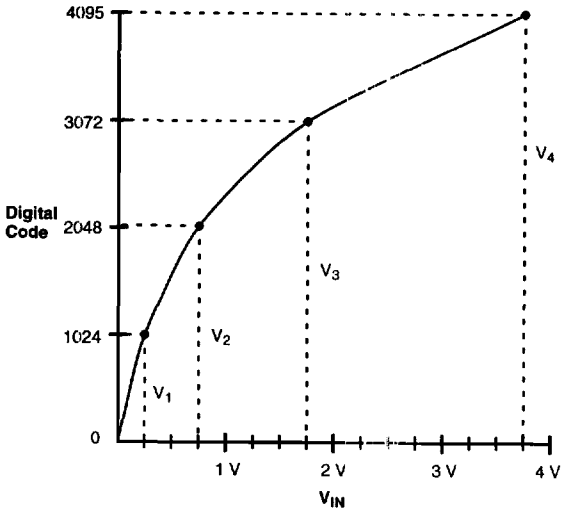
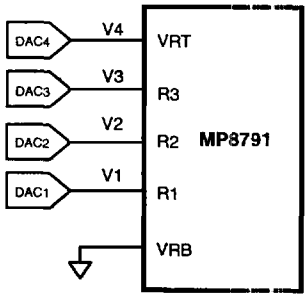


Figure 5. A Piecewise Linear Transfer Function

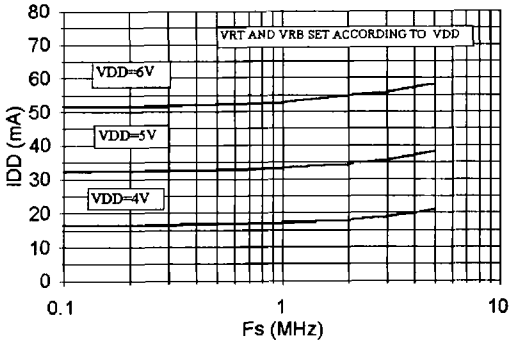


DAC MP7226

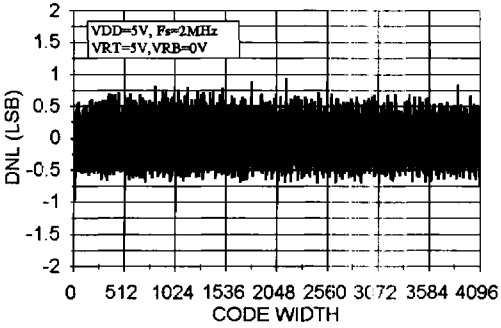
Only the Ladder detail shown.

Figure 6. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

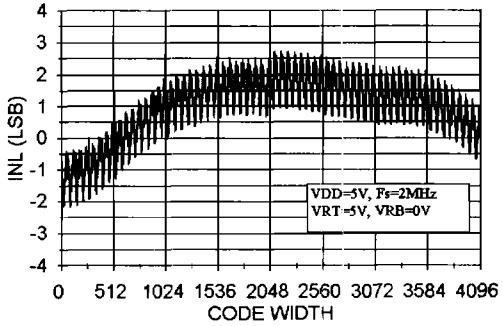
PERFORMANCE CHARACTERISTICS



Graph 1. I_{DD} vs. F_S



Graph 2. DNL Error Plot



Graph 3. INL Error Plot