REVISION RECORD

REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/12/96
A	• CORRECTION TO RH1021BM-10, DM-10, OUTPUT VOLTAGE, 100 KRAD MINIMUM LIMIT FROM "9.98 V" TO "9.938 V, PAGE 10.	02/28/97
B	• PAGE 2, ADDED PARAGRAPHS 3.2.1, 3.2.2, AND 3.2.3. PARAGRAPH 3.3.b, ADDED "(SEE PARAGRAPH 3.2)". • PAGE 4, PARAGRAPH 3.12, WAFER LOT ACCEPTANCE REDEFINED. PARAGRAPH 4.4.2, GROUP B INSPECTION, REDEFINED. PARAGRAPH 4.4.3, GROUP D INSPECTION, REDEFINED. • PAGE 5, PARAGRAPH 4.5, SOURCE INSPECTION, REDEFINED. • PAGE 6, FIGURE 1, TO5 CASE OUTLINE, ADDED θja AND θjc.	11/25/97
C	• PAGE 4, AMENDED PARAGRAPHS 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES.	05/8/98
D	• PAGE 6, FIGURE 1, CHANGED θja FROM 180°C/W TO 150°C/W.	11/17/99
E	• PAGE 4, PARAGRAPH 3.7, CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9, ADDED "HEREIN" AFTER "TABLE II", LINE 2. • PAGE 5, PARAGRAPH 4.3, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.1, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.2.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IIA OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIA IN MIL-STD-883". PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883".	12/13/99
F	• PAGE 3, PARAGRAPH 3.2.4, ADDED NEW DEVICE OPTION 4 (W10 FLATPACK). • PAGE 4, PARAGRAPH 3.8 CHANGED VERBIAGE ADDED FIGURES 5 AND 6. PARAGRAPH 3.10.1, ADDED FIGURE 2. PARAGRAPH 3.10.2, CHANGED VERBIAGE ADDED FIGURES 3 AND 4. PARAGRAPH 3.10.3, CHANGED VERBIAGE. PARAGRAPH 3.11.3, CHANGED FIGURE 4 TO 7. • PAGE 8, ADDED PAGE 7 DEVICE OPTION 4, PACKAGE OUTLINE. • PAGE 9, CHANGED FIGURE 2 TO 3. • PAGE 10, ADDED DEVICE OPTION 4, FIGURE 4 TERMINAL CONNECTIONS. • PAGE 11, CHANGED FIGURE 3 TO 5. • PAGE 12, ADDED DEVICE OPTION 4, FIGURE 6 BURN-IN CIRCUIT. • PAGE 13, CHANGED FIGURE 4 TO 7. • PAGE 15, CHANGED V_{OUT} OUTPUT VOLTAGE 10 KRAD (SI) MIN TO 9.992 AND MAX TO 10.008 AND ADDED VERBIAGE TO NOTE 3.	06/25/00

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14			
INDEX	REVISION	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**			
REVISION	PAGE NO.																	
INDEX	REVISION																	

	ORIG			**LINEAR TECHNOLOGY CORPORATION MILPITAS, CALIFORNIA**			
	DSGN						
	ENGR			TITLE:			
	MFG			**MICROCIRCUIT, LINEAR, RH1021-10, PRECISION 10V REFERENCE**			
	CM						
	QA						
	PROG			SIZE	CAGE CODE	DRAWING NUMBER	REV
	FUNCT				**94155**	**05-08-5018**	**P**
APPLICATION		SIGNOFFS	DATE	CONTRACT:			

FOR OFFICIAL USE ONLY

REVISION RECORD

REV	DESCRIPTION	DATE
G	• PAGE 8, CHANGED THETA JA TO θja = +170°C/W AND THETA JC TO θjc = +40°C/W FROM θja = 225°C/W AND θjc 18°C/W PER PACKAGE ENGINEERING.	9/05/00
H	• CONVERSION FROM WORD PERFECT TO MICROSOFT WORD. REDUCED SPEC PAGES TO 14 TOTAL. • PAGE 2, AN ADDITIONAL REVISION RECORD PAGE WAS INSTALLED • MADE THE REVISION RELEASE DATES AND THE DOCUMENT CONTROL HISTORY PAGE DATE MATCH • PAGE 3: PARAGRAPH 3.2.1 THROUGH 3.2.4, ADDED THE WORD "OPTION" PRECEDING THE NUMBER OF EACH LTC PART NUMBER FOR BETTER CUSTOMER ORDERING CONVENIENCE. • PAGE 4: PARAGRAPH 3.6, CHANGED "TABLE IA" TO "TABLE II" PARAGRAPH 3.7, CHANGED "TABLE III" TO "TABLE IV" PARAGRAPHS 3.8.1 AND 3.8.2, ADDED THE PACKAGE TYPES AND OPTIONS AFTER EACH FIGURE. PARAGRAPH 3.9, CHANGED "TABLE II" TO "TABLE III" PARAGRAPHS 3.10.1 AND 3.10.2, ADDED THE PACKAGE TYPES AFTER EACH FIGURE PARAGRAPH 3.11.1 WAS CHANGED FROM "…dosage rate of approximately 20 Rads per second" TO "…dosage rate of less than or equal to 10 Rads per second" • PAGE 5: PARAGRAPHS 4.1 THROUGH 4.4.2.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. • PAGE 6: PARAGRAPH 4.4.3 CHANGE WAS DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • PAGES 7 THROUGH 12, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • PAGE 9, MOVED FIGURE 4 TO PAGE 9 FROM PAGE 10 AS SHOWN IN PREVIOUS SPECIFICATION REVISION. • PAGE 12, FIGURE 7, TOTAL DOSE BIAS CIRCUIT REVISED BY ENGINEERING. • PAGE 13, TABLES I, II AND CORRESPONDING NOTES ALL ON ONE PAGE.	03/26/02
J	• PAGE 8, CHANGED OUTLINE DRAWING PIN 1 NOTCH MOVED TO INSIDE LEAD LOCATION.	05/19/03
K	• PAGE 4, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	03/15/05
L	• PAGE 4, ADDED NOTE: ABSOLUTE MAXIMUM RATINGS ARE THOSE VALUES BEYOND WHICH THE LIFE OF A DEVICE MAY BE IMPAIRED.	08/15/05
M	• PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1	12/07/07
N	• PAGE 4, PARAGRAPH 3.11.1 CHANGED VERBIAGE.	04/30/08
P	• **PAGE 5, PARAGRAPH 4.4.2 CHANGED VERBIAGE.** • **PAGE 8, FIGURE 2 NOTE 2 ADDED TO LEAD THICKNESS. DATA SHEET CHANGE TO ELECTRICAL TEST NOTES #7, #9 V_{IN} = 12V CHANGED TO V_{IN} = 15V.**	**07/18/08**

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1021-10, Precision 10V Reference, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH1021BMH-10 (TO5 Metal Can, 8 Leads)

3.2.2 Option 2 – RH1021CMH-10 (TO5 Metal Can, 8 Leads)

3.2.3 Option 3 – RH1021DMH-10 (TO5 Metal Can, 8 Leads)

3.2.4 Option 4 – RH1021CMW-10 (Glass Sealed Flatpack, 10 Leads)

3.3 Part Marking Includes:

3.3.1 LTC Logo

3.3.2 LTC Part Number (See Paragraph 3.2)

3.3.3 Date Code

3.3.4 Serial Number

3.3.5 ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Input Voltage	40V
Input / Output Voltage Differential	35V
Output to Ground Voltage (Shunt Mode Current Limit)	16V
Trim Pin to Ground Voltage	
Positive	Equal to V_{OUT}
Negative	-20V
Output Short Circuit Duration	
V_{IN} = 35V	10 sec
V_{IN} = $\leq$ 20V	Indefinite
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

NOTE: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in **Table I** and **Table II**.

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.

3.8 Burn-In Requirement:

3.8.1 Options 1, 2, 3 (TO5): Static Burn-In, **Figure 5**

3.8.2 Option 4 (Glass Sealed Flatpack) : Static Burn-In, **Figure 6**

3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table III** herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical, dimensions, and electrical requirements shall be as specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with **Figure 1** (TO5/8 Leads) and **Figure 2** (Glass Sealed Flatpack/10 Leads).

3.10.2 Terminal Connections: The terminal connections shall be as specified in **Figure 3** (TO5/8 Leads) and **Figure 4** (Glass Sealed Flatpack/10 Leads).

3.10.3 Lead Material and Finish: The lead material shall be Kovar for TO5 and alloy 42 for flatpack. The lead finish shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in **Figure 7**.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in **Table IV** herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in **Table IV** herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1

Group B, Subgroup 2c = 10%	Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)
Group B, Subgroup 3 = 10%	
Group B, Subgroup 4 = 5%	Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each.

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM Photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

4.6.9 A copy of outside test laboratory radiation report if ordered

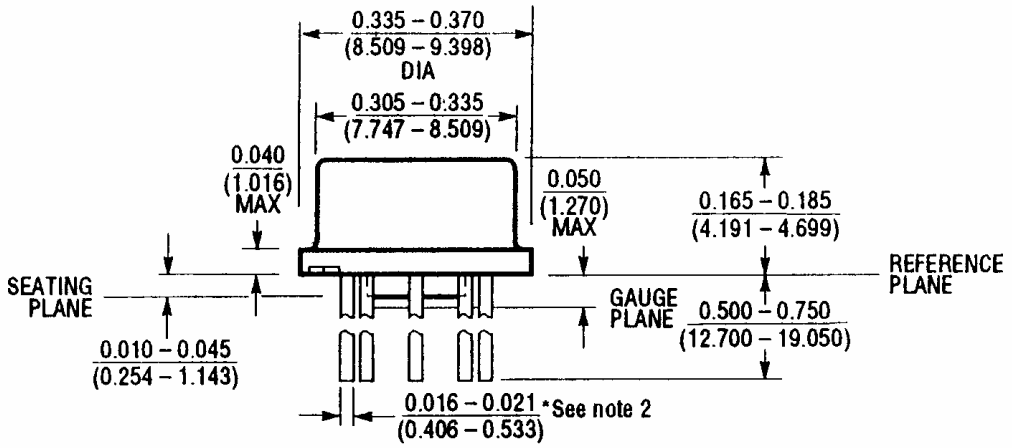
4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

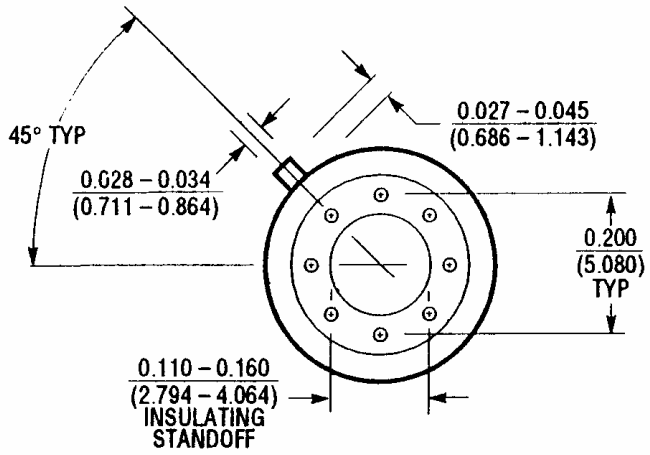
Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTIONS 1, 2, 3

TO5 METAL CAN / 8 LEADS CASE OUTLINE





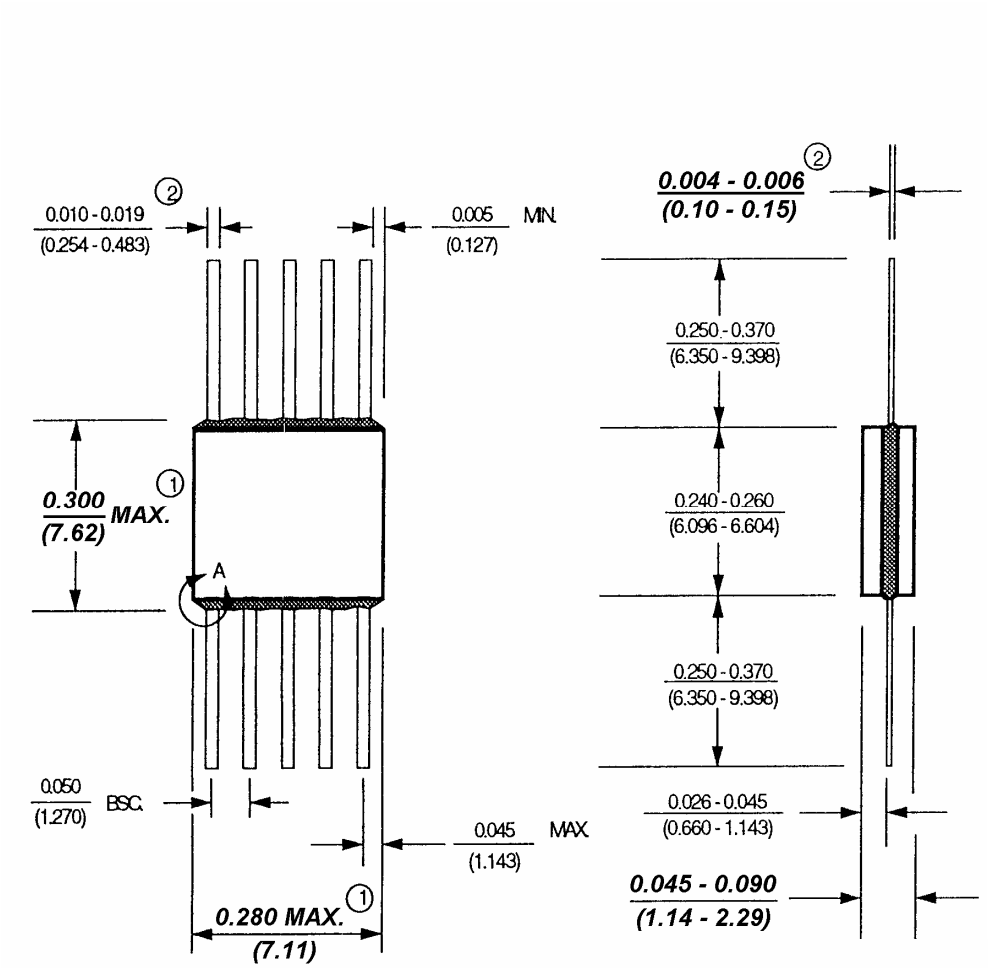
NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 – 0.024}{(0.406 – 0.610)}$

θja = +150°C/W
θjc = +40°C/W

FIGURE 1

DEVICE OPTION 4
W10, GLASS SEALED FLATPACK / 10 LEADS CASE OUTLINE



NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).

θ_{ja} = +170°C/W
θ_{jc} = +40°C/W

FIGURE 2

TERMINAL CONNECTIONS
DEVICE OPTIONS 1, 2, 3, TO5 METAL CAN / 8 LEADS

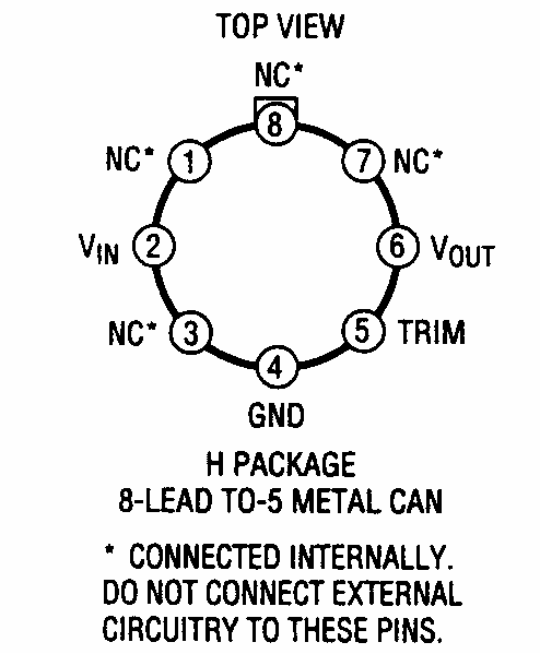


FIGURE 3

OPTION 4, GLASS SEALED FLATPACK / 10 LEADS

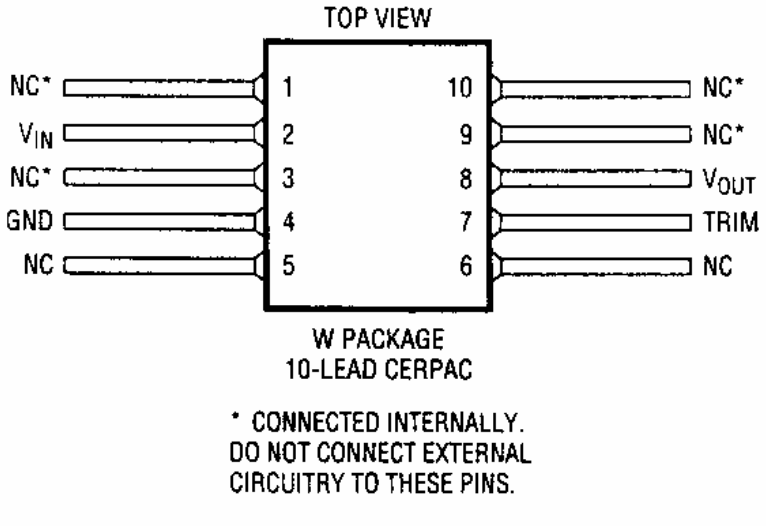
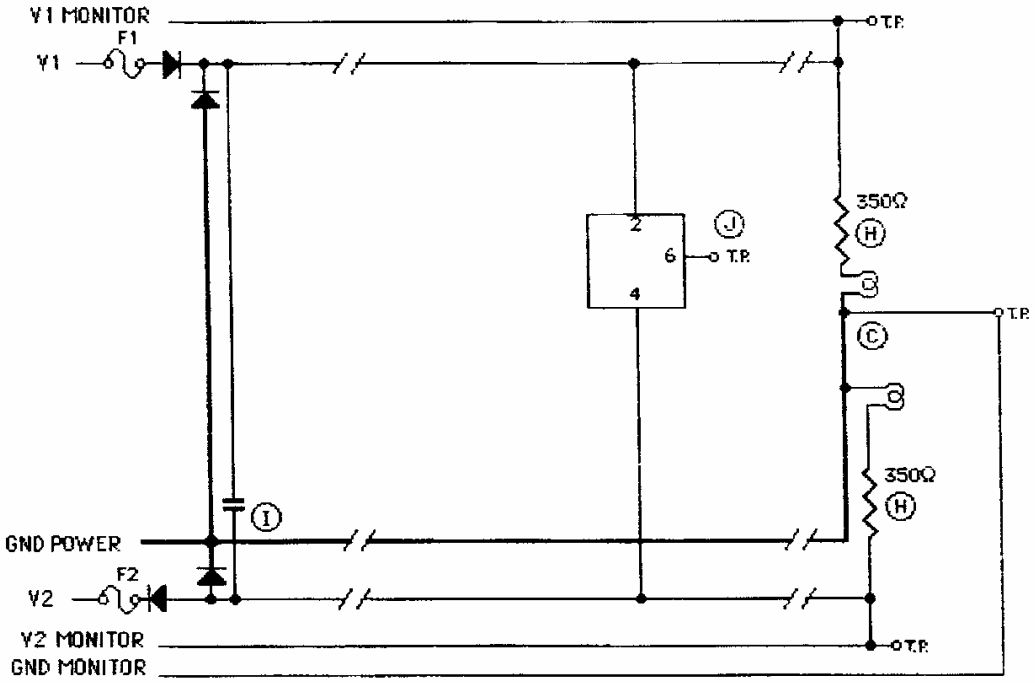


FIGURE 4

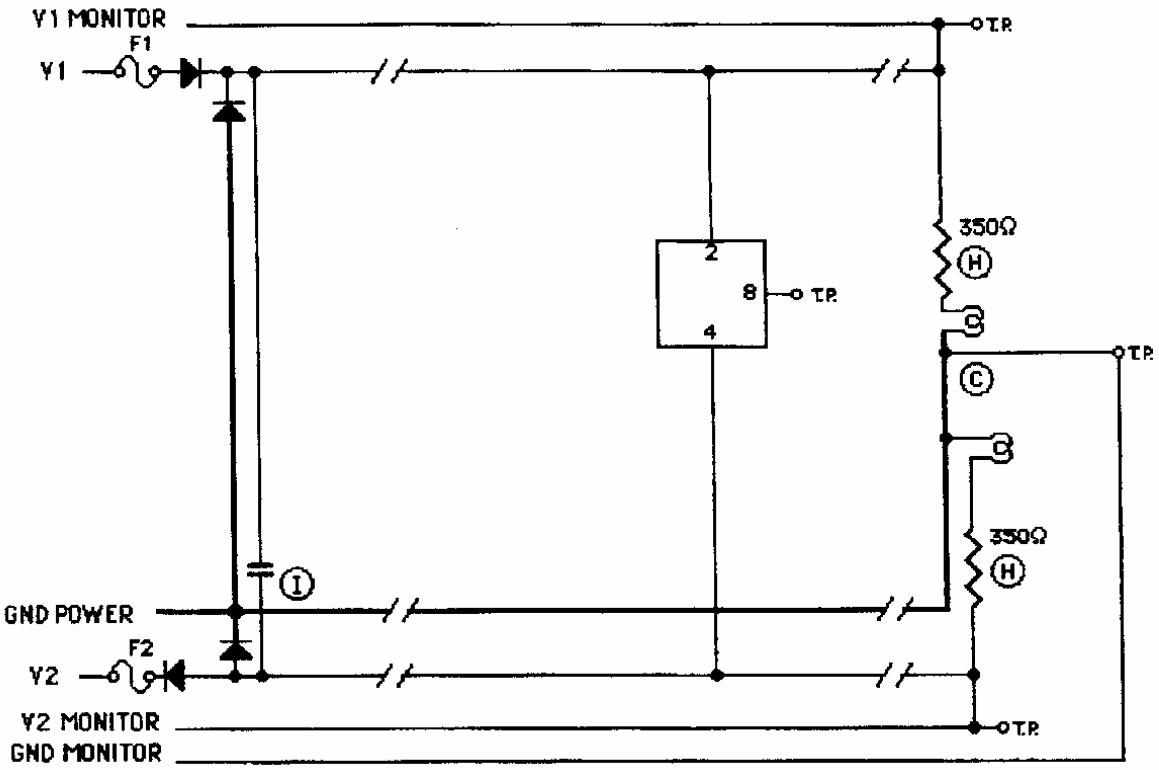
BURN-IN CIRCUIT
OPTIONS 1, 2, 3, TO5 METAL CAN / 8 LEADS



NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 168 °C maximum.
3. Ta = 150 °C.
4. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V

FIGURE 5

BURN-IN CIRCUIT
OPTION 4, GLASS SEALED FLATPACK / 10 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 168 °C maximum.
3. Ta = 150 °C.
4. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V

FIGURE 6

TOTAL DOSE BIAS CIRCUIT

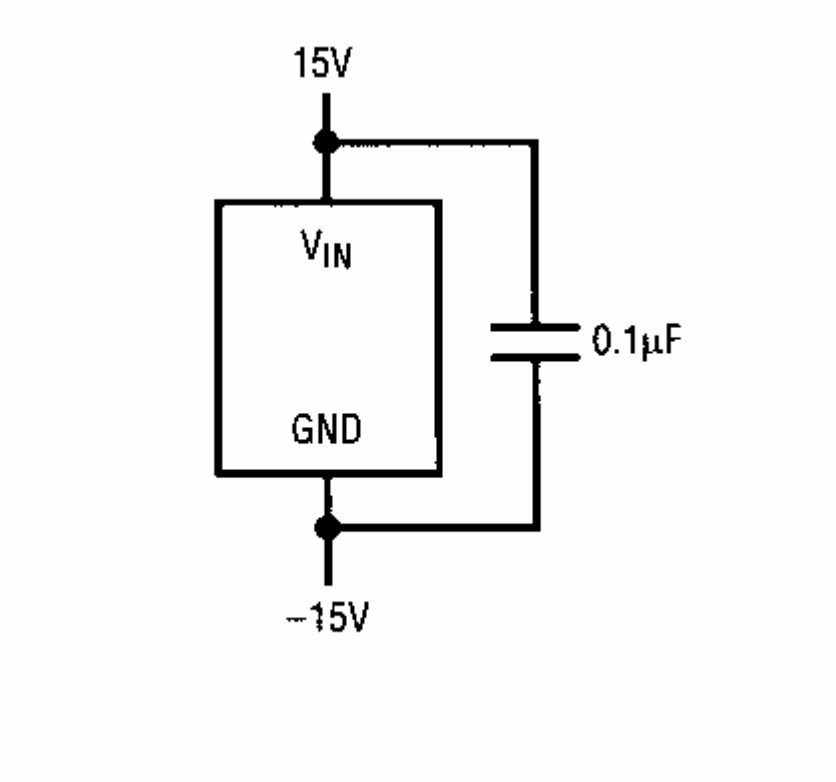


FIGURE 7

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) NOTE 9

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_A \le 125°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OUT}	Output Voltage	RH1021CM-10	1	9.995		10.005	1					V
		RH1021BM-10, DM-10	1	9.95		10.05	1					V
TCV_{OUT}	Output Voltage Temperature Coefficient	RH1021BM-10	2							5	2,3	ppm/°C
		RH1021CM-10, DM-10	2							20	2,3	ppm/°C
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$11.5V \le V_{IN} \le 14.5V$	3			4	1			6	2,3	ppm/V
		$14.5V \le V_{IN} \le 40V$	3			2	1			4	2,3	ppm/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Sourcing Current)	$0 \le I_{OUT} \le 10mA$	3			25	1			40	2,3	ppm/mA
	Load Regulation (Shunt Mode)	$1.7mA \le I_{OUT} \le 10mA$	3,4			100	1			150	2,3	ppm/mA
I_S	Supply Current (Series Mode)					1.7	1			2.0	2,3	mA
I_{MIN}	Minimum Current (Shunt Mode)	V_{IN} Is Open				1.5	1			1.7	2,3	mA
	Output Voltage Noise	$0.1Hz \le f \le 10Hz$	5		6							μV_{P-P}
		$10Hz \le f \le 1kHz$	5			6	4					μV_{RMS}
	Long-Term Stability of V_{OUT}	ΔT = 1000 Hrs Noncumulative	6		15							ppm
	Temperature Hysteresis of V_{OUT}	$\Delta T = \pm 25°C$			5							ppm

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE 7

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si) MIN	MAX	20Krad(Si) MIN	MAX	50Krad(Si) MIN	MAX	100Krad(Si) MIN	MAX	200Krad(Si) MIN	MAX	UNITS
V_{OUT}	Output Voltage	RH1021CM-10	1	9.992	10.008	9.99	10.01	9.987	10.013	9.985	10.015	9.98	10.02	V
		RH1021BM-10, DM-10	1	9.95	10.05	9.945	10.055	9.942	10.06	9.938	10.06	9.935	10.065	V
TCV_{OUT}	Output Voltage Temperature Coefficient	RH1021BM-10	2		5		5		5		7		10	ppm/°C
		RH1021CM-10, DM-10	2		20		20		20		22		25	ppm/°C
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$11.5V \le V_{IN} \le 14.5V$	3		4		4		4.5		5		6	ppm/V
		$14.5V \le V_{IN} \le 40V$	3		2		2		2		2		3	ppm/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Sourcing Current)	$0 \le I_{OUT} \le 10mA$	3,8		25		25		25		25		25	ppm/mA
	Load Regulation (Shunt Mode)	$1.7mA \le I_{OUT} \le 10mA$	3,4		100		100		100		100		150	ppm/mA
I_{MIN}	Minimum Current (Shunt Mode)	V_{IN} Is Open			1.5		1.5		1.5		1.5		1.5	mA
I_S	Supply Current (Series Mode)				1.7		1.7		1.7		1.7		1.7	mA

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is measured by dividing the change inoutput voltage over the temperature range by the change in temperature. Separate tests are done for hot and cold; T_{MIN} to 25°C and 25°C to T_{MAX}. Incremental slope is also measured at 25°C.

Note 3: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately. Package thermal resistance is 150°C/W for the TO-5 (H) package and 170°C/W for the 10-lead flatpack (W) package.

Note 4: Shunt mode regulation is measured with the input open. With the input connected, shunt mode current can be reduced to 0mA. Load regulation will remain the same.

Note 5: RMS noise is measured with a 2-pole highpass filter at 10Hz and a 2-pole lowpass filter at 1kHz. The resulting output is full wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. Correction factors are used to convert from average to RMS and to correct for the nonideal bandpass of the filters. Peak-to-peak noise is measured with a single highpass filter at 0.1Hz and a 2-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. Test time is 10 seconds.

Note 6: Consult factory for units with long term stability data.

Note 7: V_{IN} = 15V, I_{OUT} = 0, T_A = 25°C, unless otherwise noted.

Note 8: $I_{OUT(MAX)}$ (Sourcing) is 5mA for exposures greater than 100Krad (Si).

Note 9: V_{IN} = 15V, I_{OUT} = 0, unless otherwise noted.

Note 10: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_A = 25°C

APPLIES TO RH1021BM-10 AND RH1021DM-10

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OUT}	9.95	10.05	-0.003	0.003	V

APPLIES TO RH1021CM-10

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OUT}	9.995	10.005	-0.003	0.003	V

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4
Group A Test Requirements (Method 5005)	1,2,3,4
Group B and D for Class S, and Group C and D for Class B End Point Electrical Parameters (Method 5005)	1,2,3

* PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.