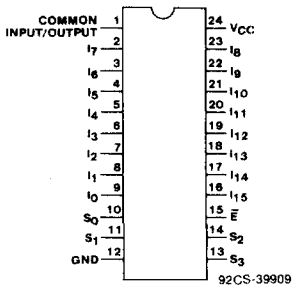
CD54/74HC4067
CD54/74HCT4067

File Number **1783**

Advance Information/ Preliminary Data

High-Speed CMOS Logic



TOP VIEW
TERMINAL ASSIGNMENT

16-Channel Analog Multiplexer/Demultiplexer

Type Features:

- *Wide analog input voltage range:*
- *Low "on" resistance:*
  70 Ω typ (V_{CC} = 4.5V)
  60 Ω typ (V_{CC} = 6V)
- *Fast switching and propagation speeds*
- *"Break-before-make" switching: (6 ns typ @ 4.5V)*
- *Available in both narrow and wide-body plastic packages*

The RCA-CD54/74HC/HCT4067 are digitally controlled analog switches which utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range. They are bidirectional switches thus allowing any analog input to be used as an output and visa-versa. The switches have low "on" resistance and low "off" leakages. In addition, these devices have an enable control which when high will disable all switches to their "off" state.

The CD54HC4067 and CD54HCT4067 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC4067 and CD74HCT4067 are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54/74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V
- *CD54/74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

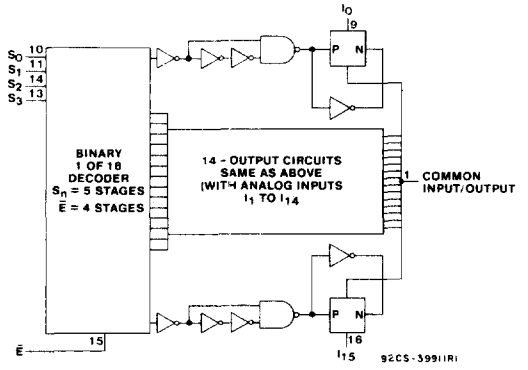


Fig. 1 - Functional diagram.

TRUTH TABLE

S0	S1	S2	S3	$\overline{E}$	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

1 = High Level
0 = Low Level
X = Don't Care.

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC} + 0.5V$) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f (Control Inputs)			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC/CD54HC4067										CD74HCT/CD54HCT4067										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS			74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	LOGIC V_I V	SWITCH V_{IS} V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		LOGIC V_I V	SWITCH V_{IS} V		+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max				Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—											V
			4.5	3.15	—	—	3.15	—	3.15	—	—	—		2	—	—	2	—	2	—	
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5											
			4.5	—	—	1.35	—	1.35	—	1.35	—	—		—	—	0.8	—	0.8	—	0.8	
			6	—	—	1.8	—	1.8	—	1.8											
Maximum "On" Resistance R_{ON} I_O = ImA	V_{CC} or Gnd	V_{CC} or Gnd	4.5	—	70	160	—	200	—	240	V_{CC} or Gnd	V_{CC} or Gnd		—	70	160	—	200	—	240	Ω
			6	—	60	140	—	175	—	210				—	—	—	—	—	—	—	
	V_{CC} to Gnd	V_{CC} to Gnd	4.5	—	90	180	—	225	—	270	V_{CC} to Gnd	V_{CC} to Gnd		—	90	180	—	225	—	270	
			6	—	80	160	—	200	—	240				—	—	—	—	—	—	—	
Maximum "On" resistance between any two switches ΔR_{ON}	—	—	4.5	—	10	—	—	—	—	—	—	—		—	10	—	—	—	—	—	
	—	—	6	—	8.5	—	—	—	—	—	—	—		—	—	—	—	—	—	—	
Switch "Off" Leakage Current I_{IZ} 16 Channels	$\overline{E}$ = V_{CC}	V_{CC} or Gnd	6	—	—	±0.8	—	±8	—	±8	$\overline{E}$ = V_{CC}	V_{CC} or Gnd		—	—	±0.8	—	±8	—	±8	μA
Logic Input Leakage Current I_I	V_{CC} or Gnd	—	6	—	—	±0.1	—	±1	—	±1	**	—		—	—	±0.1	—	±1	—	±1	
Quiescent Device Current I_O = OmA I_{CC}	V_{CC} or Gnd	—	6	—	—	8	—	80	—	160	V_{CC} or Gnd	—		—	—	8	—	80	—	160	
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*	—	—	—	—	—	—	—	—	—	—	V_{CC} -2.1	—		—	100	360	—	450	—	490	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

**Any Voltage Between V_{cc} & Gnd.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
S_0 - S_3	0.5
$\overline{E}$	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		CL (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay Time: Switch In to Switch Out	t_{PLH}, t_{PHL}	15	6	6	ns
Switch Turn Off: $\overline{E}$ to Out	t_{PLZ}, t_{PHZ}	15	23	23	ns
Switch Turn Off: Sn to Out	t_{PLZ}, t_{PHZ}	15	21	21	ns
Switch Turn On: $\overline{E}$ to Out	t_{PZL}, t_{PZH}	15	23	25	ns
Switch Turn On: Sn to Out	t_{PZL}, t_{PZH}	15	25	25	ns
Power Dissipation Capacitance*	C_{PD}	—	93	96	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where: f_i = input frequency, f_o = output frequency, C_L = load capacitance, C_S = switch capacitance, V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay Time Switch In to Out	t_{PLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{PHL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	ns
Switch Turn-On $\overline{E}$ to Out	t_{PZL}	2	—	275	—	—	—	345	—	—	—	415	—	—	ns
		4.5	—	55	—	60	—	69	—	75	—	83	—	90	ns
		6	—	47	—	—	—	59	—	—	—	71	—	—	ns
	t_{PZH}	2	—	300	—	—	—	375	—	—	—	450	—	—	ns
Sn to Out		4.5	—	60	—	60	—	75	—	75	—	90	—	90	ns
		6	—	51	—	—	—	64	—	—	—	76	—	—	ns
Switch Turn-Off $\overline{E}$ to Out	t_{PLZ}	2	—	275	—	—	—	345	—	—	—	415	—	—	ns
		4.5	—	55	—	55	—	69	—	69	—	83	—	83	ns
		6	—	47	—	—	—	59	—	—	—	71	—	—	ns
Sn to Out	t_{PHZ}	2	—	290	—	—	—	365	—	—	—	435	—	—	ns
		4.5	—	58	—	58	—	73	—	73	—	87	—	87	ns
		6	—	49	—	—	—	62	—	—	—	74	—	—	ns
Input (Control) Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

ANALOG CHANNEL CHARACTERISTICS — Typical Values at T_A = 25°C

CHARACTERISTICS		TEST CONDITION	V_{CC} V	HC/HCT	UNITS
Switch Frequency Response at - 3 dB (Fig. 12)		Fig. 3 Notes 1 & 2	4.5	89	MHz
Sine Wave Distortion		Fig. 4	4.5	0.051	%
Feedthrough Noise: $\overline{E}$ to Switch		Fig. 5 Notes 2 & 3	4.5	TBE	mV
S to Switch		Fig. 5 Notes 2 & 3	4.5	TBE	mV
Switch "OFF" Signal Feedthrough (Fig. 13)		Fig. 6	4.5	-75	dB
Switch Input Capacitance	C_S	—	—	5	pF
Common Capacitance	C_{COM}	—	—	50	pF

NOTES: 1. Adjust input level for 0 dBm at output, f = 1 kHz.
2. V_{IS} is centered at $V_{cc}/2$.
3. Adjust input for 0 dBm. at V_{IS}

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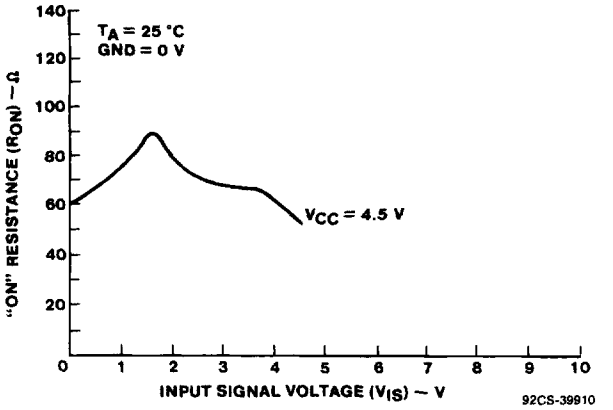

Fig. 2 - Typical "ON" resistance versus input signal voltage.

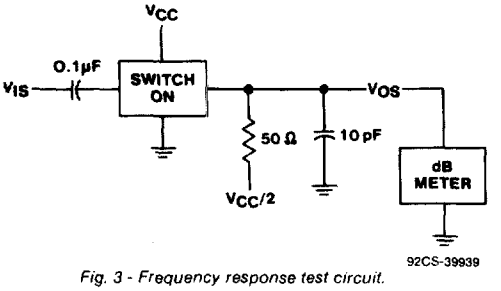

Fig. 3 - Frequency response test circuit.

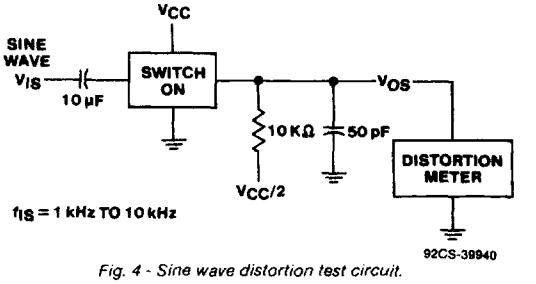

Fig. 4 - Sine wave distortion test circuit.

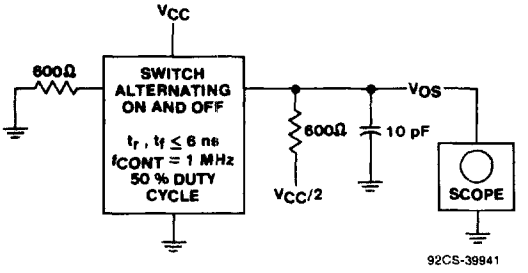

Fig. 5 - Control-to-switch feedthrough noise test circuit.

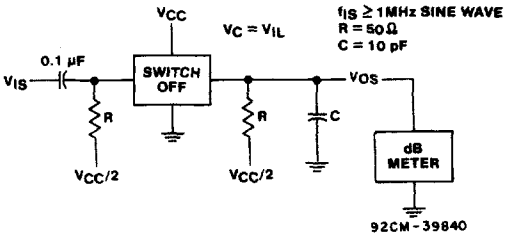

Fig. 6 - Switch off signal feedthrough test circuit.

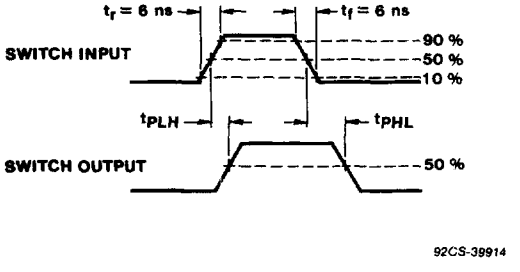

Fig. 7 - Switch propagation-delay times wave forms.

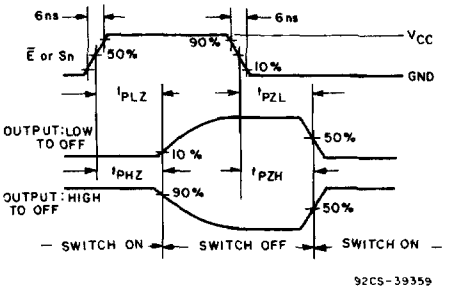

Fig. 8 - Switch turn-on and turn-off propagation delay times wareforms, for HC types.

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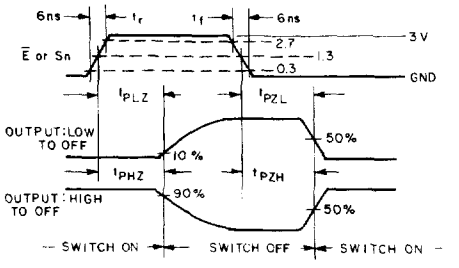

Fig. 9 - Switch turn-on and turn-off propagation delay times waveforms for HCT Types.

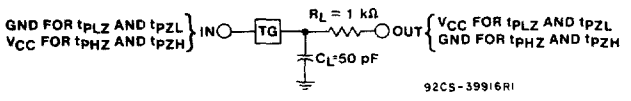

Fig. 10 - Switch on/off propagation delay time test circuit.

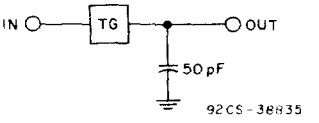

Fig. 11 - Switch In to Switch Out Propagation delay time test circuit.

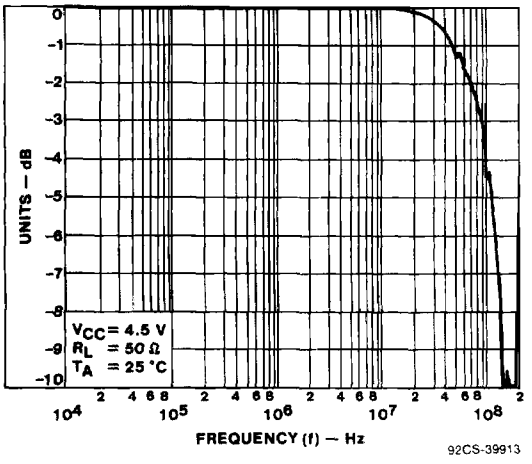

Fig. 12 - Typical switch frequency response.

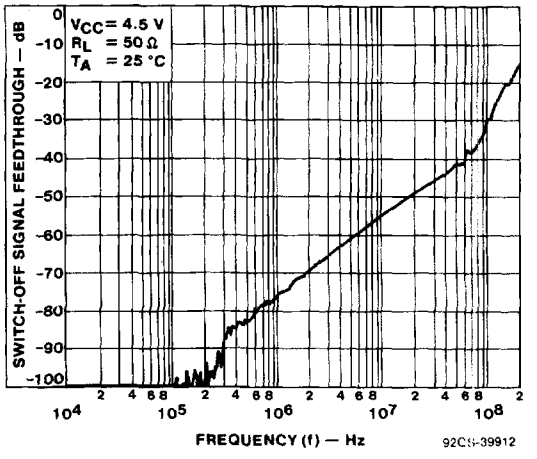

Fig. 13 - Typical switch-off signal feed through vs. frequency.