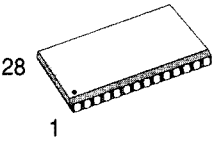
VERY FAST CMOS 1 Megabit (1M x 1) SRAM

- 1 Megabit CMOS FAST SRAM
- EQUAL CYCLE AND ACCESS TIMES: 15, 17, 20, 25ns
- LOW V_{CC} DATA RETENTION: 2V
- SEPARATE DATA INPUT AND OUTPUT
- JEDEC PLASTIC SOJ, 400 mil PACKAGE



PSOJ28 (E)
400 mils

DESCRIPTION

The M621100 is a 1 Megabit Fast CMOS SRAM, organized as 1,048,576 by 1 bit. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A19	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

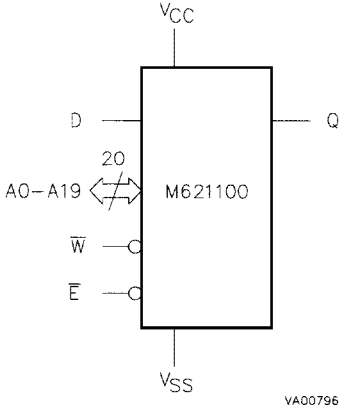


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
PD	Power Dissipation	1	W

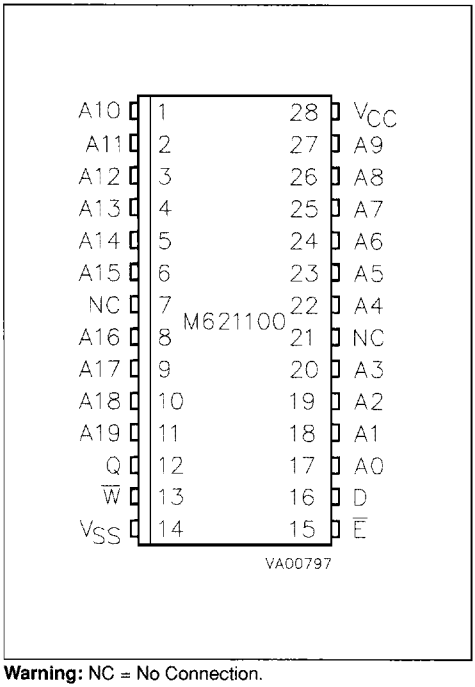
Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power
Read	V_{IL}	V_{IH}	X	Data Output	Active
Write	V_{IL}	V_{IL}	Data Input	Hi-Z	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

Figure 2. SOJ Pin Connections



Warning: NC = No Connection.

READ MODE

The M621100 is in the Read mode whenever Write Enable ($\overline{W}$) is High and Chip Enable ($\overline{E}$) is asserted. This provides access to data from one of the 1,048,576 locations in the static memory array, specified by the 20 address inputs. Valid data will be available at the output pin (Q) within t_{AVQV} after the last stable address, providing $\overline{E}$ is Low. If Chip Enable access time is not met, data access will be measured from the limiting parameter (t_{ELQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M621100 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the write input $\overline{W}$ must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}$ Low), then $\overline{W}$ will return the output to high impedance within t_{WLQZ} of its falling edge. Data input must be valid for t_{DVWH}

WRITE MODE (cont'd)

before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M621100 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E}$ High). Operational modes are determined by device control inputs $\overline{W}$, and $\overline{E}$ as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

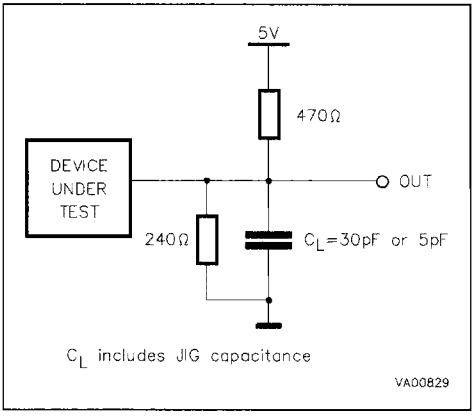


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} (2)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Output deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-15 & -17)		160	mA
		V_{CC} = 5.5V, (-20)		140	mA
		V_{CC} = 5.5V, (-25)		130	mA
I_{CC1} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E} = V_{IH}$, f = 0		25	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E} \ge V_{CC} - 0.2V$, f = 0		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$
3. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC} - 0.2V$

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M621100								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	15		17		20		25		ns
t_{AVQV} (1)	Address Valid to Output Valid		15		17		20		25	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		15		17		20		25	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	2		2		2		2		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	8	0	10	0	10	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns
t_{PU} (3)	Chip Enable Low to Power Up	0		0		0		0		ns
t_{PD} (3)	Chip Enable High to Power Down		15		17		20		25	ns

Notes: 1. C_L = 30pF
2. C_L = 5pF
3. Measured to 50% point between I_{CC} and I_{CC1}.

Figure 4. Read Mode AC Waveforms

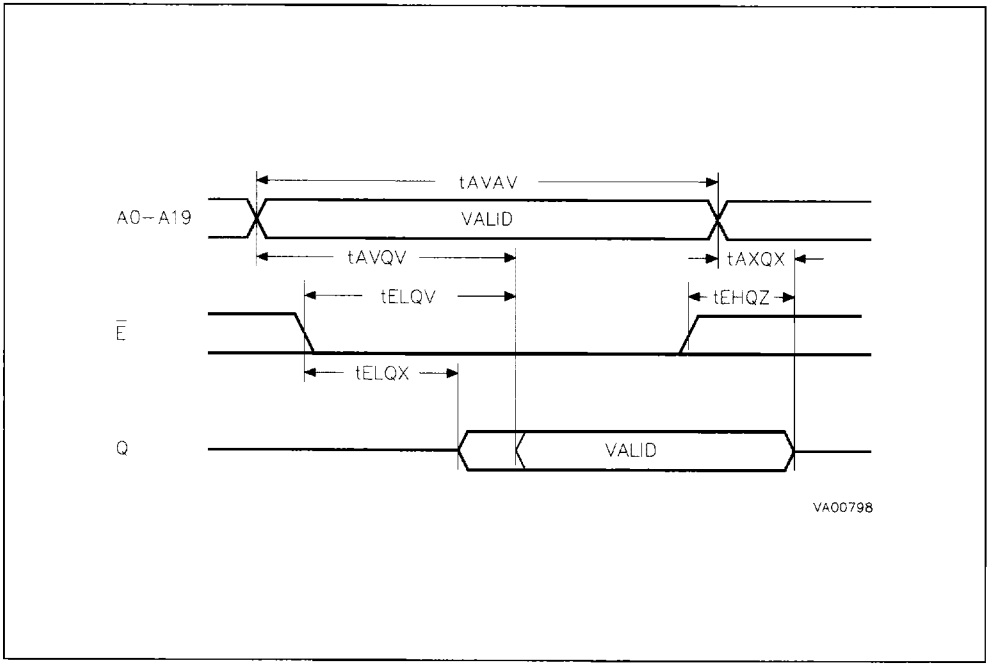


Figure 5. Standby Mode AC Waveforms

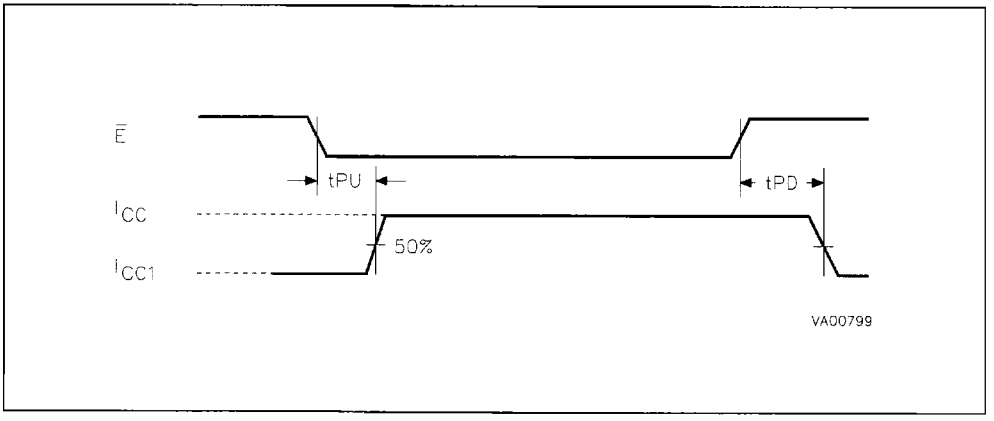


Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M621100								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	15		17		20		25		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	12		12		12		15		ns
t_{AVEH}	Address Valid to Chip Enable High	12		12		12		15		ns
t_{WLWH}	Write Enable Pulse Width	10		12		12		15		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	0	12	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	10		12		12		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	8		10		12		12		ns
t_{DVEH}	Input Valid to Chip Enable High	8		10		12		12		ns

Note: 1. C_L = 5pF

Figure 6. Write Enable Controlled, Write AC Waveforms

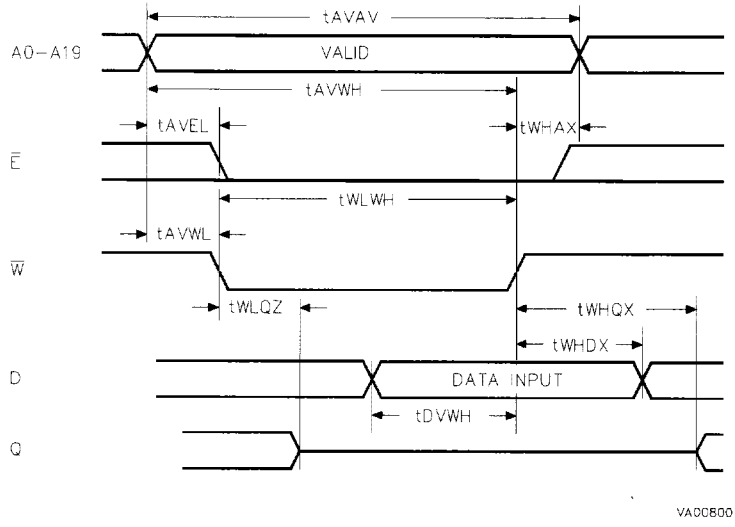


Figure 7. Chip Enable Controlled, Write AC Waveforms

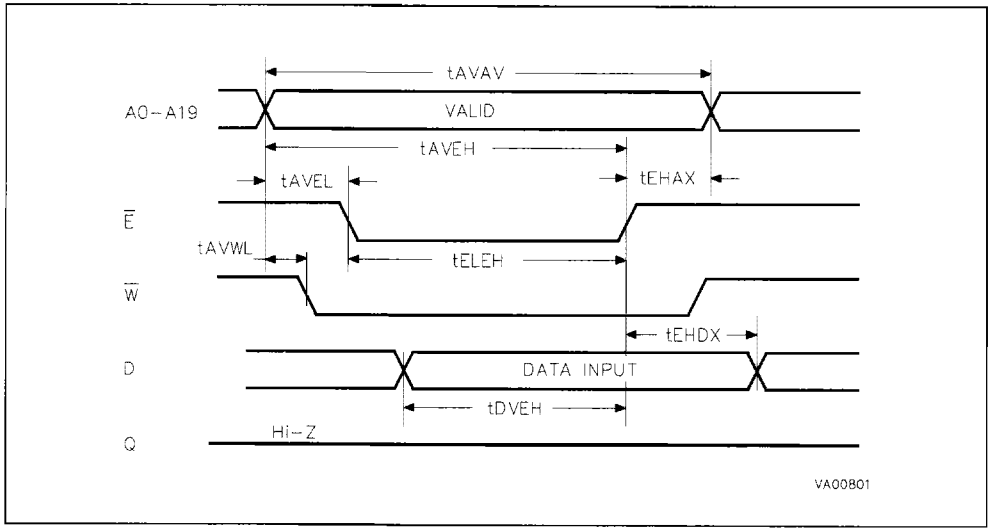
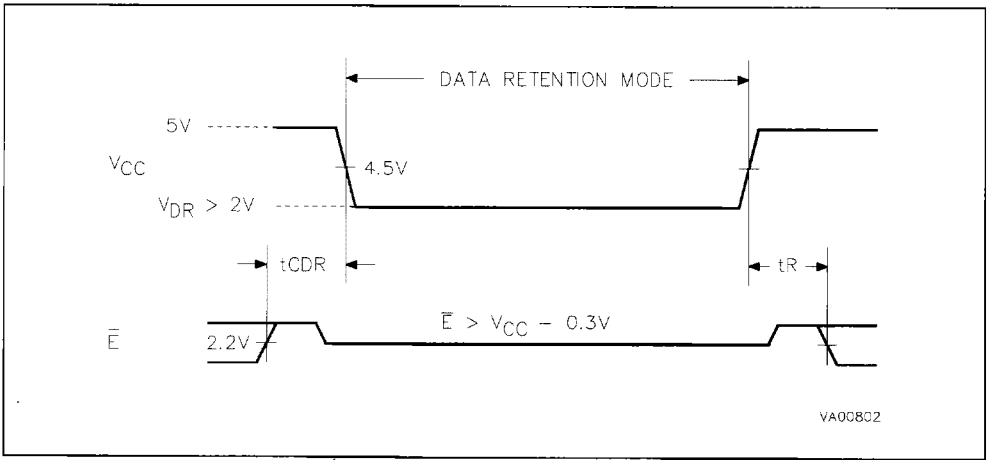


Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CC2} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E} \geq V_{CC} - 0.3V$, f = 0		1000	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

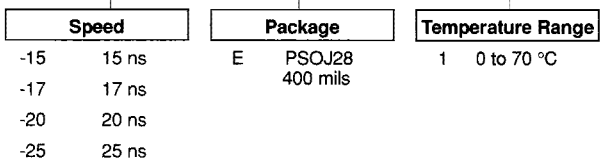
Note: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.3V$ or $V_{IL} \leq 0.3V$
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms



ORDERING INFORMATION

Example: M621100 -15 E 1



For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.