Low Capacitance, 4-/8-Channel ±15 V/+12 V *i*CMOS™ Multiplexers

ADG1208/ADG1209

FEATURES

<1 pC charge injection over full signal range
1 pF off capacitance
33 V supply range
120 Ω on resistance
Fully specified at ±15 V/+12 V
3 V logic compatible inputs
Rail-to-rail operation
Break-before-make switching action
Available in 16-lead TSSOP and 4 mm × 4 mm LFCSP_VQ
Typical power consumption < 0.03 µW

APPLICATIONS

Audio and video routing
Automatic test equipment
Data-acquisition systems
Battery-powered systems
Sample-and-hold systems
Communication systems

FUNCTIONAL BLOCK DIAGRAMS

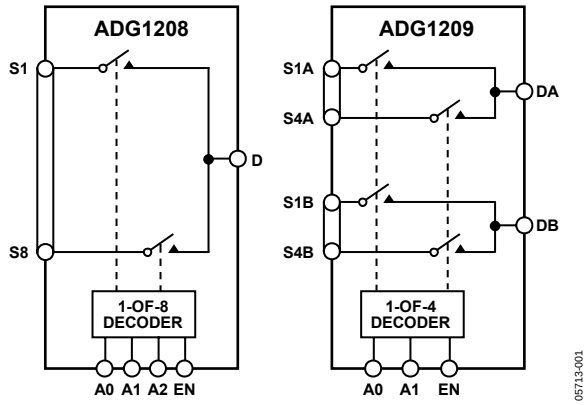

Figure 1.

GENERAL DESCRIPTION

The ADG1208 and ADG1209 are monolithic, *i*CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG1208 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The ADG1209 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off. When on, each channel conducts equally well in both directions and has an input signal range that extends to the supplies.

The *i*CMOS (industrial CMOS) modular manufacturing process combines high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and exceptionally low charge injection of these multiplexers make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Figure 2 shows that there is minimum charge injection over the entire signal range of the device. *i*CMOS construction also ensures ultralow power dissipation, making the parts ideally suited for portable and battery powered instruments.

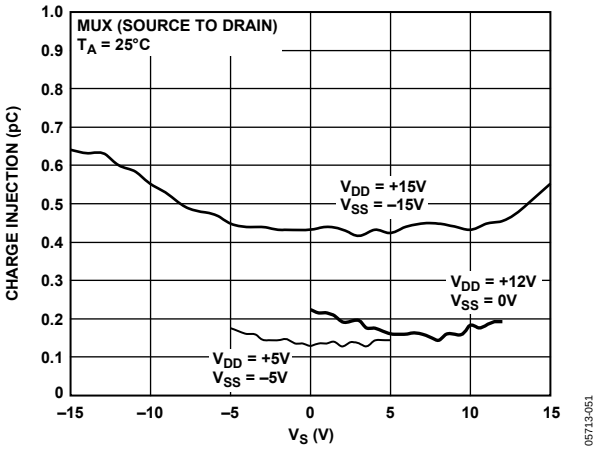

Figure 2. Source to Drain Charge Injection vs. Source Voltage

Rev. 0

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REVISION HISTORY

4/06—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.[1]

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance, R_{ON}	120			Ω typ	V_S = ±10 V, I_S = −1 mA, see Figure 29
	200	240	270	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	6	10	12	Ω max	
On Resistance Flatness, R_{FLAT} (On)	20			Ω typ	V_S = −5 V, 0 V, +5 V, I_S = −1 mA
	64	76	83	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_D = ±10 V, V_S = −10 V, see Figure 30
	±0.1	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V, 10 V; V_D = 10 V, 1 V; see Figure 30
ADG1208	±0.1	±0.6	±1	nA max	
ADG1209	±0.1	±0.6	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = ±10 V, see Figure 31
ADG1208	±0.2	±0.6	±1	nA max	
ADG1209	±0.2	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.005			μA max	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, $t_{TRANSITION}$	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	130	165	185	ns max	V_S = 10 V, see Figure 32
t_{ON} (EN)	75			ns typ	R_L = 300 Ω, C_L = 35 pF
	95	105	115	ns max	V_S = 10 V, see Figure 34
t_{OFF} (EN)	83			ns typ	R_L = 300 Ω, C_L = 35 pF
	100	125	140	ns max	V_S = 10 V, see Figure 34
Break-Before-Make Time Delay, t_{BBM}	25			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 10 V, see Figure 33
Charge Injection	0.4			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 35
Off Isolation	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
Total Harmonic Distortion + Noise	0.15			% typ	R_L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz, see Figure 39
−3 dB Bandwidth	550			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 37
C_S (Off)	1			pF typ	f = 1 MHz, V_S = 0 V
	1.5			pF max	f = 1 MHz, V_S = 0 V
C_D (Off) ADG1208	6			pF typ	f = 1 MHz, V_S = 0 V
	7			pF max	f = 1 MHz, V_S = 0 V
C_D (Off) ADG1209	3.5			pF typ	f = 1 MHz, V_S = 0 V
	4.5			pF max	f = 1 MHz, V_S = 0 V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
C_D, C_S (On) ADG1208	7			pF typ	f = 1 MHz, V_S = 0 V
	8			pF max	f = 1 MHz, V_S = 0 V
C_D, C_S (On) ADG1209	5			pF typ	f = 1 MHz, V_S = 0 V
	6			pF max	f = 1 MHz, V_S = 0 V
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{DD}	220			µA typ	Digital inputs = 5 V
			320	µA max	
I_{SS}	0.002			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{SS}	0.002			µA typ	Digital inputs = 5 V
			1.0	µA max	
V_{DD}/V_{SS}			±5/±16.5	V min/max	$\|V_{DD}\| = \|V_{SS}\|$

[1] Temperature range is as follows: Y version: –40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.[1]

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance, R_{ON}	300			Ω typ	V_S = 0 V to10 V, I_S = −1 mA, see Figure 29
	475	567	625	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels, ΔR_{ON}	5			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	16	26	27	Ω max	
On Resistance Flatness, R_{FLAT} (On)	60			Ω typ	V_S = 3 V, 6 V, 9 V; I_S = −1 mA
LEAKAGE CURRENTS					V_{DD} = 13.2 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 30
	±0.1	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 30
ADG1208	±0.1	±0.6	±1	nA max	
ADG1209	±0.1	±0.6	±1	nA max	
Channel On Leakage I_D, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 10 V; see Figure 31
ADG1208	±0.2	±0.6	±1	nA max	
ADG1209	±0.2	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.001				
			±0.1	μA max	V_{IN} = V_{INL} or V_{INH}
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, $t_{TRANSITION}$	100			ns typ	R_L = 300 Ω, C_L = 35 pF
	170	210	235		V_S = 8 V, see Figure 32
t_{ON} (EN)	90			ns typ	R_L = 300 Ω, C_L = 35 pF
	110	140	160		V_S = 8 V, see Figure 34
t_{OFF} (EN)	105			ns typ	R_L = 300 Ω, C_L = 35 pF
	130	155	175		V_S = 8 V, see Figure 34
Break-Before-Make Time Delay, t_{BBM}	45			ns typ	R_L = 300 Ω, C_L = 35 pF
			20	ns min	V_{S1} = V_{S2} = 8 V, see Figure 33
Charge Injection	−0.2			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 35
Off Isolation	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
−3 dB Bandwidth	450			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 37
C_S (Off)	1.2			pF typ	f = 1 MHz, V_S = 6 V
	1.8			pF max	f = 1 MHz, V_S = 6 V
C_D (Off) ADG1208	7.5			pF typ	f = 1 MHz, V_S = 6 V
	9			pF max	f = 1 MHz, V_S = 6 V
C_D (Off) ADG1209	4.5			pF typ	f = 1 MHz, V_S = 6 V
	5.5			pF max	f = 1 MHz, V_S = 6 V
C_D, C_S (On) ADG1208	9			pF typ	f = 1 MHz, V_S = 6 V
	10.5			pF max	f = 1 MHz, V_S = 6 V
C_D, C_S (On) ADG1209	6			pF typ	f = 1 MHz, V_S = 6 V
	7.5			pF max	f = 1 MHz, V_S = 6 V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.002			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{DD}	220			µA typ	Digital inputs = 5 V
			330	µA max	
V_{DD}			5/16.5	V min/max	V_{SS} = 0 V, GND = 0 V

[1] Temperature range is as follows: Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog, Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle max)	100 mA
Operating Temperature Range	
Industrial (Y Version)	–40°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
TSSOP, θ_{JA}, Thermal Impedance	112°C/W
LFCSP_VQ, θ_{JA}, Thermal Impedance	30.4°C/W
Reflow Soldering Peak Temperature (Pb-Free)	260(+0/−5)°C

[1] Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

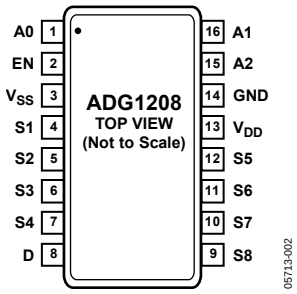


Figure 3. ADG1208 Pin Configuration (TSSOP)

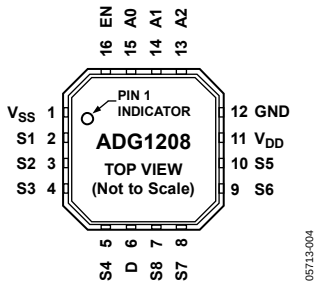


Figure 4. ADG1208 Pin Configuration (LFCSP_VQ), Exposed Pad Tied to Substrate, V_{SS}

Table 4. ADG1208 Pin Function Descriptions

Pin Number			
TSSOP	**LFCSP_VQ**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	1	V_{SS}	Most Negative Power Supply Potential. In single supply applications, it can be connected to ground.
4	2	S1	Source Terminal 1. Can be an input or an output.
5	3	S2	Source Terminal 2. Can be an input or an output.
6	4	S3	Source Terminal 3. Can be an input or an output.
7	5	S4	Source Terminal 4. Can be an input or an output.
8	6	D	Drain Terminal. Can be an input or an output.
9	7	S8	Source Terminal 8. Can be an input or an output.
10	8	S7	Source Terminal 7. Can be an input or an output.
11	9	S6	Source Terminal 6. Can be an input or an output.
12	10	S5	Source Terminal 5. Can be an input or an output.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	GND	Ground (0 V) Reference.
15	13	A2	Logic Control Input.
16	14	A1	Logic Control Input.

Table 5. ADG1208 Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

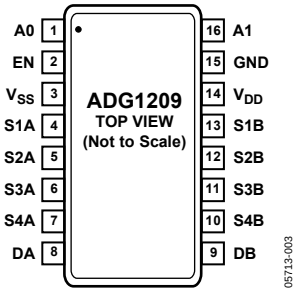


Figure 5. ADG1209 Pin Configuration (TSSOP)

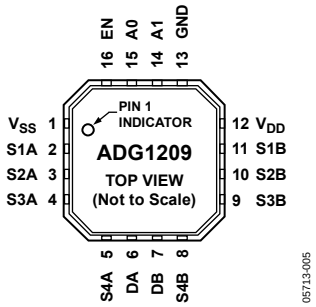


Figure 6. ADG1209 Pin Configurations (LFCSP_VQ), Exposed Pad Tied to Substrate, V_{SS}

Table 6. ADG1209 Pin Function Descriptions

Pin Number			
TSSOP	**LFCSP_VQ**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	1	V_{SS}	Most Negative Power Supply Potential. In single supply applications, it can be connected to ground.
4	2	S1A	Source Terminal 1A. Can be an input or an output.
5	3	S2A	Source Terminal 2A. Can be an input or an output.
6	4	S3A	Source Terminal 3A. Can be an input or an output.
7	5	S4A	Source Terminal 4A. Can be an input or an output.
8	6	DA	Drain Terminal A. Can be an input or an output.
9	7	DB	Drain Terminal B. Can be an input or an output.
10	8	S4B	Source Terminal 4B. Can be an input or an output.
11	9	S3B	Source Terminal 3B. Can be an input or an output.
12	10	S2B	Source Terminal 2B. Can be an input or an output.
13	11	S1B	Source Terminal 1B. Can be an input or an output.
14	12	V_{DD}	Most Positive Power Supply Potential.
15	13	GND	Ground (0 V) Reference.
16	14	A1	Logic Control Input.

Table 7. ADG1209 Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TYPICAL PERFORMANCE CHARACTERISTICS

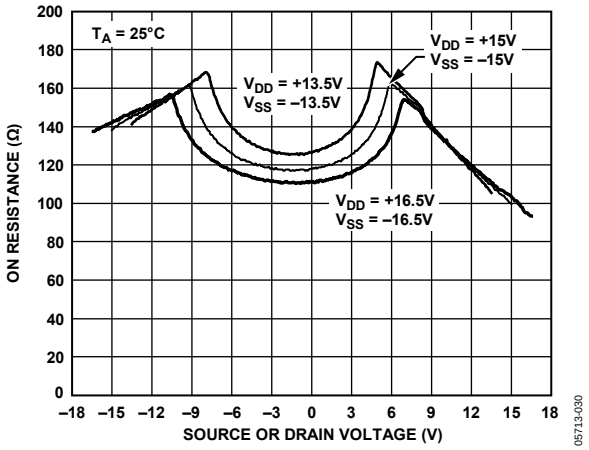


Figure 7. On Resistance as a Function of V_D (V_S) for Dual Supply

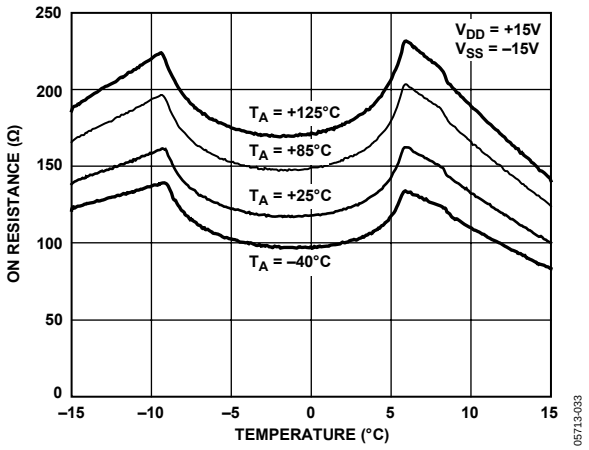


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

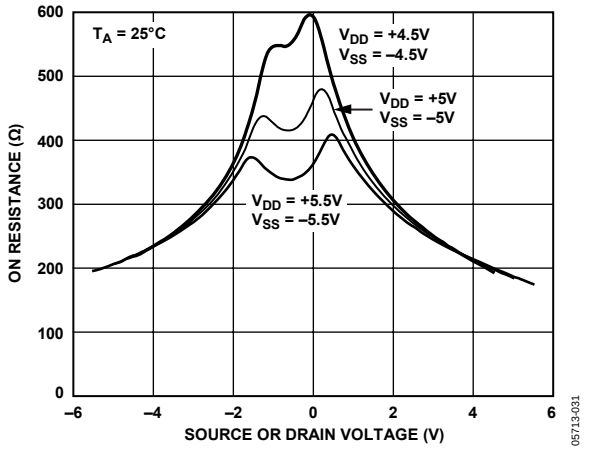


Figure 8. On Resistance as a Function of V_D (V_S) for Dual Supply

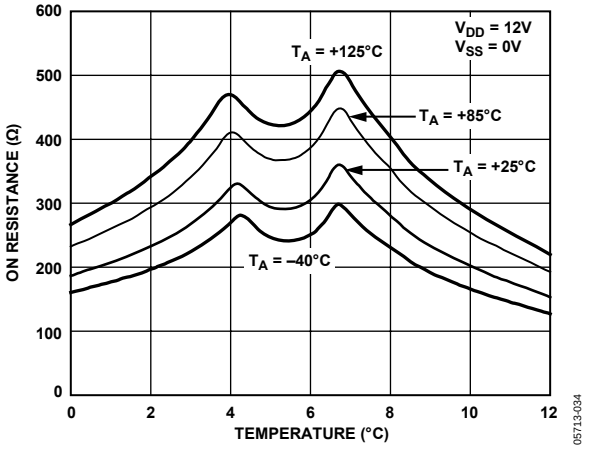


Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

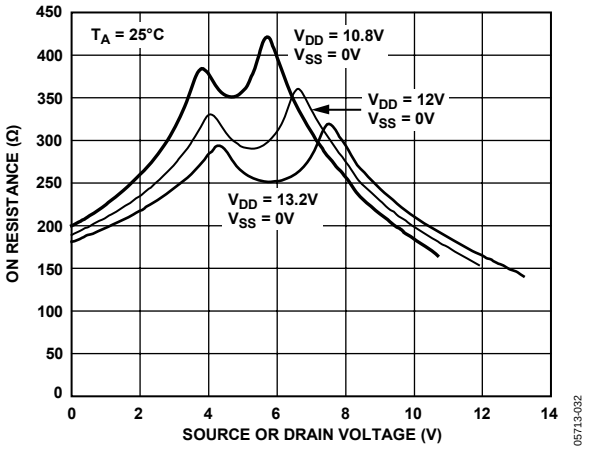


Figure 9. On Resistance as a Function of V_D (V_S) for Single Supply

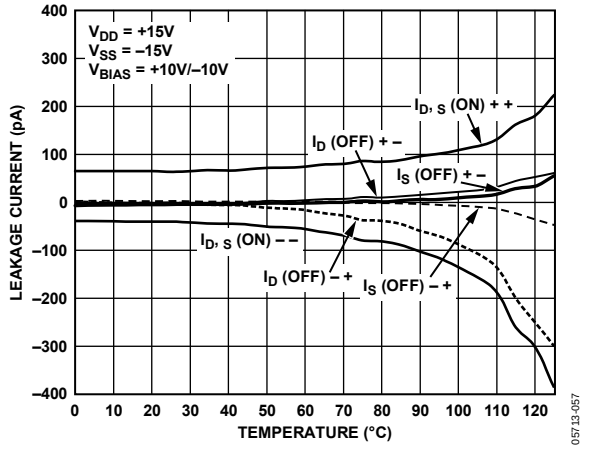


Figure 12. ADG1208 Leakage Currents as a Function of Temperature, Dual Supply

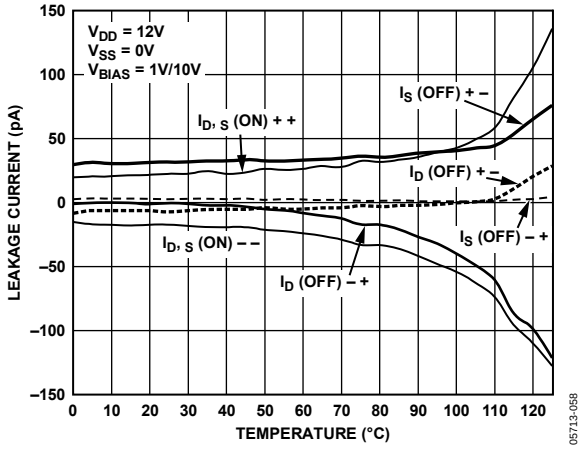


Figure 13. ADG1208 Leakage Currents as a Function of Temperature, Single Supply

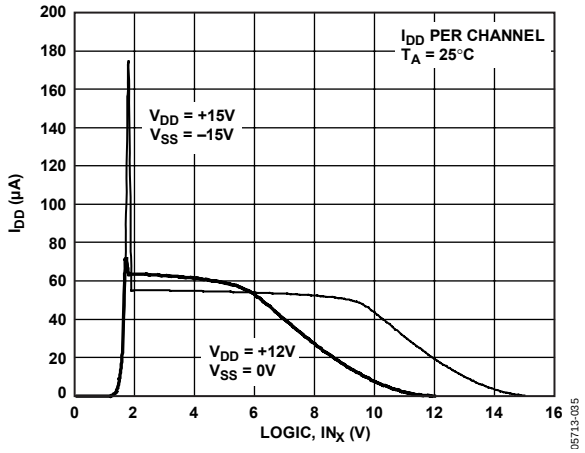


Figure 14. I_{DD} vs. Logic Level

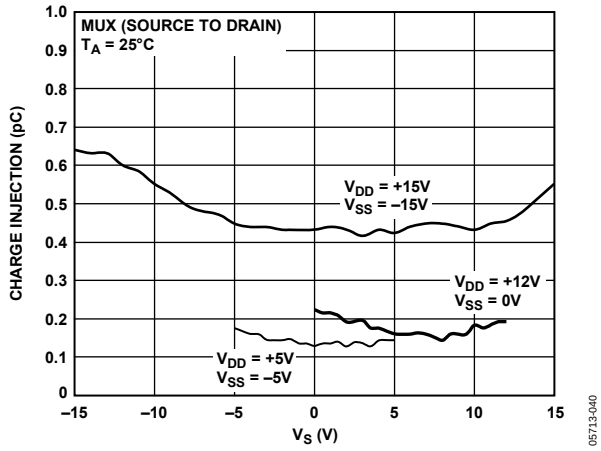


Figure 15. Source-to-Drain Charge Injection vs. Source Voltage

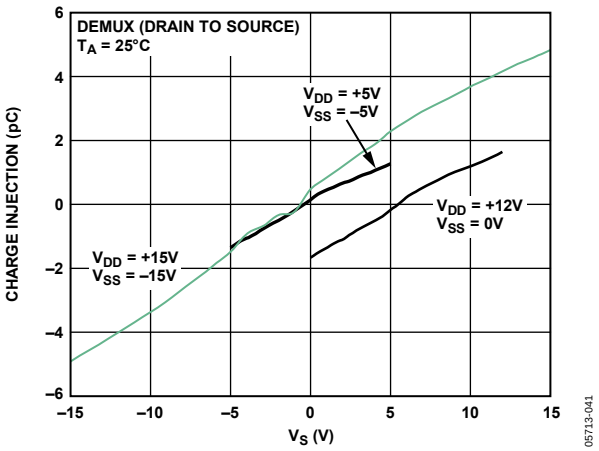


Figure 16. Drain-to-Source Charge Injection vs. Source Voltage

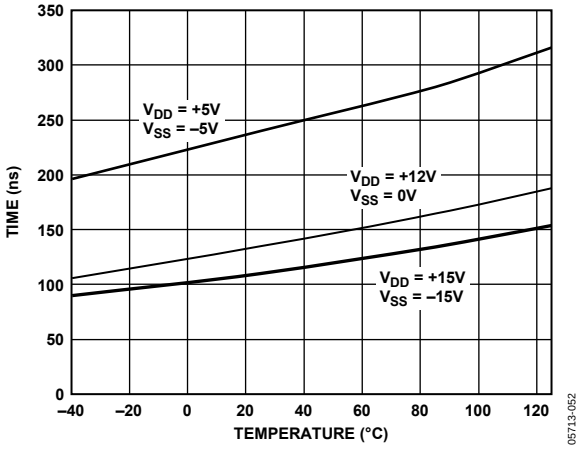


Figure 17. t_{ON}/t_{OFF} Times vs. Temperature

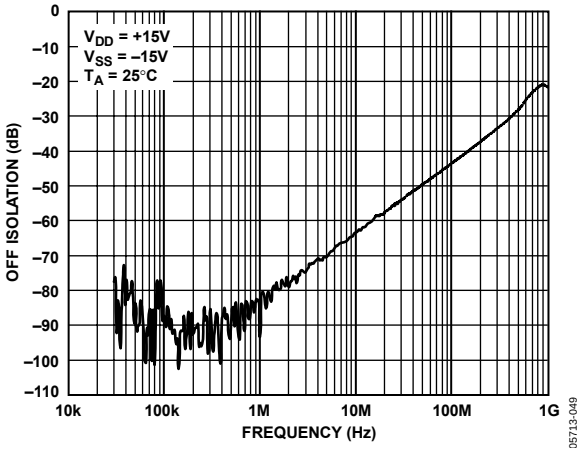


Figure 18. Off Isolation vs. Frequency

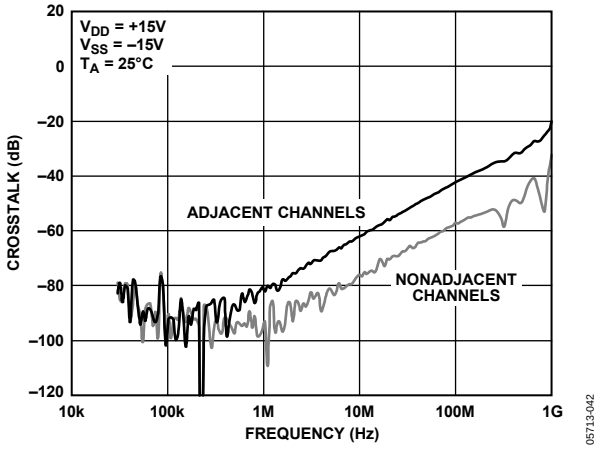


Figure 19. ADG1208 Crosstalk vs. Frequency

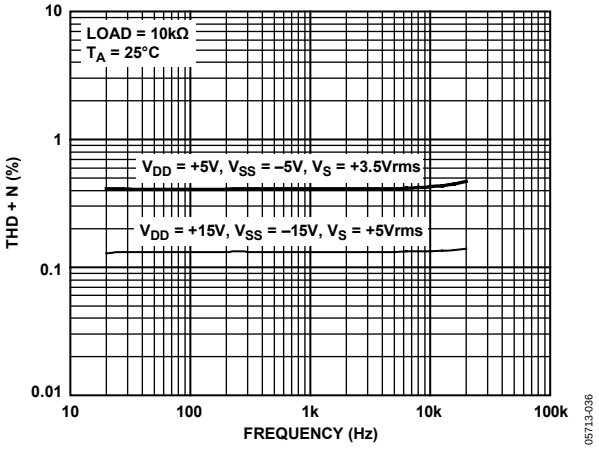


Figure 22. THD + N vs. Frequency

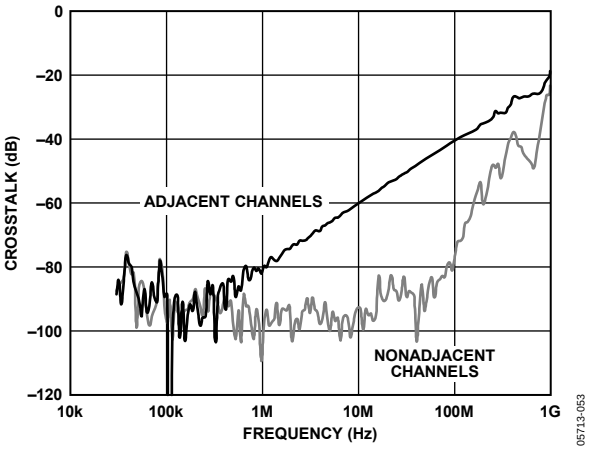


Figure 20. ADG1209 Crosstalk vs. Frequency

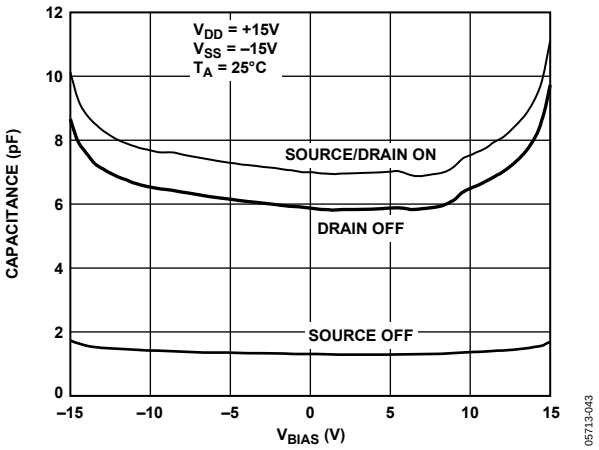


Figure 23. ADG1208 Capacitance vs. Source Voltage, ±15 V Dual Supply

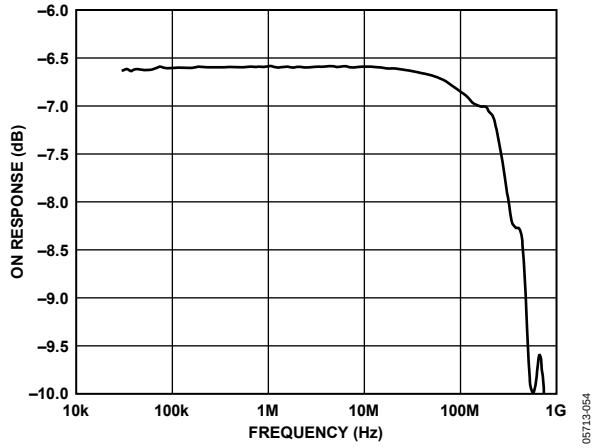


Figure 21. On Response vs. Frequency

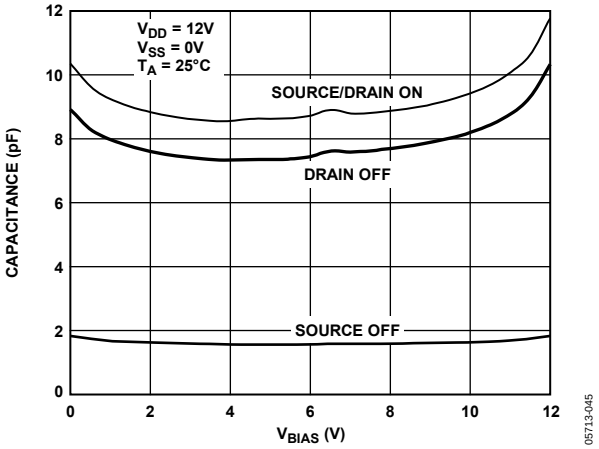


Figure 24. ADG1208 Capacitance vs. Source Voltage, 12 V Single Supply

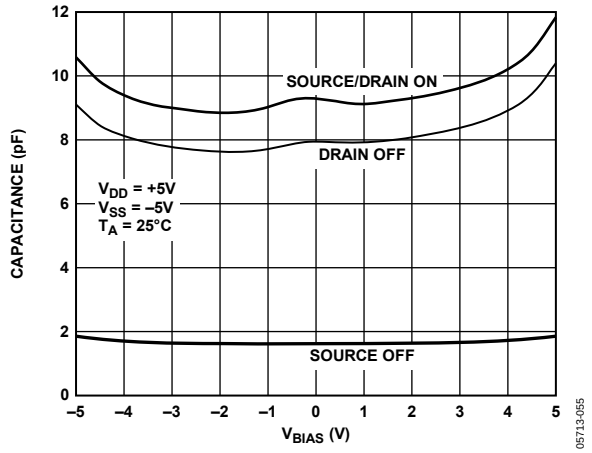


Figure 25. ADG1208 Capacitance vs. Source Voltage, ±5 V Dual Supply

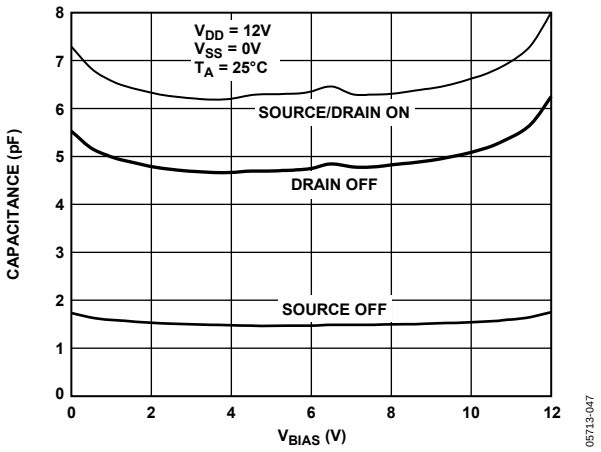


Figure 27. ADG1209 Capacitance vs. Source Voltage, 12 V Single Supply

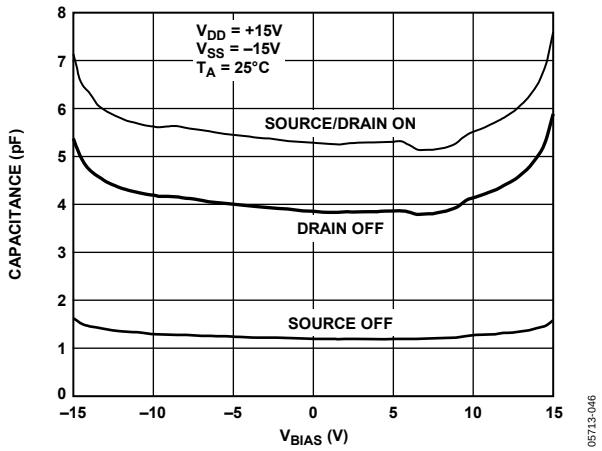


Figure 26. ADG1209 Capacitance vs. Source Voltage, ±15 V Dual Supply

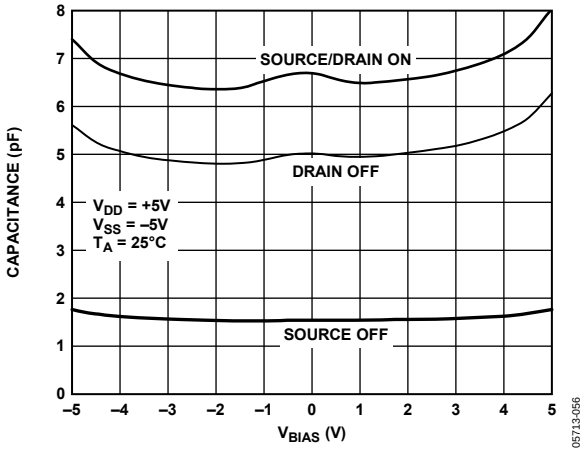


Figure 28. ADG1209 Capacitance vs. Source Voltage, ±5 V Dual Supply

TERMINOLOGY

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
Difference between the R_{ON} of any two channels.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on terminals D, S.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

T_{BBM}
Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TEST CIRCUITS

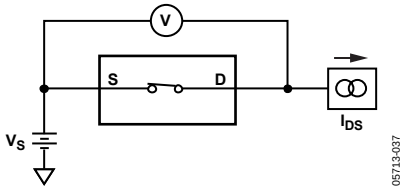


Figure 29. On Resistance

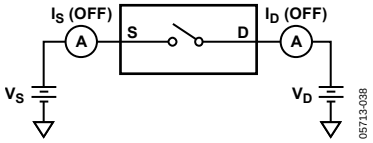


Figure 30. Off Leakage

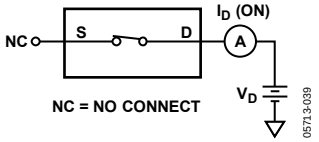


Figure 31. On Leakage

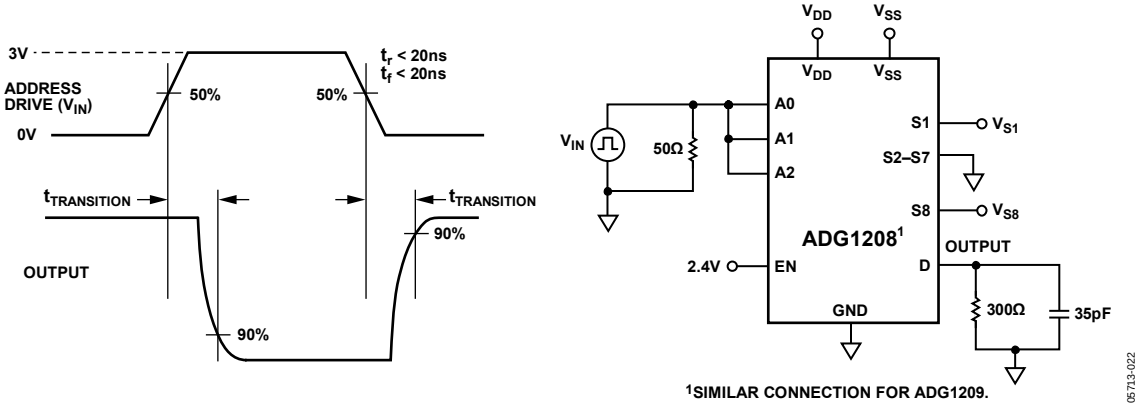


Figure 32. Address to Output Switching Times, $t_{TRANSITION}$

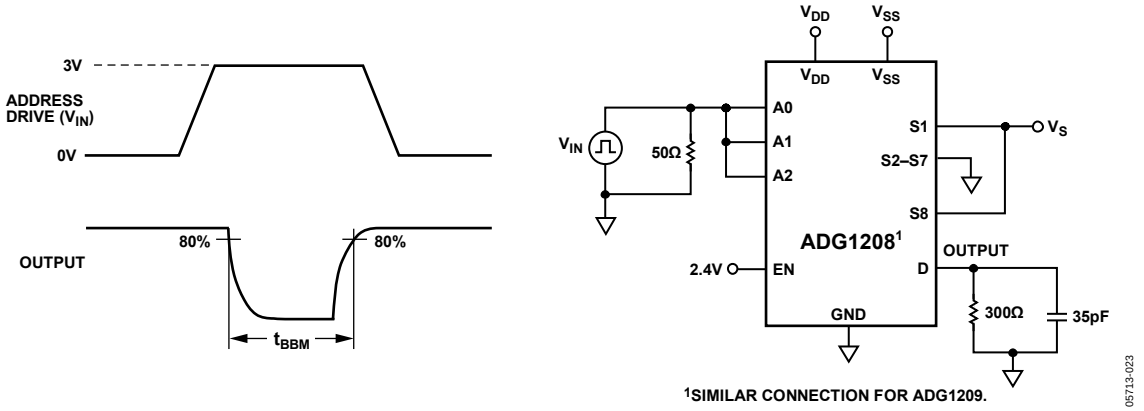


Figure 33. Break-Before-Make Delay, t_{BBM}

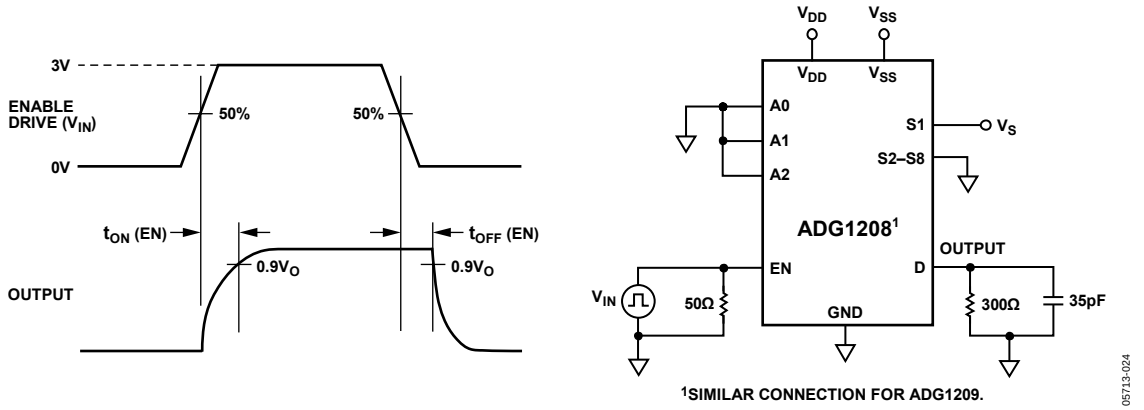


Figure 34. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

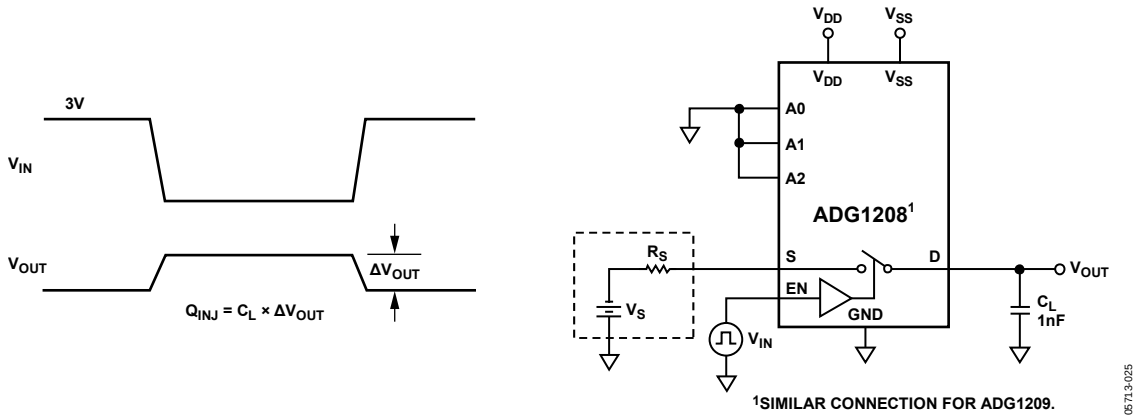


Figure 35. Charge Injection

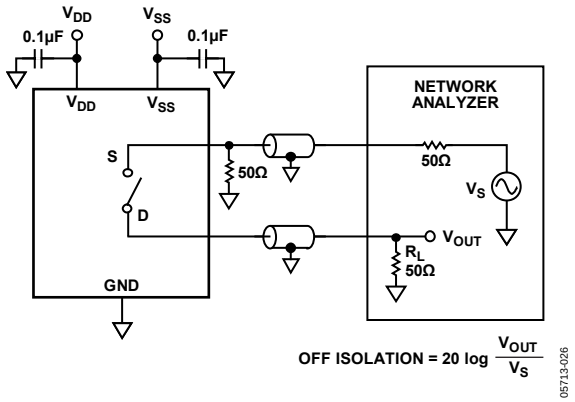


Figure 36. Off Isolation

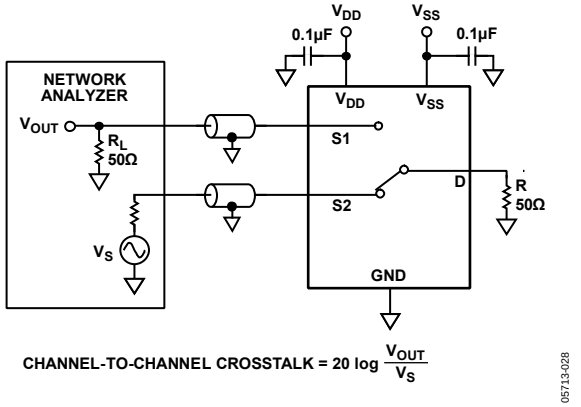


Figure 38. Channel-to-Channel Crosstalk

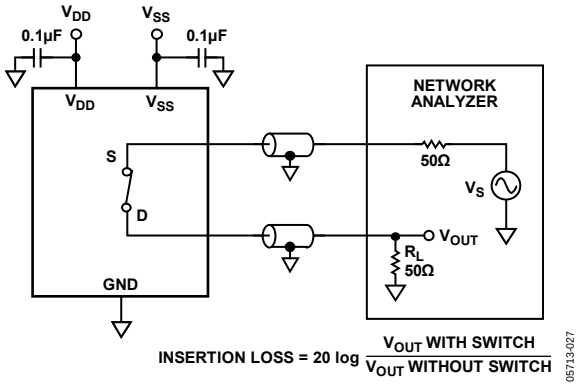


Figure 37. Bandwidth

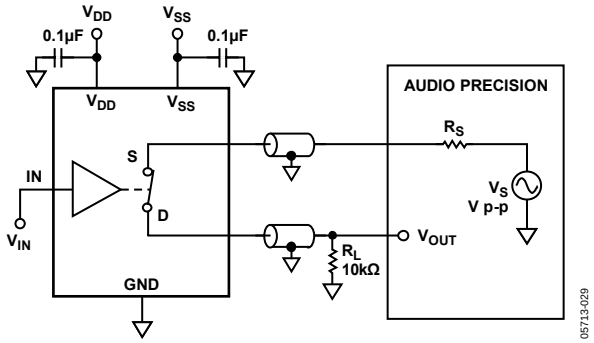
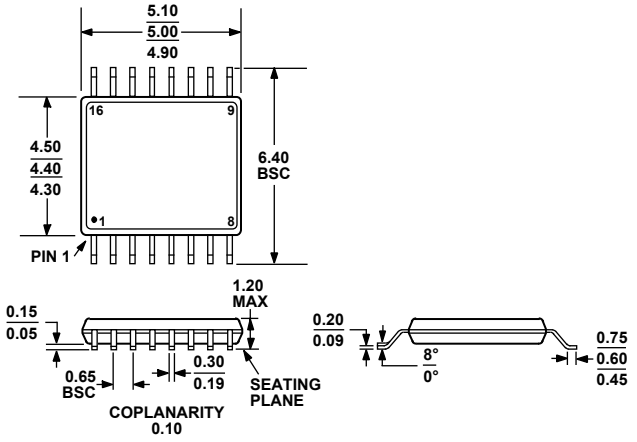


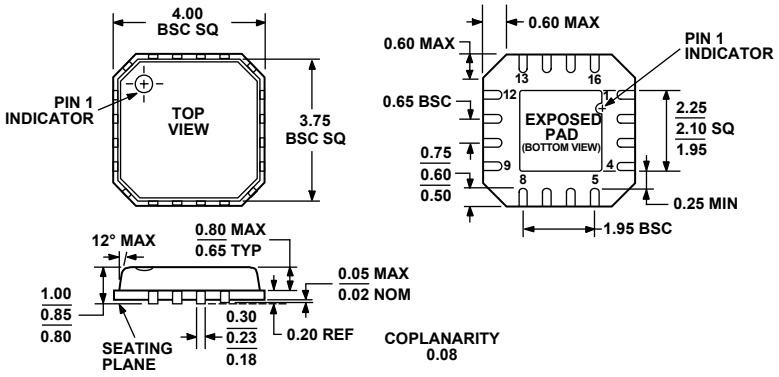
Figure 39. THD + Noise

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 40. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 41. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1208YRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1208YRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1208YCPZ-REEL[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADG1208YCPZ-REEL7[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADG1209YRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1209YRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1209YCPZ-REEL[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADG1209YCPZ-REEL7[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4

[1] Z = Pb-free part.

NOTES

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D05713-0-4/06(0)