Product Preview
8MB Double Data Rate HSTL I/O Fast SRAM

MCM64E918
MCM64E836

FC PACKAGE
FLIPPED CHIP PBGA
CASE 1107A–01

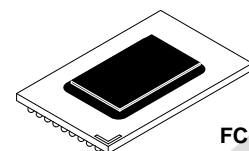**RS PACKAGE**
FLIPPED CHIP CBGA
CASE 1107B–01

The MCM64E918/MCM64E836 are 8M–bit pipelined burst synchronous late write fast static RAMs designed to provide very high data bandwidth in secondary cache applications. The MCM64E918 (organized as 512K words by 18 bits wide) and the MCM64E836 (organized as 256K words by 36 bits wide) are fabricated in Motorola's high performance silicon gate MOS technology.

The differential clock (CK) inputs control the timing of read/write operations of the RAM. At the rising edge of CK, all addresses and burst control inputs are registered. An internal buffer and special logic enables the memory to accept write data on the rising or rising and falling edges of the clock, a cycle following address and control signals. Read data is driven on the rising or rising and falling edges of the CK clock and is referenced to echo clock (CQ and $\overline{CQ}$) outputs.

The MCM64E918/MCM64E836 have HSTL inputs and outputs. The adjustable input trip–point (V_{ref}) and output power supply voltage (V_{DDQ}) gives the system designer greater flexibility in optimizing system performance.

The impedance of the output buffers is programmable, allowing the outputs to match the impedance of the circuit traces, which reduces signal reflections.

- Single 2.5 V ± 5% Power Supply
- Single Data Rate (SDR) and Double Data Rate (DDR) Burst Read and Write
- Pin Selectable Linear or Interleaved Burst Order
- Four Tick Burst with Automatic Wrap–Around
- Differential Clock Inputs
- Active High and Active Low Echo Clock Outputs
- 1.8 V Expanded HSTL — I/O (JEDEC Standard JESD8–6 Class I Compatible)
- 1.8 V Expanded HSTL — Compatible Programmable Impedance Output Drivers
- Pipelined (Register to Register) Synchronous Operation
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Stop Clock Functionality Supported
- Optional x18 or x36 Organization
- MCM64E918/MCM64E836–3.0 = 3.0 ns Clock Cycle Time
  MCM64E918/MCM64E836–3.3 = 3.3 ns Clock Cycle Time
  MCM64E918/MCM64E836–4.0 = 4.0 ns Clock Cycle Time
  MCM64E918/MCM64E836–4.4 = 4.4 ns Clock Cycle Time
  MCM64E918/MCM64E836–5.0 = 5.0 ns Clock Cycle Time
- 9 x 17 (153) Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Flipped Chip Plastic Ball Grid Array (PBGA) or Flipped Chip Ceramic Ball Grid Array (CBGA) Packages
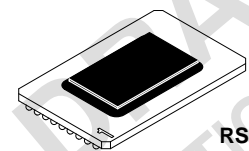
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MOTOROLA

PIN ASSIGNMENTS

MCM64E918
TOP VIEW 153–BUMP

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA	SA	ZQ	SA	SA	V_{DDQ}	V_{SS}
B	NC	DQ	SA	V_{SS}	B1	V_{SS}	SA	NC	DQ
C	V_{SS}	V_{DDQ}	SA	SA	$\overline{G}$	SA	SA	V_{DDQ}	V_{SS}
D	DQ	NC	NC	V_{SS}	V_{DD}	V_{SS}	SA	DQ	NC
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{ref}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	NC	CQ	NC	V_{DD}	V_{DD}	V_{DD}	DQ	NC	DQ
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	CK	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ	NC	DQ	V_{DD}	$\overline{CK}$	V_{DD}	NC	DQ	NC
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	NC	DQ	NC	V_{SS}	B2	V_{SS}	DQ	NC	DQ
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B3	NC	V_{SS}	V_{DDQ}	V_{SS}
M	DQ	NC	DQ	V_{DD}	V_{DD}	V_{DD}	NC	$\overline{CQ}$	NC
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{ref}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	NC	DQ	SA	V_{SS}	V_{DD}	V_{SS}	SA	NC	DQ
R	V_{SS}	V_{DDQ}	V_{DD}	SA	SA1	SA	V_{DD}	V_{DDQ}	V_{SS}
T	DQ	NC	SA	V_{SS}	SA0	V_{SS}	SA	DQ	NC
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK*	TDO	NC	V_{DDQ}	V_{SS}

MCM64E836
TOP VIEW 153–BUMP

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA	SA	ZQ	SA	SA	V_{DDQ}	V_{SS}
B	DQ	DQ	SA	V_{SS}	B1	V_{SS}	SA	DQ	DQ
C	V_{SS}	V_{DDQ}	SA	SA	$\overline{G}$	SA	SA	V_{DDQ}	V_{SS}
D	DQ	DQ	NC	V_{SS}	V_{DD}	V_{SS}	SA	DQ	DQ
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{ref}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	DQ	CQ	DQ	V_{DD}	V_{DD}	V_{DD}	DQ	CQ	DQ
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	CK	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ	DQ	DQ	V_{DD}	$\overline{CK}$	V_{DD}	DQ	DQ	DQ
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	DQ	DQ	DQ	V_{SS}	B2	V_{SS}	DQ	DQ	DQ
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B3	NC	V_{SS}	V_{DDQ}	V_{SS}
M	DQ	$\overline{CQ}$	DQ	V_{DD}	V_{DD}	V_{DD}	DQ	$\overline{CQ}$	DQ
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{ref}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	DQ	DQ	NC	V_{SS}	V_{DD}	V_{SS}	SA	DQ	DQ
R	V_{SS}	V_{DDQ}	V_{DD}	SA	SA1	SA	V_{DD}	V_{DDQ}	V_{SS}
T	DQ	DQ	SA	V_{SS}	SA0	V_{SS}	SA	DQ	DQ
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK*	TDO	NC	V_{DDQ}	V_{SS}

* If JTAG is not used, TCK pin must be tied to V_{DD} or V_{SS}.

MCM64E918 x18 PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
5B	B1	Input	Synchronous Function Control Input: B1 = 0 initiates a load new address.
5K	B2	Input	Synchronous Function Control Input: B2 = 0 initiates a WRITE, B2 = 1 initiates a READ.
5L	B3	Input	Synchronous Function Control Input: B3 = 0 initiates a double (or burst) operation, B3 = 1 initiates a single operation.
5G	CK	Input	Address, data in, and control input register clock. Active high.
5H	$\overline{CK}$	Input	Address, data in, and control input register clock. Active low.
2F	CQ	Output	Echo Clock Output: Active high.
8M	$\overline{CQ}$	Output	Echo Clock Output: Active low.
2B, 9B, 1D, 8D, 7F, 9F, 1H, 3H, 8H, 2K, 7K, 9K, 1M, 3M, 2P, 9P, 1T, 8T	DQ	I/O	Synchronous data I/O.
5C	$\overline{G}$	Input	Output Enable functionality not supported. Must be tied to V_{SS} or driven to $\leq V_{IL}$ Max.
4L	$\overline{LBO}$	Input	Linear Burst Order: This is a mode pin. It must be tied to V_{DD} or V_{SS} before power up. $\overline{LBO}$ = 1 selects interleaved mode. $\overline{LBO}$ = 0 selects linear mode.
3A, 4A, 6A, 7A, 3B, 7B, 3C, 4C, 6C, 7C, 7D, 3P, 7P, 4R, 6R, 3T, 7T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5R, 5T	SA1, SA0	Input	Synchronous burst counter preload address inputs: SA0 = LSB.
5U	TCK	Input	JTAG pin, test clock. If JTAG is not used, TCK must be tied to V_{SS} or V_{DD}.
4U	TDI	Input	JTAG pin, Test Data In.
6U	TDO	Output	JTAG, Test Data Out.
3U	TMS	Input	JTAG pin.
5A	ZQ	Input	Output impedance programming input.
5E, 5N	V_{ref}	Supply	Input Reference: Provides reference voltage for input buffers.
5D, 4E, 6E, 4F, 5F, 6F, 4H, 6H, 4J, 5J, 6J, 4M, 5M, 6M, 4N, 6N, 5P, 3R, 7R	V_{DD}	Supply	Core Power Supply: These pins act as thermal vias to PCB power plane.
2A, 8A, 2C, 8C, 2E, 8E, 2G, 8G, 2J, 8J, 2L, 8L, 2N, 8N, 2R, 8R, 2U, 8U	V_{DDQ}	Supply	Output Power Supply: Provides operating power for output buffers.
1A, 9A, 4B, 6B, 1C, 9C, 4D, 6D, 1E, 3E, 7E, 9E, 1G, 3G, 4G, 6G, 7G, 9G, 1J, 3J, 7J, 9J, 4K, 6K, 1L, 3L, 7L, 9L, 1N, 3N, 7N, 9N, 4P, 6P, 1R, 9R, 4T, 6T, 1U, 9U	V_{SS}	Supply	Ground: These pins act as thermal vias to PCB ground plane.
1B, 8B, 2D, 3D, 9D, 1F, 3F, 8F, 2H, 7H, 9H, 1K, 3K, 8K, 6L, 2M, 7M, 9M, 1P, 8P, 2T, 9T, 7U	NC	—	No Connection: This means there is no connection to the chip.

MCM64E836 x36 PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
5B	B1	Input	Synchronous Function Control Input: B1 = 0 initiates a load new address.
5K	B2	Input	Synchronous Function Control Input: B2 = 0 initiates a WRITE, B2 = 1 initiates a READ.
5L	B3	Input	Synchronous Function Control Input: B3 = 0 initiates a double (or burst) operation, B3 = 1 initiates a single operation.
5G	CK	Input	Address, data in, and control input register clock. Active high.
5H	$\overline{CK}$	Input	Address, data in, and control input register clock. Active low.
2F, 8F	CQ	Output	Echo Clock Output: Active high.
2M, 8M	$\overline{CQ}$	Output	Echo Clock Output: Active low.
1B, 2B, 8B, 9B, 1D, 2D, 8D, 9D, 1F, 3F, 7F, 9F, 1H, 2H, 3H, 7H, 8H, 9H, 1K, 2K, 3K, 7K, 8K, 9K, 1M, 3M, 7M, 9M, 1P, 2P, 8P, 9P, 1T, 2T, 8T, 9T	DQ	I/O	Synchronous data I/O.
5C	$\overline{G}$	Input	Output Enable functionality not supported. Must be tied to V_{SS} or driven to $\leq V_{IL}$ Max.
4L	$\overline{LBO}$	Input	Linear Burst Order: This is a mode pin. It must be tied to V_{DD} or V_{SS} before power up. $\overline{LBO}$ = 1 selects interleaved mode. $\overline{LBO}$ = 0 selects linear mode.
3A, 4A, 6A, 7A, 3B, 7B, 3C, 4C, 6C, 7C, 7D, 7P, 4R, 6R, 3T, 7T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge.
5R, 5T	SA1, SA0	Input	Synchronous burst counter preload address inputs: SA0 = LSB.
5U	TCK	Input	JTAG pin, test clock. If JTAG is not used, TCK must be tied to V_{SS} or V_{DD}.
4U	TDI	Input	JTAG pin, Test Data In.
6U	TDO	Output	JTAG, Test Data Out.
3U	TMS	Input	JTAG pin.
5A	ZQ	Input	Output impedance programming input.
5E, 5N	V_{ref}	Supply	Input Reference: Provides reference voltage for input buffers.
5D, 4E, 6E, 4F, 5F, 6F, 4H, 6H, 4J, 5J, 6J, 4M, 5M, 6M, 4N, 6N, 5P, 3R, 7R	V_{DD}	Supply	Core Power Supply: These pins act as thermal vias to PCB power plane.
2A, 8A, 2C, 8C, 2E, 8E, 2G, 8G, 2J, 8J, 2L, 8L, 2N, 8N, 2R, 8R, 2U, 8U	V_{DDQ}	Supply	Output Power Supply: Provides operating power for output buffers.
1A, 9A, 4B, 6B, 1C, 9C, 4D, 6D, 1E, 3E, 7E, 9E, 1G, 3G, 4G, 6G, 7G, 9G, 1J, 3J, 7J, 9J, 4K, 6K, 1L, 3L, 7L, 9L, 1N, 3N, 7N, 9N, 4P, 6P, 1R, 9R, 4T, 6T, 1U, 9U	V_{SS}	Supply	Ground: These pins act as thermal vias to PCB ground plane.
3D, 6L, 3P, 7U	NC	—	No Connection: This means there is no connection to the chip.

BUS CYCLE STATE DIAGRAM
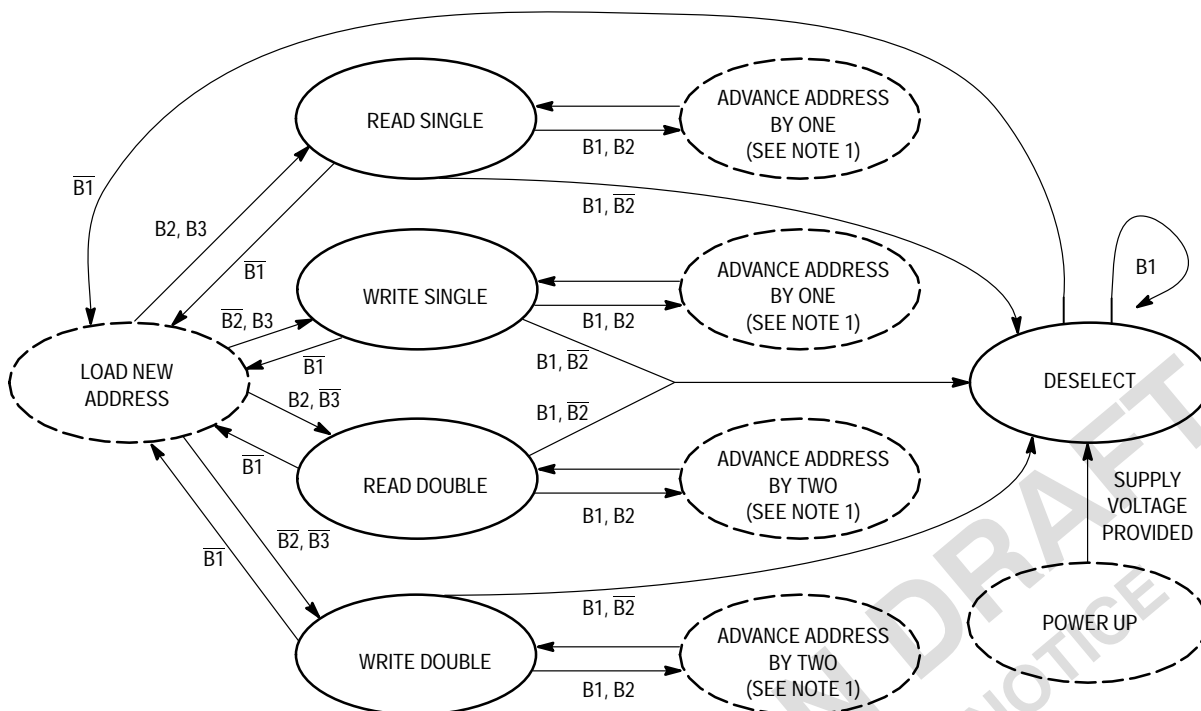
NOTE:
    1. Advance internal address in accordance with burst order with wrap–around. Burst–length of four.

THREE–WIRE SYNCHRONOUS FUNCTION CONTROLS (See Notes 1 through 4)

B1	B2	B3	Function Launched at Next Clock	D	Q (n)	Q (n + 1)
0	0	1	Write Single, Load New Address	Next Edge	High–Z	High–Z
0	0	0	Write Double, Load New Address	Both Edges	High–Z	High–Z
0	1	1	Read Single, Load New Address	High–Z	Next CQ + Edge	Next CQ + Edge
0	1	0	Read Double, Load New Address	High–Z	Both CQ Edges	Both CQ Edges
1	1	X	Increment Address, Continue Previous Function	X	X	X
1	0	X	Deselect, Pipeline High–Z	X	X	High–Z

NOTES:
    1. X = don't care.
    2. Deselect usage is discussed in the Functional Description section.
    3. Outputs will be in high–Z during power up, except CQ and $\overline{CQ}$.
    4. Double reads and writes occur per burst sequence.

BURST SEQUENCES

Interleaved Burst					Binary							
Address	Hex				SA1	SA0	SA1	SA0	SA1	SA0	SA1	SA0
Start — Base Address	0	1	2	3	0	0	0	1	1	0	1	1
2nd Address	1	0	3	2	0	1	0	0	1	1	1	0
3rd Address	2	3	0	1	1	0	1	1	0	0	0	1
4th Address	3	2	1	0	1	1	1	0	0	1	0	0

Linear Burst					Binary							
Address	Hex				SA1	SA0	SA1	SA0	SA1	SA0	SA1	SA0
Start — Base Address	0	1	2	3	0	0	0	1	1	0	1	1
2nd Address	1	2	3	0	0	1	1	0	1	1	0	0
3rd Address	2	3	0	1	1	0	1	1	0	0	0	1
4th Address	3	0	1	2	1	1	0	0	0	1	1	0

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{DD}	−0.5 to 3.6	V
Output Supply Voltage	V_{DDQ}	−0.5 to 2.5	V
Voltage On Any Pin Other Than JTAG	V_{in}	−0.5 to 2.5	V
Voltage On Any JTAG Pin	V_{JTAG}	−0.5 to 3.0	V
Input Current (per I/O)	I_{in}	±50	mA
Output Current (per I/O)	I_{out}	±25	mA
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

PBGA PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (Still Air)		$R_{\theta JA}$	50	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Single–Layer Board	$R_{\theta JA}$	39	°C/W	1, 2
Junction to Ambient (@200 ft/min)	Four–Layer Board	$R_{\theta JA}$	27	°C/W	3
Junction to Board (Bottom)		$R_{\theta JB}$	23	°C/W	4
Junction to Case (Top)		$R_{\theta JC}$	1	°C/W	5

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Measured using a four–layer test board with two internal planes.
4. Indicates the average thermal resistance between the die and the printed circuit board as measured by the ring cold plate method.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

$(2.375\ V \le V_{DD} \le 2.625\ V,\ 0°C \le T_A \le 70°C,\ \text{Unless Otherwise Noted})$

RECOMMENDED OPERATING CONDITIONS (See Notes 1 through 4)

Parameter	Symbol	Min	Max –3.0	Max –3.3	Max –4.0	Max –4.4	Max –5.0	Max	Unit	Notes
Core Power Supply Voltage	V_{DD}	2.375	—	—	—	—	—	2.625	V	
Output Driver Supply Voltage	V_{DDQ}	1.4	—	—	—	—	—	1.9	V	
AC Supply Current (Device Selected, All Outputs Open, Freq = Max, V_{DD} = Max, V_{DDQ} = Max). Includes Supply Currents for V_{DD}.	I_{DD1}	— —	720	700	680	660	640	—	mA	5
Quiescent Active Power Supply Current (Device Selected, All Outputs Open, Freq = 0, V_{DD} = Max, V_{DDQ} = Max). Includes supply currents for V_{DD}.	I_{DD2}	—	200	200	200	200	200	—	mA	6
Active Standby Power Supply Current (Device Deselected, Freq = Max, V_{DD} = Max, V_{DDQ} = Max)	I_{SB1}	—	225	220	210	205	200	—	mA	7
Stop Clock Current (Device Deselected, Freq = 0, V_{DD} = Max, V_{DDQ} = Max, All Inputs Static at CMOS Levels)	I_{SB2}	—	200	200	200	200	200	—	mA	6, 7
Input Reference DC Voltage	V_{ref} (dc)	0.6	—	—	—	—	—	1.3	V	8

NOTES:
1. All data sheet parameters specified to full range of V_{DD} unless otherwise noted. All voltages are referenced to voltage applied to V_{SS} bumps.
2. Supply voltage applied to V_{DD} connections.
3. Supply voltage applied to V_{DDQ} connections.
4. All power supply currents measured with outputs open or deselected.
5. All inputs are toggling per CMOS I/O levels (see Note 6).
6. Input levels for I/Os are $V_{SS} \le V_{in} \le 0.2\ V$ or $V_{DDQ} - 0.2\ V \le V_{in} \le V_{DDQ}$.
7. Device deselected as defined by the Truth Table.
8. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak to peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.

DC CHARACTERISTICS AND POWER SUPPLY CURRENTS (See Notes 1 and 2)

Parameter	Symbol	Min	Typ	Max	Unit
DC Input Logic High	V_{IH} (DC)	$V_{ref} + 0.1$	—	$V_{DDQ} + 0.3$	V
DC Input Logic Low	V_{IL} (DC)	-0.5	—	$V_{ref} - 0.1$	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DDQ})	$I_{lkg(I)}$	—	—	±5	µA
Output Low Current ($V_{OL} = V_{DDQ}/2$)	I_{OL}	$(V_{DDQ}/2) / [(RQ/5) + 10\%]$	—	$(V_{DDQ}/2) / [(RQ/5) - 10\%]$	V
Output High Current ($V_{OH} = V_{DDQ}/2$)	I_{OH}	$(V_{DDQ}/2) / [(RQ/5) + 10\%]$	—	$(V_{DDQ}/2) / [(RQ/5) - 10\%]$	V
Light Load Output Logic Low $I_{OL} \leq 100$ µA	V_{OL1}	V_{SS}	—	0.2	V
Light Load Output Logic High $|I_{OH}| \leq 100$ µA	V_{OH1}	$V_{DDQ} - 0.2$	—	V_{DDQ}	V
Clock Input Signal Voltage	V_{in}	-0.3	—	$V_{DDQ} + 0.3$	V
Clock Input Differential Voltage (See Figure 2)	V_{DIF} (DC)	0.1	—	$V_{DDQ} + 0.6$	V
Clock Input Common Mode Voltage Range (See Figure 2)	V_{CM} (DC)	0.6	—	1.3	V

NOTES:
1. The impedance controlled mode is expected to be used in point–to–point applications, driving high–impedance inputs.
2. The ZQ pin is connected through RQ to V_{SS} for the controlled impedance mode.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $0°C \leq T_A \leq 70°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs	C_{in}	3.2	5	pF
	$\overline{G}$ and $\overline{W}$	C_{ck}	3.7	5	
I/O Capacitance	DQ	$C_{I/O}$	3.8	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(2.375 V ≤ V_{DD} ≤ 2.625 V, 1.4 V ≤ V_{DDQ} ≤ 1.9 V, Unless Otherwise Noted)

Input Pulse Levels . . . . 0.25 V to 1.25 V
Input Rise/Fall Time . . . . 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level . . . . V_{DDQ}/2

Output Timing Measurement Reference Level . . . . V_{DDQ}/2
Output Load . . . . Differential Cross–Point
$R_{\theta JA}$ Device . . . . TBD

READ AND WRITE CYCLE TIMING

Parameter	Symbol	64E918–3.0 64E836–3.0 Min	Max	64E918–3.3 64E836–3.3 Min	Max	64E918–4.0 64E836–4.0 Min	Max	64E918–4.4 64E836–4.4 Min	Max	64E918–5.0 64E836–5.0 Min	Max	Unit	Notes
Cycle Time	t_{KHKH}	3	—	3.3	—	4	—	4.4	—	5	—	ns	
CK Clock High Pulse Width	t_{KHKL}	1.2	—	1.3	—	1.6	—	1.8	—	2	—	ns	
CK Clock Low Pulse Width	t_{KLKH}	1.2	—	1.3	—	1.6	—	1.8	—	2	—	ns	
CQ Low to CQ High	t_{CLCH}	t_{KLKH} – 100 ps	t_{KLKH} + 100 ps	t_{KLKH} – 100 ps	t_{KLKH} + 100 ps	t_{KLKH} – 100 ps	t_{KLKH} + 100 ps	t_{KLKH} – 100 ps	t_{KLKH} + 100 ps	t_{KLKH} – 100 ps	t_{KLKH} + 100 ps		
CQ High to CQ Low	t_{CHCL}	t_{KHKL} – 100 ps	t_{KHKL} + 100 ps	t_{KHKL} – 100 ps	t_{KHKL} + 100 ps	t_{KHKL} – 100 ps	t_{KHKL} + 100 ps	t_{KHKL} – 100 ps	t_{KHKL} + 100 ps	t_{KHKL} – 100 ps	t_{KHKL} + 100 ps		
Setup Times: Address Valid to CK Crossing	t_{AVKH}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Burst Control Valid to CK Crossing	t_{BVKH}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—		
Data In Valid to CK Crossing	t_{DVKX}	0.3	—	0.3	—	0.3	—	0.3	—	0.3	—		1
Hold Times: CK Crossing to Address Don't Care	t_{KHAX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
CK Crossing to Burst Control Don't Care	t_{KHBX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—		
CK Crossing to Data In Don't Care	t_{KXDX}	0.3	—	0.3	—	0.3	—	0.3	—	0.3	—		1
CK Crossing to CQ High	t_{KXCH}	0.7	1.5	0.7	1.65	0.7	2	0.7	2.2	0.7	2.5	ns	
CK Crossing to CQ Low	t_{KXCL}	0.7	1.5	0.7	1.65	0.7	2	0.7	2.2	0.7	2.5	ns	
CQ High to Output Valid	t_{CHQV}	—	0.20	—	0.20	—	0.20	—	0.20	—	0.20	ns	1
CQ Low to Output Valid	t_{CLQV}	—	0.20	—	0.20	—	0.20	—	0.20	—	0.20	ns	1
CQ High to Output Hold	t_{CHQX}	– 0.20	—	– 0.20	—	– 0.20	—	– 0.20	—	– 0.20	—	ns	1, 2
CQ Low to Output Hold	t_{CLQX}	– 0.20	—	– 0.20	—	– 0.20	—	– 0.20	—	– 0.20	—	ns	1, 2
CK High to Output Low–Z	t_{KHQX1}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	2, 3
CQ High to Output High–Z	t_{CHQZ}	– 0.20	0.25	– 0.20	0.3	– 0.20	0.35	– 0.20	0.35	– 0.20	0.35	ns	2, 4

NOTES:
1. Guaranteed by design and characterization.
2. This parameter sampled and not 100% tested.
3. Measured at ± 200 mV from steady state.
4. Measured at ± 200 mV from steady state. See Figure 1b.
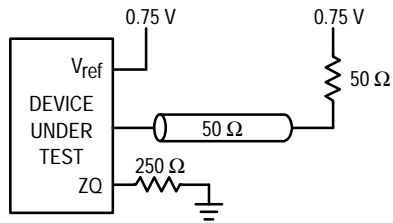
(a) Test Load
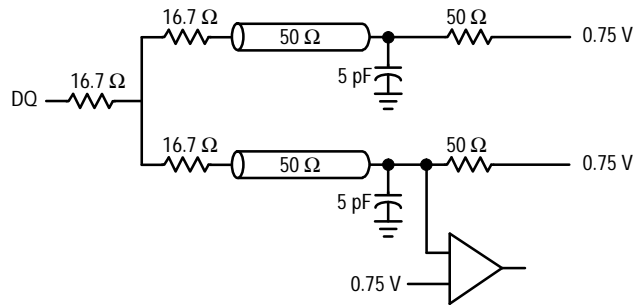
(b) Test Load

Figure 1. Test Loads

AC INPUT CHARACTERISTICS (See Notes 1 through 3)

Parameter	Symbol	Min	Max	Notes
AC Input Logic High (See Figure 2)	V_{IH} (ac)	V_{ref} + 200 mV	—	
AC Input Logic Low (See Figure 3)	V_{IL} (ac)	—	V_{ref} – 200 mV	
Input Reference Peak–to–Peak AC Voltage	V_{ref} (ac)	—	5% V_{ref} (dc)	4
Clock Input Differential Voltage	V_{dif} (ac)	400 mV	V_{DDQ} + 600 mV	

NOTES:
1. Inputs may undershoot to V_{SS} – 1 V (peak) for up to 35% t_{KHKH} or 1.0 ns, whichever is smaller, and V_{SS} – 1.5 V instantaneous peak undershoot.
2. Inputs may overshoot to 3.3 V for up to 35% t_{KHKH} or 1.0 ns, whichever is smaller, and 3.6 V instantaneous peak overshoot.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Although considerable latitude in the selection of the nominal dc value (i.e., rms value) of V_{ref} is supported, the peak–to–peak ac component superimposed on V_{ref} may not exceed 5% of the dc component of V_{ref}.
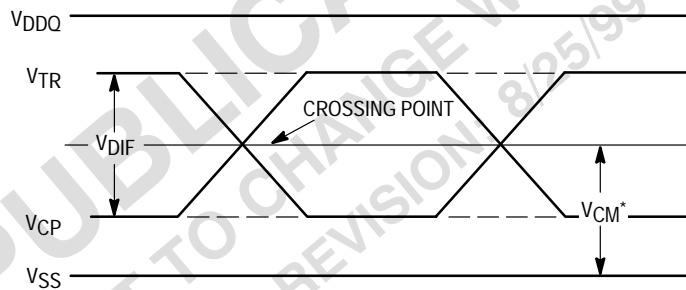
* V_{CM}, the Common Mode Input Voltage, equals $V_{TR} - [(V_{TR} - V_{CP})/2]$.

Figure 2. Differential Inputs/Common Mode Input Voltage

V_{IH}

V_{SS}

$- 0.5\ V$

$35\%\ t_{KHKH}$
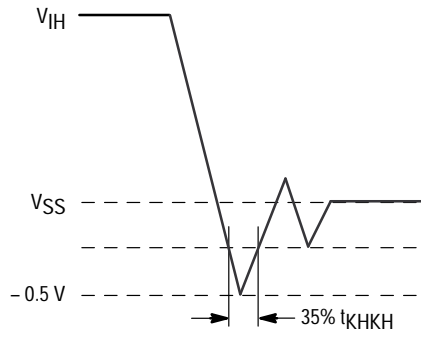
Figure 3. Undershoot Voltage

$V_{IH(ac)}$

V_{ref}

$V_{IL(ac)}$
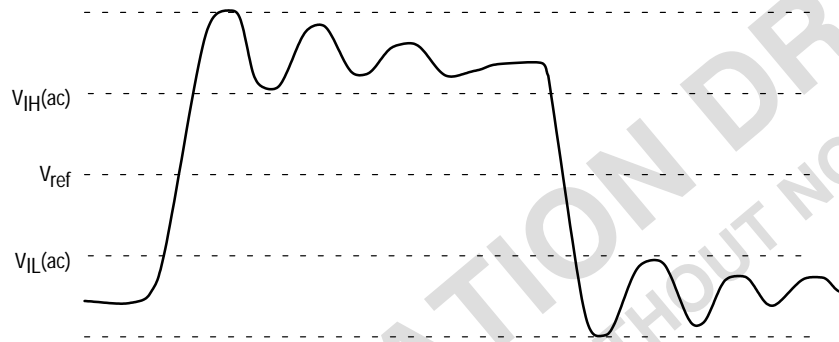
Figure 4. Differential Inputs/Common Mode Input Voltage

FUNCTIONAL DESCRIPTION

USING DESELECT

Function control pins B1:B2 set to 1:0 will be latched on a rising edge of the input clock (CK), and launch a deselect at the next CK clock (pipelined). Deselect puts the data bus into a high–impedance state. Deselect can be used to avoid bus contention by putting the data bus into a high–impedance state before performing a write. The sequence for switching from a read to a write should be: READ, DESELECT, WRITE.

COHERENCY

This part is fully coherent. This means that when a write is performed at an address, and a read of that same address follows immediately, the data just written is read back.

BURSTING

Function control pins are used to select single or double reads and writes. When a double read or write is selected, the data is managed on both the rising and falling edges of the echo clock, which is the double data rate feature of this FSRAM. All burst sequences are determined with the $\overline{LBO}$ pin per the Burst Sequence table.

Function control pins B1:B2 set to 1:1 increments the address and continues the previous function. This combination of B1:B2 can immediately follow any of the other read or write functions. As long as the B1:B2 pins are set to 1:1 on rising edges of the input clock, a continuous read or write from sequential addresses can be performed without having to resupply the address (refer to the Bus Cycle State diagram and Three–Wire Synchronous Function Control table).

READS/WRITES

The DDR latches address and control lines on the rising edge of the input (CK) clock.

Single reads are selected by setting function control lines B1:B2:B3 = 0:1:1. This functionality resembles the non–burst read timing of a pipelined BurstRAM (pre–DDR). Only 1 byte of data will result from each address and control clocked into the part. Data changes only on the rising edge of the clock.

Double reads are selected by setting B1:B2:B3 = 0:1:0. This will cause a burst of two, but at twice the input clock rate. Data is available after the rising and the falling clock edges of the output clock (refer to the Double and Single Read Timing diagram).

Single writes have late write functionality. Single writes are selected with B1:B2:B3 = 0:0:1. Data In must meet setup and hold times with respect to the rising edge of the input clock, CK.

Double writes are also late writes. Double writes are selected with B1:B2:B3 = 0:0:0. The data rate is twice the applied clock in a double write, so Data In must meet setup and hold times with respect to the rising and falling edges of the input clock, CK.

ECHO CLOCK

This part is equipped with an echo clock. The echo clock is an output clock that aids in the synchronization of data. After power up, the echo clock is free running. The data that is output during a read cycle is referenced to the echo clock outputs.

STARTUP CONDITIONS/STOP CLOCK

Power up conditions are expected to vary from application to application. Echo clocks (CQ and $\overline{CQ}$) are not pipelined, and will respond to the input clock (CK) immediately. One way to design for this situation is to power up and start the DDR, run until all signals are transitioning smoothly, and then stop the clock and start it again, using the echo clock edges after the stop clock and not before the stop clock. This will allow for synchronization of the echo clock. The stop clock can be used anywhere as long as the minimum and maximum clock pulse specifications are not violated.
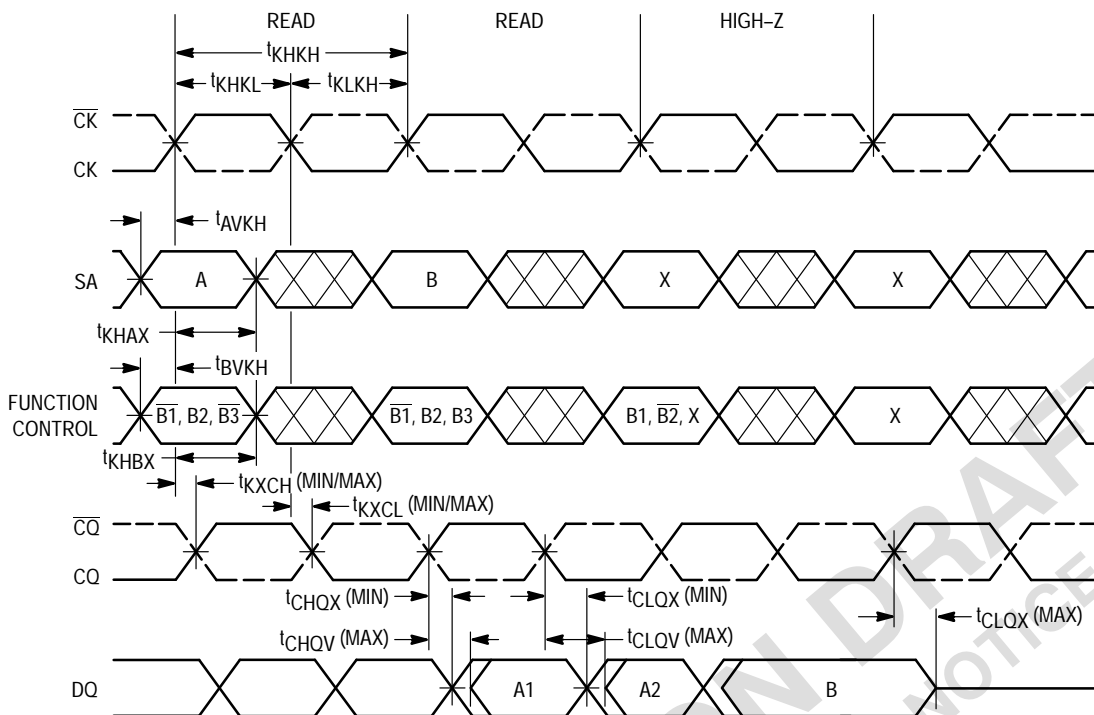
OUTPUT IMPEDANCE CIRCUITRY

The designer can program the RAMs output buffer impedance by terminating the $\overline{ZQ}$ pin to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. For example, a 250 Ω resistor will give an output impedance of 50 Ω.

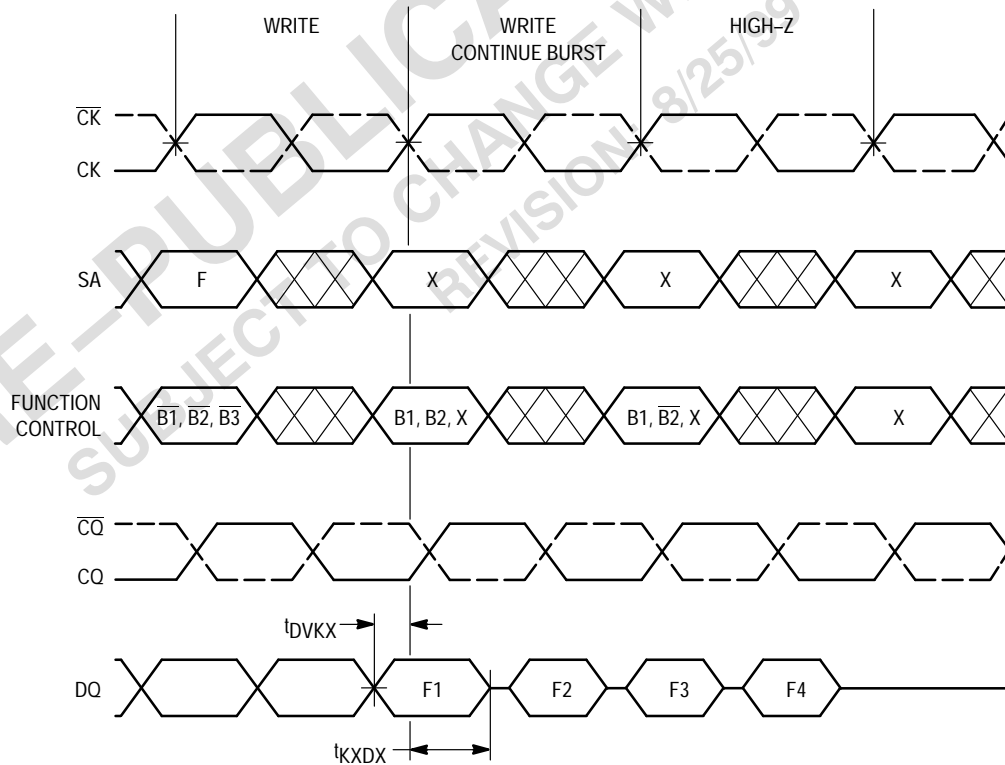Impedance updates occur during write and deselect cycles.

The actual change in the impedance occurs in small increments and is binary. The binary impedance has 256 values and therefore, there are no significant disturbances that occur on the output because of this smooth update method.

At power up, the output impedance will take up to 65,000 cycles for the impedance to be completely updated.
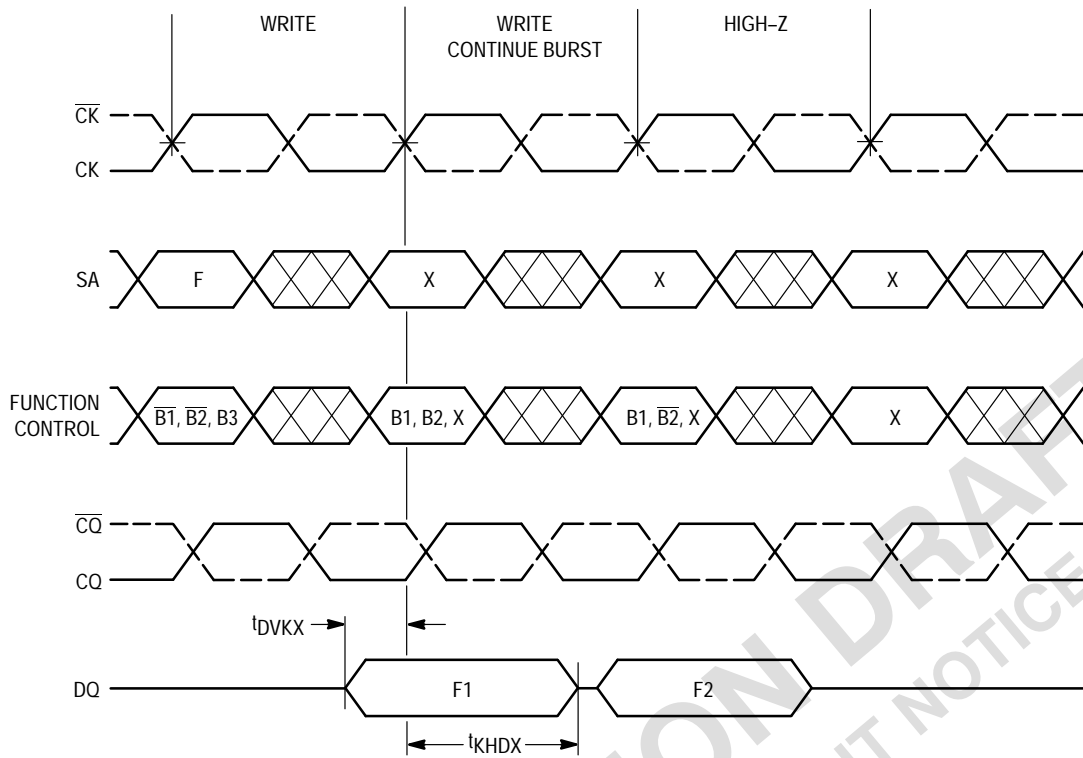

DOUBLE AND SINGLE READ TIMING
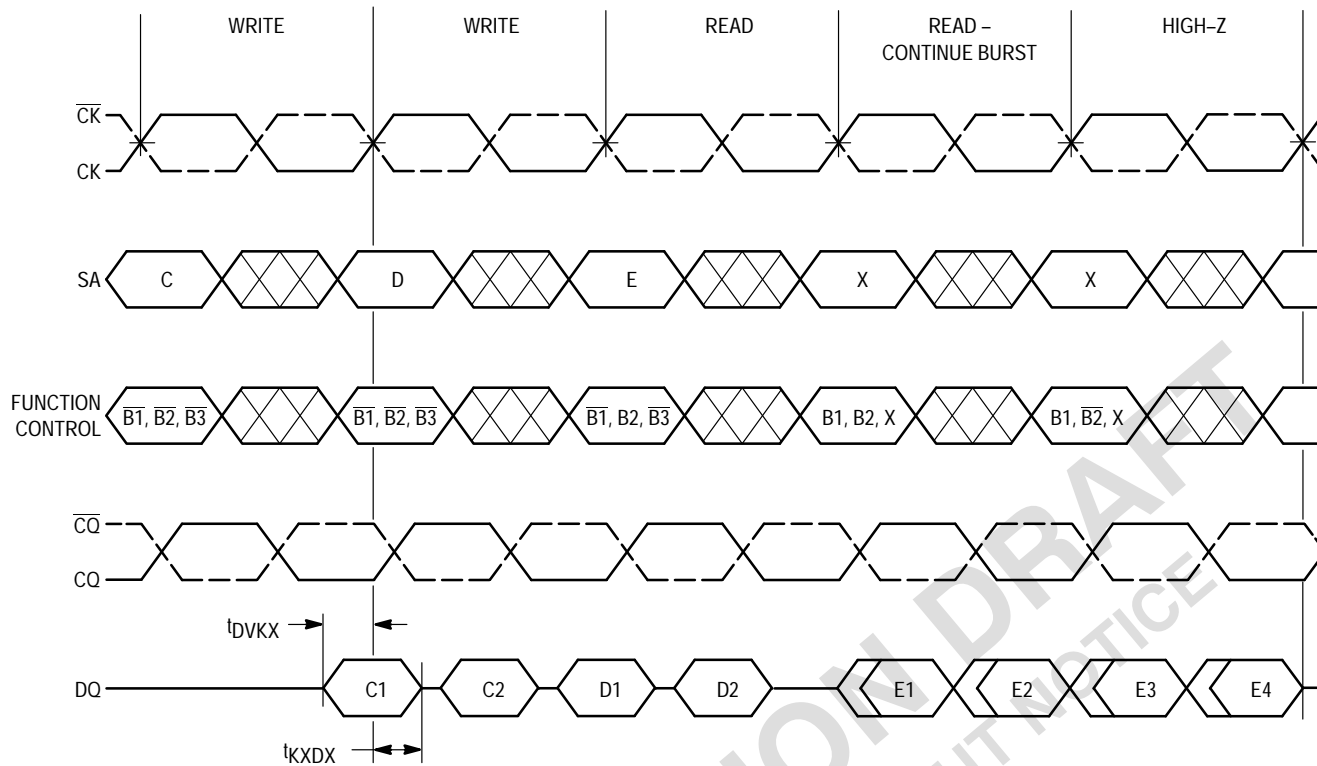

DOUBLE WRITE TIMING

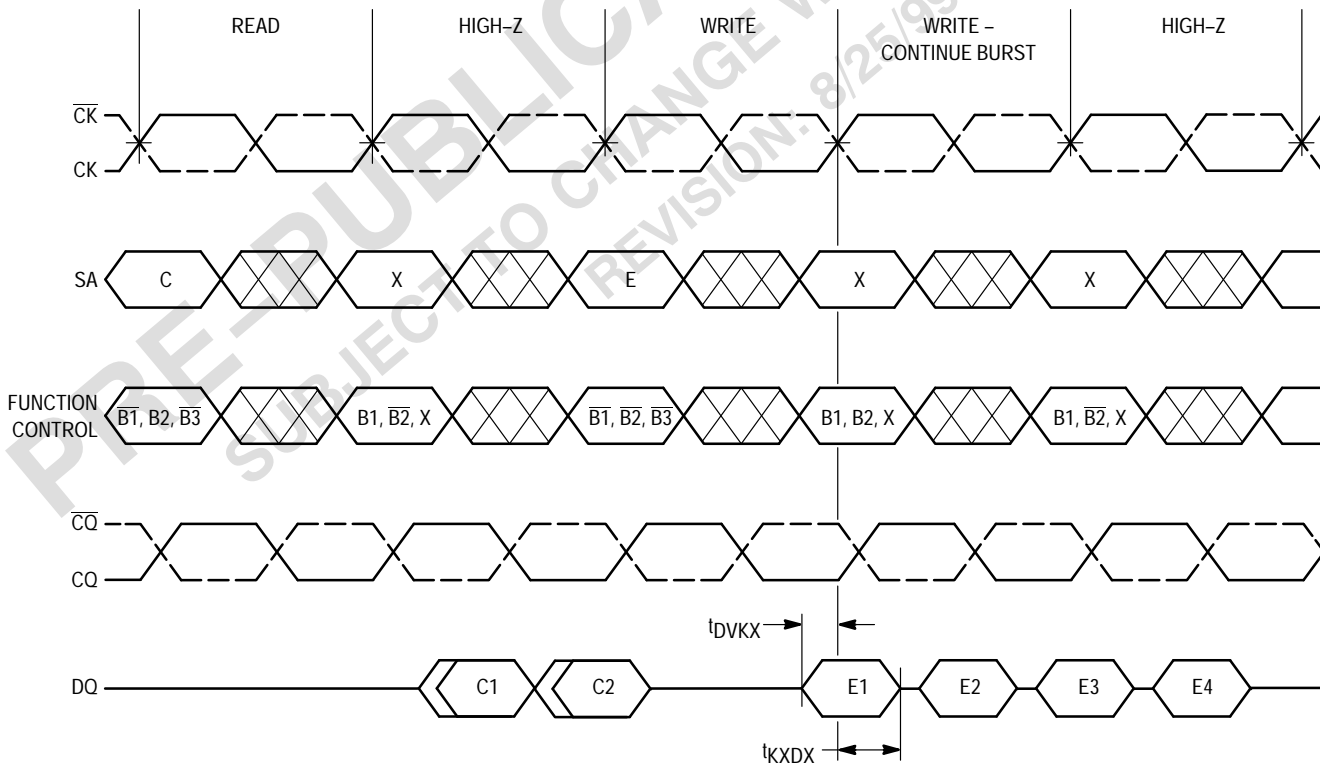MOTOROLA FAST SRAM

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SINGLE WRITE TIMING

| WRITE | WRITE CONTINUE BURST | HIGH–Z |

$\overline{CK}$

CK

SA: F, X, X, X

FUNCTION CONTROL: $\overline{B1}$, $\overline{B2}$, B3 | B1, B2, X | B1, $\overline{B2}$, X | X

$\overline{CQ}$

CQ

t_{DVKX}

DQ: F1, F2

t_{KHDX}

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WRITE AND READ TIMING

	WRITE	WRITE	READ	READ – CONTINUE BURST	HIGH–Z

$\overline{CK}$

CK

SA: C, D, E, X, X

FUNCTION CONTROL: $\overline{B1}, \overline{B2}, \overline{B3}$ | $\overline{B1}, \overline{B2}, \overline{B3}$ | $\overline{B1}, B2, \overline{B3}$ | B1, B2, X | B1, $\overline{B2}$, X

$\overline{CQ}$

CQ

t_{DVKX}

DQ: C1, C2, D1, D2, E1, E2, E3, E4

t_{KXDX}

READ AND WRITE TIMING

	READ	HIGH–Z	WRITE	WRITE – CONTINUE BURST	HIGH–Z

$\overline{CK}$

CK

SA: C, X, E, X, X

FUNCTION CONTROL: $\overline{B1}, B2, \overline{B3}$ | B1, $\overline{B2}$, X | $\overline{B1}, \overline{B2}, \overline{B3}$ | B1, B2, X | B1, $\overline{B2}$, X

$\overline{CQ}$

CQ

t_{DVKX}

DQ: C1, C2, E1, E2, E3, E4

t_{KXDX}

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SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for IEEE 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture (the TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with IEEE 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–5 (2.5 V) logic level signaling.

DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid–level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 k resistor. TDO should be left unconnected.

TAP DC OPERATING CHARACTERISTICS

(2.375 V $\leq V_{DD} \leq$ 2.625 V, 0°C $\leq T_A \leq$ 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit	Notes
Logic Input Logic High	$V_{IH}1$	1.2	$V_{DD} + 0.3$	V	
Logic Input Logic Low	$V_{IL}1$	– 0.3	0.4	V	
Logic Input Leakage Current	I_{lkg}	—	±5	µA	1
CMOS Output Logic Low	$V_{OL}1$	—	0.2	V	2
CMOS Output Logic High	$V_{OH}1$	$V_{DDQ} - 0.2$	—	V	3

NOTES:
1. 0 V $\leq V_{in} \leq V_{DD}$ for all logic input pins.
2. $I_{OL}1 \leq$ 100 µA @ V_{OL} = 0.2 V. Sampled, not 100% tested.
3. $|I_{OH}1| \leq$ 100 µA @ $V_{DDQ} - 0.2$ V. Sampled, not 100% tested.

TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T$_A$ ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . 0 to 2.2 V
Input Rise/Fall Time . . . . 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level . . . . 1.1 V
Output Timing Reference Level . . . . 1.1 V

Output Test Load . . . . . 50 Ω Parallel Terminated T–Line with 20 pF
Receiver Input Capacitance
Test Load Termination Supply Voltage (V$_T$) . . . . 1.1 V

TAP CONTROLLER TIMING

Parameter	Symbol	Min	Max	Unit	Notes
Cycle Time	t$_{THTH}$	100	—	ns	
Clock High Time	t$_{THTL}$	40	—	ns	
Clock Low Time	t$_{TLTH}$	40	—	ns	
TMS Setup	t$_{MVTH}$	10	—	ns	
TMS Hold	t$_{THMX}$	10	—	ns	
TDI Valid to TCK High	t$_{DVTH}$	10	—	ns	
TCK High to TDI Don't Care	t$_{THDX}$	10	—	ns	
Capture Setup	t$_{CS}$	10	—	ns	1
Capture Hold	t$_{CH}$	10	—	ns	1
TCK Low to TDO Unknown	t$_{TLQX}$	0	—	ns	
TCK Low to TDO Valid	t$_{TLOV}$	—	20	ns	

NOTE:
1. t$_{CS}$ + t$_{CH}$ defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

AC TEST LOAD
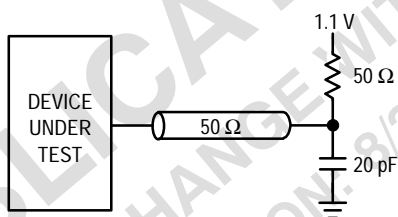
TAP CONTROLLER TIMING DIAGRAM
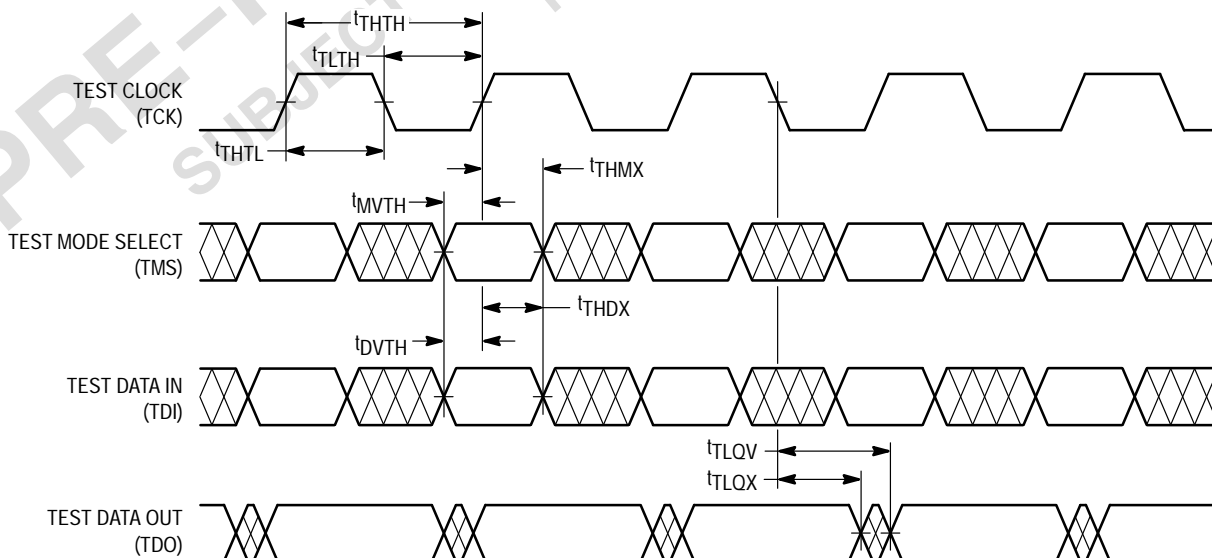
TEST ACCESS PORT PINS

TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic 1 input level.

TDI — TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 6). An undriven TDI pin will produce the same result as a logic 1 input level.

TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 6). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

TRST — TAP RESET

This device does not have a TRST pin. TRST is optional in IEEE 1149.1. The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

TEST ACCESS PORT REGISTERS

OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of 1s and 0s input to the TMS pin as the TCK is strobed. Each of the TAP registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected, it is "placed" between the TDI and TDO pins.

INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are 3 bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power up or whenever the controller is placed in test–logic–reset state.

BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 68 bits in the case of the x36 device and 49 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

IDENTIFICATION (ID) REGISTER

The ID register is a 32–bit register that is loaded with a device and vendor specific 32–bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32–bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Presence Indicator

Bit No.	0
Value	1

Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1–1990

Bit No.	11	10	9	8	7	6	5	4	3	2	1
Value	0	0	0	0	0	0	0	1	1	1	0

Reserved For Future Use

Bit No.	17	16	15	14	13	12
Value	x	x	x	x	x	x

Device Width

Configuration	Bit No.	22	21	20	19	18
256K x 36	Value	0	0	1	0	0
512K x 18	Value	0	0	0	1	1

Device Depth

Configuration	Bit No.	27	26	25	24	23
256K x 36	Value	0	0	1	1	0
512K x 18	Value	0	0	1	1	1

Revision Number

Bit No.	31	30	29	28
Value	x	x	x	x

Figure 5. ID Register Bit Meanings

MCM64E918 x18 Boundary Scan Order

Bit No.	Signal Name	Bump ID	Bit No.	Signal Name	Bump ID
1	SA1	5R	36	DQ	1H
2	SA0	5T	37	ZQ	5A
3	SA	6R	38	B1	5B
4	SA	7T	39	B2	5K
5	SA	7P	40	B3	5L
6	DQ	8T	41	$\overline{LBO}$	4L
7	DQ	9P	42	DQ	2K
8	$\overline{CQ}$	8M	43	DQ	1M
9	DQ	7K	44	DQ	3M
10	DQ	9K	45	DQ	2P
11	NC [1,2]	6L	46	DQ	1T
12	$\overline{CK}$	5H	47	SA	3P
13	CK	5G	48	SA	3T
14	$\overline{G}$	5C	49	SA	4R
15	DQ	8H			
16	DQ	9F			
17	DQ	7F			
18	DQ	8D			
19	DQ	9B			
20	SA	7D			
21	SA	7C			
22	SA	7B			
23	SA	7A			
24	SA	6C			
25	SA	6A			
26	SA	4A			
27	SA	4C			
28	SA	3A			
29	SA	3B			
30	SA	3C			
31	NC [1,3]	3D			
32	DQ	2B			
33	DQ	1D			
34	CQ	2F			
35	DQ	3H			

MCM64E836 x36 Boundary Scan Order

Bit No.	Signal Name	Bump ID	Bit No.	Signal Name	Bump ID
1	SA1	5R	36	SA	4A
2	SA0	5T	37	SA	4C
3	SA	6R	38	SA	3A
4	SA	7T	39	SA	3B
5	SA	7P	40	SA	3C
6	DQ	8T	41	NC [1,3]	3D
7	DQ	9T	42	DQ	2B
8	DQ	8P	43	DQ	1B
9	DQ	7M	44	DQ	2D
10	DQ	9P	45	DQ	3F
11	$\overline{CQ}$	8M	46	DQ	1D
12	DQ	9M	47	CQ	2F
13	DQ	7K	48	DQ	1F
14	DQ	8K	49	DQ	3H
15	DQ	9K	50	DQ	2H
16	NC [1,2]	6L	51	DQ	1H
17	$\overline{CK}$	5H	52	ZQ	5A
18	CK	5G	53	B1	5B
19	$\overline{G}$	5C	54	B2	5K
20	DQ	9H	55	B3	5L
21	DQ	8H	56	$\overline{LBO}$	4L
22	DQ	7H	57	DQ	1K
23	DQ	9F	58	DQ	2K
24	CQ	8F	59	DQ	3K
25	DQ	9D	60	DQ	1M
26	DQ	7F	61	$\overline{CQ}$	2M
27	DQ	8D	62	DQ	1P
28	DQ	9B	63	DQ	3M
29	DQ	8B	64	DQ	2P
30	SA	7D	65	DQ	1T
31	SA	7C	66	DQ	2T
32	SA	7B	67	SA	3T
33	SA	7A	68	SA	4R
34	SA	6C			
35	SA	6A			

NOTES:
1. NC pads are place holder bits and are true no–connects. When reading out the boundary scan register, these bits are forced high.
2. Place holder for Mode pin.
3. Placeholder for 16M DDR.

TAP CONTROLLER INSTRUCTION SET

OVERVIEW

There are two classes of instructions defined in the IEEE Standard 1149.1–1990; the standard (public) instructions and device specific (private) instructions. Some public instructions are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in capture–IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

STANDARD (PUBLIC) INSTRUCTIONS

BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK), it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be

expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register, has the same effect as the pause–DR command. This functionality is not IEEE 1149.1 compliant.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore, this device is not IEEE 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all 0s instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register, the RAM responds just as it does in response to the SAMPLE/PRELOAD instruction described above, except the DQ pins are forced to High–Z (CQ pins are not) any time the instruction is loaded.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

DEVICE SPECIFIC (PUBLIC) INSTRUCTION

SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all DQ pins are forced to an inactive drive state (High–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

DEVICE SPECIFIC (PRIVATE) INSTRUCTION

NO OP

Do not use these instructions; they are reserved for future use.

STANDARD (PUBLIC) INSTRUCTION CODES

| Instruction	Code*	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all DQ pins to High–Z state. **NOT IEEE 1149.1 COMPLIANT.**
IDCODE	001**	Preloads ID register and places it between TDI and TDO. Does not affect RAM operation.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement IEEE 1149.1 PRELOAD function. **NOT IEEE 1149.1 COMPLIANT.**
BYPASS	111	Places bypass register between TDI and TDO. Does not affect RAM operation.
SAMPLE–Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all DQ pins to High–Z state.

* Instruction codes expressed in binary; MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

STANDARD (PRIVATE) INSTRUCTION CODES

Instruction	Code*	Description
NO OP	011	Do not use these instructions; they are reserved for future use.
NO OP	101	Do not use these instructions; they are reserved for future use.
NO OP	110	Do not use these instructions; they are reserved for future use.

* Instruction codes expressed in binary; MSB on left, LSB on right.
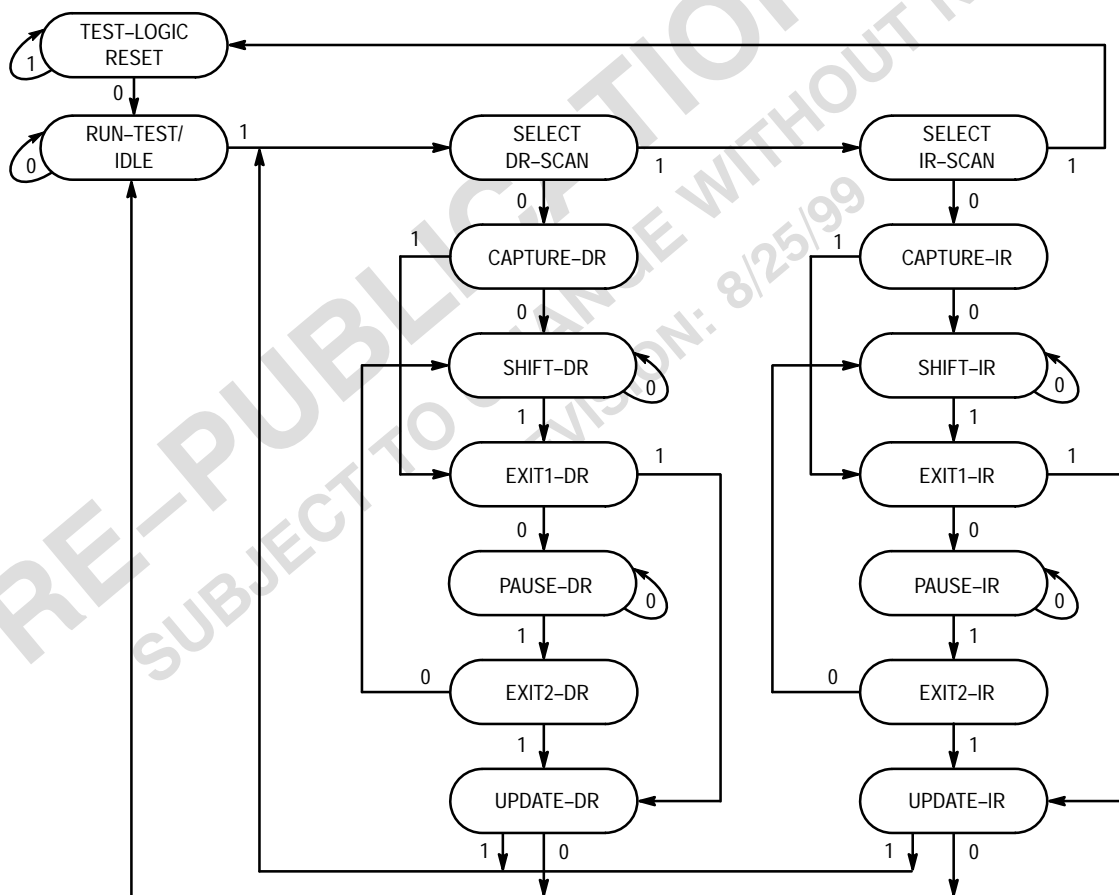
NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 6. TAP Controller State Diagram

ORDERING INFORMATION
(Order by Full Part Number)

```
                    64E918
          MCM       64E836       FC    X    X

Motorola PowerPC Prefix ─────────┘      │    │    └── Shipping Method (R = Tape and Reel,
                                        │    │            Blank = Rails)
Part Number ────────────────────────────┘    └────── Speed (3.0 = 3.0 ns, 3.3 = 3.3 ns, 4.0 = 4.0 ns,
                                        │                4.4 = 4.4 ns, 5.0 = 5.0 ns)
                                        └─────────── Package (FC = Flipped Chip PBGA,
                                                         RS = Flipped Chip CBGA)
```
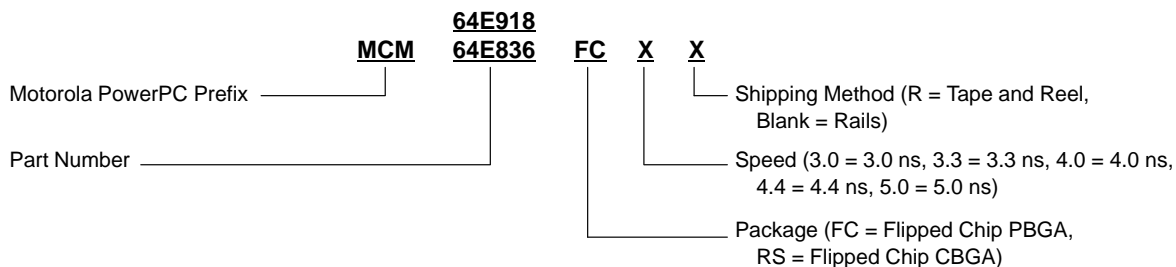
Full Part Numbers —

MCM64E918FC3.0	MCM64E918FC3.0R	MCM64E836FC3.0	MCM64E836FC3.0R
MCM64E918FC3.3	MCM64E918FC3.3R	MCM64E836FC3.3	MCM64E836FC3.3R
MCM64E918FC4.0	MCM64E918FC4.0R	MCM64E836FC4.0	MCM64E836FC4.0R
MCM64E918FC4.4	MCM64E918FC4.4R	MCM64E836FC4.4	MCM64E836FC4.4R
MCM64E918FC5.0	MCM64E918FC5.0R	MCM64E836FC5.0	MCM64E836FC5.0R
MCM64E918RS3.0	MCM64E918RS3.0R	MCM64E836RS3.0	MCM64E836RS3.0R
MCM64E918RS3.3	MCM64E918RS3.3R	MCM64E836RS3.3	MCM64E836RS3.3R
MCM64E918RS4.0	MCM64E918RS4.0R	MCM64E836RS4.0	MCM64E836RS4.0R
MCM64E918RS4.4	MCM64E918RS4.4R	MCM64E836RS4.4	MCM64E836RS4.4R
MCM64E918RS5.0	MCM64E918RS5.0R	MCM64E836RS5.0	MCM64E836RS5.0R

PACKAGE DIMENSIONS

FC PACKAGE
153–BUMP FLIPPED CHIP PBGA
CASE 1107A–01
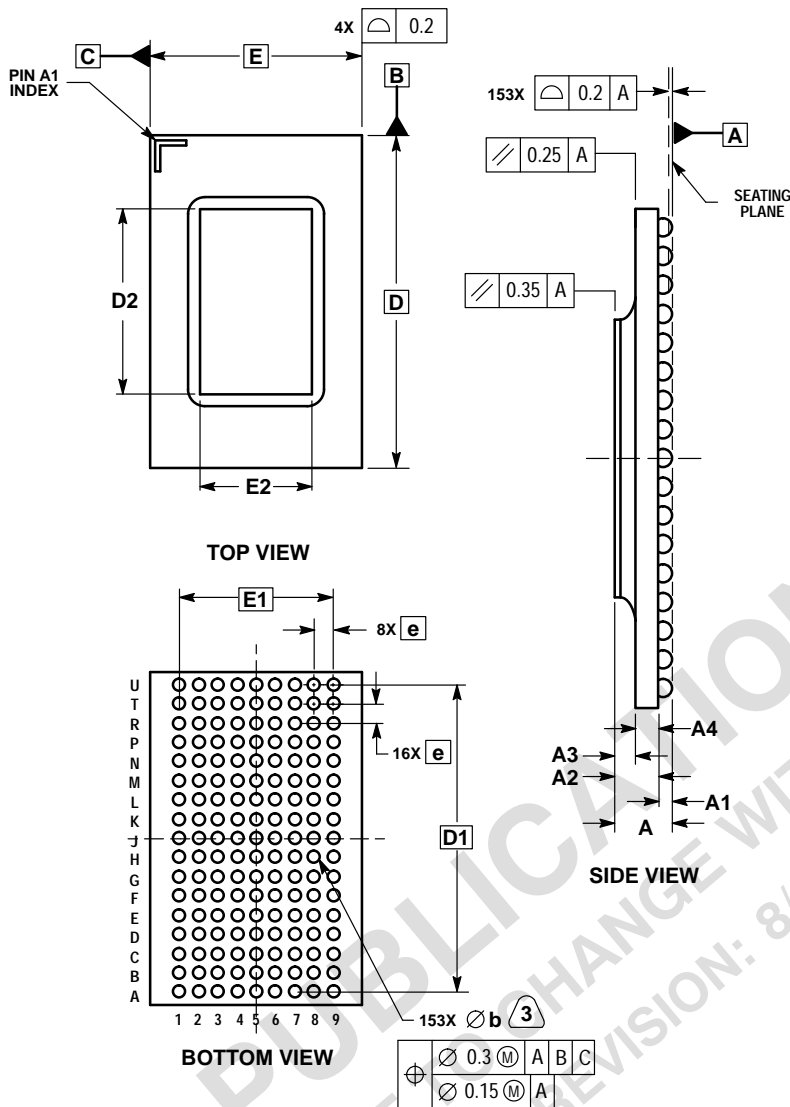
TOP VIEW

SIDE VIEW

BOTTOM VIEW

PIN A1 INDEX

SEATING PLANE

4X ⌒ 0.2

153X ⌒ 0.2 A

0.25 A

0.35 A

153X ⌀ b 3

⌀ 0.3 Ⓜ A B C
⌀ 0.15 Ⓜ A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1992.
2. ALL DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM PLANE A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. D2 AND E2 DEFINE THE AREA OCCUPIED BY THE DIE. D3 AND E3 ARE THE MINIMUM CLEARANCE FROM THE PACKAGE EDGE TO THE CHIP CAPACITORS.
6. CAPACITORS MAY NOT BE PRESENT ON ALL DEVICES.
7. CAUTION MUST BE TAKEN NOT TO SHORT EXPOSED METAL CAPACITOR PADS ON PACKAGE TOP.

DIM	MILLIMETERS	
	MIN	MAX
A	——	2.77
A1	0.50	0.70
A2	1.75	2.07
A3	0.80	0.92
A4	0.92	1.15
D	22.00 BSC	
D1	20.32 BSC	
D2	11.60	11.90
E	14.00 BSC	
E1	7.62 BSC	
E2	6.80	6.11
b	0.60	0.90
e	1.27 BSC	

TOP VIEW

BOTTOM VIEW

SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1992.
2. ALL DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM PLANE A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. D2 AND E2 DEFINE THE AREA OCCUPIED BY THE DIE. D3 IS THE MINIMUM CLEARANCE FROM THE PACKAGE EDGE TO THE CHIP CAPACITORS.
6. CAPACITORS MAY NOT BE PRESENT ON ALL DEVICES.
7. CAUTION MUST BE TAKEN NOT TO SHORT EXPOSED METAL CAPACITOR PADS ON PACKAGE TOP.

DIM	MILLIMETERS	
	MIN	MAX
A	–––	3.02
A1	0.80	1.00
A2	1.70	2.02
A3	0.80	0.92
A4	0.90	1.10
D	22.00 BSC	
D1	20.32 BSC	
D2	11.60	11.90
E	14.00 BSC	
E1	7.62 BSC	
E2	6.80	6.11
b	0.82	0.93
e	1.27 BSC	

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MCM64E918/D