FOUR QUADRANT MULTIPLYING SIN/COS DAC, MICROPROCESSOR COMPATIBLE, 16-BIT HYBRID

DESCRIPTION

The DS-11802 is a small size, high accuracy, 16-bit digital-to-sine/cosine converter. Available in accuracies up to 1 arc minute, the DS-11802 is contained in a 28-pin DDIP and requires +15 Vdc and -15 Vdc power supplies. The reference input is buffered through an op-amp to minimize loading on the input signal and can accept up to ±10 V peak. The DS-11802 is pin programmable for gains of 0.5, 1.0, and 2.0. Two registers for the input of the 16-bit (CMOS/TTL) natural binary angle data allow for compatibility with an 8-bit or 16-bit data bus. Internally, the DS-11802 has a multiplying digital-to-sin/cos converter consisting of two function generators and a quadrant select network. Quadrant information is available from the two most significant bits (MSBs). The two function generators use the remaining angular data along with the buffered reference voltage. Similar to a multiplying DAC (digital-to-analog converter), the DS-11802 uses high-accuracy resistive ladder networks and solid-state switching to control the attenuation of the reference voltage. The output buffer amplifiers allow for up to 2 mA output drive.

APPLICATIONS

Due to the high accuracy, high reliability, small size, low power consumption and MIL-PRF-38534 processing available, the DS-11802 is suitable for industrial and military ground or avionic applications. Possible applications include digital remote positioning, resolver angle simulation, flight trainers, flight instrumentation, radar and navigational systems, and PPI displays including moving target indicators. Other applications are synchro/resolver system development and testing, and wraparound test of synchro/resolver-to-digital converters.

FEATURES

- ***28-Pin Ceramic DDIP Package***
- ***1 Arc Minute Accuracy***
- ***0.03% Radius Accuracy***
- ***Microprocessor Compatible - 8- and 16-Bit***
- ***Double-Buffered Inputs***
- ***Pin-Programmable Gain - 0.5, 1.0 or 2.0***
- ***Buffered Reference Input***
- ***DC-Coupled Reference and Outputs***
- ***Requires Only ±15 V Power Supplies***
- ***TTL and CMOS Compatible***
- ***Pin-for-Pin Replacement for Natel's HDSC2306***

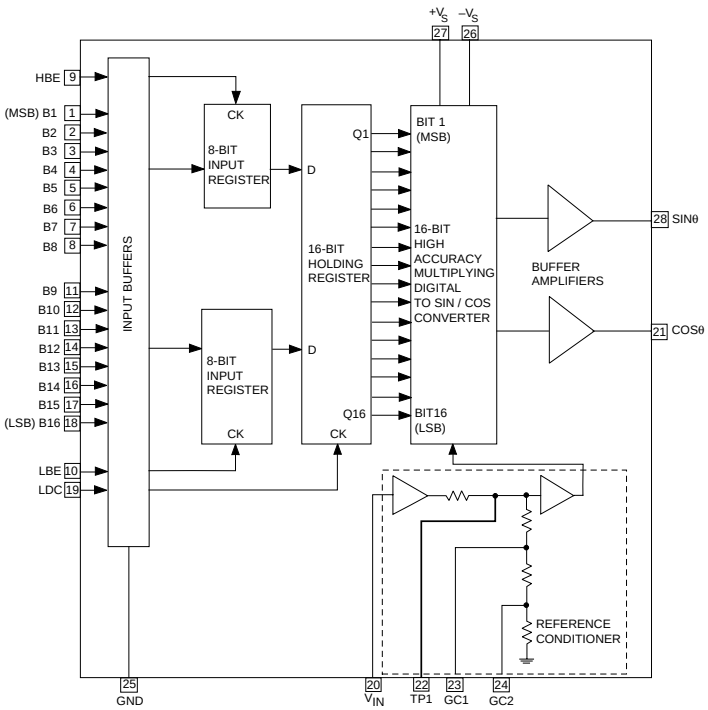


FIGURE 1. DS-11802 BLOCK DIAGRAM

TABLE 1. DS-11802 SPECIFICATIONS		
PARAMETER	**VALUE**	**REMARKS**
DIGITAL ANGULAR		
Resolution	16 Bits	Bit 1 = MSB, Bit 16 = LSB
Accuracy	±4 arc-minutes ±2 arc-minutes ±1 arc-minutes	Accuracy applies over operating temperature range.
ANALOG INPUT (V_{IN})		
Voltage	0 to ±10 Vp ac or dc	
Frequency Range	dc to 1000 Hz	
Input Resistance	1 MΩ min	Op amp buffer
ANALOG OUTPUTS		
SIN θ	K • Vin • SIN θ	±10 Vp AC or DC
COS θ	K • Vin • COS θ	±10 Vp AC or DC
Converter Gain (K)	0.5 ±0.2%	Pin 23 connected to gnd. Pin 24 no connection.
	1.0 ±0.2%	Pin 24 connected to gnd. Pin 23 no connection.
	2.0 ±0.2%	Pin 23 and 24 floating.
Radius Accuracy	±0.1%	Guaranteed, but not tested.
Output Current	2 mA rms	
Output Impedance	< 1 ohm	Op amp output.
Zero Offset (dc)	±10 mV typical ±25 mV max	
Offset Drift	25 µV/°C	
Output Settling Time	30 µsec max to accuracy of converter	For any digital step change.
DIGITAL INPUTS		
Logic Voltage Levels		No external logic voltages required.
Logic 0	-0.3 V DC to 0.8 V DC	
Logic 1	2.4 V DC to 5.5 V DC	
Loading	0.1 TTL load	CMOS transient protected.
Input Current		
Data Bits (B1-B16)	15 µA typ, "active" pull-down to gnd	For less than 16 bits, unused pins can be left unconnected.
HBE, LBE, LDC	-15 µA typ, "active" pull-up to internal logic supply	Pins not used can be left unconnected.
REGISTER CONTROLS		
HBE (High Byte Enable)	Logic 1	8 MSBs enter high byte input register.
	Logic 0	High byte register remains unaffected.
LBE (Low Byte Enable)	Logic 1	8 LSBs enter low byte input register.
	Logic 0	Low byte register remains unaffected.
LDC (Load Converter)	Logic 1	Data from input registers transferred to holding register.
	Logic 0	Data in holding register remains unaffected.

TABLE 1. DS-11802 SPECIFICATIONS (CONTINUED)		
PARAMETER	**VALUE**	**REMARKS**
REGISTER CONTROLS (Continued)		
Data Set-up Time	200 ηsec min	Before data transfer.
Data Hold Time	200 ηsec min	Before input data changes.
POWER SUPPLIES		
Supply Voltages (±Vs)	±15 V dc ±10%	For ±10 V pk output.
Supply Current	±25 mA max	
Supply Rejection	80 db typ	
TEMPEATURE RANGES		
Operating Case		
-3XX and -8XX	0°C to +70°C	
-5XX and -2XX	-40°C to +85°C	
-1XX and -4XX	-55°C to +125°C	
Storage	-65°C to +135°C	
PHYSICAL CHARACTERISTICS		
Type	28 Pin Double DIP	
Size	0.6 x 1.4 x 0.2 in. (15 x 36 x 5) mm	
Weight	0.5 oz (15 gm) max	
ABSOLUTE MAXIMUM RATINGS		
Reference Input:	-Vs to +Vs	
Power Supply Voltage (±Vs):	±18 V dc	
Digital Inputs:	-0.3 V dc to +6.5 V dc	

ANALOG OUTPUT GAIN CONTROL AND PHASING

The DS-11802 is pin-programmable for gains of 0.5, 1.0 and 2.0. TABLE 2 details the programming of gain control pins 23 (GC1) and 24 (GC2). When both pins are left unconnected or open, the gain of the converter is 2.0. The output signal would be: 2 Vin sinθ and 2 Vin cosθ. When GC2 is connected to GND and GC1 is left open, the converter gain is 1.0. When GC1 is connected to GND and GC2 is left open, the converter gain is 0.5. When looking at the equivalent gain circuit (see FIGURE 2) the gain of the converter can be modified by adding a resistor between GC1 or GC2 and GND.

TABLE 2. GAIN CONTROL PINS		
GC1 (PIN 23)	**GC2 (PIN 24)**	**GAIN (K)**
Gnd	Open	0.5
Open	Gnd	1.0
Open	Open	2.0

Users are cautioned against using a large value resistor to modify the gain, as the temperature coefficient of the external resistor will not be matched with the TCR of the internal resistor. The internal gain resistors have an accuracy of 0.05%.

FIGURE 3 illustrates the output phasing between the reference voltage Vin and the analog output signals as a function of the digital angle and the converter gain K (0.5, 1.0, or 2.0).

DIGITAL INTERFACE

The DS-11802 has double-buffered input registers which allow easy implementation of an interface with 8-bit or 16-bit data buses. The DS-11802 can also be set up for asynchronous data inputs. If the LBE, HBE and LDC input pins are left open, the internal pull-up circuitry will set these pins to a high state and the information at the data inputs (B1-B16) is continuously converted to sinθ and cosθ at the analog outputs. For applications requiring less than 16-bit resolution, the unused data bit pins can be left open. The data bits (B1-B16) are internally pulled-down to apply a logic “0” to unconnected data inputs.

DATA TRANSFER FROM AN 8-BIT DATA BUS

Applications with a 8-bit data bus require two-byte loading of the digital input (see FIGURE 4).

FIGURE 5 shows the timing for two-byte data transfers.

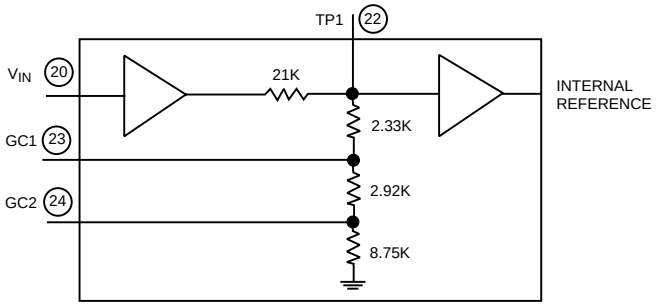


FIGURE 2. REFERENCE CONDITIONER

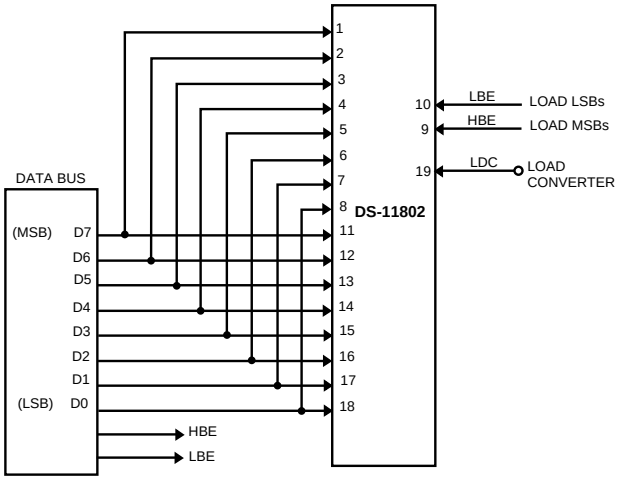
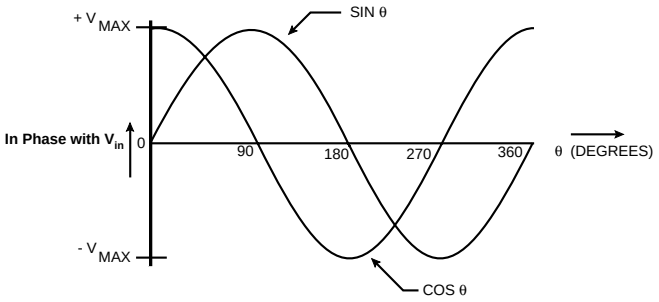


FIGURE 4. DATA TRANSFER FROM 8-BIT BUS



SIN OUTPUT = K • Vin • (1+n) SINθ

COS OUTPUT = K • Vin • (1+n) COSθ

WHERE:

K IS THE GAIN OF THE CONVERTER.

n IS THE SCALE FACTOR VARIATION AS A FUNCTION OF DIGITAL ANGLE(± 0.2%)

FIGURE 3. OUTPUT PHASING

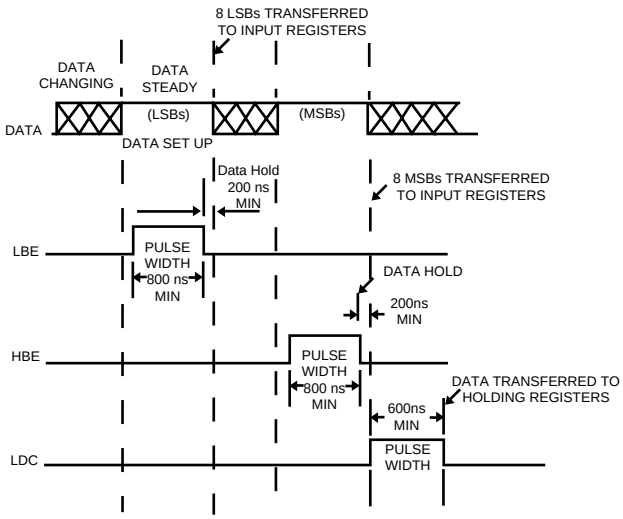


FIGURE 5. TIMING FOR 8-BIT BUS TRANSFER

1. The LDC is low (logic 0) so that the contents of the holding register are latched and will remain unaffected by the changes on the input registers.

2. When the LBE is set high (logic 1) the 8 LSBs (B9-B16) are transferred to the low byte. The LBE must remain high for a minimum of 800 nsec after the data is stable. The data should remain stable for 200 nsec after the LBE is set low (logic 0).

3. When the HBE is set high (logic 1) the 8 MSBs (B1-B8) are transferred to the low byte. The HBE must remain high for a minimum of 800 nsec after the data is stable. The data should remain stable for 200 nsec after the HBE is set low (logic 0).

4. When the LDC is set high (logic 1) the data is transferred from the two input registers to the holding register. The LDC should be held high for 600 nsec minimum. Once the LDC is set low, the cycle can begin again.

Note: LBE, HBE, and LDC are level-actuated functions. Refer to TABLE 3 for bit values.

TABLE 3. DIGITAL ANGLE INPUTS

BIT	DEG/BIT	MIN/BIT
1 MSB	180.0	10800.0
2	90.0	5400.0
3	45.0	2700.0
4	22.5	1350.0
5	11.25	675.0
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

Note: HBE enables the MSBs and LBE enables the LSBs.

DATA TRANSFER FROM A 16-BIT DATA BUS

Applications interfacing with a 16-bit data bus require only single byte loading (see FIGURE 6). LBE and HBE are either unconnected or tied together and pulsed high to load data.

As shown in the timing diagram (see FIGURE 7) 200 nsec after the data has been stable, the LDC is set high (logic 1) to transfer the data to the holding register. Since LDC is level actuated, it must remain high for the time specified (600 nsec).

DIGITAL-TO-RESOLVER/SYNCHRO CONVERTERS

The output of the DS-11802 is a single-ended sin/cos. FIGURE 8 illustrates a schematic for a 4-Wire Digital-to-Resolver Converter (S1, S2, S3, and S4) using external power amplifiers and transformers.

FIGURE 9 illustrates a schematic for 3-Wire Digital-to-Synchro Converter (S1, S2, and S3) using an additional power stage and external transformers.

A benefit to the designs shown in FIGURES 8 and 9 is the ability to keep the converters near the digital data and control signals, and to mount the power amplifiers and transformers in a better thermal location. This would isolate heat dissipating circuits from high-accuracy computing circuits.

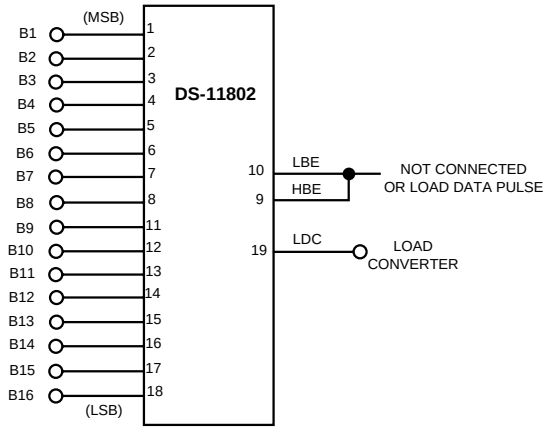


FIGURE 6. DATA TRANSFER FROM 16-BIT BUS

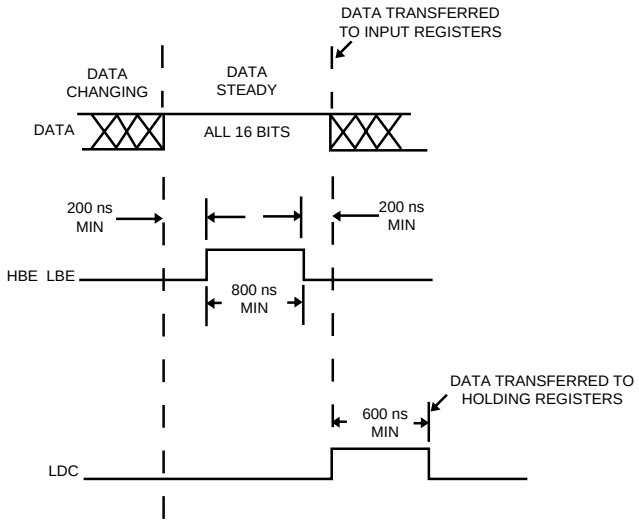


FIGURE 7. TIMING FOR 16-BIT BUS TRANSFER

LOW FREQUENCY SINE WAVE OSCILLATOR

The DS-11802 can be used to create a low frequency sine wave oscillator with very low distortion (see FIGURE 10). The output amplitude is determined by the amplitude of the dc reference input and the gain control pin configuration. When using a 16-bit counter and a square wave of 65,536 Hz (2N, where N = 16 bit resolution) the output will be at 1 Hz.

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on the +Vs and -Vs. supplies. A 1 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor should be mounted as close to the supply as possible.

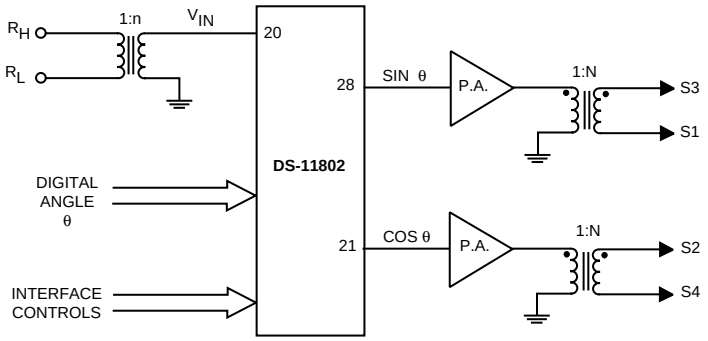


FIGURE 8. 4-WIRE DIGITAL-TO-RESOLVER CONVERTER

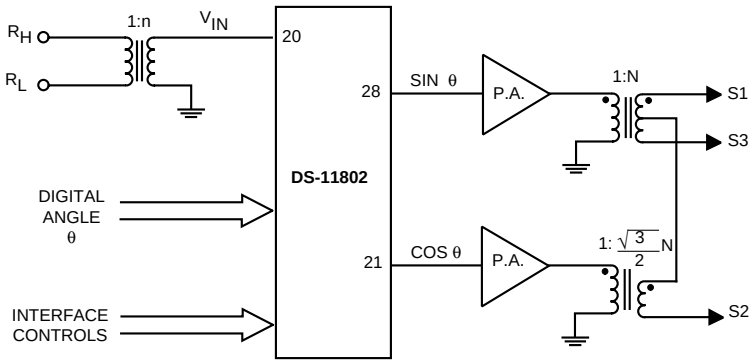


FIGURE 9. 3-WIRE DIGITAL-TO-SYNCHRO CONVERTER

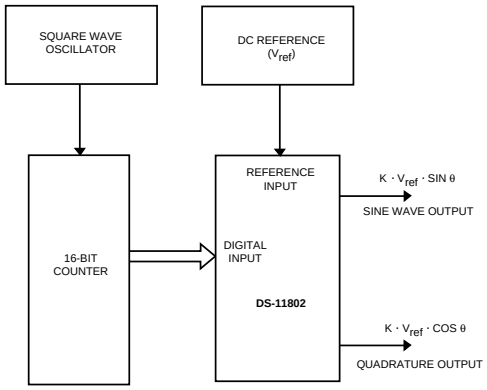


FIGURE 10. LOW FREQUENCY SINEWAVE OSCILLATOR

TABLE 4. DS-11802 PINOUTS			
PIN	**FUNCTION**	**PIN**	**FUNCTION**
1	B1	15	B13
2	B2	16	B14
3	B3	17	B15
4	B4	18	B16
5	B5	19	LDC
6	B6	20	V_{IN}
7	B7	21	COS θ
8	B8	22	TP1
9	HBE	23	GC1
10	LBE	24	GC2
11	B9	25	GND
12	B10	26	-Vs
13	B11	27	+Vs
14	B12	28	SIN θ

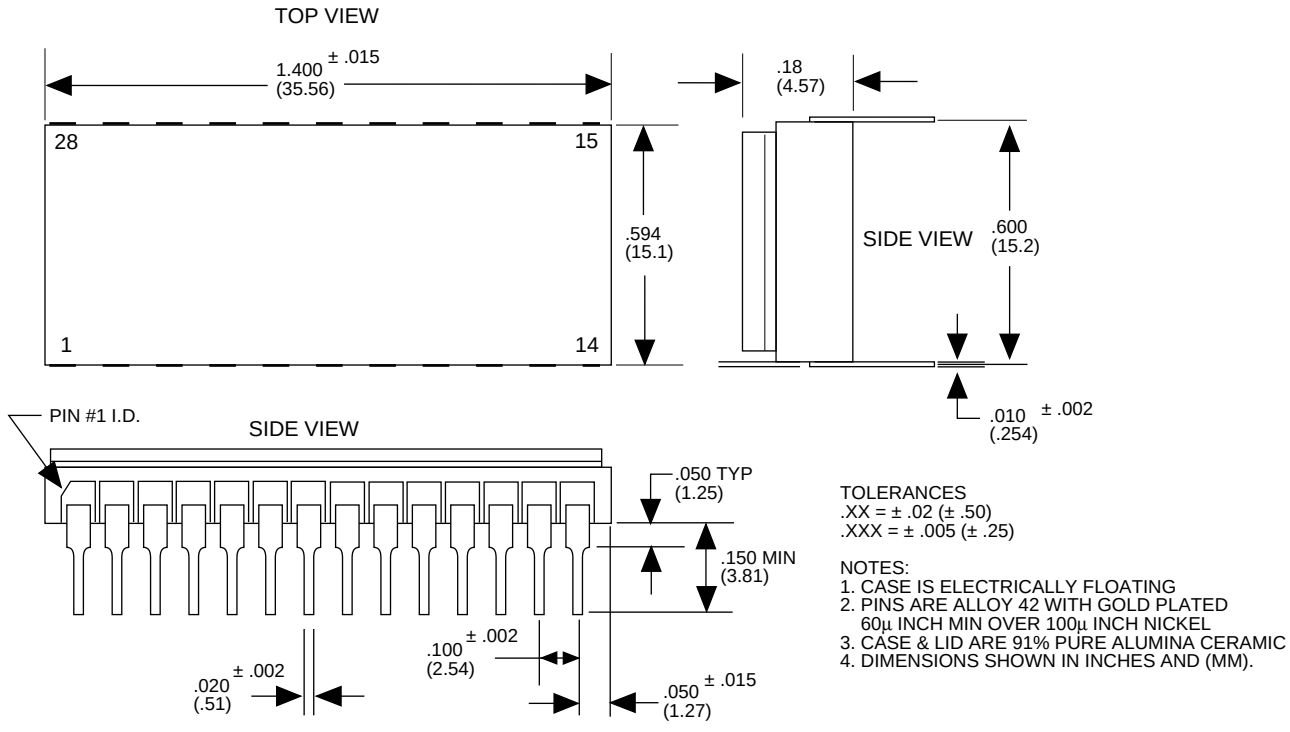


FIGURE 11. DS-11802 MECHANICAL OUTLINE

ORDERING INFORMATION

DS-11802DX-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 3 = ±4 Minutes
- 4 = ±2 Minutes
- 5 = ±1 Minute

Process Requirements*:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 2 = B*
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Frequency Range:
- 4 = DC to 1 kHz

* For availability of Fully Compliant MIL-PRF-38534 parts, please contact the DDC office nearest you.
**Standard DDC Processing with burn-in and full temperature test — see table below.

STANDARD DDC PROCESSING		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

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