INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT
TC5165165AJ/AFT-40
TC5165165AJ/AFT-50
TC5165165AJ/AFT-60
SILICON GATE CMOS

TENTATIVE DATA

4,194,304 WORD ×16 BIT EDO (HYPER PAGE) DYNAMIC RAM

DESCRIPTION

The TC5165165AJ/AFT is EDO (hyper page) dynamic RAM organized 4,194,304 words by 16 bits. The TC5165165AJ/AFT utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5165165AJ/AFT to be packaged in a 50 pin plastic SOJ, 50 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 3.3V±0.3V tolerance, direct interfacing capability with high performance logic families such as LVTTL.

FEATURES

- 4,194,304 word by 16bit organization
- Fast access time and cycle time

		TC5165165AJ/AFT		
		-40	-50	-60
t_{RAC}	$\overline{RAS}$ Access Time	40ns	50ns	60ns
t_{AA}	Column Address Access Time	20ns	25ns	30ns
t_{CAC}	$\overline{CAS}$ Access Time	11ns	13ns	15ns
t_{RC}	Cycle Time	69ns	84ns	104ns
t_{HPC}	Hyper Page Mode Cycle Time	16ns	20ns	25ns

- Single power supply of 3.3V±0.3V with a built-in V_{BB} generator
- Low Power
  612mW MAX. Operating (TC5165165AJ/AFT-40)
  504mW MAX. Operating (TC5165165AJ/AFT-50)
  432mW MAX. Operating (TC5165165AJ/AFT-60)
  1.8mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, EDO (Hyper Page Mode) and Test Mode capability
- All inputs and outputs LVTTL compatible
- 4096 refresh cycles/64ms
- Package TC5165165AJ : SOJ50-P-400
  TC5165165AFT : TSOP50-P-400D

PIN CONNECTION (TOP VIEW)

Plastic SOJ

V_{CC}	1	50	V_{SS}
I/O1	2	49	I/O16
I/O2	3	48	I/O15
I/O3	4	47	I/O14
I/O4	5	46	I/O13
V_{CC}	6	45	V_{SS}
I/O5	7	44	I/O12
I/O6	8	43	I/O11
I/O7	9	42	I/O10
I/O8	10	41	I/O9
NC	11	40	NC
V_{CC}	12	39	V_{SS}
$\overline{WE}$	13	38	$\overline{LCAS}$
$\overline{RAS}$	14	37	$\overline{UCAS}$
NC	15	36	$\overline{OE}$
NC	16	35	NC
NC	17	34	NC
NC	18	33	NC
A0	19	32	A11R
A1	20	31	A10R
A2	21	30	A9
A3	22	29	A8
A4	23	28	A7
A5	24	27	A6
V_{CC}	25	26	V_{SS}

Plastic TSOP (Normal Bend Type)

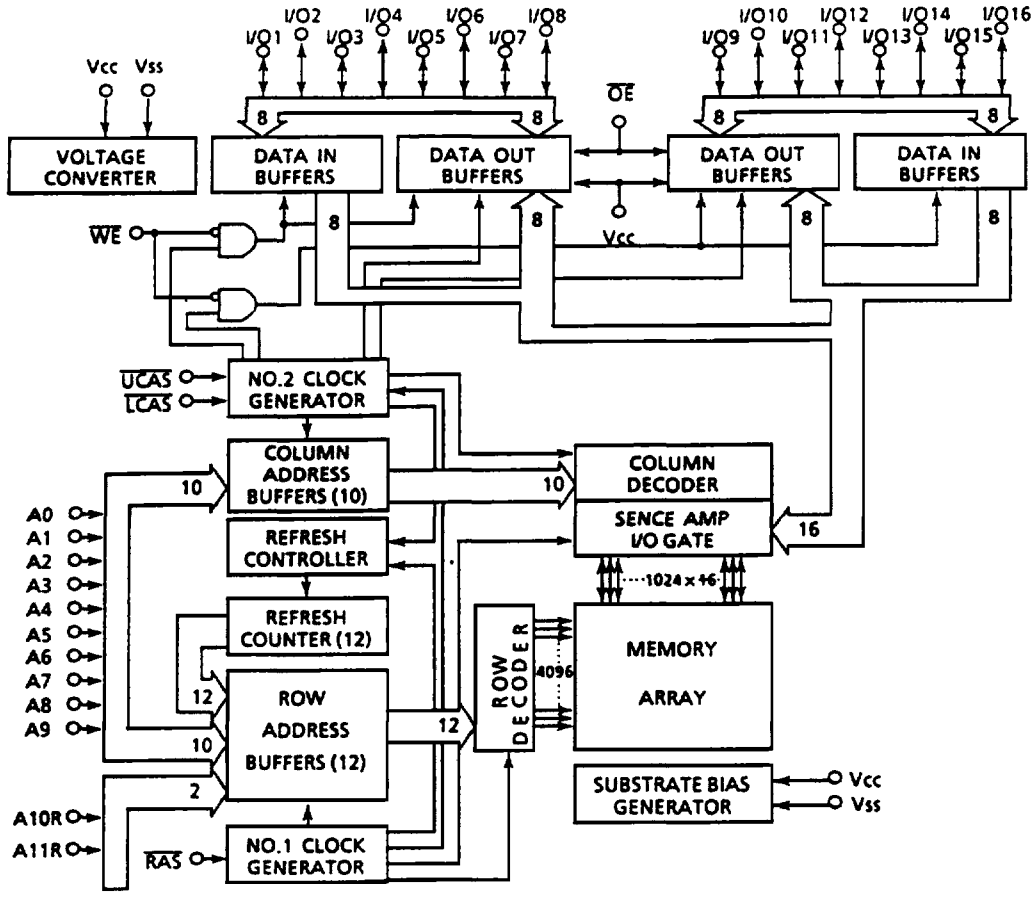
V_{CC}	1	50	V_{SS}
I/O1	2	49	I/O16
I/O2	3	48	I/O15
I/O3	4	47	I/O14
I/O4	5	46	I/O13
V_{CC}	6	45	V_{SS}
I/O5	7	44	I/O12
I/O6	8	43	I/O11
I/O7	9	42	I/O10
I/O8	10	41	I/O9
NC	11	40	NC
V_{CC}	12	39	V_{SS}
$\overline{WE}$	13	38	$\overline{LCAS}$
$\overline{RAS}$	14	37	$\overline{UCAS}$
NC	15	36	$\overline{OE}$
NC	16	35	NC
NC	17	34	NC
NC	18	33	NC
A0	19	32	A11R
A1	20	31	A10R
A2	21	30	A9
A3	22	29	A8
A4	23	28	A7
A5	24	27	A6
V_{CC}	25	26	V_{SS}

PIN NAMES

A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe / Upper Byte Control
$\overline{LCAS}$	Column Address Strobe / Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1~I/O16	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
N.C.	No Connection

TOSHS083

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC5165165AJ/AFT-40	–	170	mA	3, 4, 5
		TC5165165AJ/AFT-50	–	140		
		TC5165165AJ/AFT-60	–	120		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	1	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN.)	TC5165165AJ/AFT-40	–	170	mA	3, 5
		TC5165165AJ/AFT-50	–	140		
		TC5165165AJ/AFT-60	–	120		
I_{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{HPC} = t_{HPC} MIN.)	TC5165165AJ/AFT-40	–	130	mA	3, 4, 5
		TC5165165AJ/AFT-50	–	105		
		TC5165165AJ/AFT-60	–	85		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	500	μA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC5165165AJ/AFT-40	–	170	mA	3, 5
		TC5165165AJ/AFT-50	–	140		
		TC5165165AJ/AFT-60	–	120		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ Vcc, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ Vcc)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 2mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2mA)		–	0.4	V	

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−0.3~Vcc+0.3	V	1
Output Voltage	V_{OUT}	−0.3~Vcc+0.3	V	1
Power Supply Voltage	V_{CC}	−0.3~4.6	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature (10s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	1.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	2.0	–	Vcc+0.3*	V	2
V_{IL}	Input Low Voltage	−0.3**	–	0.8	V	2

* Vcc + 1.2V at pulse width ≦ 20ns. (pulse width is measured at Vcc)
** -1.2V at pulse width ≦ 20ns. (pulse width is measured at Vss)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 3.3V ± 0.3V, Ta = 0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC5165165AJ/AFT						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	69	–	84	–	104	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	92	–	111	–	135	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	40	–	50	–	60	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	–	11	–	13	–	15	ns	9, 14
t_{AA}	Access Time from Column Address	–	20	–	25	–	30	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	22	–	28	–	35	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	11	0	13	0	15	ns	10, 16
t_T	Transition Time (Rise and Fall)	1	50	1	50	1	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	25	–	30	–	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	40	10,000	50	10,000	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	40	100,000	50	100,000	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	6	–	8	–	10	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Hyper Page Mode)	22	–	28	–	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	30	–	35	–	40	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	6	10,000	8	10,000	10	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	9	29	11	37	14	45	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	7	20	9	25	12	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	6	–	8	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	5	–	7	–	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	5	–	7	–	10	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	5	–	7	–	10	–	ns	
t_{WP}	Write Command Pulse Width	5	–	7	–	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	6	–	8	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC5165165AJ/AFT						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	5	–	7	–	10	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	5	–	7	–	10	–	ns	12
t_{REF}	Refresh Period	–	64	–	64	–	64	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	26	–	30	–	34	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	55	–	67	–	79	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	35	–	42	–	49	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	37	–	45	–	54	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	7	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	5	–	7	–	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	11	–	13	–	15	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	11	–	13	–	15	–	ns	
t_{OLZ}	$\overline{OE}$ to output in Low-Z	0	–	0	–	0	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	11	0	13	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	5	–	7	–	10	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	0	–	ns	
t_{WTS}	Write Commamd Set-Up Time (Test Mode In)	5	–	5	–	5	–	ns	
t_{WTH}	Write Commamd Hold Time (Test Mode In)	5	–	7	–	10	–	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	7	–	10	–	ns	
t_{RNCD}	$\overline{RAS}$ to next $\overline{CAS}$ Delay Time (Hyper Page Mode)	40	–	50	–	60	–	ns	
t_{HPC}	Hyper Page Mode Cycle Time	16	–	20	–	25	–	ns	
t_{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	46	–	56	–	68	–	ns	
t_{COH}	Output Data Hold Time	5	–	5	–	5	–	ns	
t_{REZ}	Output Buffer Turn-off Delay from $\overline{RAS}$	0	11	0	13	0	15	ns	10, 16
t_{WEZ}	Output Buffer Turn-off Delay from $\overline{WE}$	0	11	0	13	0	15	ns	10
t_{WED}	$\overline{WE}$ to Data Delay	11	–	13	–	15	–	ns	
t_{OE}	$\overline{OE}$ Pulse Width	11	–	13	–	15	–	ns	
t_{OEP}	$\overline{OE}$ Precharge Time	6	–	8	–	10	–	ns	
t_{CPO}	$\overline{CAS}$ to $\overline{OE}$ Precharge Time	5	–	5	–	5	–	ns	
t_{OCH}	$\overline{CAS}$ Hold Time referenced to $\overline{OE}$	5	–	7	–	10	–	ns	

NOTES:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed once or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a hyper page mode cycle (t_{HPC}).
6. An initial pause of 200μs is required after power-up followed by a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles before proper device operation is achieved.
7. AC measurement assume $t_T=2ns$.
8. V_{IH} (min.)and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 100pF at $V_{OH}=2.0V$ ($I_{OUT}=-2mA$), $V_{OL}=0.8V$ ($I_{OUT}=2mA$).
10. t_{OFF} (max.), t_{OEZ} (max.), t_{REZ} (max.) and t_{WEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage leveles.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Hyper Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
16. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going (t_{OFF}). If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achicved by $\overline{RAS}$ high going (t_{REZ}).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC5165165AJ/AFT						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	74	–	89	–	109	–	ns	
t_{HPC}	Hyper Page Mode Cycle Time	21	–	25	–	30	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	45	–	55	–	65	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	16	–	18	–	20	ns	9,14
t_{AA}	Access Time from Column Address	–	25	–	30	–	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	27	–	33	–	40	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	45	10,000	55	10,000	65	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	45	100,000	55	100,000	65	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	11	–	13	–	15	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	35	–	40	–	45	–	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	27	–	33	–	40	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	11	10,000	13	10,000	15	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	–	30	–	35	–	ns	

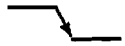
CAPACITANCE (V_{CC} = 3.3V ± 0.3V, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A11)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O16)	–	7	pF

Data Out Hi-Z control Logic

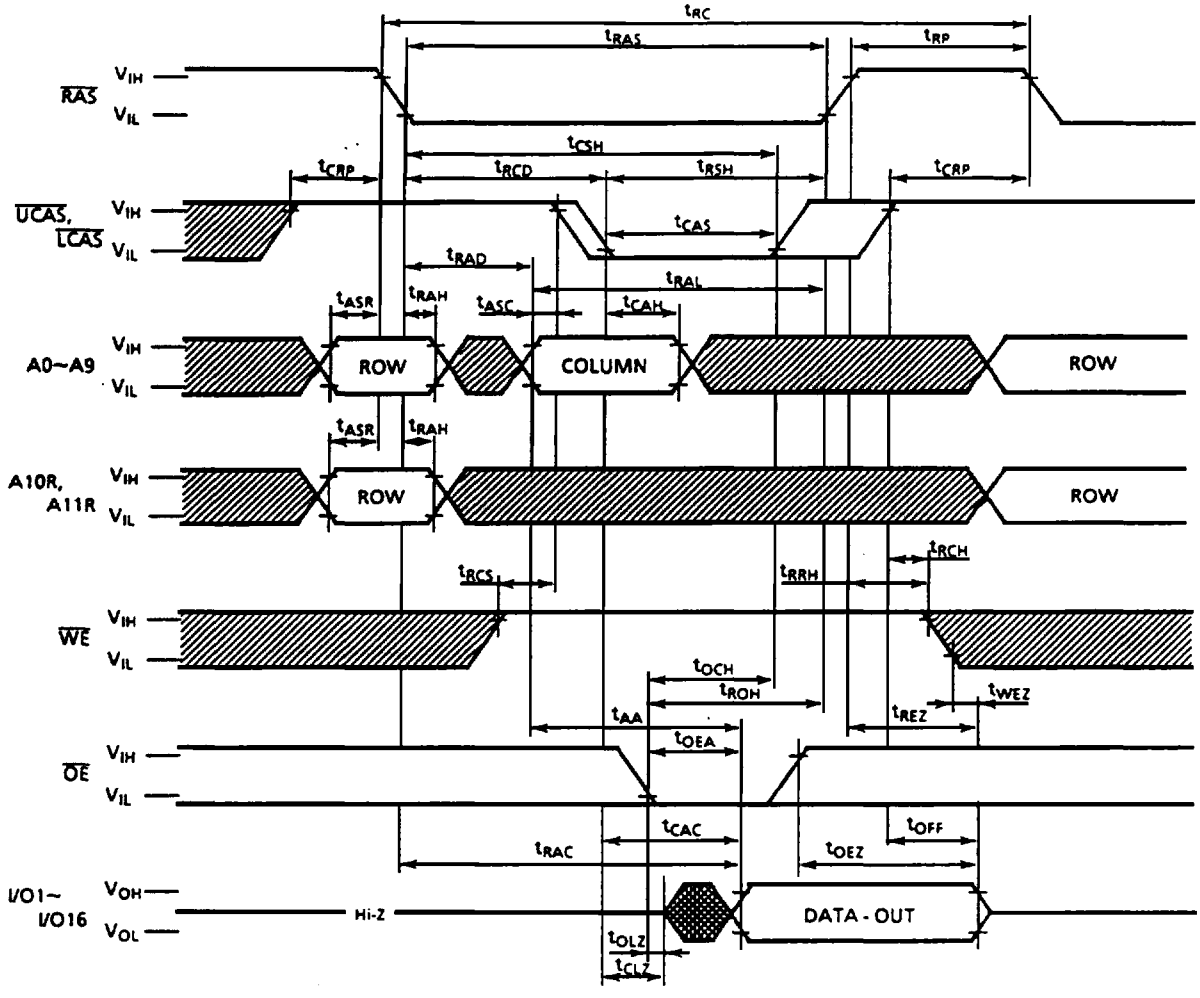
$\overline{RAS}$	$\overline{UCAS}$, $\overline{LCAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
"H"		"L"	"H"	t_{OFF}
	"H"	"L"	"H"	t_{REZ}
"L"	"L"		"H"	t_{OEZ}
"L"	"H"	"L"		t_{WEZ}

Data Out Lo-Z control Logic

$\overline{RAS}$	$\overline{UCAS}$, $\overline{LCAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
"L"		"L"	"H"	t_{CLZ}
"L"	"L"		"H"	t_{OLZ}
"L"	"L"		"H"	t_{OLZ}

TIMING DIAGRAMS

READ CYCLE

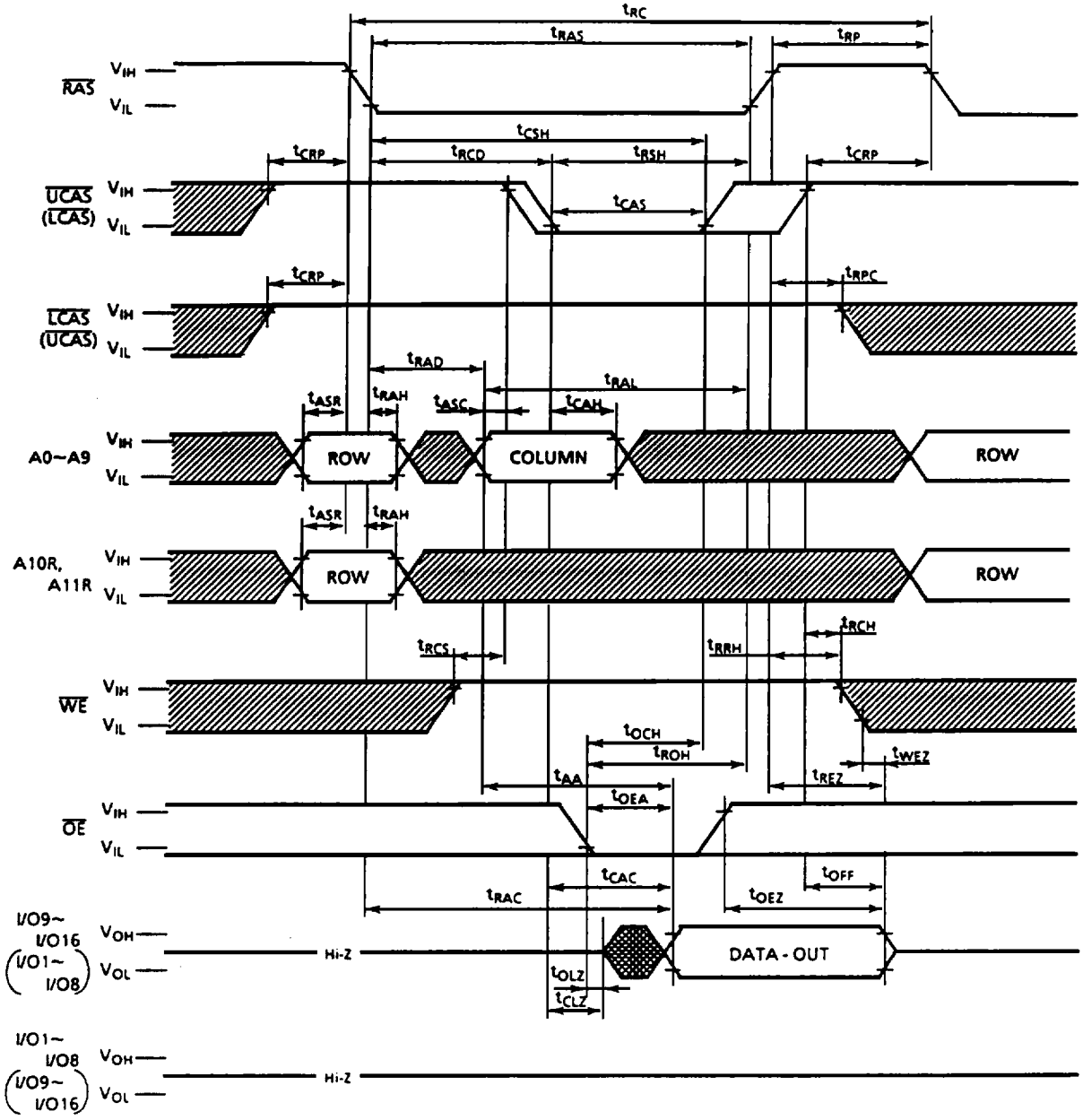


Note: D_{IN} = Hi-Z

: "H" or "L"

: Invalid Data

BYTE READ CYCLE

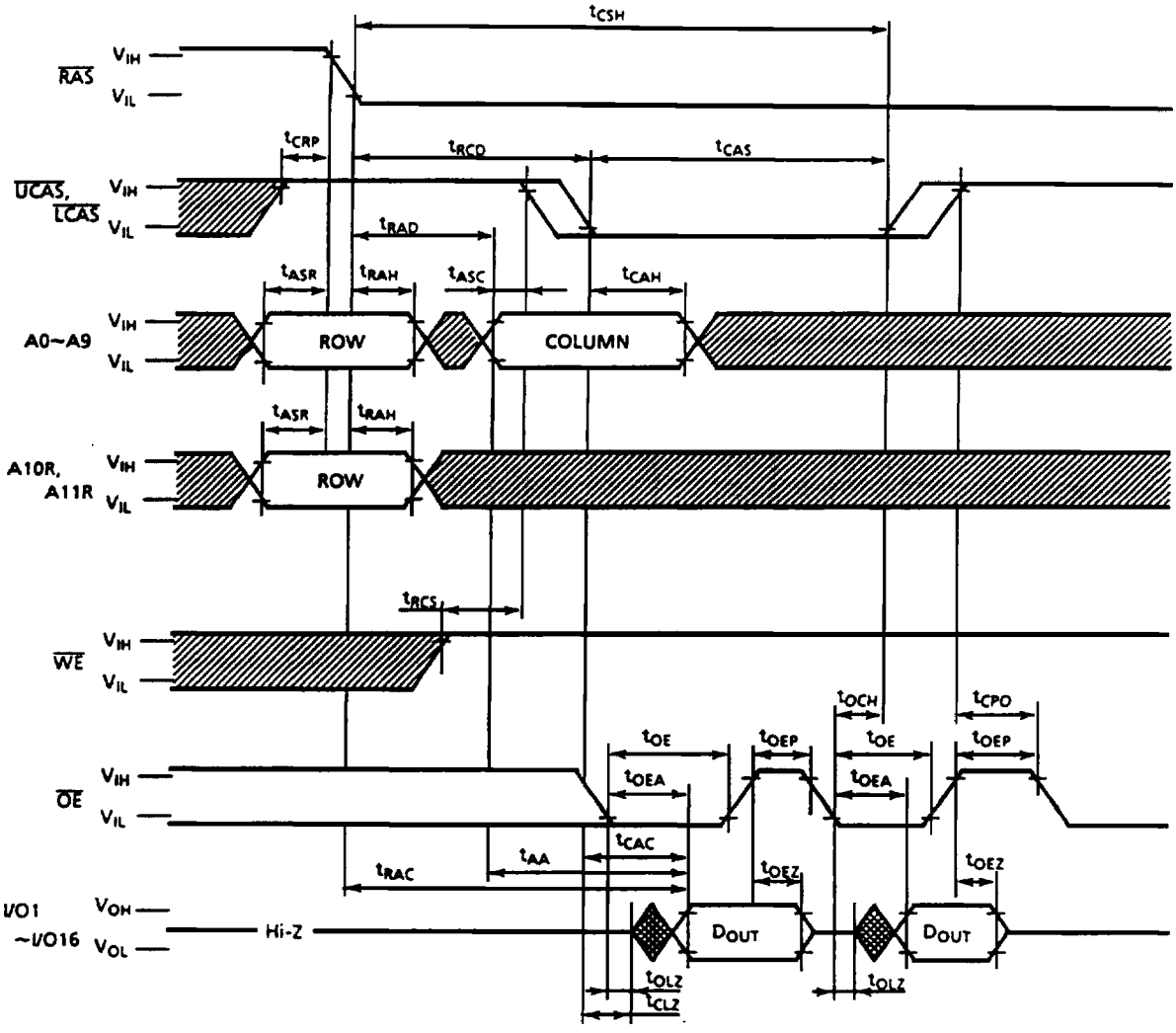


Note : D_{IN}(I/O1~I/O8) = Don't Care
D_{IN}(I/O9~I/O16) = Hi-Z
(D_{IN}(I/O1~I/O8) = Hi-Z
D_{IN}(I/O9~I/O16) = Don't Care)

▨ : "H" or "L"

▩ : Invalid Data

READ CYCLE ($\overline{OE}$ CONTROLLED READ)

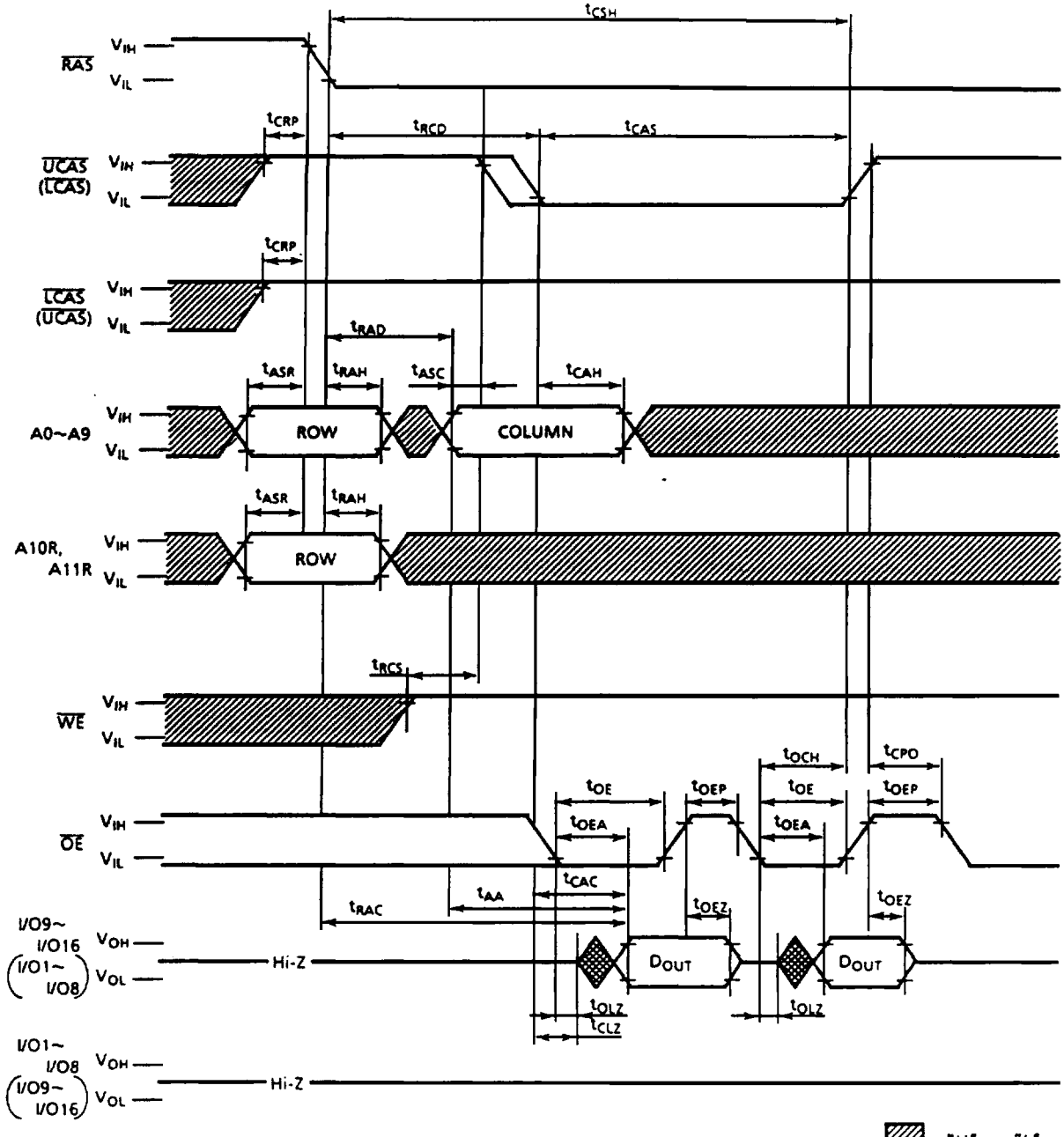


Note : D_{IN} = Hi-Z

: "H" or "L"

: Invalid Data

BYTE READ CYCLE ($\overline{OE}$ CONTROLLED READ)

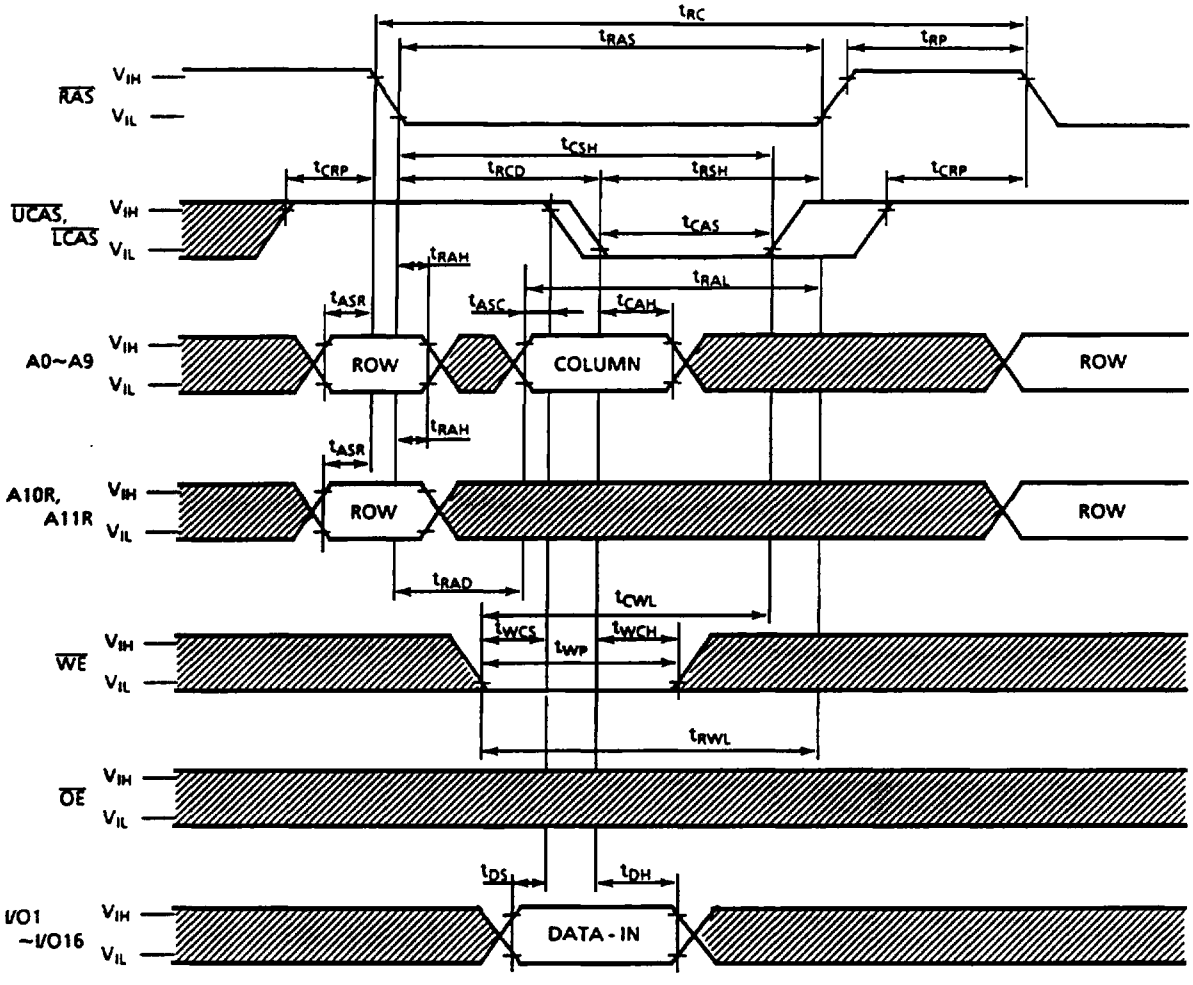


Note : D_{IN} = Hi-Z

▨ : "H" or "L"

▩ : Invalid Data

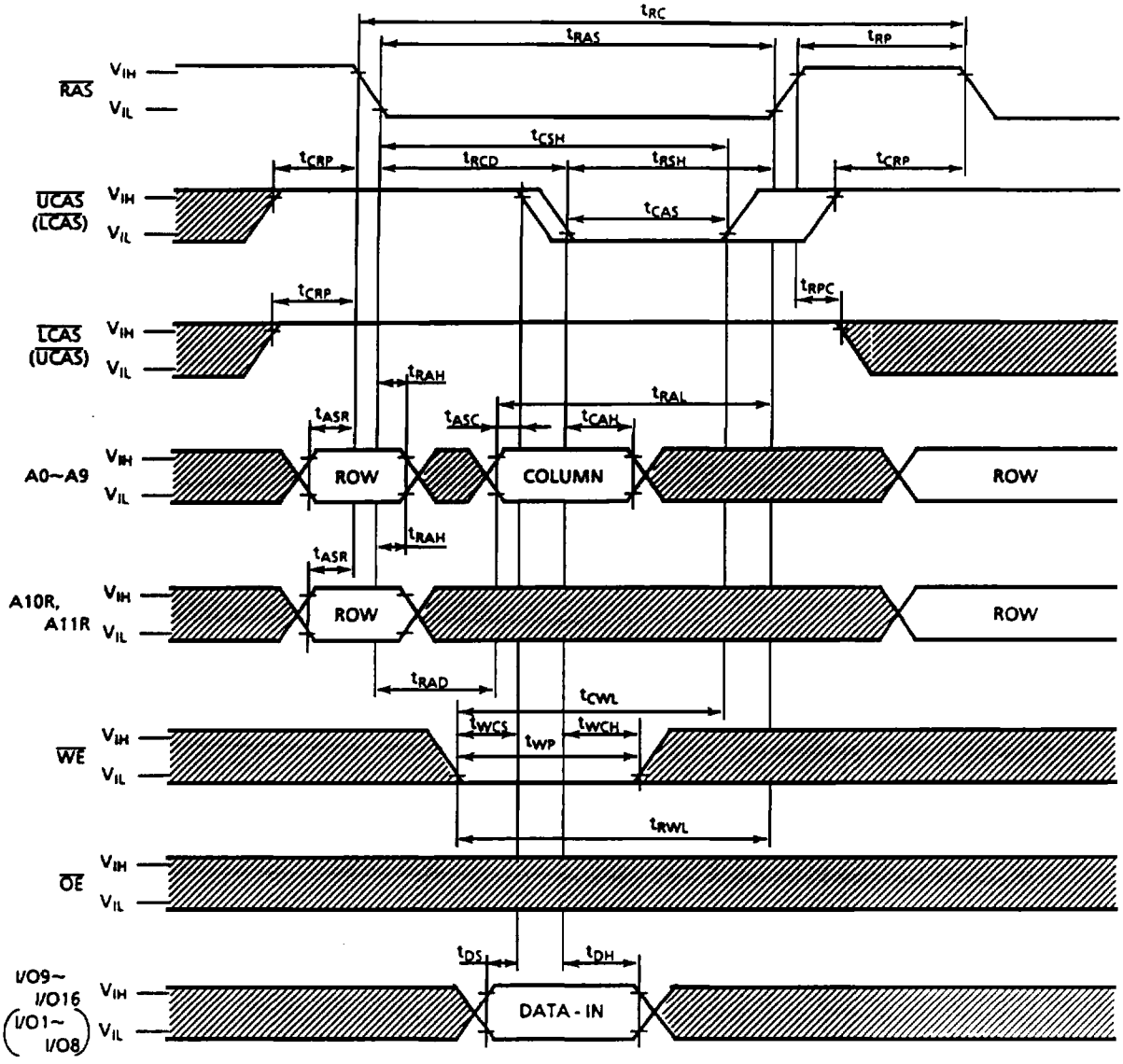
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

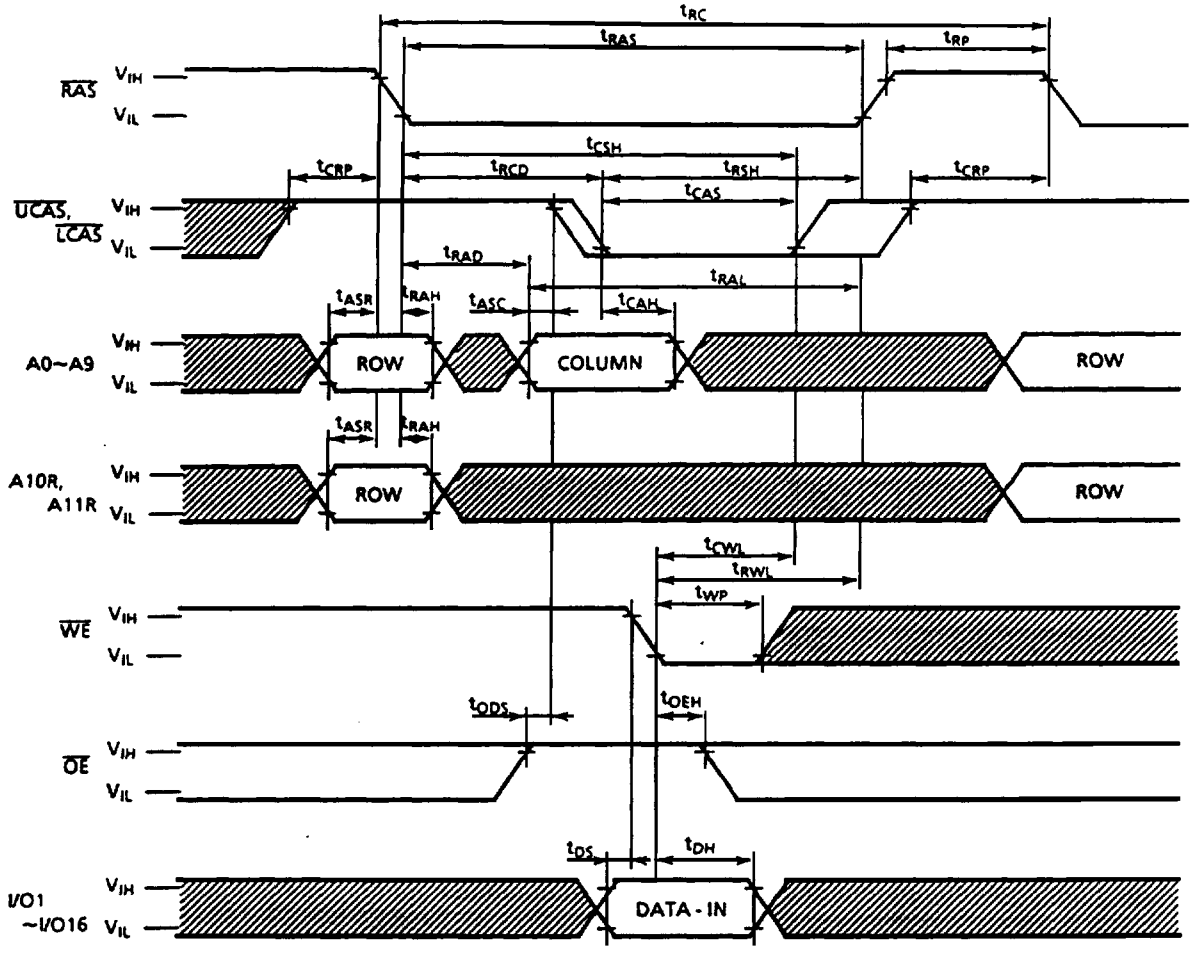
BYTE WRITE CYCLE (EARLY WRITE)



Note : D_{IN}(I/O1~I/O8) = Don't Care
D_{OUT} = Hi-Z
(D_{IN}(I/O9~I/O16) = Don't Care
D_{OUT} = Hi-Z)

▨ : "H" or "L"

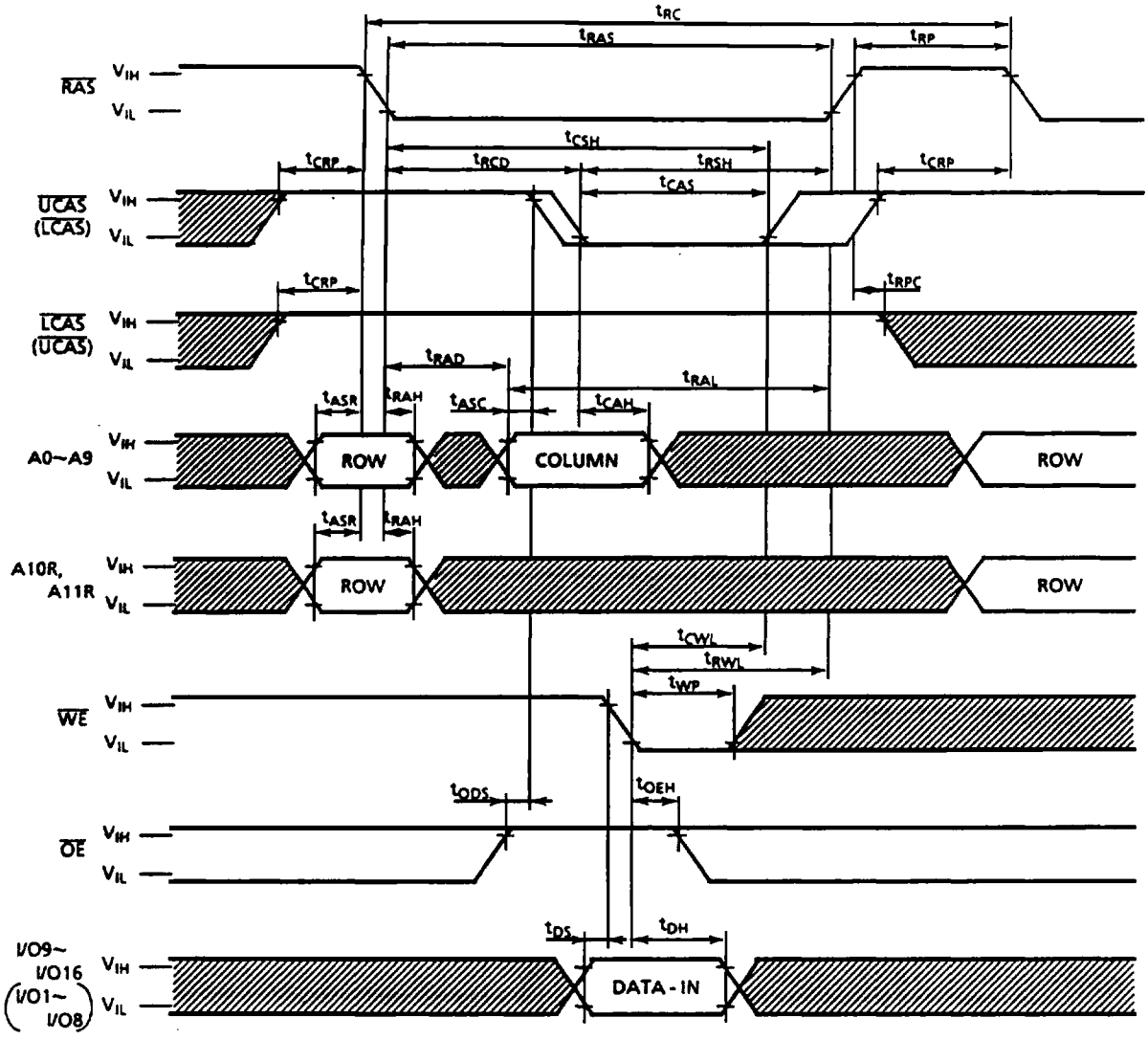
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

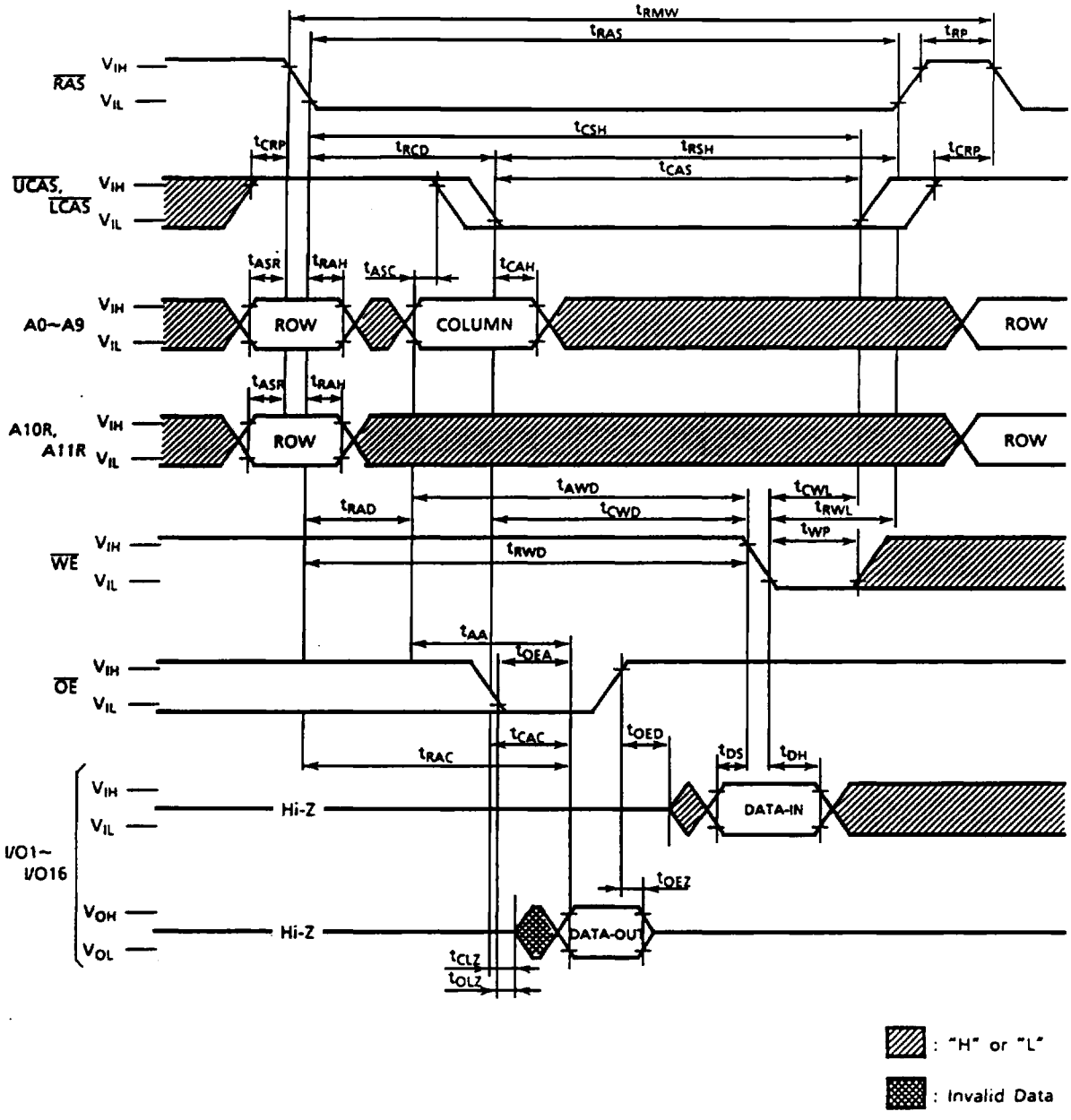
BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



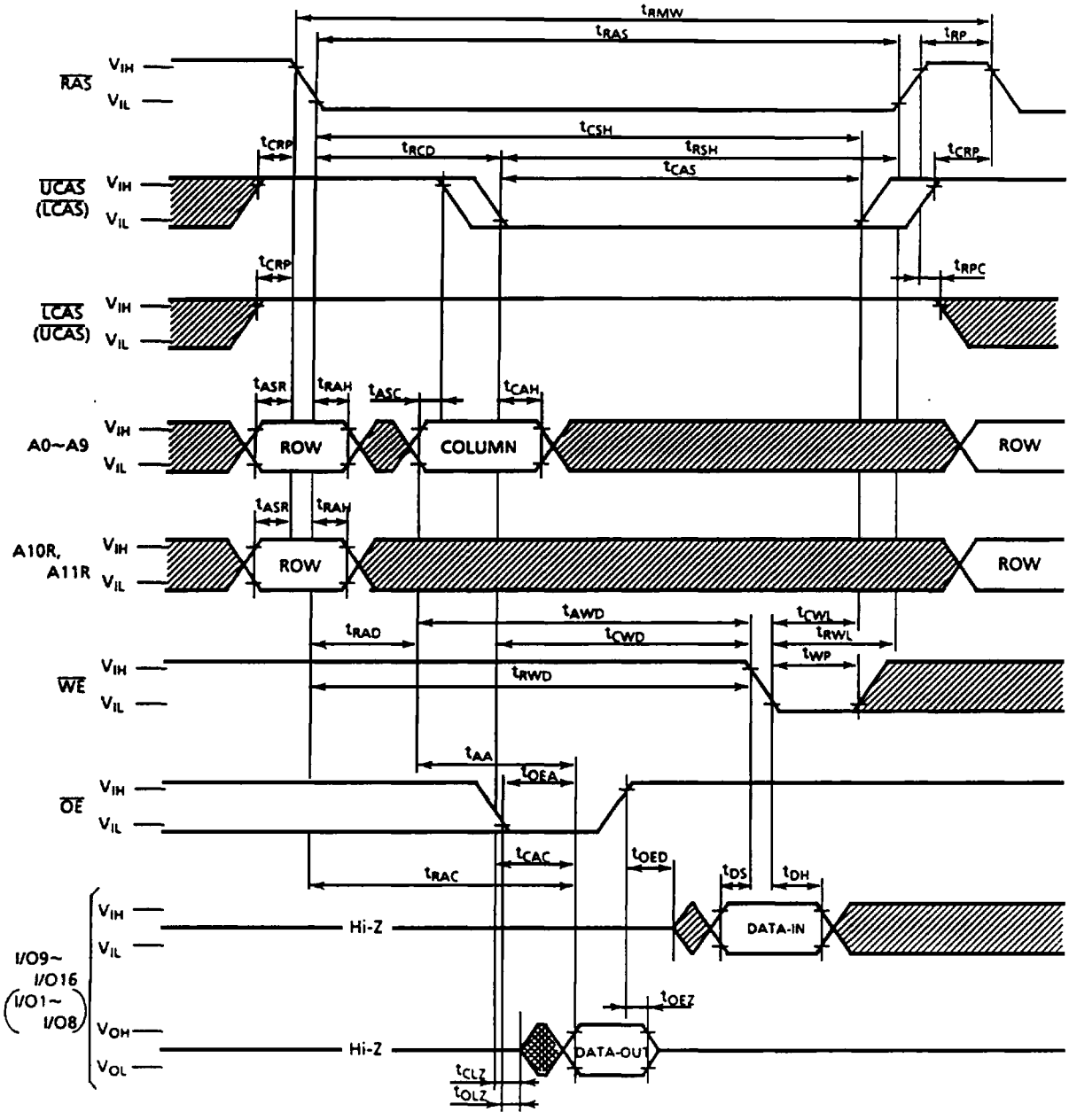
Note : D_{IN}(I/O1~I/O8) = Don't Care
(D_{OUT} = Hi-Z, D_{IN}(I/O9~I/O16) = Don't Care)

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



BYTE READ-MODIFY-WRITE CYCLE

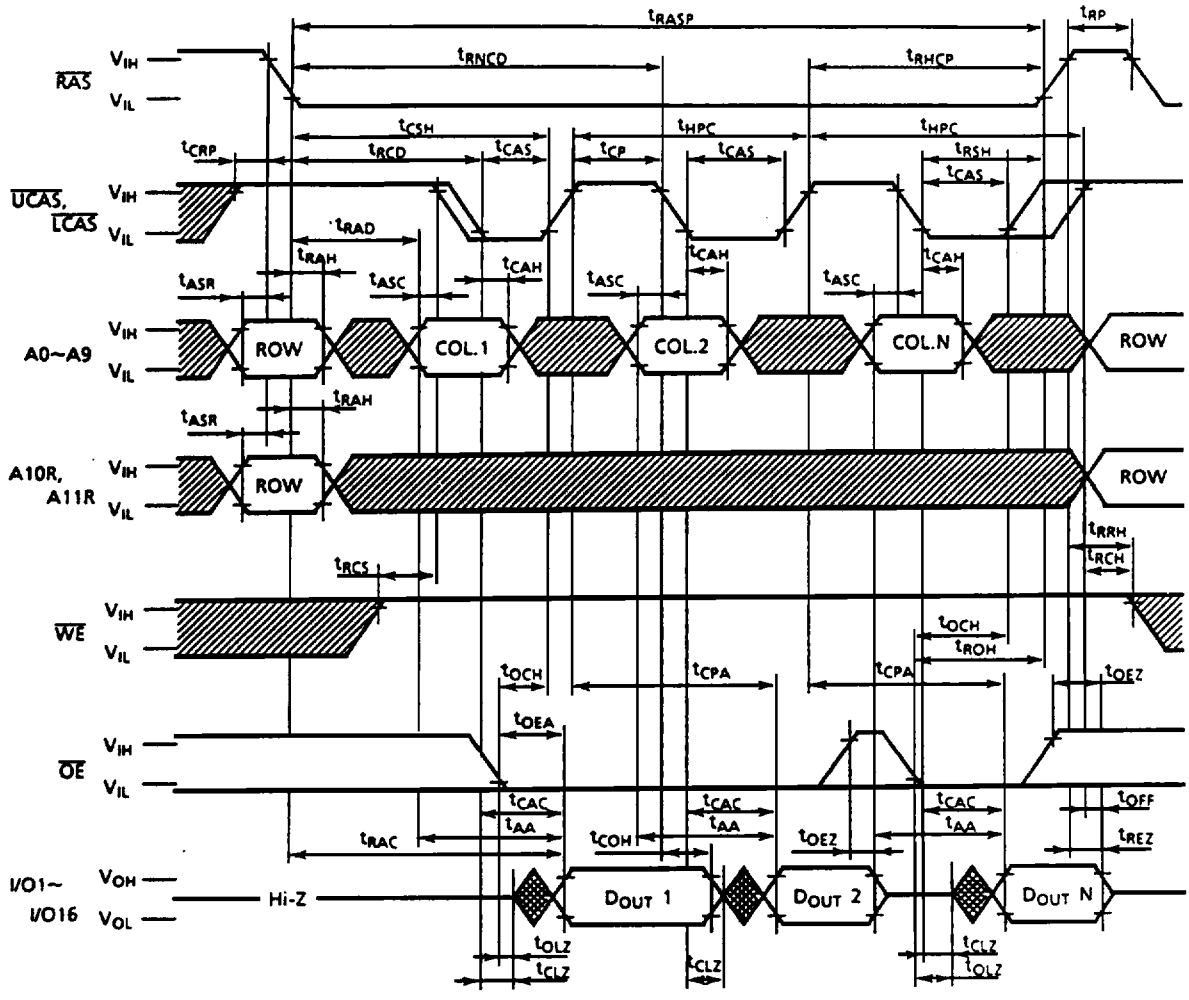


Note : D_{IN}(I/O1~I/O8) = Don't Care
D_{OUT}(I/O1~I/O8) = Hi-Z
(D_{IN}(I/O9~I/O16) = Don't Care
D_{OUT}(I/O9~I/O16) = Hi-Z)

: "H" or "L"

: Invalid Data

HYPER PAGE MODE READ CYCLE

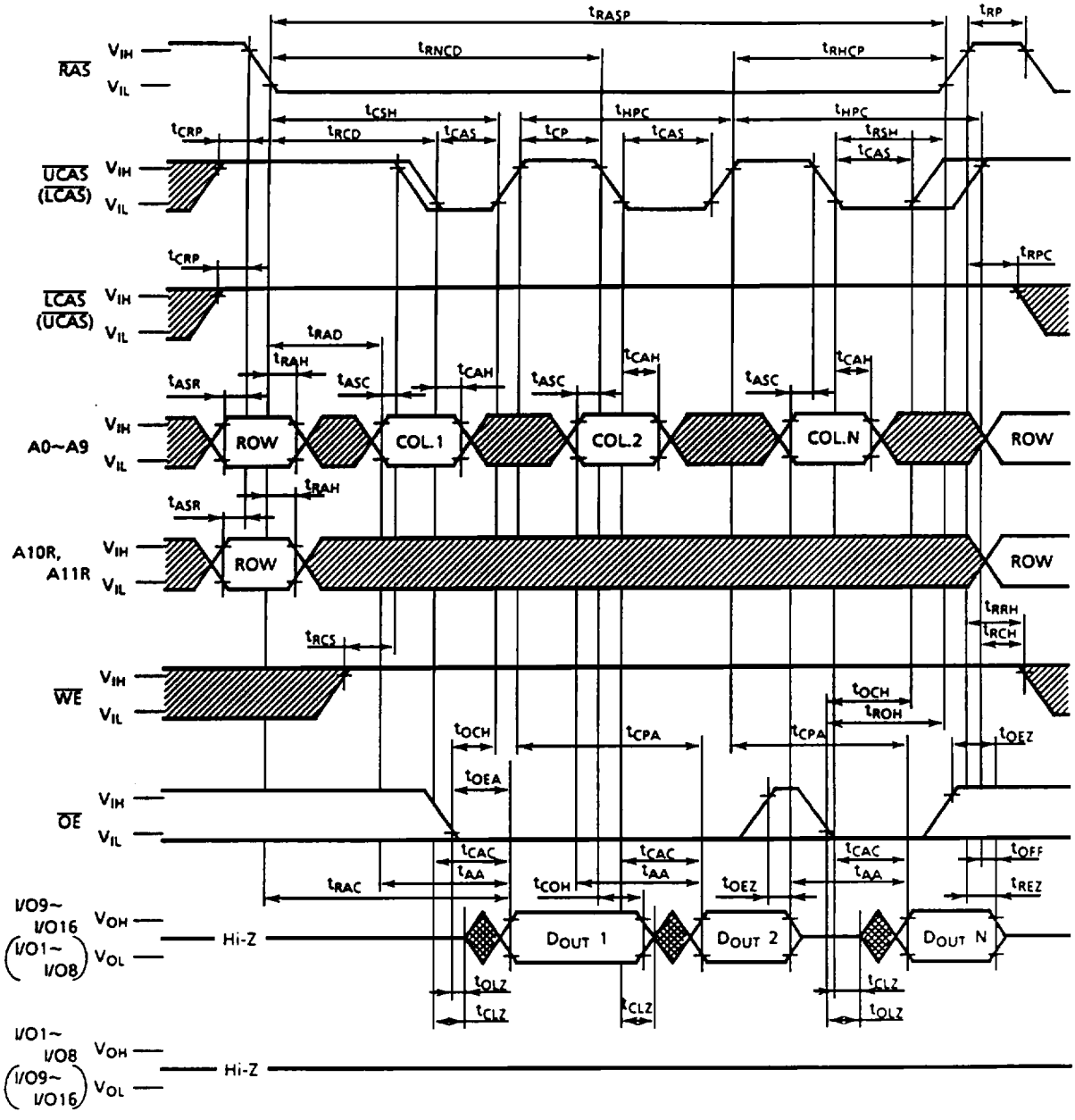


Note: D_{IN} = Hi-Z

: "H" or "L"

Invalid Data

HYPER PAGE MODE BYTE READ CYCLE

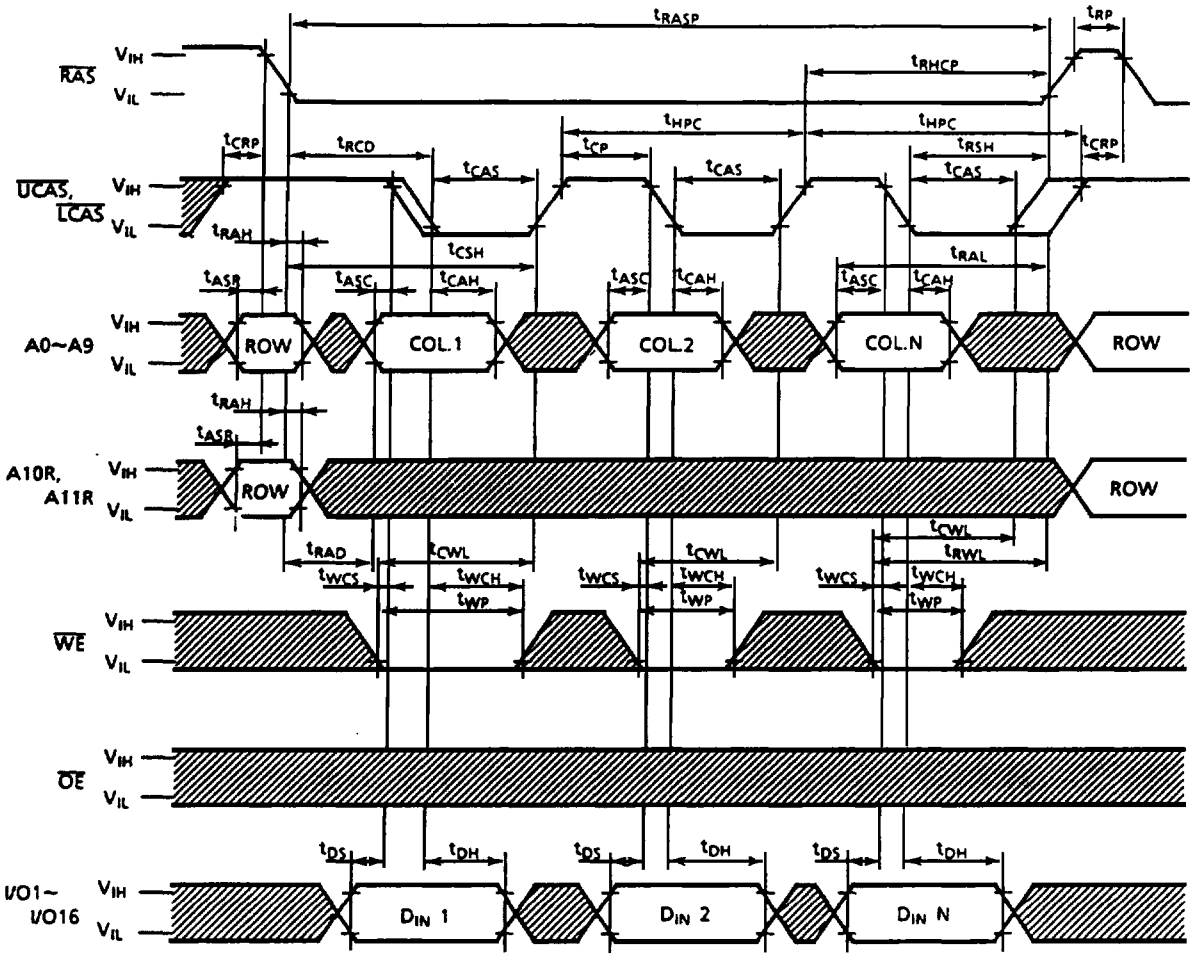


Note : D_{IN}(I/O1~I/O8) = Don't Care
D_{OUT}(I/O9~I/O16) = Hi-Z
(D_{IN}(I/O1~I/O8) = Hi-Z
D_{OUT}(I/O9~I/O16) = Don't Care)

▨ : "H" or "L"

▩ : Invalid Data

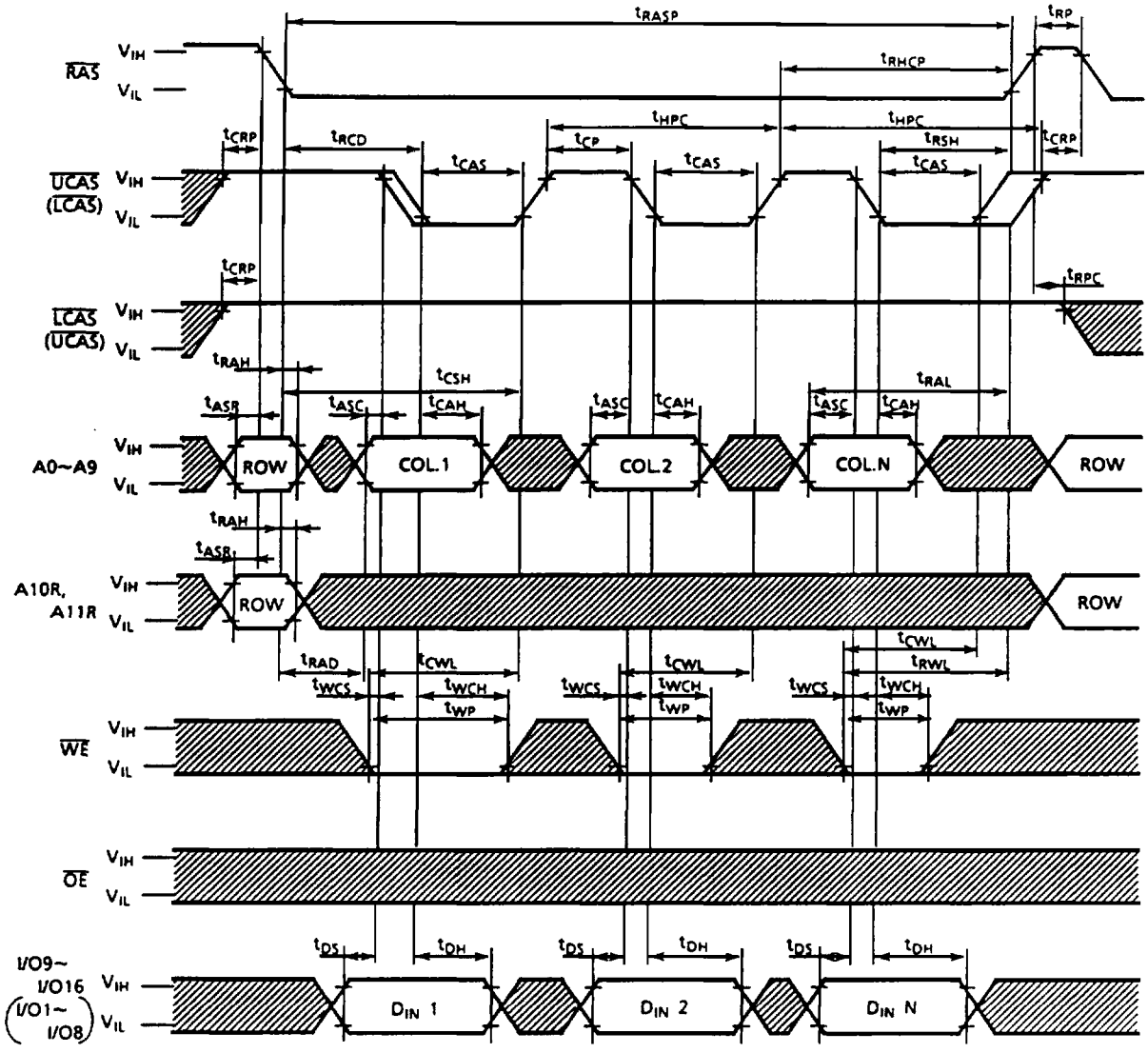
HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

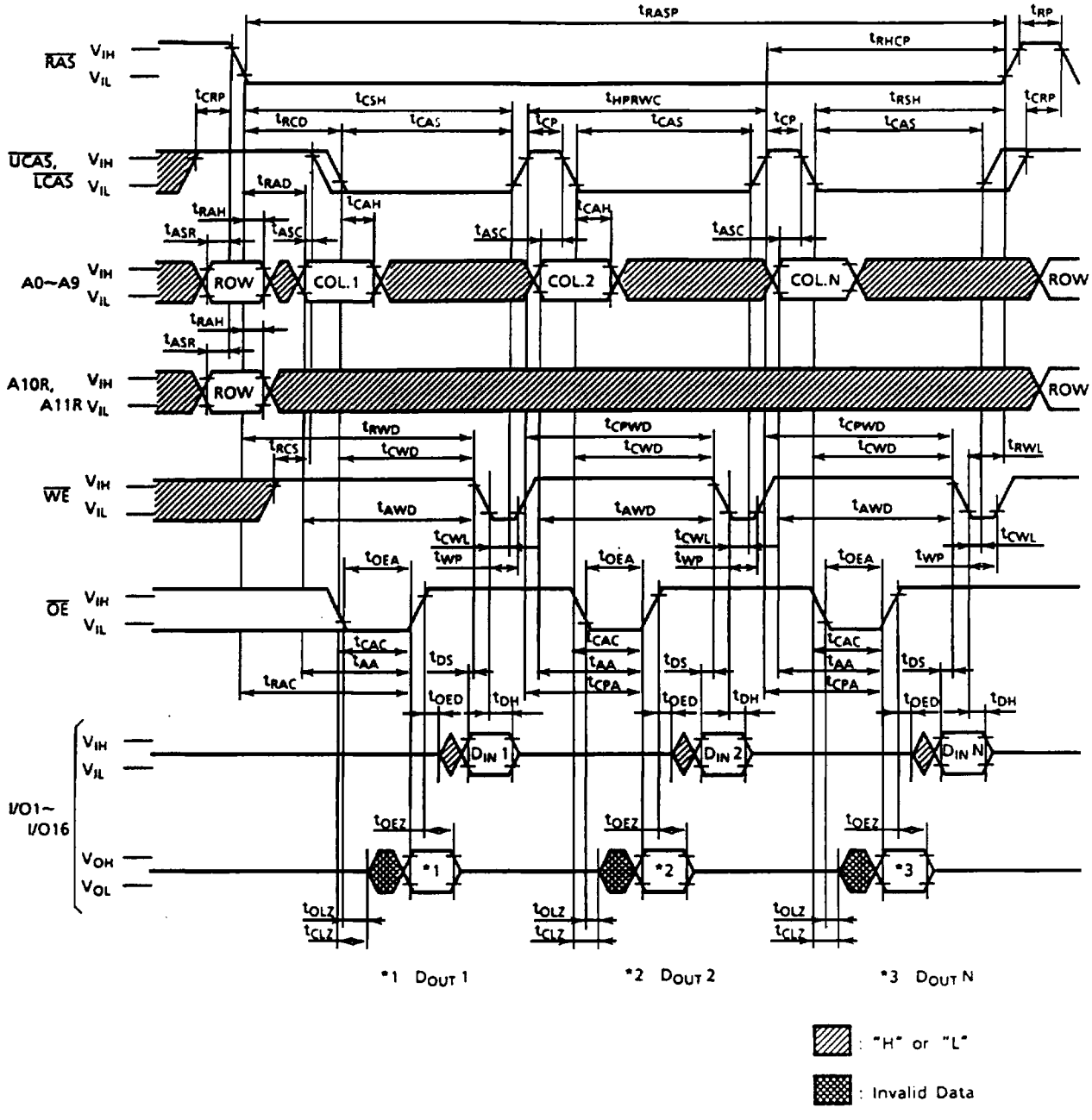
HYPER PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



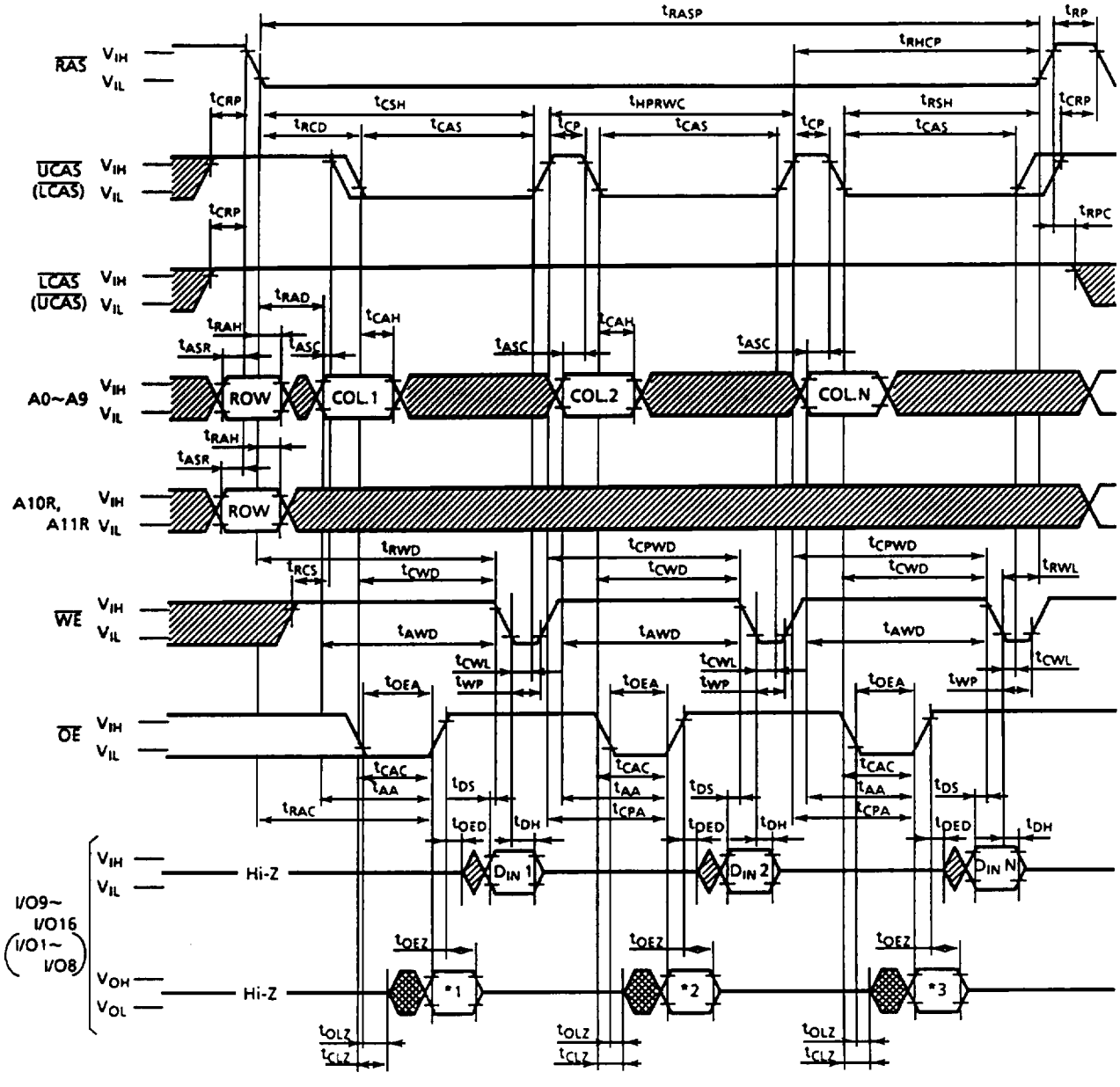
Note : D_{IN}(I/O1~I/O8) = Don't Care
(D_{IN}(I/O9~I/O16) = Don't Care)
D_{OUT} = Hi-Z

: "H" or "L"

HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE BYTE READ-MODIFY-WRITE CYCLE

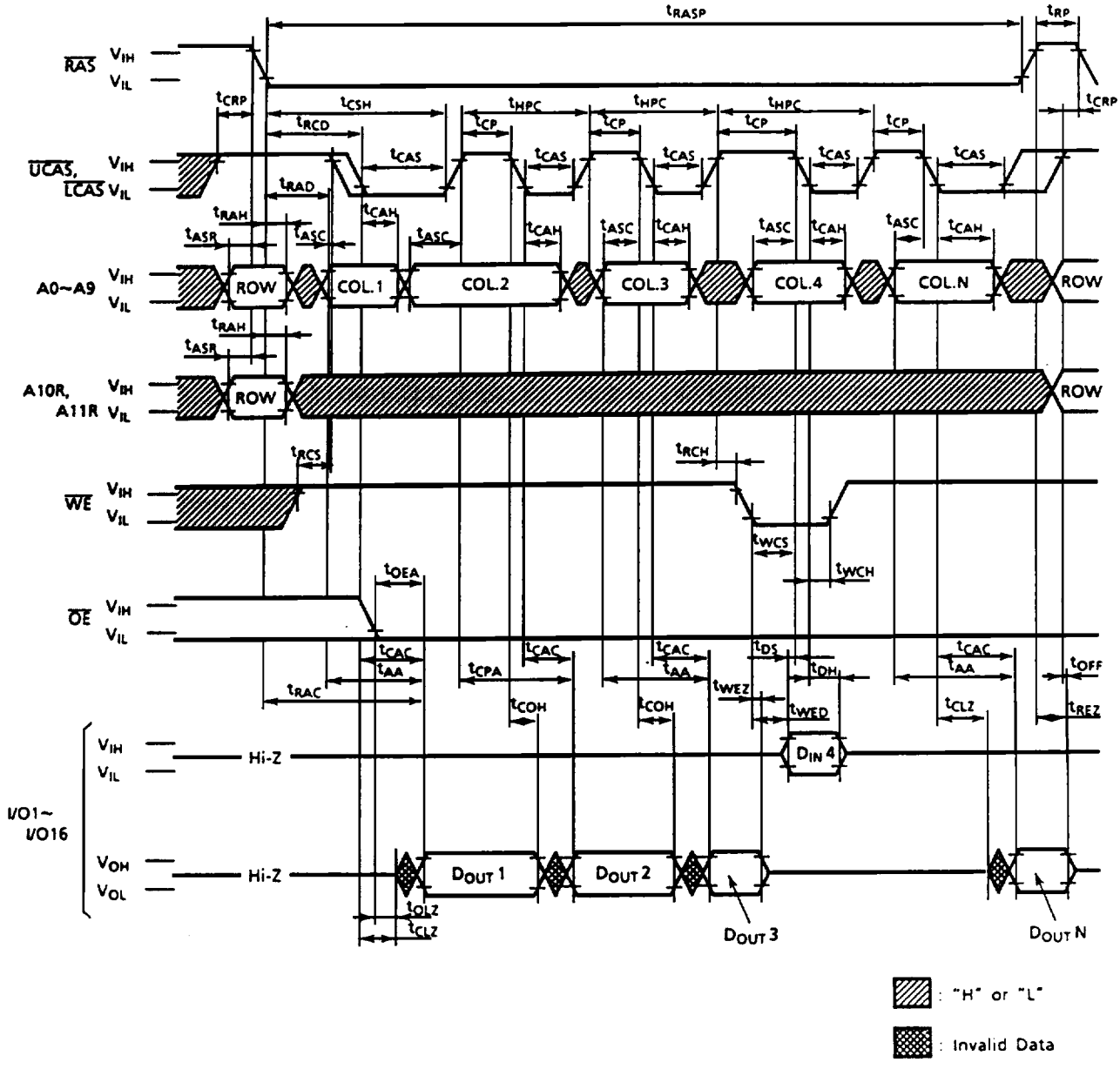


Note : D_{IN}(I/O1~I/O8) = Don't Care
D_{OUT}(I/O1~I/O8) = Hi-Z
(D_{IN}(I/O9~I/O16) = Don't Care
D_{OUT}(I/O9~I/O16) = Hi-Z)

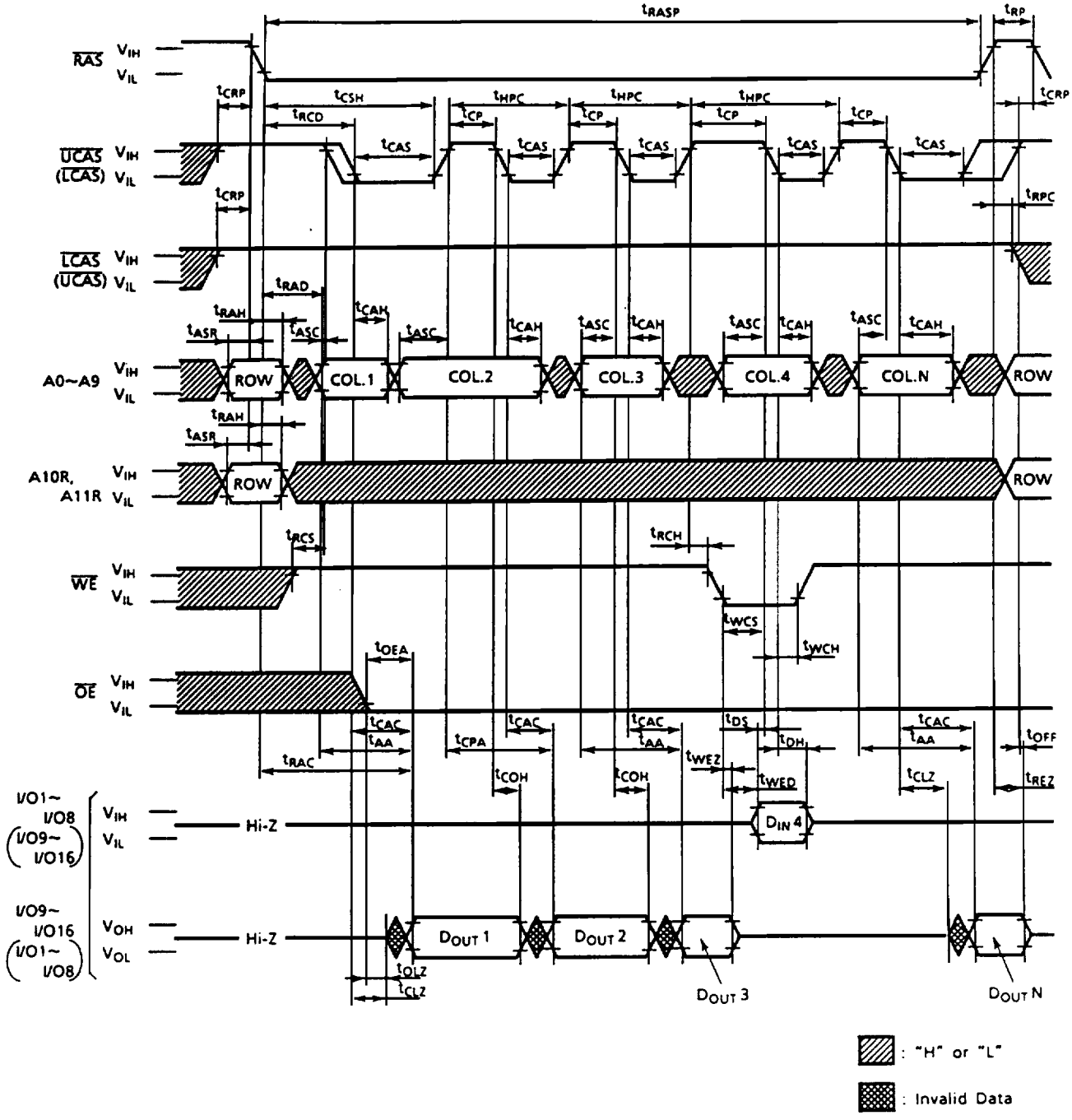
: "H" or "L"

: Invalid Data

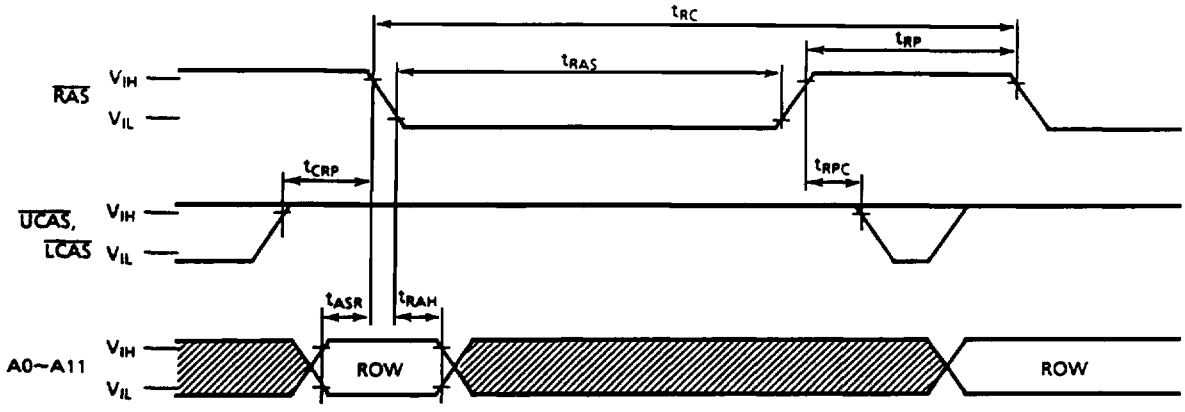
HYPER PAGE MODE READ WRITE MIXED CYCLE



HYPER PAGE MODE BYTE READ WRITE MIXED CYCLE



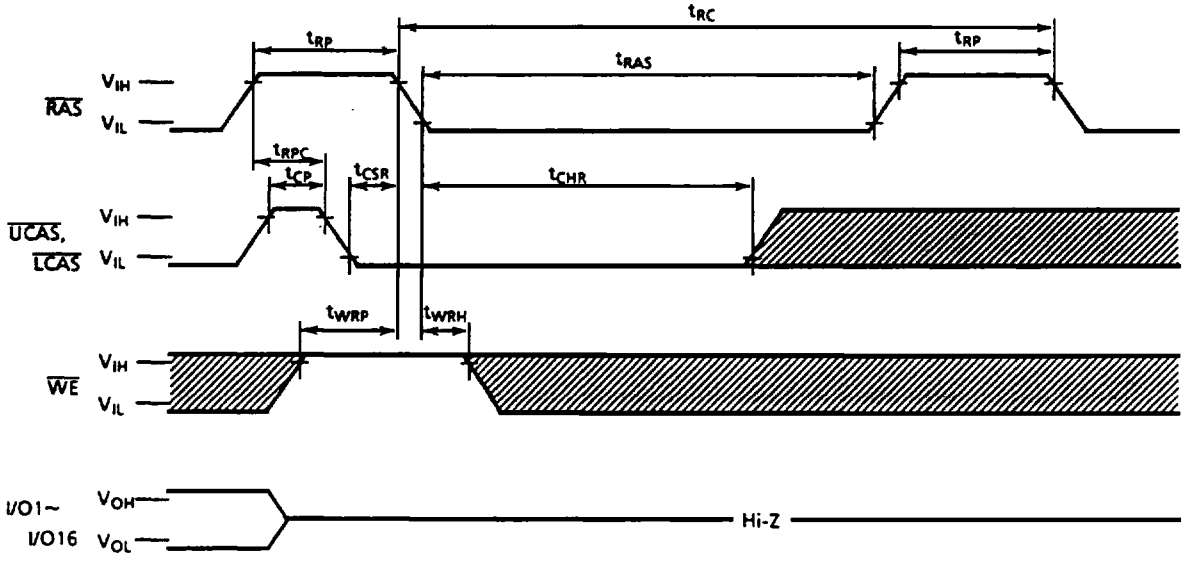
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

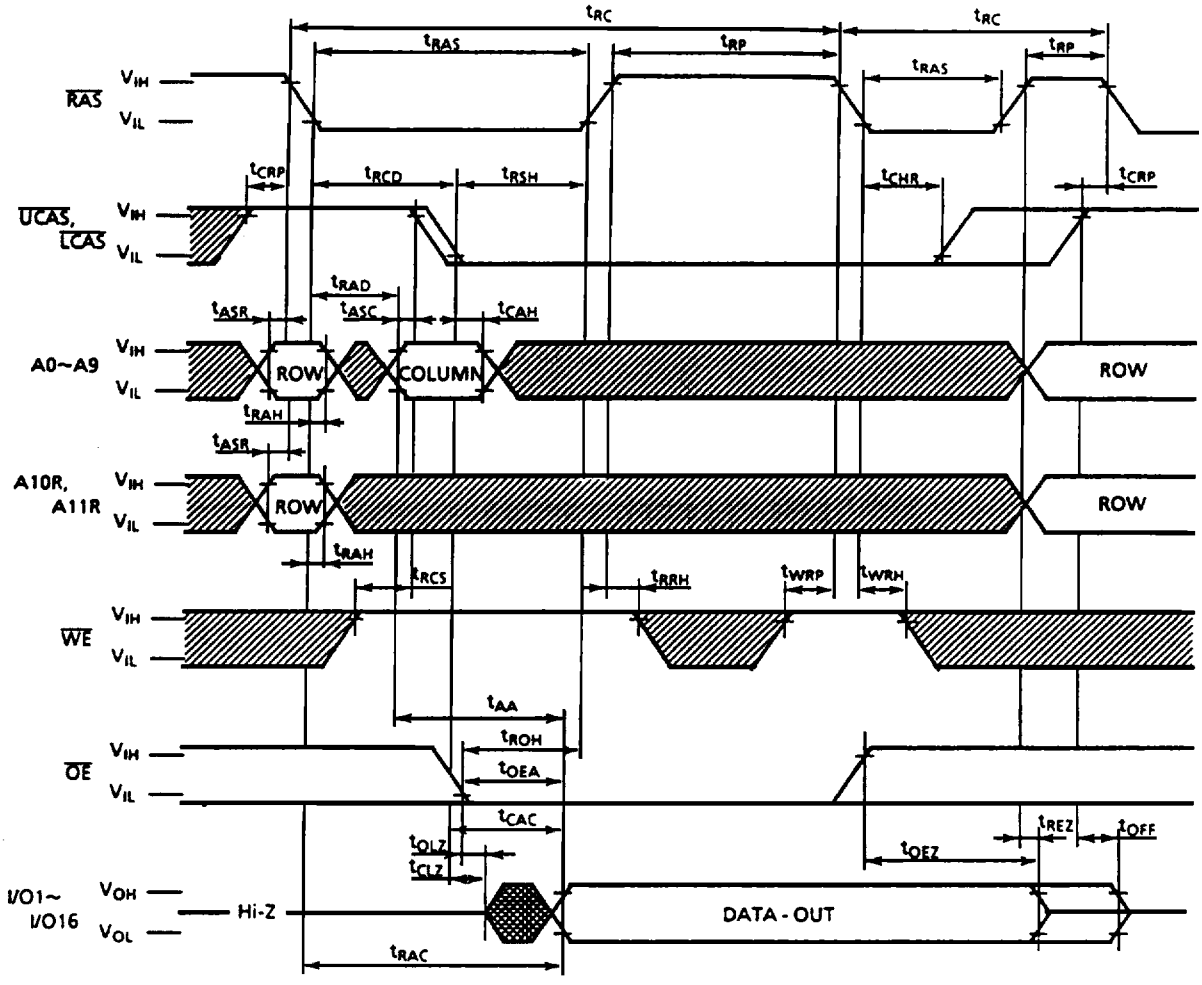
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9, A10R, A11R = "H" or "L"

▨ : "H" or "L"

HIDDEN REFRESH CYLCE (READ)

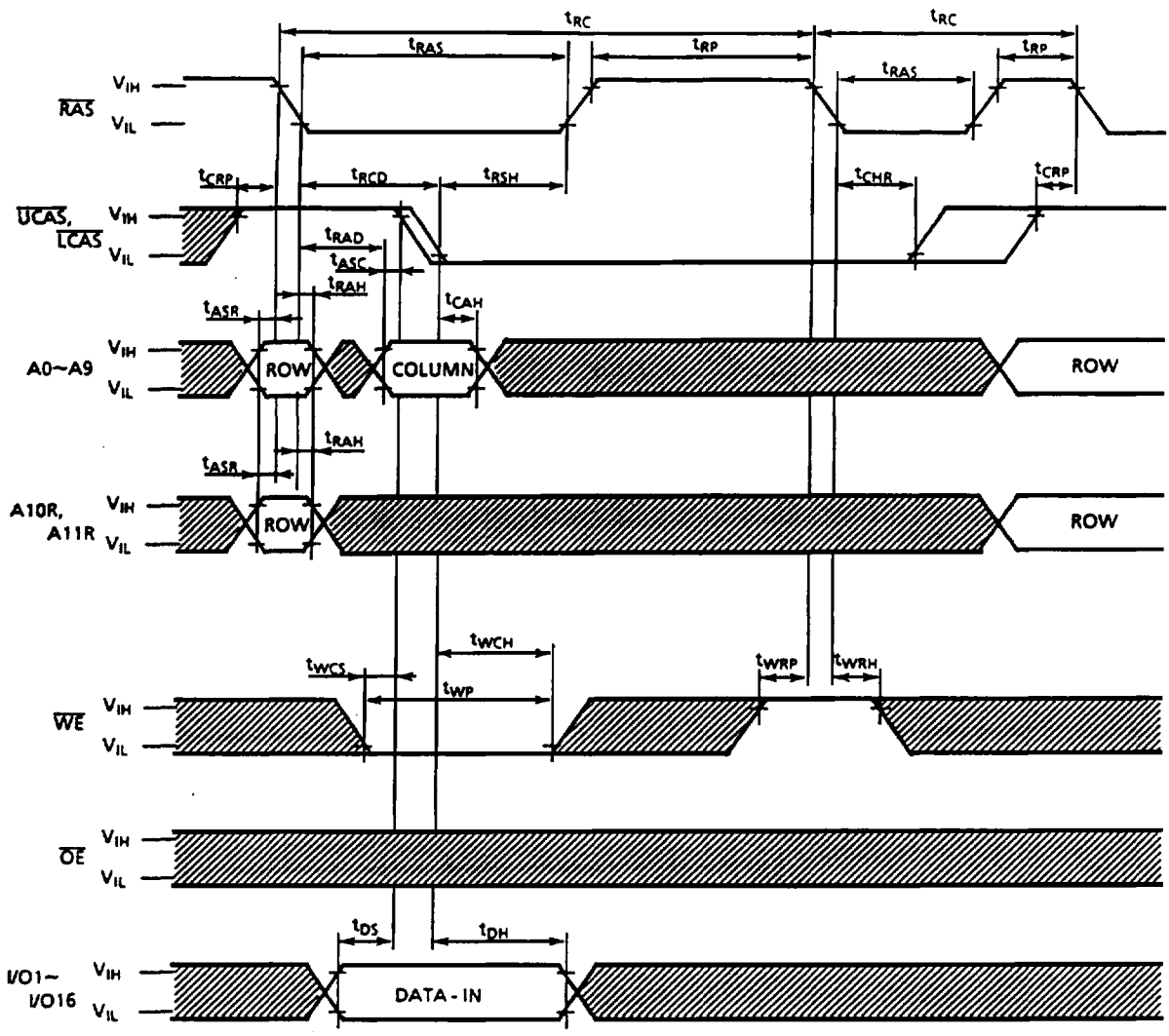


Note: D_{IN} = Hi-Z

: "H" or "L"

: Invalid Data

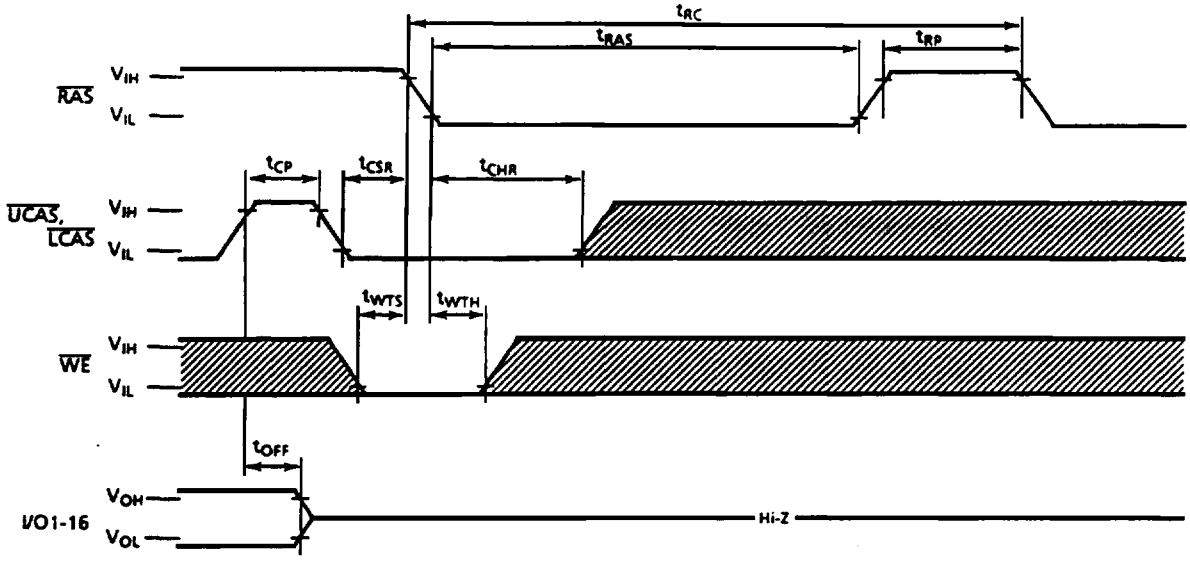
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

WE, CAS BEFORE RAS REFRESH CYCLE



Note : D_{IN}, $\overline{OE}$, A0~A9, A10R, A11R = "H" or "L"

▨ : "H" or "L"

TEST MODE

The TC5165165AJ/AFT is the RAM organized 4,194,304 words by 16 bits, it is internally organized 2,097,152 words by 32 bits. In "Test Mode", data are written into 32 sectors in parallel by using only I/O16. A9C are not used. If, upon reading, 32 bits are equal (all "1"s or "0"s), the I/O16 pin indicates a "1". If they were not equal, the I/O16 pin would indicate a "0". Other I/O pins (I/O1~I/O15) always indicate a "Hi-Z" state during test mode read cycle. Fig.1 shows the block diagram of TC5165165AJ/AFT. In "Test Mode", the 4M×16 DRAM can be tested as if it were a 2M×32 DRAM.

"$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

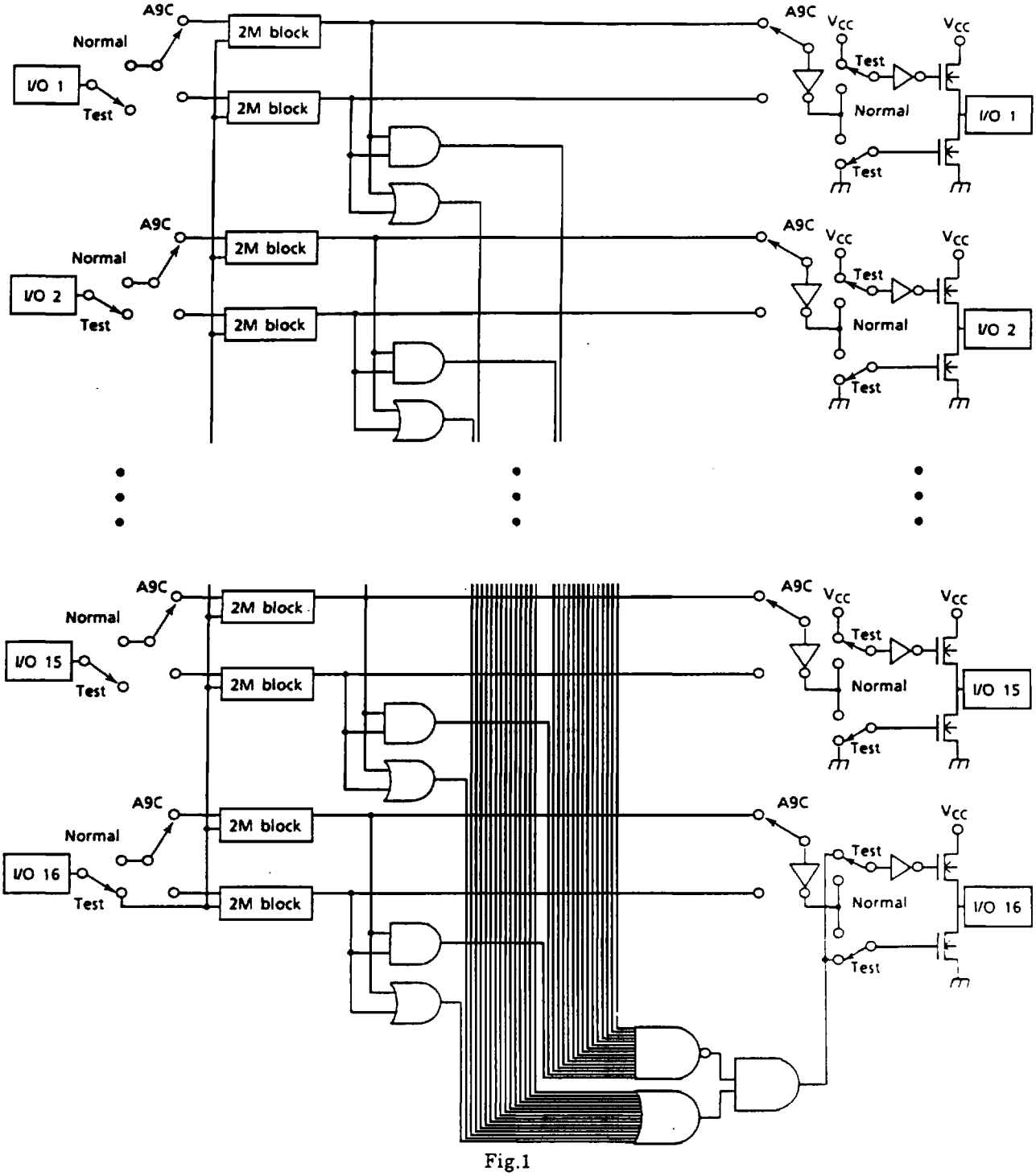
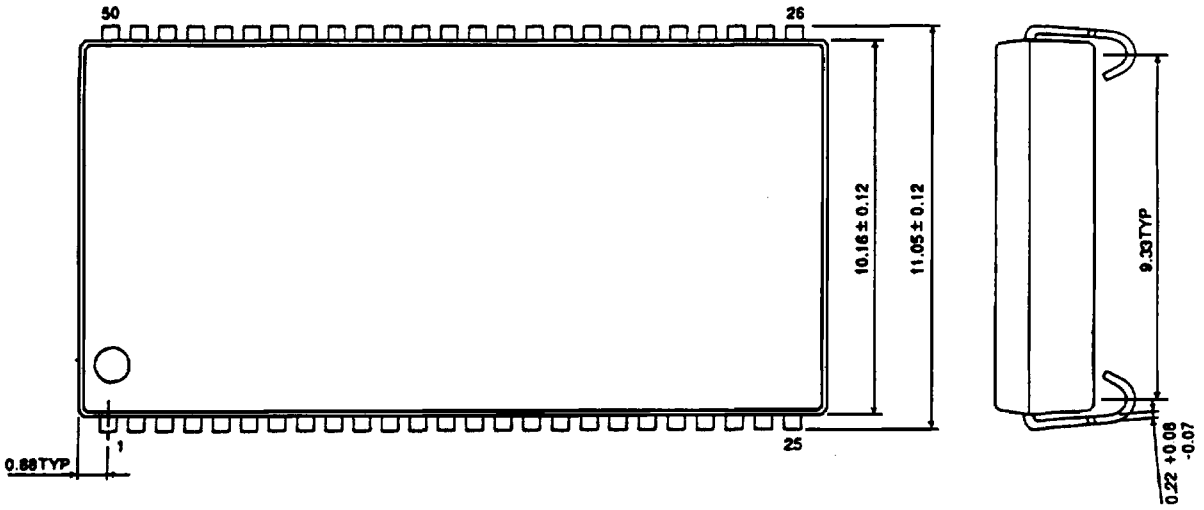
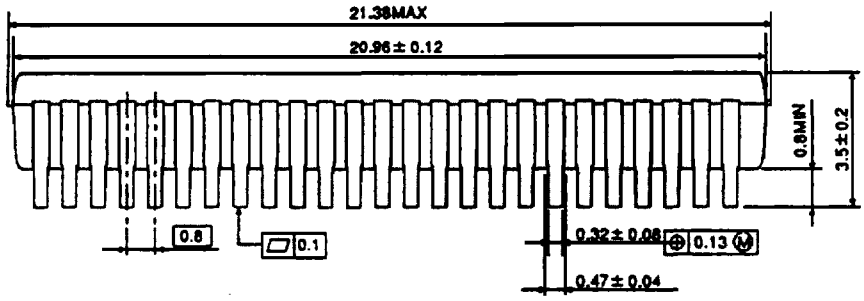


Fig.1

OUTLINE DRAWING (SOJ50 – P – 400)

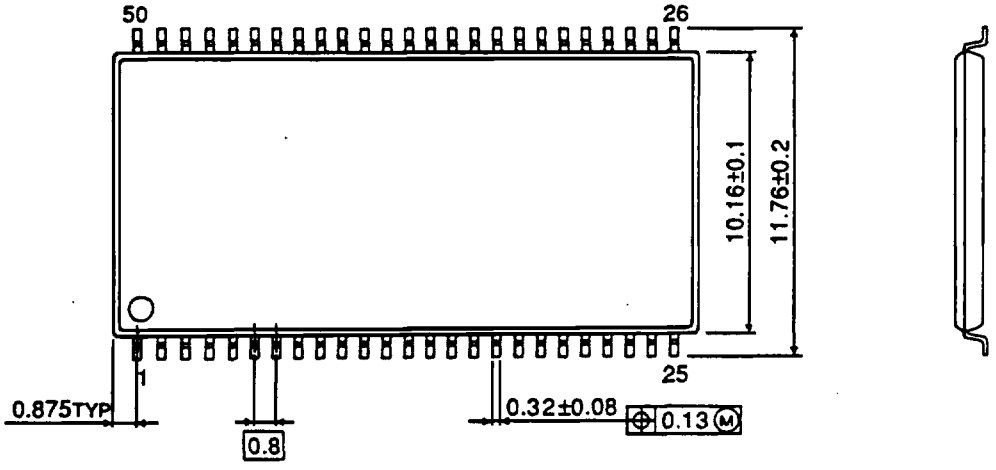
Unit in mm

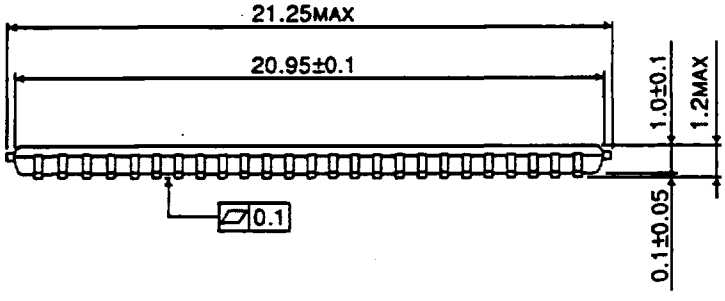


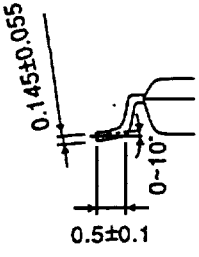


OUTLINE DRAWING (TSOP50 – P – 400D)

Unit in mm







TC5165165AJ/AFT – 35*
1996 - 06 - 01
TOSHIBA CORPORATION