2.5 GHz bi-directional I²C-bus controlled synthesizer

TSA5055T

GENERAL DESCRIPTION

The TSA5055T is a single chip PLL frequency synthesizer designed for satellite TV tuning systems. Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, program the six output ports and set the charge-pump current. Four of these ports can also be used as input ports (3 general purpose I/O ports, one A/D converter). Digital information concerning these ports can be read out of the TSA5055T on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I²C-bus address and 3 programmable addresses, programmed by applying a specific voltage to port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

FEATURES

- Complete 2.5 GHz single-chip system
- Low power 5 V, 60 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- 5-level A/D converter
- Address selection for Picture-In-Picture (PIP), DBS tuner, etc.
- 6 controllable outputs, 4 bi-directional
- Power-down flag
- Available in SOT109A package

APPLICATIONS

- Satellite TV
- High IF cable tuning systems

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.75	5	5.5	V
I_{CC}	supply current	–	60	80	mA
Δf	frequency range	1	–	2.5	GHz
$V_{I\ (RMS)}$	input voltage level (RMS value)				
	1 GHz to 1.8 GHz	50	–	300	mV
	1.8 GHz to 2.6 GHz	70	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current				
	P7, P6, P5, P4	–	–	10	mA
	output current				
	P3, P0	–	1	–	mA
T_{amb}	operating ambient temperature range	–10	–	70	°C
T_{stg}	storage temperature range	–40	–	125	°C
$R_{th\ j-a}$	thermal resistance	–	110	–	K/W

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5055T	16	SO	plastic	SOT109A

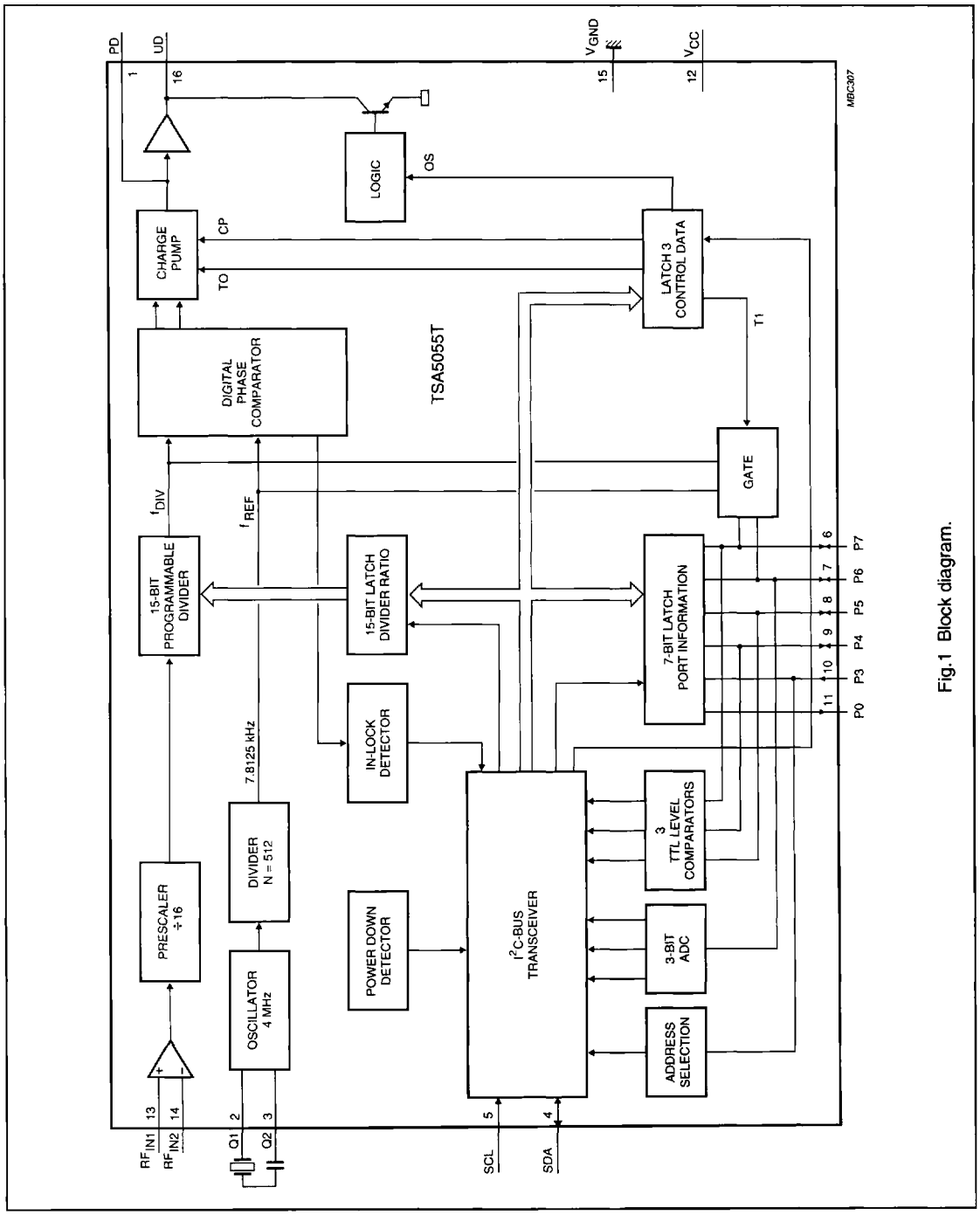


Fig.1 Block diagram.

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	6	V
V_{P1}	charge-pump output voltage	−0.3	V_{CC}	V
V_{P2}	crystal (Q1) input voltage	−0.3	V_{CC}	V
V_{P4}	serial data input/output	−0.3	6	V
V_{P5}	serial clock input	−0.3	6	V
V_{P6}	input/output ports P7 - P0	−3	16	V
V_{P13}	prescaler inputs	−0.3	2.5	V
V_{P16}	drive output	−0.3	V_{CC}	V
I_{6L}	output ports P7 - P4 (open collector)	−1	15	mA
I_{4L}	SDA output (open collector)	−1	5	mA
T_{stg}	storage temperature range	−40	125	°C
T_j	junction temperature	−	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	110 K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C, category A (1000 V).

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

PINNING

SYMBOL	PIN	DESCRIPTION
PD	1	charge-pump output
Q1	2	crystal oscillator input 1
Q2	3	crystal oscillator input 2
SDA	4	serial data input/output
SCL	5	serial clock input
P7	6	port output/input (general purpose)
P6	7	port output/input (A/D converter)
P5	8	port output/input (general purpose)
P4	9	port output/input (general purpose)
P3	10	port output/input (address selection)
P0	11	port output
V_{CC}	12	voltage supply
RF_{IN1}	13	UHF/VHF signal input 1
RF_{IN2}	14	UHF/VHF signal input 2 (decoupled)
GND	15	ground
UD	16	drive output

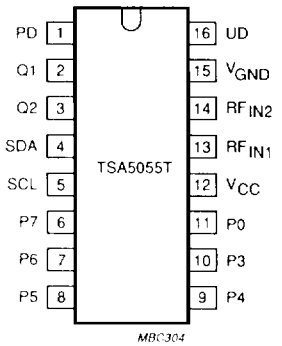


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TSA5055T is controlled via the two-wire I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode :
R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5055T. The bus transceiver has an auto-increment facility that permits the programming of the TSA5055T within one single transmission (address + 4 data bytes).

The TSA5055T can also be partly programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning. At power-on, the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of the UHF/VHF signal is first divided by 16, the step size is 125 kHz. A 3.2 MHz crystal can offer a step size of 100 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	X	X	P0	A	byte 5

MA1, MA0 programmable address bits (see Table 4)

A acknowledge bit

N14 to N0 programmable divider bits

$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 µA

CP = 1 220 µA

P7 - P4 = 1 open-collector outputs are active

P7 - P0 = 0 outputs are in high impedance state

P3 - P0 = 1 current-limited outputs are active

T1, T0, OS = 0 0 0 normal operation

T1 = 1 P6 = f_{ref}, P7 = f_{Div}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

X don't care.

READ mode :

R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5055T by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5055T generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5055T if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.The TSA5055T will then release the data line to allow the processor to generate a STOP condition. When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.

The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5055T (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL, which indicates (FL = 1) when the loop is phase-locked.

The I2, I1 and I0 bits represent the status of the I/O ports P7, P5 and P4 respectively. A logic '0' indicates a low level and a logic '1' a high level (TTL levels). A built-in 5-level A/D converter is available at I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television, as shown in Fig. 3. The relationship between bits A2, A1, A0 and the input voltage at port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I1	I1	I0	A2	A1	A0	–	byte 2

POR power-on-reset flag. (POR = 1 on power-on)

FL in-lock flag (FL = 1 when the loop is phase-locked).

I2, I1, I0 digital information for I/O ports P7, P5 and P4 respectively

A2, A1, A0 digital outputs of the 5-level A/D converter. Accuracy is ½ LSB (see Table 3).

MSB is transmitted first.

Address selection (see Table 4)

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having several synthesizers (up to 3) in one system. The relationship between MA1 and MA0 and the input voltage at port P3 is given in Table 4.

Table 3 A/D converter levels

Voltage applied on port P6	A2	A1	A0
0.6 V_{CC} to V_{CC}	1	0	0
0.45 V_{CC} to 0.6 $_{CC}$	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V_{CC}	0	0	0

Table 4 Address selection

MA1	MA0	Voltage applied on port P3
0	0	0 to 0.1 V_{CC}
0	1	open
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

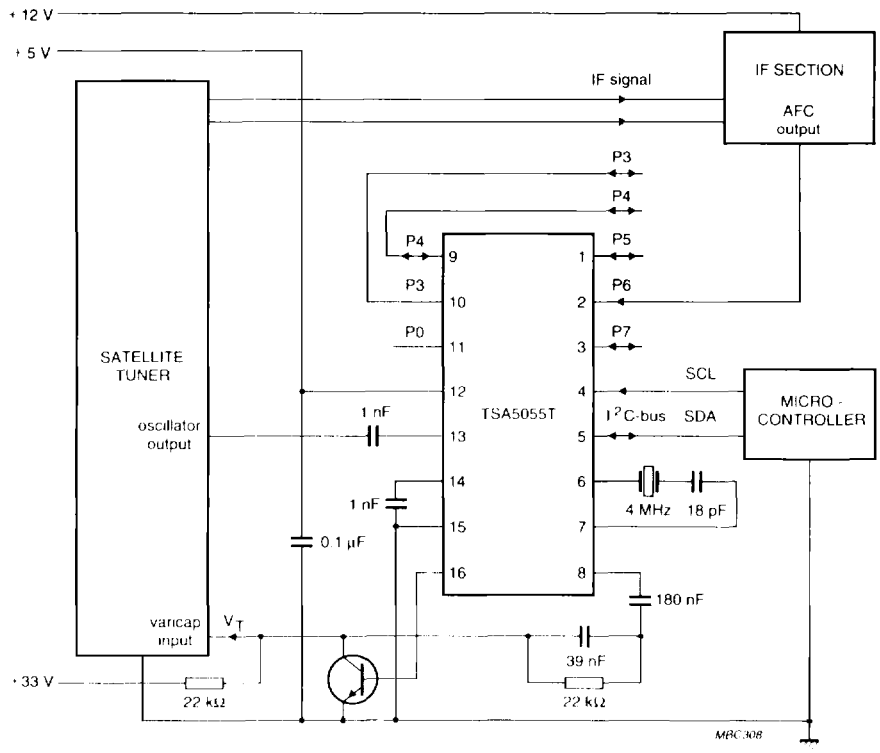


Fig.3 Typical application diagram.

CHARACTERISTICS

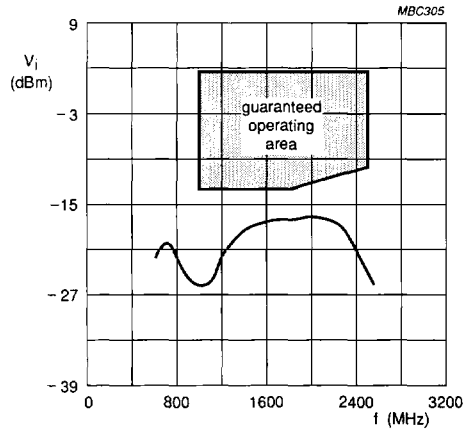
V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range		4.75	–	5.5	V
T_{amb}	operating ambient temperature range		−10	–	70	°C
f_{RF}	RF input frequency range		1	–	2.5	GHz
N	divider		256	–	32767	
I_{CC}	supply current		–	60	80	mA
f_{XTAL}	crystal oscillator frequency		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		−480	−400	−320	Ω
$V_{I\ (RMS)}$	input voltage level (RMS value) f = 1 to 1.8 GHz f = 1.8 to 2.5 GHz	V_{CC} = 4.75 to 5.5 V; T_{amb} = −10 to 70 °C see typical sensitivity curve in Fig. 4	 50/−13 70/−10	 – –	 300/2.6 300/2.6	 mV mV
R_I	prescaler input impedance	see Smith chart in Fig. 5	–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports P3, P0 (current limited)						
I_{LO}	leakage current	V_{10H} = 13.5 V	–	–	10	µA
I_{OS}	output sink current	V_{10} = 13.5 V	0.7	1	1.5	mA
Output ports P7 to P4 (open collector) (see note 1)						
I_{LO}	leakage current	V_{6H} = 13.5 V	–	–	10	µA
V_{OL}	output voltage LOW	I_{6L} = 10 mA note 2	–	–	0.7	V
Input ports P6, P3						
I_{IH}	input current HIGH	V_{7H} = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_{7L} = 0	−10	–	–	µA
Input ports P7, P5, P4						
V_{IH}	input voltage HIGH		2.7	–	–	V
V_{IL}	input voltage LOW		–	–	0.8	V
I_{IH}	input current HIGH	V_{6H} = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_{6L} = 0	−10	–	–	µA
Bus inputs SCL, SDA						
V_{IH}	input voltage HIGH		3	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_{5H} = 5 V; V_{CC} = 0	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bus inputs SCL, SDA						
I_{IL}	input current LOW	V_{5H} = 5 V; V_{CC} = 5 V	–	–	10	µA
		V_{5L} = 0; V_{CC} = 0	−10	–	–	µA
		V_{5L} = 0; V_{CC} = 5 V	−10	–	–	µA
Output SDA (open collector)						
I_{4H}	leakage current	V_{4H} = 5.5 V	–	–	10	µA
V_{4L}	output voltage	I_{4L} = 3 mA	–	–	0.4	V
Charge-pump output PD						
I_{OH}	output current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{OL}	output current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1leak}	off-state leakage current	T0 = 1	−5	–	5	nA
Operational amplifier output UD (test mode: T0 = 1)						
V_{16}	output voltage	V_{IL} = 0	–	–	100	mV
	output voltage when switched off	T0 = 1; OS = 1; V_{IL} = 2 V	–	–	250	mV
h_{FE}	operational amplifier current gain $I_{16}/(I_1 - I_{1leak})$	T0 = 1; OS = 0; V_{IL} = 2 V; I_{16} = 10 µA	2000	–	–	

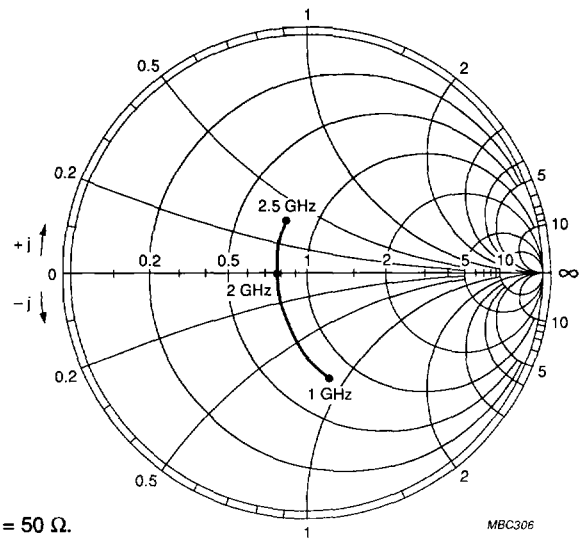
Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open collector active.



V_{CC} = 5 V; T_{amb} = 25 °C.

Fig.4 Prescaler typical input sensitivity curve.



V_{CC} = 5 V; reference value = 50 Ω.

Fig.5 Prescaler Smith chart of typical input impedance.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

where:

K_{VCO} = oscillator slope (Hz/V)

I_{CP} = charge-pump current (A)

K_O = 4×10^6

C1 and C2 = loop filter capacitors.

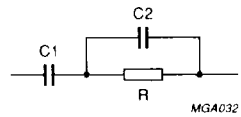


Fig.6 Loop filter.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	µs
Time span between the loop losing lock and FL-flag resetting	0	128	µs

FLOCK FLAG APPLICATION

- K_{VCO} = 50 MHz/V (UHF band)
- I_{CP} = 220 µA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ±85.8 kHz.