3-Channel, Isolated, Sigma-Delta ADC with SPI

Data Sheet

ADE7912/ADE7913

FEATURES

- Two (ADE7912) or three (ADE7913) 24-bit isolated, Σ-Δ analog-to-digital converters (simultaneously sampling ADCs)
- Integrated *iso*Power, isolated dc-to-dc converter
- On-chip temperature sensor
- 4-wire SPI serial interface
- Up to 4 ADE7912/ADE7913 devices clocked from a single crystal or an external clock
- Synchronization of multiple ADE7912/ADE7913 devices
- ±31.25 mV peak input range for current channel
- ±500 mV peak input range for voltage channels
- Reference drift: 10 ppm/°C typical
- Single 3.3 V supply
- 20-lead, wide-body SOIC package with 8.3 mm creepage
- Operating temperature: −40°C to +85°C
- Safety and regulatory approvals (pending)
  - UL recognition
    - 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
    - IEC 61010-1: 400 V rms
  - VDE certificate of conformity
    - DIN VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 846 V peak

APPLICATIONS

- Shunt-based polyphase meters
- Power quality monitoring
- Solar inverters
- Process monitoring
- Protective devices
- Isolated sensor interfaces
- Industrial PLCs

TYPICAL APPLICATIONS CIRCUIT

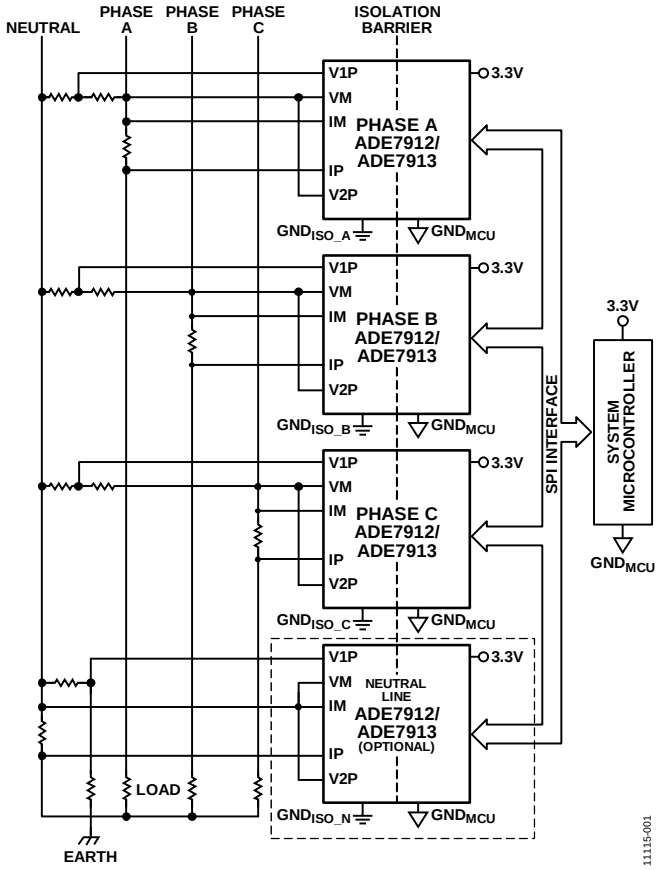

Figure 1.

GENERAL DESCRIPTION

The ADE7912/ADE7913[1] are isolated, 3-channel Σ-Δ ADCs for polyphase energy metering applications using shunt current sensors. Data and power isolation are based on the Analog Devices, Inc., *i*Coupler® technology. The ADE7912 features two 24-bit ADCs, and the ADE7913 features three ADCs. The current ADC provides a 67 dB signal-to-noise ratio over a 3 kHz signal bandwidth, whereas the voltage ADCs provide a SNR of 72 dB over the same bandwidth. One channel is dedicated to measuring the voltage across a shunt when the shunt is used for current sensing. Up to two additional channels are dedicated to measuring voltages, which are usually sensed using resistor dividers. One voltage channel can be used to measure the temperature of the die via an internal sensor. The ADE7913 includes three channels: one current and two voltage channels. The ADE7912 has one voltage channel but is otherwise identical to the ADE7913.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329; 6,262,600; 7,489,526; 7,558,080. Other patents are pending.

Rev. 0 Document Feedback

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REVISION HISTORY

11/13—Revision 0: Initial Version

The ADE7912/ADE7913 include *iso*Power®, an integrated, isolated dc-to-dc converter. Based on the Analog Devices *i*Coupler technology, the dc-to-dc converter provides the regulated power required by the first stage of the ADCs at a 3.3 V input supply. *iso*Power eliminates the need for an external dc-to-dc isolation block. The *i*Coupler chip scale transformer technology is also used to isolate the logic signals between the first and second stages of the ADC. The result is a small form factor, total isolation solution.

The ADE7912/ADE7913 configuration and status registers are accessed via a bidirectional SPI serial port for easy interfacing with microcontrollers.

The ADE7912/ADE7913 can be clocked from a crystal or an external clock signal. To minimize the system bill of materials, the master ADE7912/ADE7913 can drive the clocks of up to three additional ADE7912/ADE7913 devices.

Multiple ADE7912/ADE7913 devices can be synchronized to sample at the same moment and provide coherent outputs.

The ADE7912/ADE7913 are available in a 20-lead, Pb-free, wide-body SOIC package with 8.3 mm creepage.

FUNCTIONAL BLOCK DIAGRAMS

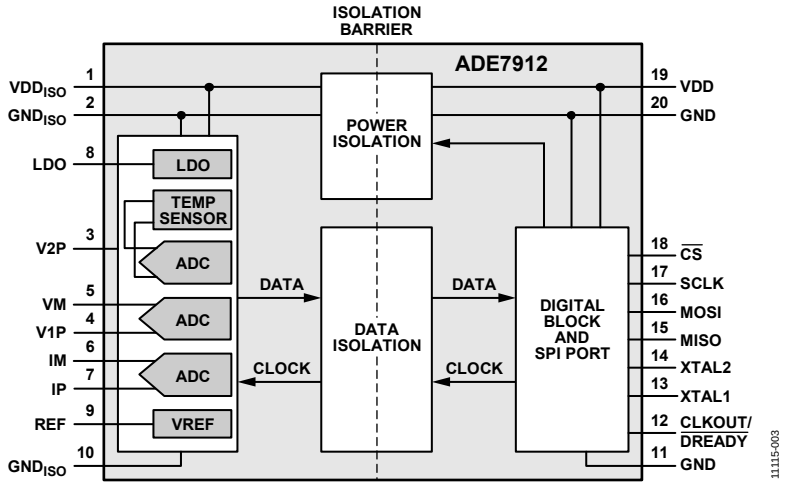


Figure 2. ADE7912 Functional Block Diagram

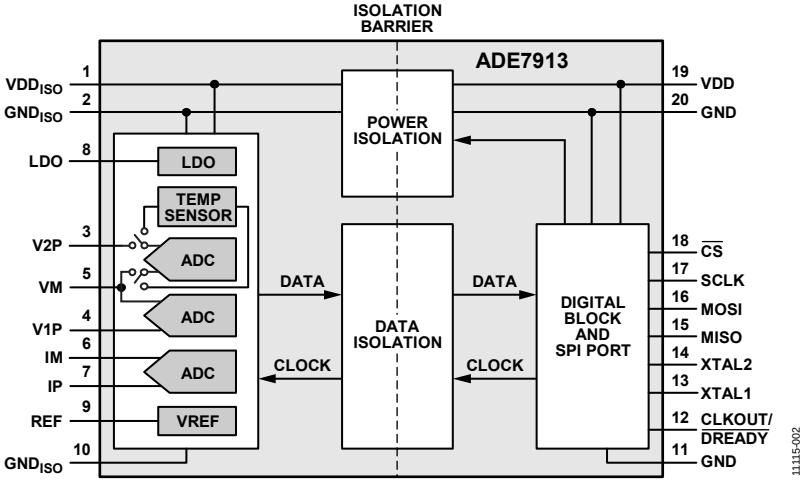


Figure 3. ADE7913 Functional Block Diagram

SPECIFICATIONS

VDD = 3.3 V ± 10%, GND = 0 V, on-chip reference, XTAL1 = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_A = 25°C (typical).

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS[1]					
Pseudo Differential Signal Voltage Range Between IP and IM Pins	−31.25		+31.25	mV peak	IM pin connected to GND_{ISO}
Pseudo Differential Signal Voltage Range Between V1P and VM Pins and Between V2P and VM Pins	−500		+500	mV peak	Pseudo differential inputs between V1P and VM pins and between V2P and VM pins; VM pin connected to GND_{ISO}
Maximum VM and IM Voltage	−25		+25	mV	
Crosstalk		−90		dB	IP and IM inputs set to 0 V (GND_{ISO}) when V1P and V2P inputs at full scale
		−105		dB	V2P and VM inputs set to 0 V (GND_{ISO}) when IP and V1P inputs at full scale; V1P and VM inputs set to 0 V (GND_{ISO}) when IP and V2P inputs at full scale
Input Impedance to GND_{ISO} (DC)					
IP, IM, V1P, and V2P Pins	480			kΩ	
VM Pin	240			kΩ	
Current Channel ADC Offset Error		−2		mV	
Voltage Channels ADC Offset Error		−35		mV	V2 channel applies to the ADE7913 only
ADC Offset Drift over Temperature	−500		+500	ppm/°C	V1 channel only
Gain Error	−4		+4	%	
Gain Drift over Temperature	−135		+135	ppm/°C	Current channel
	−65		+65	ppm/°C	V1 and V2 channels
AC Power Supply Rejection, PSR		−90		dB	V_{DD} = 3.3 V + 120 mV rms (50 Hz/100 Hz), IP = V1P = V2P = GND_{ISO}
DC Power Supply Rejection, PSR		−80		dB	V_{DD} = 3.3 V ± 330 mV dc, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
TEMPERATURE SENSOR					
Accuracy		±5		°C	
WAVEFORM SAMPLING—CURRENT CHANNEL[1]					
Signal-to-Noise Ratio, SNR		67		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		68		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		72		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		74		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Signal-to-Noise-and-Distortion Ratio, SINAD		66		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		68		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		72		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		73		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Total Harmonic Distortion, THD		−79		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		−78		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		−82		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		−82		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Spurious-Free Dynamic Range, SFDR		83		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		83		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		85		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		85		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
VOLTAGE CHANNELS[1]					
Signal-to-Noise Ratio, SNR		72		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		74		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		77		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		79		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Signal-to-Noise-and-Distortion Ratio, SINAD		72		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		74		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		77		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		78		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Total Harmonic Distortion, THD		−83		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		−83		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		−85		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		−85		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Spurious-Free Dynamic Range, SFDR		86		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		86		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		87		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		87		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
CLKIN[2]					All specifications for CLKIN = 4.096 MHz
Input Clock Frequency, CLKIN	3.6	4.096	4.21	MHz	
CLKIN Duty Cycle	45	50	55	%	
XTAL1 Logic Inputs					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
XTAL1 Total Capacitance[3]		40		pF	
XTAL2 Total Capacitance[3]		40		pF	
CLKOUT Delay from XTAL1[4]			100	ns	
LOGIC INPUTS—MOSI, SCLK, $\overline{CS}$					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}			15	nA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—CLKOUT/$\overline{DREADY}$ AND MISO					
Output High Voltage, V_{OH}	2.5			V	I_{SOURCE} = 800 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
POWER SUPPLY					For specified performance
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		12.5	19	mA	Bit 2 (PWRDWN_EN) in CONFIG register cleared to 0
		2.7	3	mA	Bit 2 (PWRDWN_EN) in CONFIG register set to 1
		50		µA	Bit 2 (PWRDWN_EN) in CONFIG register set to 1 and no CLKIN signal at XTAL1 pin

[1] See the Terminology section for a definition of the parameters.
[2] CLKIN is the internal clock of the ADE7912/ADE7913. It is the frequency at which the part is clocked at the XTAL1 pin.
[3] XTAL1/XTAL2 total capacitances refer to the net capacitances on each pin. Each capacitance is the sum of the parasitic capacitance at the pin and the capacitance of the ceramic capacitor connected between the pin and GND. See the ADE7912/ADE7913 Clock section for more details.
[4] CLKOUT delay from XTAL1 is the delay that occurs from a high to low transition at the XTAL1 pin to a synchronous high to low transition at the CLKOUT/$\overline{DREADY}$ pin when CLKOUT functionality is enabled.

REGULATORY APPROVALS (PENDING)

The ADE7912/ADE7913 are pending approval by the organizations listed in Table 2. Refer to Table 8 and the Insulation Lifetime section for more information about the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 2. Regulatory Approvals

UL	CSA	VDE
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN VDE V 0884-10[2] (VDE V 0884-10):2006-12
Single Protection, 5000 V rms Isolation Voltage	Basic insulation per IEC 61010-1, 400 V rms (564 V peak) maximum working voltage	Reinforced insulation, 846 V peak

[1] In accordance with UL 1577, each ADE7912/ADE7913 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADE7912/ADE7913 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 3. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.3	mm	Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PCB layout
Minimum External Tracking (Creepage)	L(I02)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	IEC 60112
Isolation Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

The ADE7912/ADE7913 are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits.

Table 4. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	846	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A		$V_{pd(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1273	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

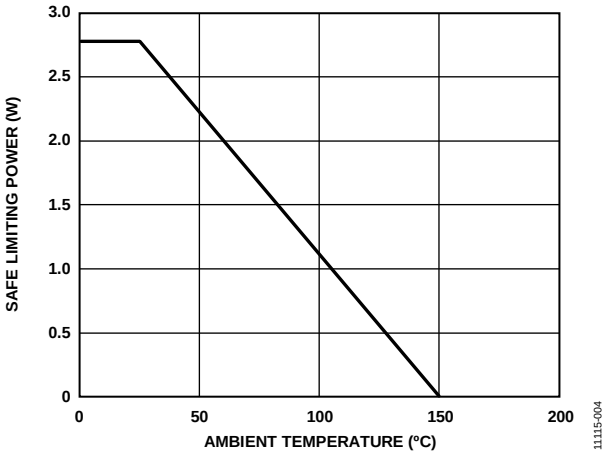


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, GND = 0 V, on-chip reference, CLKIN = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 5. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{CS}$ to SCLK Positive Edge	t_{SS}	50		ns
SCLK Frequency[1]		250	5600	kHz
SCLK Low Pulse Width	t_{SL}	80		ns
SCLK High Pulse Width	t_{SH}	80		ns
Data Output Valid After SCLK Edge	t_{DAV}		80	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	70		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	20		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{CS}$ Rising Edge	t_{DIS}	5	40	ns
$\overline{CS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Minimum and maximum specifications are guaranteed by design.

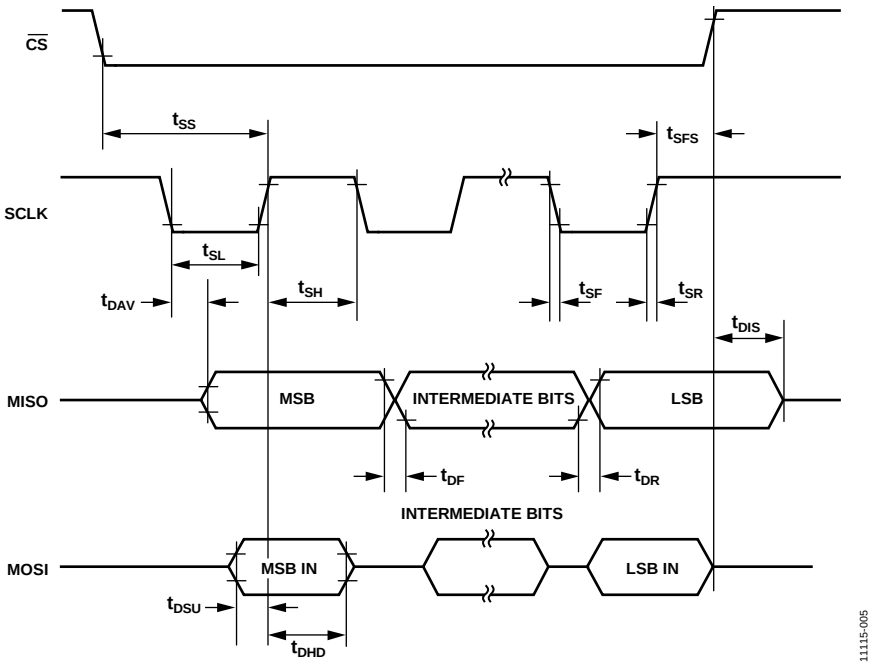


Figure 5. SPI Interface Timing

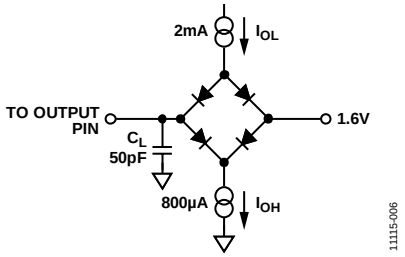


Figure 6. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
VDD to GND	−0.3 V to +3.7 V
Analog Input Voltage to GND_{ISO}, IP, IM, V1P, V2P, VM	−2 V to +2 V
Reference Input Voltage to GND_{ISO}	−0.3 V to VDD + 0.3 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Common-Mode Transients[1]	-100 kV/µs to +100 kV/µs
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[2]	260°C

[1] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

[2] Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} and θ_{JC} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead SOIC_IC	48.0	6.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 8. Maximum Continuous Working Voltage Supporting a 50-Year Minimum Lifetime[1]

Parameter	Max	Unit	Applicable Certification
AC Voltage, Bipolar Waveform	564	V peak	All certifications, 50-year operation
DC Voltage, Basic Insulation	600	V peak	

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

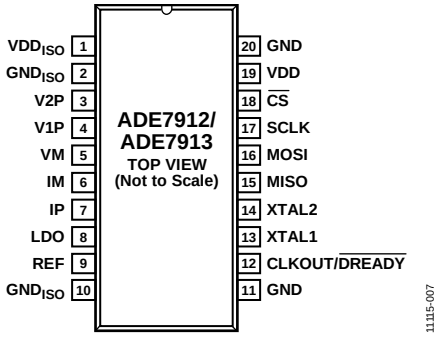


Figure 7. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD_{ISO}	Isolated Secondary Side Power Supply. This pin provides access to the 3.3 V on-chip isolated power supply. Do not connect external load circuitry to this pin. Decouple this pin with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor using Pin 2, GND_{ISO}.
2, 10	GND_{ISO}	Ground Reference of the Isolated Secondary Side. These pins provide the ground reference for the analog circuitry. Use these quiet ground references for all analog circuitry. These two pins are connected together internally.
3, 4, 5	V2P, V1P, VM	Analog Inputs for the Voltage Channels. The voltage channels are used with the voltage transducers. V2P and V1P are pseudo differential voltage inputs with a maximum signal level of ±500 mV with respect to VM for specified operation. Use these pins with the related input circuitry, as shown in Figure 20. If V1P or V2P is not used, connect it to the VM pin. On the ADE7912, connect the V2P pin to the VM pin because the V2P voltage channel is not available. The second voltage channel is available on the ADE7913 only.
6, 7	IM, IP	Analog Inputs for the Current Channel. The current channel is used with shunts. IM and IP are pseudo differential voltage inputs with a maximum differential level of ±31.25 mV. Use these pins with the related input circuitry, as shown in Figure 20.
8	LDO	2.5 V Output of Analog Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor to GND_{ISO}, Pin 10. Do not connect external load circuitry to this pin.
9	REF	Voltage Reference. This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. Decouple this pin to GND_{ISO}, Pin 10, with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
11, 20	GND	Primary Ground Reference.
12	CLKOUT/$\overline{\text{DREADY}}$	Clock Output (CLKOUT). When CLKOUT functionality is selected (see the Synchronizing Multiple ADE7912/ADE7913 Devices section for details), the ADE7912/ADE7913 generate a digital signal synchronous to the master clock at the XTAL1 pin. Use CLKOUT to provide a clock to other ADE7912/ADE7913 devices on the board. Data Ready, Active Low ($\overline{\text{DREADY}}$). When $\overline{\text{DREADY}}$ functionality is selected (see the Synchronizing Multiple ADE7912/ADE7913 Devices section for details), the ADE7912/ADE7913 generate an active low signal synchronous to the ADC output frequency. Use this signal to start reading the ADC outputs of the ADE7912/ADE7913.
13	XTAL1	Master Clock Input. An external clock can be provided at this logic input. The CLKOUT/$\overline{\text{DREADY}}$ signal of another appropriately configured ADE7912/ADE7913 (see the Synchronizing Multiple ADE7912/ADE7913 Devices section for details) can be provided at this pin. Alternatively, a crystal with a maximum drive level of 0.5 mW and an equivalent series resistance (ESR) of 20 Ω can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7912/ADE7913. The clock frequency for specified operation is 4.096 MHz, but lower frequencies down to 3.6 MHz can be used. See the ADE7912/ADE7913 Clock section for more details.
14	XTAL2	Crystal, Second Input. A crystal with a maximum drive level of 0.5 mW and an ESR of 20 Ω can be connected across XTAL2 and XTAL1 to provide a clock source for the ADE7912/ADE7913.
15	MISO	Data Output for SPI Port. Pull up this pin with a 10 kΩ resistor (see the ADE7912/ADE7913 Clock section for details).
16	MOSI	Data Input for SPI Port.
17	SCLK	Serial Clock Input for SPI Port. All serial data transfers are synchronized to this clock (see the

Pin No.	Mnemonic	Description
		ADE7912/ADE7913 Clock section).
18	$\overline{CS}$	Chip Select for SPI Port.
19	VDD	Primary Supply Voltage. This pin provides the supply voltage for the ADE7912/ADE7913. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple this pin to GND, Pin 20, with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

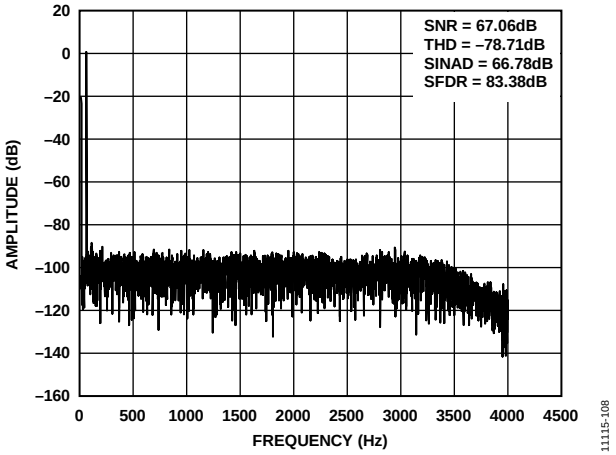


Figure 8. Current Channel FFT, ±31.25 mV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

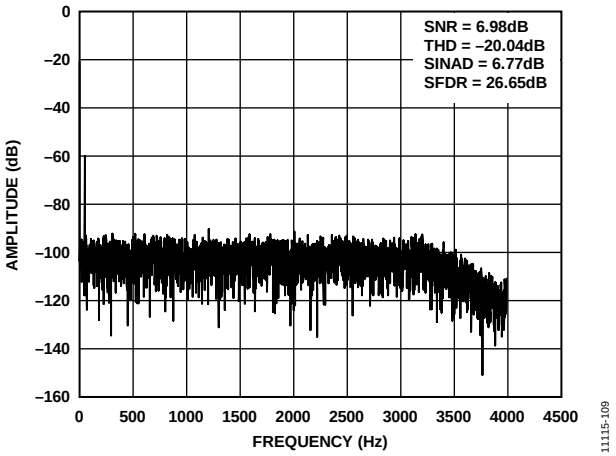


Figure 9. Current Channel FFT, ±31.25 µV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

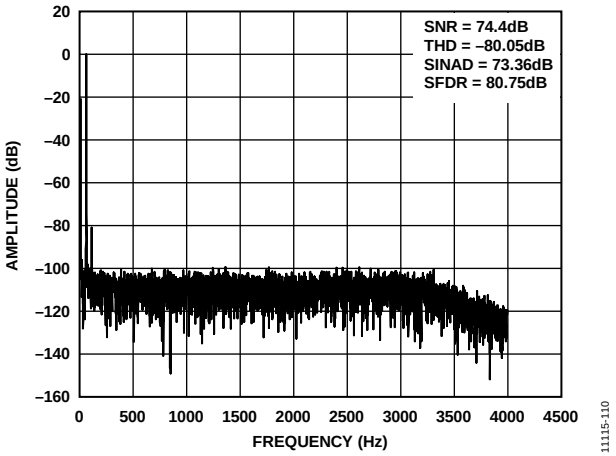


Figure 10. Voltage Channel V1 FFT, ±500 mV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

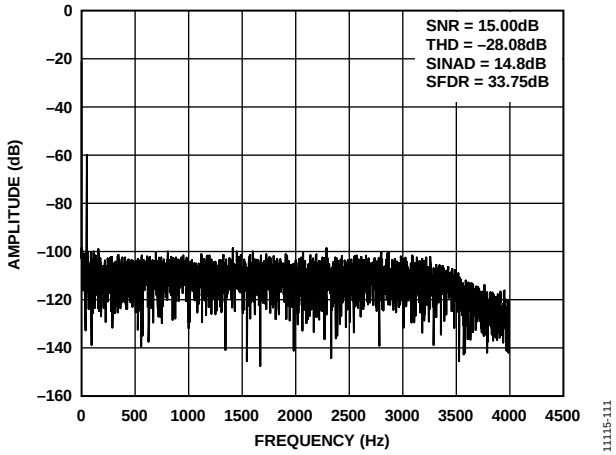


Figure 11. Voltage Channel V1 FFT, ±500 µV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

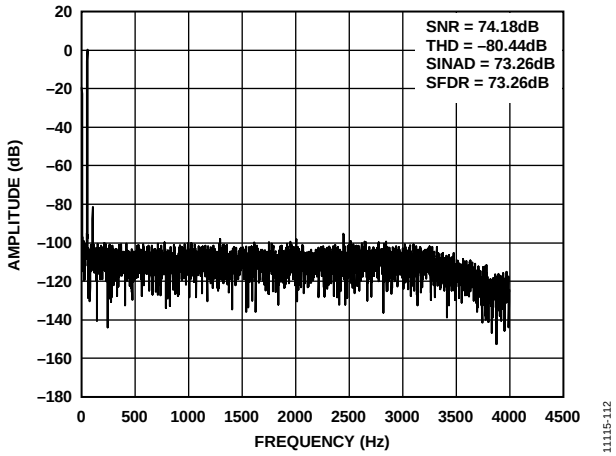


Figure 12. Voltage Channel V2 FFT, ±500 mV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

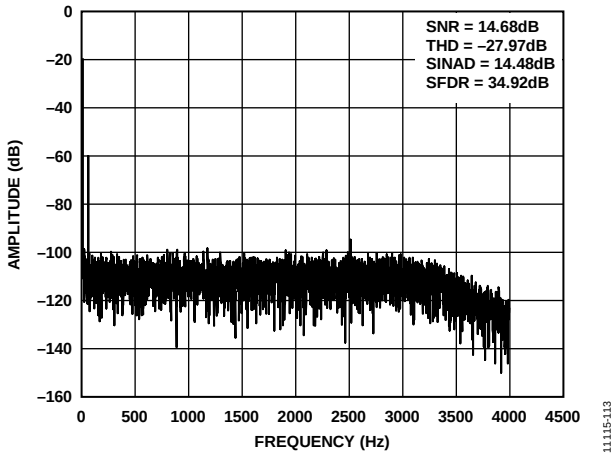


Figure 13. Voltage Channel V2 FFT, ±500 µV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

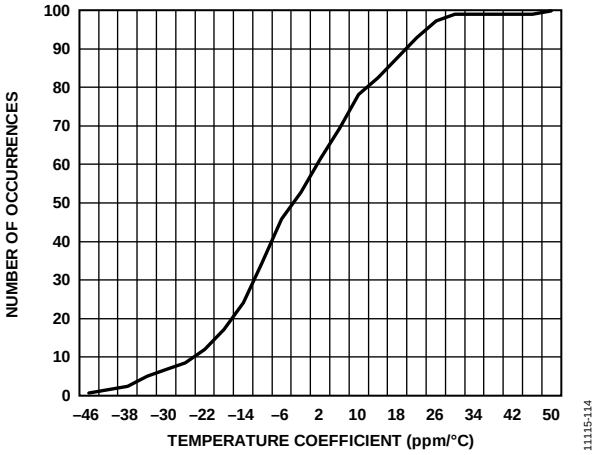


Figure 14. Cumulative Histogram of the Current Channel ADC Gain Temperature Coefficient for Temperatures Between −40°C and +25°C

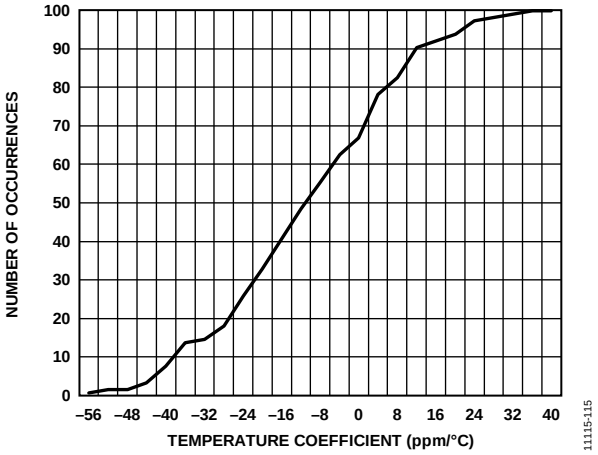


Figure 15. Cumulative Histogram of the Current Channel ADC Gain Temperature Coefficient for Temperatures Between +25°C and +85°C

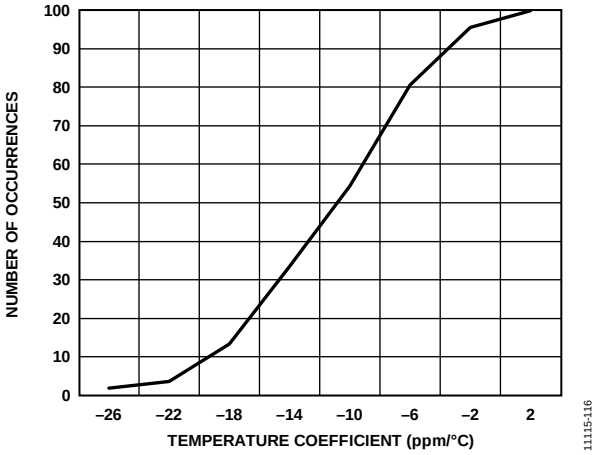


Figure 16. Cumulative Histogram of the Voltage Channel V1 ADC Gain Temperature Coefficient for Temperatures Between −40°C and +25°C

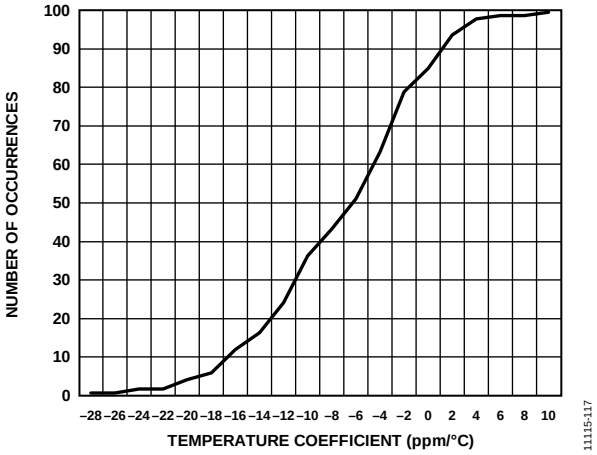


Figure 17. Cumulative Histogram of the Voltage Channel V1 ADC Gain Temperature Coefficient for Temperatures Between +25°C and +85°C

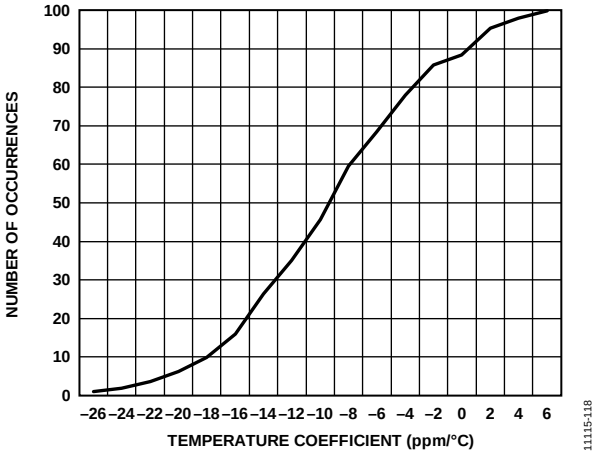


Figure 18. Cumulative Histogram of the Voltage Channel V2 ADC Gain Temperature Coefficient for Temperatures Between −40°C and +25°C

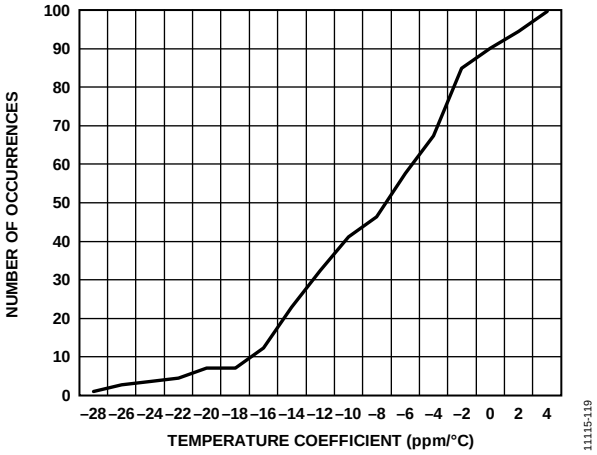
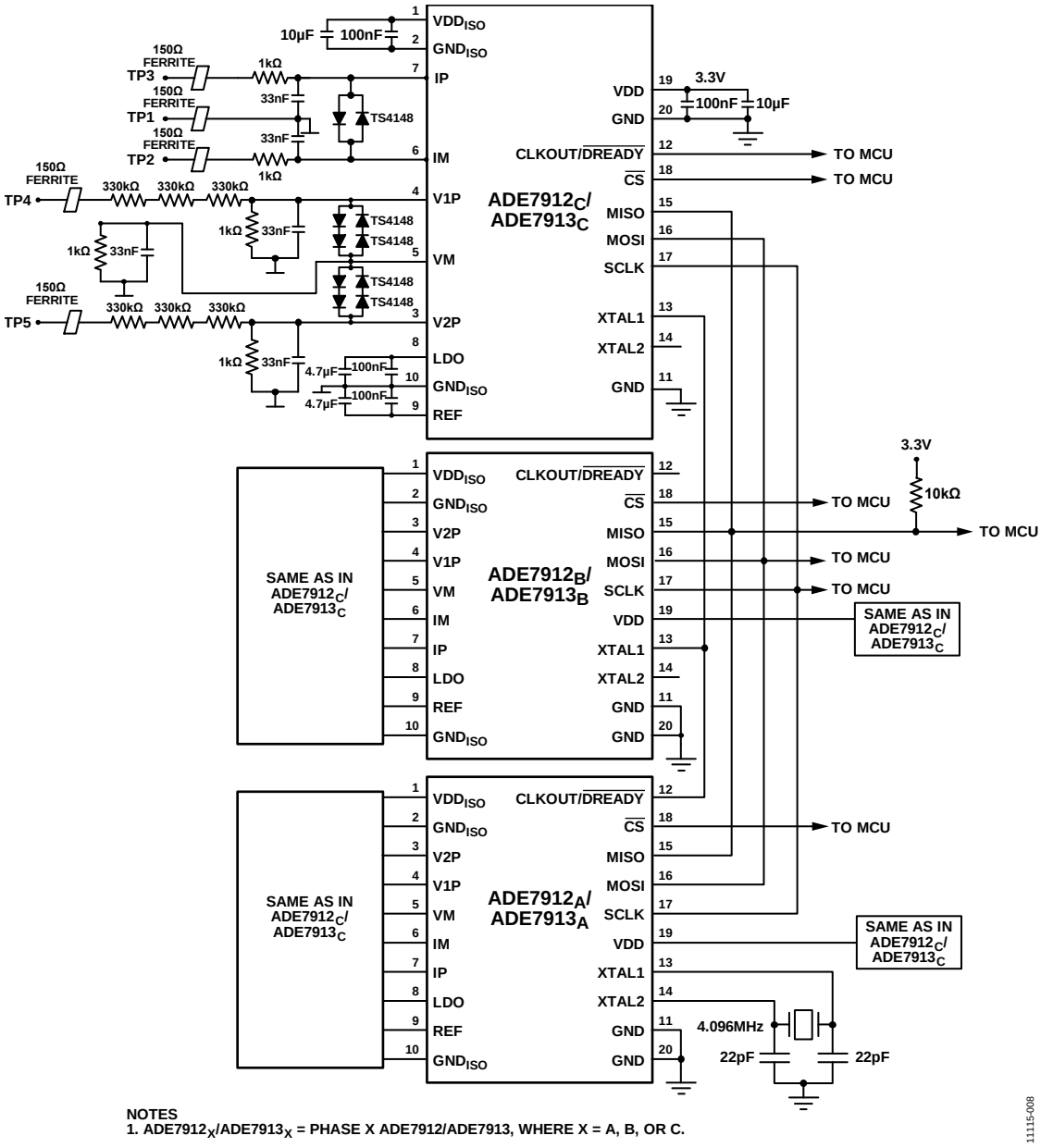


Figure 19. Cumulative Histogram of the Voltage Channel V2 ADC Gain Temperature Coefficient for Temperatures Between +25°C and +85°C

TEST CIRCUIT



NOTES
1. ADE7912X/ADE7913X = PHASE X ADE7912/ADE7913, WHERE X = A, B, OR C.

Figure 20. Test Circuit

TERMINOLOGY

Pseudo Differential Signal Voltage Range Between IP and IM, V1P and VM, and V2P and VM Pins

The range represents the peak-to-peak pseudo differential voltage that must be applied to the ADCs to generate a full-scale response when the IM and VM pins are connected to GND_{ISO}, Pin 2. The IM and VM pins are connected to GND_{ISO} using antialiasing filters (see Figure 20). Figure 21 illustrates the input voltage range between IP and IM; Figure 22 illustrates the input voltage range between V1P and VM and between V2P and VM.

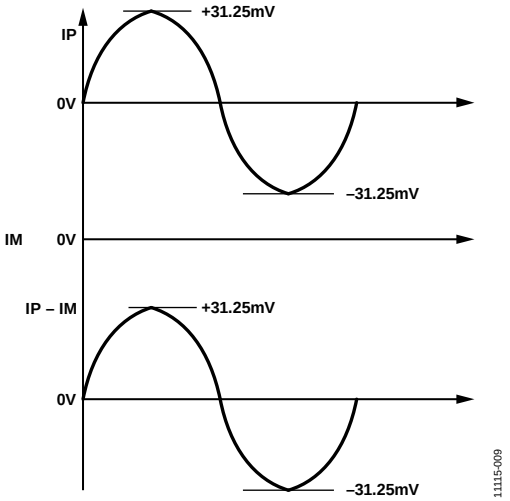


Figure 21. Pseudo Differential Input Voltage Range Between IP and IM Pins

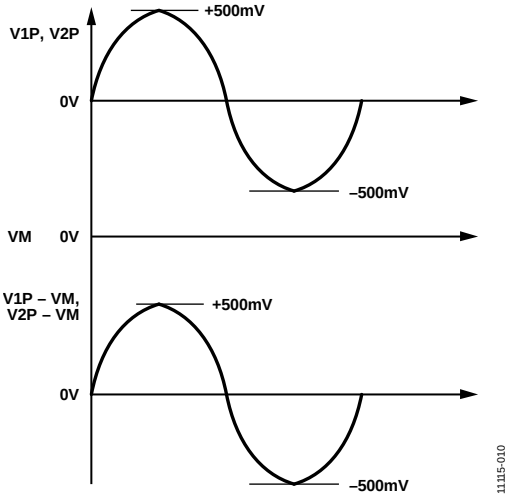


Figure 22. Pseudo Differential Input Voltage Range Between V1P and VM Pins and Between V2P and VM

Maximum VM and IM Voltage Range

The range represents the maximum allowed voltage at VM and IM pins relative to GND_{ISO}, Pin 10.

Crosstalk

Crosstalk represents leakage of signals, usually via capacitance between circuits. Crosstalk is measured in the current channel by setting the IP and IM pins to GND_{ISO}, Pin 10, supplying a full-scale alternate differential voltage between the V1P and VM pins and between the V2P and VM pins of the voltage channel, and measuring the output of the current channel. It is measured in the V1P voltage channel by setting the V1P and VM pins to GND_{ISO}, Pin 10, supplying a full-scale alternate differential voltage at the IP and V2P pin, and measuring the output of the V1P channel. Crosstalk is measured in the V2P voltage channel by setting the V2P and VM pins to GND_{ISO}, Pin 10, supplying a full-scale alternate differential voltage at the IP and V1P pins, and measuring the output of the V2P channel. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full-scale output value. The ADC outputs are acquired for 2 sec. Crosstalk is expressed in decibels.

Input Impedance to Ground (DC)

The input impedance to ground represents the impedance measured at each ADC input pin (IP, IM, V1P, V2P, and VM) with respect to GND_{ISO}, Pin 10.

Differential Input Impedance (DC)

The differential input impedance represents the impedance measured between the ADC inputs: IP and IM, V1P and VM, and V2P and VM (ADE7913 only).

ADC Offset Error

ADC offset error is the difference between the average measured ADC output code with both inputs connected to GND_{ISO} and the ideal ADC output code. The magnitude of the offset depends on the input range of each channel.

ADC Offset Drift over Temperature

The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +85°C. The offset drift over temperature is computed as follows:

$$Drift = \max\left[\left|\frac{Offset(-40)-Offset(25)}{Offset(25)\times(-40-25)}\right|,\left|\frac{Offset(85)-Offset(25)}{Offset(25)\times(85-25)}\right|\right]$$

Offset drift is expressed in nV/°C.

Gain Error

The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when the internal voltage reference is used (see the Analog-to-Digital Conversion section). The difference is expressed as a percentage of the ideal code. It represents the overall gain error of one current or voltage channel.

Gain Drift over Temperature
This temperature coefficient includes the temperature variation of the ADC gain and of the internal voltage reference. It represents the overall temperature coefficient of one current or voltage channel. With the internal voltage reference in use, the ADC gain is measured at −40°C, +25°C, and +85°C. Then the temperature coefficient is computed as follows:

$$Drift = \max\left[\left|\frac{Gain(-40)-Gain(25)}{Gain(25)\times(-40-25)}\right|,\left|\frac{Gain(85)-Gain(25)}{Gain(25)\times(85-25)}\right|\right]$$

Gain drift is measured in ppm/°C.

Power Supply Rejection (PSR)
PSR quantifies the measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken when the voltage at the input pins is 0 V. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 50 Hz or 100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of the reading (power supply rejection ratio, PSRR). PSR = 20 $\log_{10}$ (PSRR).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken when the voltage between the IP and IM pins is 6.25 mV rms, and the voltages between the V1P and VM pins and between the V2P and VM pins are 100 mV rms. A second reading is obtained with the same input signal levels when the power supplies are varied by ±10%. Any error introduced is expressed as a percentage of the reading (PSRR). Then PSR = 20 $\log_{10}$ (PSRR).

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The spectral components are calculated over a 2 sec window. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The spectral components are calculated over a 2 sec window. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of all harmonics (excluding the noise components) to the rms value of the fundamental. The spectral components are calculated over a 2 sec window. The value for THD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the ratio of the rms value of the actual input signal to the rms value of the peak spurious component over the measurement bandwidth of the waveform samples. The spectral components are calculated over a 2 sec window. The value of SFDR is expressed in decibels relative to full scale, dBFS.

THEORY OF OPERATION

ANALOG INPUTS

The ADE7913 has three analog inputs: one current channel and two voltage channels. The ADE7912 does not include the second voltage channel. The current channel has two fully differential voltage input pins, IP and IM, that accept a maximum differential signal of ±31.25 mV.

The maximum V_{IP} signal level is also ±31.25 mV. The maximum V_{IM} signal level allowed at the IM input is ±25 mV. Figure 23 shows a schematic of the input for the current channel and its relation to the maximum IM pin voltage.

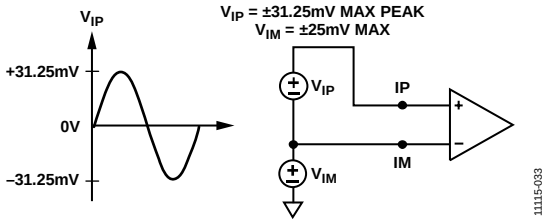


Figure 23. Maximum Input Level, Current Channel

Note that the current channel is used to sense the voltage across a shunt. In this case, one pole of the shunt becomes the ground of the meter (see Figure 33) and, therefore, the current channel is used in a pseudo differential configuration, similar to the voltage channel configuration (see Figure 24).

The voltage channel has two pseudo differential, single-ended voltage input pins: V1P and V2P. These single-ended voltage inputs have a maximum input voltage of ±500 mV with respect to VM. The maximum signal allowed at the VM input is ±25 mV. Figure 24 shows a schematic of the voltage channel inputs and their relation to the maximum VM voltage.

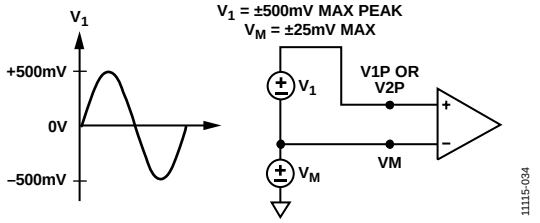


Figure 24. Maximum Input Level, Voltage Channels

ANALOG-TO-DIGITAL CONVERSION

The ADE7912/ADE7913 have three second-order Σ-Δ ADCs. For simplicity, the block diagram in Figure 25 shows a first-order Σ-Δ ADC. The converter is composed of the Σ-Δ modulator and the digital low-pass filter, separated by the digital isolation block.

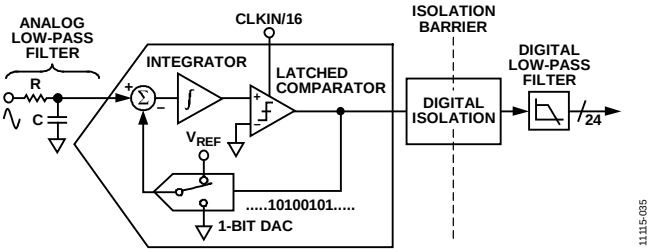


Figure 25. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7912/ADE7913, the sampling clock is equal to CLKIN/4 (1.024 MHz when CLKIN = 4.096 MHz). The 1-bit DAC in the feedback loop is driven by the serial stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. A meaningful result is obtained only when a large number of samples is averaged. This averaging is completed in the second part of the ADC, the digital low-pass filter, after the data is passed through the digital isolators. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first technique is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, when CLKIN = 4.096 MHz, the sampling rate in the ADE7912/ADE7913 is 1.024 MHz, and the bandwidth of interest is 40 Hz to 3.3 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the bandwidth of interest is lowered, as shown in Figure 26.

However, oversampling alone is not sufficient to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling factor of 4 is required to increase the SNR by a mere 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. Noise shaping is the second technique used to achieve high resolution. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass type response for the quantization noise. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 26.

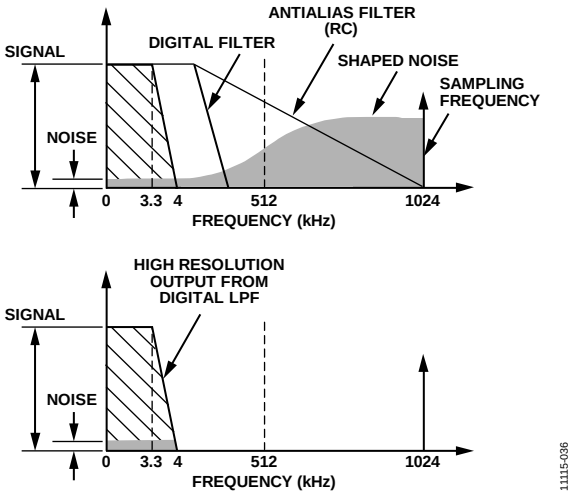


Figure 26. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

The bandwidth of interest is a function of the input clock frequency, the ADC output frequency (selectable by Bits[5:4] (ADC_FREQ) in the CONFIG register; see the ADC Output Values section for details), and Bit 7 (BW) of the CONFIG register. When CLKIN is 4.096 MHz and the ADC output frequency is 8 kHz, if BW is cleared to 0 (the default value) the ADC bandwidth is 3.3 kHz. If BW is set to 1, the ADC bandwidth is 2 kHz. Table 10 shows the ADC output frequencies and the ADC bandwidth function of the input clock (CLKIN) frequency. Three cases are shown: one for CLKIN = 4.096 MHz, the typical clock input frequency value, one for CLKIN = 4.21 MHz, the maximum clock input frequency, and one for CLKIN = 3.6 MHz, the minimum clock input frequency.

Antialiasing Filter

Figure 25 also shows an analog low-pass filter (RC) on the input to the ADC. This filter is placed outside the ADE7912/ADE7913, and its role is to prevent aliasing. Aliasing is an artifact of all sampled systems, as shown in Figure 27. Aliasing refers to the frequency components in the input signal to the ADC that are higher than half the sampling rate of the ADC and appear in the sampled signal at a frequency below half the sampling rate. Frequency components above half the sampling frequency (also known as the Nyquist frequency, that is, 512 kHz) are imaged or folded back down below 512 kHz. This happens with all ADCs, regardless of the architecture. In Figure 27, only frequencies near the sampling frequency of 1.024 MHz move into the bandwidth of interest for metering, that is, 40 Hz to 3.3 kHz or 40 Hz to 2 kHz. To attenuate the high frequency noise (near 1.024 MHz) and prevent the distortion of the bandwidth of interest, a low-pass filer (LPF) must be introduced. It is recommended that one RC filter with a corner frequency of 5 kHz be used for the attenuation to be sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing.

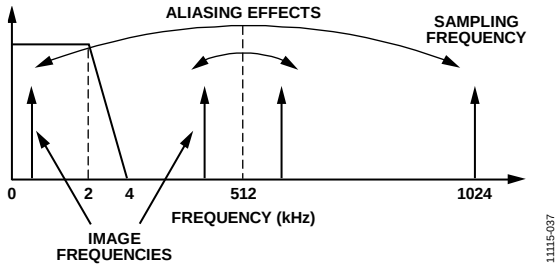


Figure 27. Aliasing Effects

Table 10. ADC Output Frequency and ADC Bandwidth as a Function of CLKIN Frequency

CLKIN (MHz)	Bits ADC_FREQ in CONFIG Register	ADC Output Frequency (Hz)	ADC Bandwidth When Bit BW in CONFIG Register Cleared to 0 (Hz)	ADC Bandwidth When Bit BW in CONFIG Register Set to 1 (Hz)
4.096	00	8000	3300	2000
	01	4000	1650	1000
	10	2000	825	500
	11	1000	412	250
4.21	00	8222	3391	2055
	01	4111	1695	1027
	10	2055	847	513
	11	1027	423	256
3.6	00	7031	2900	1757
	01	3515	1450	878
	10	1757	725	439
	11	878	362	219

ADC Transfer Function

All ADCs in the ADE7912/ADE7913 produce 24-bit signed output codes. With a full-scale input signal of 31.25 mV on the current channel and 0.5 V on the voltage channels, and with an internal reference of 1.2 V, the ADC output code is nominally 5,320,000 and usually varies for each ADE7912/ADE7913 around this value. The code from the ADC can vary between 0x800000 (−8,388,608) and 0x7FFFFF (+8,388,607); this is equivalent to an input signal level of ±49.27 mV on the current channel and ±0.788 V on the voltage channels. However, for specified performance, do not exceed the nominal range of ±31.25 mV for the current channel and ±500 mV for the voltage channels; ADC performance is guaranteed only for input signals within these limits.

ADC Output Values

The ADC output values are stored in three 24-bit signed registers, IWV, V1WV, and V2WV, at a rate defined by Bits[5:4] (ADC_FREQ) in the CONFIG register. The output frequency is 8 kHz (CLKIN/512), 4 kHz (CLKIN/1024), 2 kHz (CLKIN/2048), or 1 kHz (CLKIN/4096) based on ADC_FREQ being equal to 00, 01, 10, or 11, respectively, when CLKIN is 4.096 MHz.

The microcontroller reads the ADC output registers one at a time or in burst mode. See the SPI Read Operation and the SPI Read Operation in Burst Mode sections for more information.

REFERENCE CIRCUIT

The nominal reference voltage at the REF pin is 1.2 V. This reference voltage is used for the ADCs in the ADE7912/ADE7913. Because the on-chip dc-to-dc converter cannot supply external loads, the REF pin cannot be overdriven by a standalone external voltage reference.

The voltage of the ADE7912/ADE7913 reference drifts slightly with temperature. Table 1 lists the gain drift over temperature specification of each ADC channel. This value includes the temperature variation of the ADC gain, together with the temperature variation of the internal voltage reference.

CRC OF ADC OUTPUT VALUES

Every output cycle, the ADE7912/ADE7913 compute the cyclic redundancy check (CRC) of the ADC output values stored in the IWV, V1WV, and V2WV registers. Bits[5:4] (ADC_FREQ) in the CONFIG register determine the ADC output frequency and, therefore, the update rate of the CRC. The CRC algorithm is based on the CRC-16-CCITT algorithm. The registers are introduced into a linear feedback shift register (LFSR) based generator one byte at a time, least significant byte first, as shown in Figure 28. Each byte is then used with the most significant bit first. The 16-bit result is written in the ADC_CRC register.

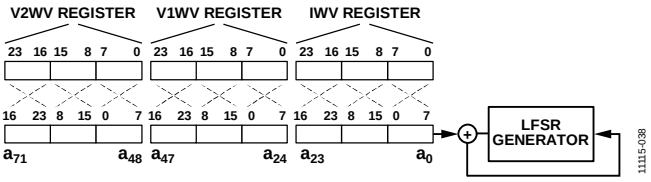


Figure 28. CRC Calculation of ADC Output Values

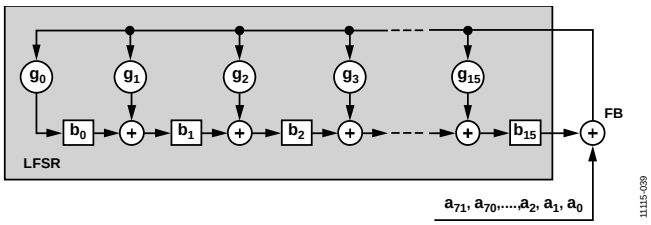


Figure 29. LFSR Generator Used for ADC_CRC Calculation

Figure 29 shows how the LFSR works. The IWV, V1WV, and V2WV registers form the [a_{71}, a_{70},…, a_0] bits used by the LFSR. Bit a_0 is Bit 7 of the first register to enter the LFSR; Bit a_{71} is Bit 16 of V2WV, the last register to enter the LFSR. The formulas that govern the LFSR are as follows:

$b_i(0)$ = 1, where i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{15} is the most significant bit.

g_i, where i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm as follows:

$$G(x) = x^{16} + x^{12} + x^5 + 1 \quad (1)$$

$$g_0 = g_5 = g_{12} = 1 \quad (2)$$

All other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (3)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (4)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, \ldots, 15 \quad (5)$$

Equation 3, Equation 4, and Equation 5 must be repeated for j = 1, 2, …, 72. The value written into the ADC_CRC register contains Bit $b_i(72)$, i = 0, 1, …, 15.

The ADC_CRC register can be read by executing an SPI register read access or as part of the SPI burst mode read operation. See the SPI Read Operation and the SPI Read Operation in Burst Mode sections for more details.

TEMPERATURE SENSOR

The ADE7912/ADE7913 contain a temperature sensor that is multiplexed with the V2P input of the voltage channel. Bit 3 (TEMP_EN) of the CONFIG register selects what the third ADC of the ADE7913 measures. If the TEMP_EN bit is 0, its default value, the ADC measures the voltage between the V2P and VM pins. If the TEMP_EN bit is 1, the ADC measures the temperature sensor. In the case of the ADE7912, the ADC always measures the temperature sensor, and the state of the TEMP_EN bit has no significance. In both the ADE7912 and the ADE7913, the conversion result is stored in the V2WV register. The time it

takes for the temperature sensor measurement to settle after the TEMP_EN bit is set to 1 is 5 ms.

The expression used to calculate the temperature in the microcontroller is:

$$temp = 8.72101 \times 10^{-5} \times (V2WV + TEMPOS \times 2^{11}) - 306.47$$

where:
temp is the temperature value measured in degrees Celsius. The gain used to convert the bit information provided by the ADE7912/ADE7913 into degrees Celsius has a default value of 8.72101×10^{-5}°C/LSB. The temperature measurement accuracy is ±5°C.
TEMPOS is the 8-bit signed read-only register in which the temperature sensor offset is stored. The offset information is calculated during the manufacturing process, and it is stored with the opposite sign. For example, if the offset is 5, −5 is written into the ADE7912/ADE7913. One least significant bit (LSB) of the TEMPOS register is equivalent to 2^{11} LSBs of the V2WV register.

Instead of using the default gain value, the gain can be calibrated as part of the overall meter calibration process. Measure the temperature, TEMP, of every ADE7912/ADE7913, read the V2WV register containing the temperature sensor reading of every ADE7912/ADE7913, and compute the gains as follows:

$$Temperature\ gain = \frac{TEMP}{V2WV + TEMPOS \times 2^{11}} \quad (6)$$

PROTECTING THE INTEGRITY OF CONFIGURATION REGISTERS

The configuration registers of the ADE7912/ADE7913 are either user accessible registers (CONFIG, EMI_CTRL, SYNC_SNAP, COUNTER0, and COUNTER1) or internal registers. The internal registers are not user accessible, and they must remain at their default values. To protect the integrity of all configuration registers, a write protection mechanism is available.

By default, the protection is disabled and the user accessible configuration registers can be written without restriction. When the protection is enabled, no writes to any configuration register are allowed. The registers can always be read, without restriction, independent of the write protection state.

To enable the protection, write 0xCA to the 8-bit lock register (Address 0xA). To disable the protection, write 0x9C to the 8-bit lock register. It is recommended that the write protection be enabled after the CONFIG and EMI_CTRL registers are initialized. If any user accessible register must be changed, for example, during the synchronization process of multiple ADE7912/ADE7913 devices, disable the protection, change the value of the register, and then reenable the protection.

CRC OF CONFIGURATION REGISTERS

Every output cycle, the ADE7912/ADE7913 compute the CRC of the CONFIG, EMI_CTRL, and TEMPOS registers, as well as Bit 2 (IC_PROT) of the STATUS0 register, and Bit 7 of the STATUS1 register. The CRC algorithm is called CRC-16-CCITT. The 16-bit result is written in the CTRL_CRC register.

The input registers to the CRC circuit form a 64-bit array that is introduced bit by bit into an LFSR-based generator, similar to Figure 28 and Figure 29, with one byte at a time, least significant byte first. Each byte is then processed with the most significant bit first.

The formulas that govern the LFSR are as follows:

$b_i(0) = 1$, where i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{15} is the most significant bit.

g_i, where i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm in Equation 1 and Equation 2.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (7)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (8)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, \ldots, 15 \quad (9)$$

Equation 7, Equation 8, and Equation 9 must be repeated for j = 1, 2, … , 64. The value written into the CTRL_CRC register contains Bit $b_i(64)$, i = 0, 1, …, 15. Because each ADE7912/ADE7913 has a particular TEMPOS register value, each ADE7912/ADE7913 has a different CTRL_CRC register default value.

ADE7912/ADE7913 STATUS

The bits in the STATUS0 and STATUS1 registers of the ADE7912/ADE7913 characterize the state of the device.

If the value of the CTRL_CRC register changes, Bit 1 (CRC_STAT) is set to 1 in the STATUS0 register. This bit clears to 0 when the STATUS0 register is read.

After the configuration registers are protected by writing 0xCA into the lock register, Bit 2 (IC_PROT) in the STATUS0 register is set to 1. It clears to 0 when the STATUS0 register is read, and it is set back to 1 at the next ADC output cycle.

At power-up, or after a hardware or software reset, the ADE7912/ADE7913 signal the end of the reset period by clearing Bit 0 (RESET_ON) to 0 in the STATUS0 register.

If the ADC output values of IWV, V1WV, and V2WV are not read during an output cycle, Bit 3 (ADC_NA) in the STATUS1 register becomes 1. It clears to 0 when the STATUS1 register is read.

The STATUS0 and STATUS1 registers can be read by executing an SPI register read. STATUS0 can also be read as part of the SPI burst mode read operation. See the SPI Read Operation and the SPI Read Operation in Burst Mode sections for more information.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period of time. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADE7912/ADE7913 devices. Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 8 summarize the maximum CSA/VDE approved working voltage for 50 years of service life for a bipolar ac operating condition. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADE7912/ADE7913 devices depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 30, Figure 31, and Figure 32 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 3.+year service life.

The working voltages listed in Table 8 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage case. Treat any cross-insulation voltage waveform that does not conform to Figure 31 or Figure 32 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 8.

The voltage shown in Figure 31 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

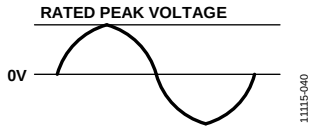


Figure 30. Bipolar AC Waveform

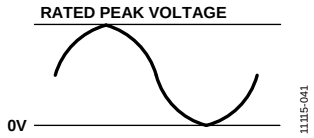


Figure 31. Unipolar AC Waveform

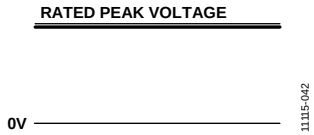


Figure 32. DC Waveform

APPLICATIONS INFORMATION

ADE7912/ADE7913 IN POLYPHASE ENERGY METERS

The ADE7912/ADE7913 are designed for use in 3-phase energy metering systems in which two, three, or four ADE7912/ADE7913 devices are managed by a master device containing an SPI interface, usually a microcontroller.

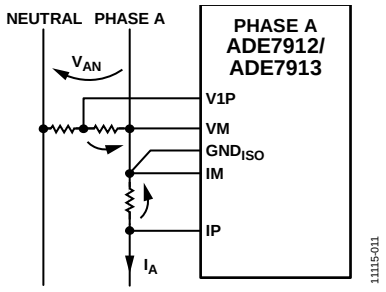


Figure 33. Phase A ADE7912/ADE7913 Current and Voltage Sensing

Figure 33 shows the Phase A of a 3-phase energy meter. The Phase A current, I_A, is sensed with a shunt. A pole of the shunt is connected to the IM pin of the ADE7912/ADE7913 and becomes the ground, GND_{ISO} (Pin 10), of the isolated side of the ADE7912/ADE7913. The Phase A to neutral voltage, V_{AN}, is sensed with a resistor divider, and the VM pin is also connected to the IM and GND_{ISO} pins. Note that the voltages measured by the ADCs of the ADE7912/ADE7913 are opposite to V_{AN} and I_A, a classic approach in single-phase metering. The other ADE7912/ADE7913 devices that monitor Phase B and Phase C are connected in a similar way.

The V2P voltage channel is intended to measure an auxiliary voltage, and it is available only on the ADE7913. If V2P is not used, as is the case of the ADE7912, connect V2P to VM.

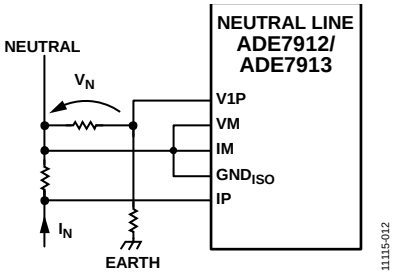


Figure 34. Neutral Line and Neutral to Earth Voltage Monitoring with the ADE7912/ADE7913

Figure 34 shows how the ADE7912/ADE7913 inputs are connected when the neutral line of a 3-phase system is monitored. The neutral current is sensed using a shunt and the voltage across the shunt is measured at the fully differential inputs, IP and IM. The earth to neutral voltage is sensed with a voltage divider at the single-ended inputs, V1P and VM.

Figure 35 shows a block diagram of a 3-phase energy meter that uses three ADE7912/ADE7913 devices and a microcontroller. The neutral current is not monitored in this example. One 4.096 MHz crystal provides the clock to the ADE7912/ADE7913 that senses the Phase A current and voltage. The ADE7912/ADE7913 devices that sense the Phase B and Phase C currents and voltages are clocked by a signal generated at the CLKOUT/DREADY pin of the ADE7912/ADE7913 that is placed to sense the Phase A current and voltage. As an alternative configuration, the microcontroller can generate a 4.096 MHz clock to all ADE7912/ADE7913 devices at the XTAL1 pin (see Figure 36). Note that the XTAL1 pin can receive a clock with a frequency within the 3.6 MHz to 4.21 MHz range, as specified in Table 1.

The microcontroller uses the SPI port to communicate with the ADE7912/ADE7913 devices. Three of its I/O pins, CS_A, CS_B, and CS_C, are used to generate the SPI $\overline{CS}$ signals. The SCLK, MOSI, and MISO pins of the microcontroller are directly connected to the corresponding SCLK, MOSI, and MISO pins of each ADE7912/ADE7913 device (see Figure 39). To simplify Figure 35 to Figure 38, these connections are not shown.

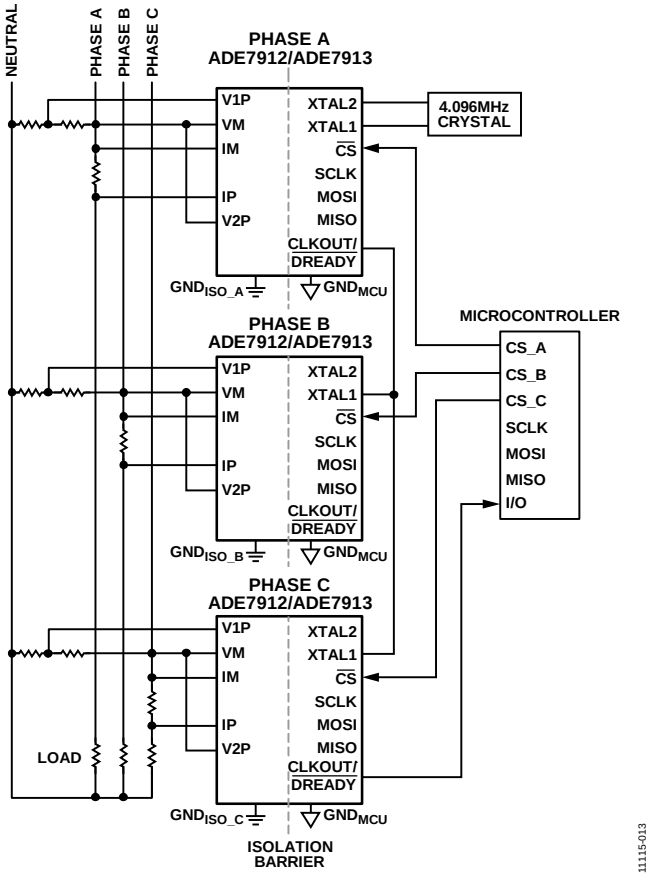


Figure 35. 3-Phase Energy Meter Using Three ADE7912/ADE7913 Devices

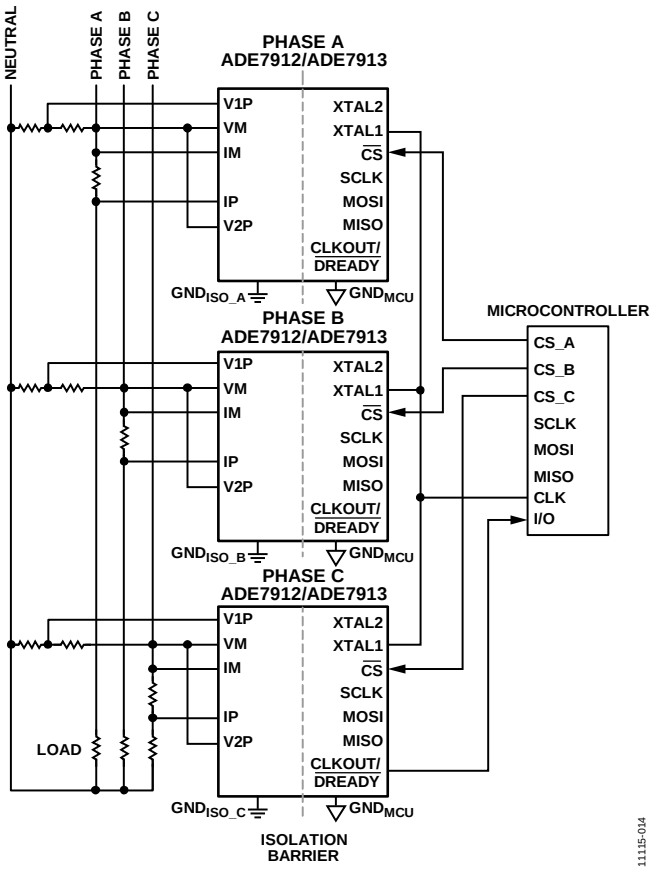


Figure 36. Microcontroller Generating Clock to Three ADE7912/ADE7913 Devices

In Figure 36, the CLKOUT/$\overline{\text{DREADY}}$ pin of the ADE7912/ADE7913 that is used to sense the Phase C current and voltage is connected to the I/O pin of the microcontroller. CLKOUT/$\overline{\text{DREADY}}$ provides an active low pulse for 64 CLKIN cycles (15.625 µs at CLKIN = 4.096 MHz) when the ADC conversion data is available. It signals when the ADC outputs of all ADE7912/ADE7913 devices become available and when the microcontroller starts to read them. See the Synchronizing Multiple ADE7913 Devices section for more information about synchronizing multiple ADE7912/ADE7913 devices.

At power-up, or after a hardware or software reset, follow the procedure described in the Power-Up Procedure for Systems with Multiple Devices That Use a Single Crystal section or the Power-Up Procedure for Systems with Multiple Devices That Use Clock Generated from Microcontroller section to ensure that the ADE7912/ADE7913 devices function appropriately.

The configuration of an energy meter using four ADE7912/ADE7913 devices is similar, shown in Figure 37. The microcontroller uses an additional I/O pin, CS_N, to generate the SPI $\overline{\text{CS}}$ signal to the ADE7912/ADE7913 device that is monitoring the neutral current.

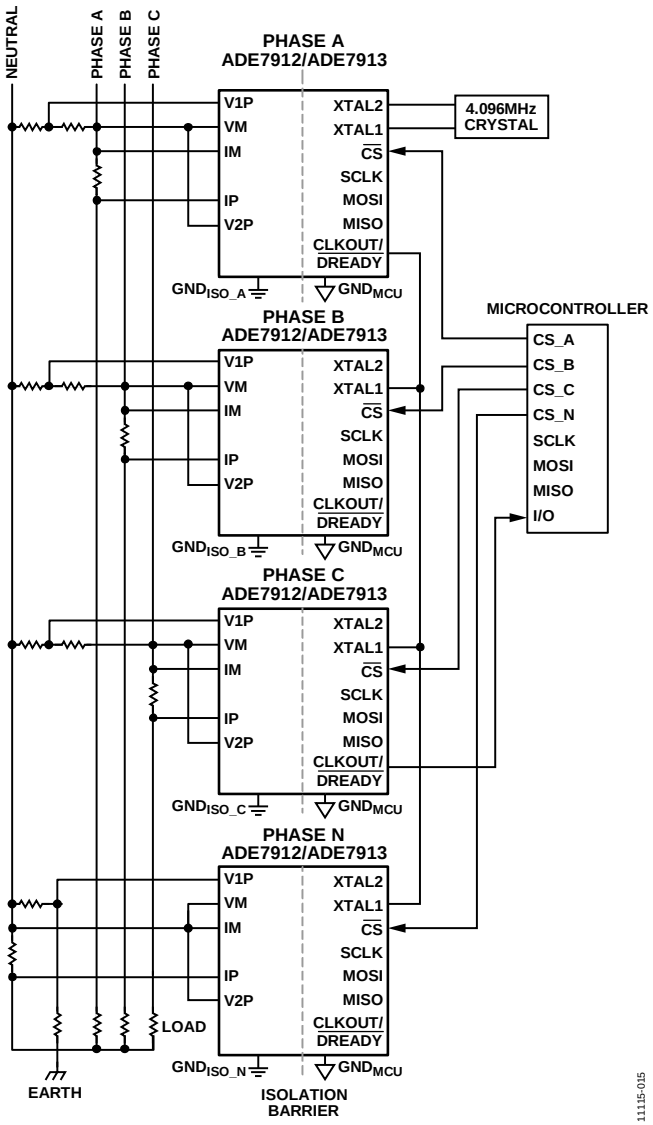


Figure 37. 3-Phase Energy Meter Using Four ADE7912/ADE7913 Devices

Figure 38 shows an energy meter using two ADE7912/ADE7913 devices in a delta configuration. The meter ground is on the Phase B line. One ADE7912/ADE7913 device measures Phase A current and Phase A to Phase B voltage. A second ADE7912/ADE7913 device measures Phase C current and Phase C to Phase B voltage. Phase B current and Phase A to Phase C voltage are computed by the system microcontroller.

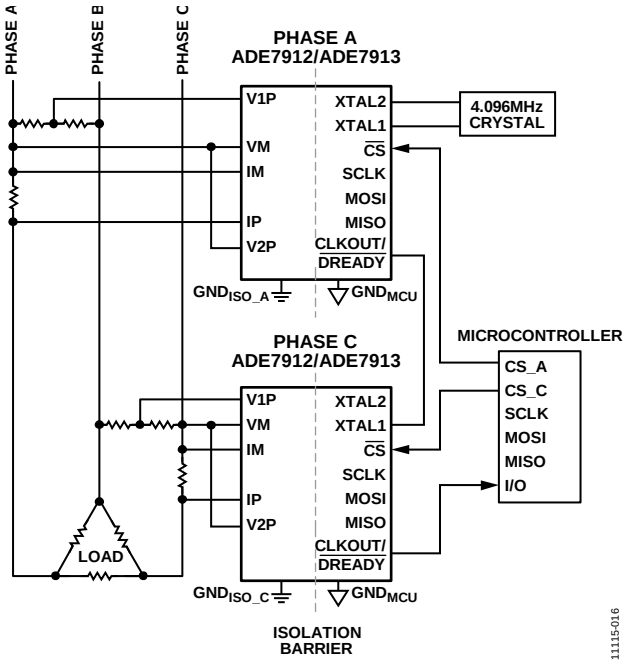


Figure 38. 3-Phase Meter Using Two ADE7912/ADE7913 Devices in Delta Configuration

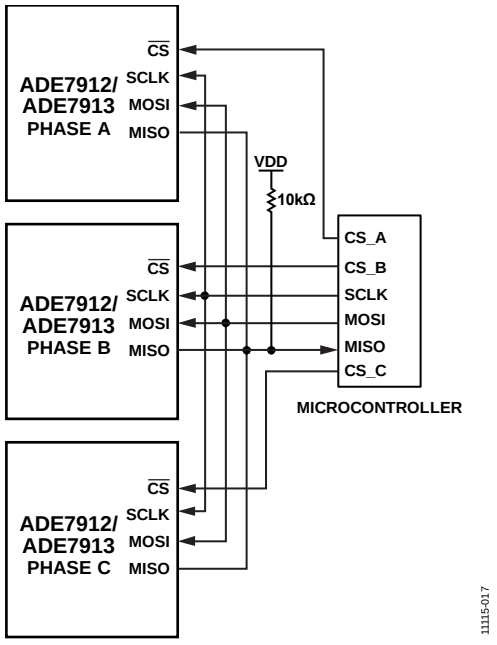


Figure 39. SPI Connections Between Three ADE7912/ADE7913 Devices and a Microcontroller

ADE7912/ADE7913 CLOCK

Provide a digital clock signal at the XTAL1 pin to clock the ADE7912/ADE7913. The frequency at which the ADE7912/ADE7913 are clocked at XTAL1 is called CLKIN. The ADE7912/ADE7913 are specified for CLKIN = 4.096 MHz, but frequencies between 3.6 MHz and 4.21 MHz are acceptable.

Alternatively, a 4.096 MHz crystal with a typical drive level of 0.5 mW and an equivalent series resistance (ESR) of 20 Ω can be connected across the XTAL1 and XTAL2 pins to provide a clock source for the ADE7912/ADE7913 (see Figure 40).

The total capacitance, TC, at the XTAL1 and XTAL2 pins is

$$TC = C1 + CP1 = C2 + CP2$$

where:
C1 and *C2* are the ceramic capacitors between XTAL1 and GND and between XTAL2 and GND, respectively.
CP1 and *CP2* are the parasitic capacitors of the wires connecting the crystal to the ADE7912/ADE7913.

The load capacitance, LC, of the crystal is equal to half the total capacitance, TC, because it is the capacitance of the series circuit composed by C1 + CP1 and C2 + CP2.

$$LC = \frac{C1 + CP1}{2} = \frac{C2 + CP2}{2} = \frac{TC}{2}$$

Therefore, the value of the C1 and C2 capacitors as a function of the load capacitance of the crystal is

$$C1 = C2 = 2 \times LC - CP1 = 2 \times LC - CP2$$

In the case of the ADE7912/ADE7913, the typical total capacitance, TC, of the XTAL1 and XTAL2 pins is 40 pF (see Table 1). Select a crystal with a load capacitance of

$$LC = \frac{TC}{2} = 20 \text{ pF}$$

Assuming the parasitic capacitances, CP1 and CP2, are equal to 20 pF, select Capacitors C1 and C2 equal to 20 pF.

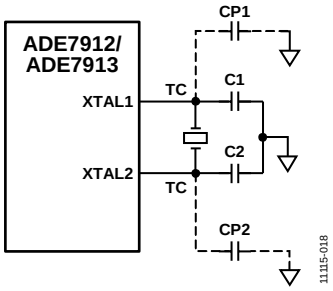


Figure 40. Crystal Circuitry

SPI-COMPATIBLE INTERFACE

The SPI of the ADE7912/ADE7913 is the slave of the communication and consists of four pins: SCLK, MOSI, MISO, and $\overline{CS}$. The serial clock for a data transfer is applied at the SCLK logic input. All data transfer operations synchronize to the serial clock. Data shifts into the ADE7912/ADE7913 at the MOSI logic input on the falling edge of SCLK, and the ADE7912/ADE7913 sample the data on the rising edge of SCLK. Data shifts out of the ADE7912/ADE7913 at the MISO logic output on the falling edge of SCLK and can be sampled by the master device on the rising edge of SCLK. The most significant bit of the word is shifted in and out first. The maximum and minimum serial clock frequencies supported by this interface are 5.6 MHz and 250 kHz, respectively. MISO stays in high impedance when no data is transmitted from the ADE7912/ADE7913. At power-up or during hardware or software reset, the microcontroller reads the STATUS0 register to detect when Bit 0 (RESET_ON) clears to 0. See Figure 39 for details of the connections between the SPI ports of three ADE7912/ADE7913 devices and a microcontroller containing an SPI interface.

The $\overline{CS}$ logic input is the chip select input. Drive the $\overline{CS}$ input low for the entire data transfer operation. Bringing $\overline{CS}$ high during a data transfer operation leaves the ADE7912/ADE7913 register that is the object of the data transfer unaffected, but aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by returning the $\overline{CS}$ logic input to low.

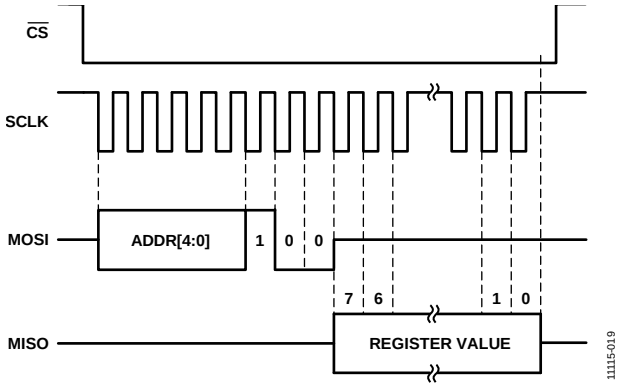


Figure 41. SPI Read Operation of an 8-Bit Register

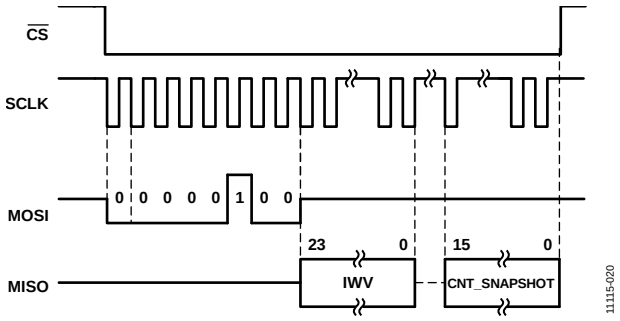


Figure 42. SPI Read Operation in Burst Mode

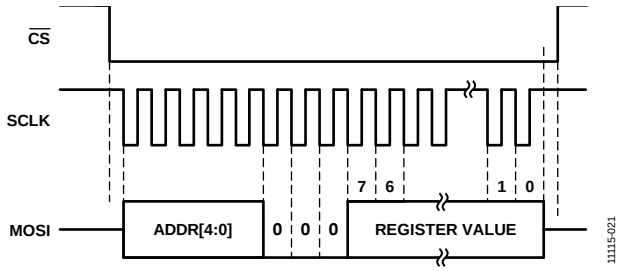


Figure 43. SPI Write Operation

SPI Read Operation

The read operation using the ADE7912/ADE7913 SPI interface is initiated when the master sets the $\overline{CS}$ pin low and begins sending one command byte on the MOSI line. The master places data on the MOSI line starting with the first high to low transition of SCLK.

The bit composition of the command byte is shown in Table 11. Bits[1:0] are don't care bits, and they can have any value. The examples presented throughout this section show them set to 00. Bit 2 (READ_EN) determines the type of the operation. For a read, READ_EN must be set to 1. For a write, READ_EN must be cleared to 0. Bits[7:3] (ADDR) represent the address of the register to be read or written.

The ADE7912/ADE7913 SPI samples data on the low to high transitions of SCLK. After the ADE7912/ADE7913 device receives the last bit of the command byte on a low to high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high to low transition occurs; thus, the master can sample the data on a low to high SCLK transition. After the master receives the last bit, it sets the $\overline{CS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. Figure 41 shows an 8-bit register read operation; 16-bit and 32-bit registers are read in the same manner.

Table 11. Command Byte for SPI Read/Write Operations

Bit Location	Bit Name	Description
1:0	Reserved	These bits can have any value.
2	READ_EN	Set this bit to 1 if a SPI read operation is executed. Clear this bit to 0 if a SPI write operation is executed.
7:3	ADDR	Address of the register to be read or written.

SPI Read Operation in Burst Mode

All ADE7912/ADE7913 output registers (IWV, V1WV, V2WV, ADC_CRC, STATUS0, and CNT_SNAPSHOT) can be read in one of two ways: one register at a time (see the SPI Read Operation section) or by reading multiple consecutive registers simultaneously in burst mode. Burst mode is initiated when the master sets the $\overline{CS}$ pin low and begins sending the command byte (see Table 11) on the MOSI line with Bits[7:3] (ADDR) set to the IWV register address, 00000. This means a command byte set to 0x04. The master places data on the MOSI line starting with the first high to low transition of SCLK. The SPI of the ADE7912/ADE7913 samples data on the low to high transitions of SCLK. After the ADE7912/ADE7913 device receives the last bit of the command byte on a low to high transition of SCLK, it begins to transmit the 24-bit IWV register on the MISO line when the next SCLK high to low transition occurs; thus, the master can sample the data on a low to high SCLK transition. After the master receives the last bit of the IWV register, the ADE7912/ADE7913 device sends V1WV, which is placed at the next location, and continues in this manner until the master sets the $\overline{CS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 42 for details of the SPI read operation in burst mode.

If a register does not need to be read, for example, the 16-bit CNT_SNAPSHOT register, the master sets the $\overline{CS}$ and SCLK lines high after the STATUS0 register is received.

If the IWV register, for example, is not required, but V1WV is, set the ADDR bits to the V1WV address, 00001, in the command byte, and execute the burst mode operation.

SPI Write Operation

The SPI write operation is initiated when the master sets the $\overline{CS}$ pin low and begins sending one command byte (see Table 11). Bit 2 (READ_EN) must be cleared to 0. The master places data on the MOSI line starting with the first high to low transition of SCLK. The SPI of the ADE7912/ADE7913 samples data on the low to high transitions of SCLK. Next, the master sends the 8-bit value of the register without losing any SCLK cycles. After the last bit is transmitted, at the end of the SCLK cycle, the master sets the $\overline{CS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 43 for details of the SPI write operation.

Note that the SPI write operation can execute 8-bit writes only. The 16-bit synchronization counter register (composed of COUNTER0 and COUNTER1) is written by executing the write operation twice: the less significant byte is written first, followed by the most significant byte. See the Synchronizing Multiple ADE7912/ADE7913 Devices section for details on the functionality controlled by the synchronization counter register.

Because the ADE7912/ADE7913 do not need to acknowledge a write command in any way, this operation can be broadcast to multiple ADE7912/ADE7913 devices when the same register must be initialized with the same value.

After executing a write operation, it is recommended to read back the register to ensure that it was initialized correctly.

SYNCHRONIZING MULTIPLE ADE7912/ADE7913 DEVICES

The ADE7912/ADE7913 allow the user to sample all currents and voltages simultaneously and to provide coherent ADC output samples, which is a highly desired feature in polyphase metering systems. The EMI reduction scheme managed by the EMI_CTRL register (see the DC-to-DC Converter section for details) requires that the ADE7912/ADE7913 provide coherent samples.

The ADE7912/ADE7913 in Polyphase Energy Meters section describes how a polyphase energy meter containing multiple ADE7912/ADE7913 devices can use one crystal to clock all the ADE7912/ADE7913 devices. At power-up, only one ADE7912/ADE7913 device is clocked from the crystal, as the other devices are set to receive the clock from the CLKOUT/$\overline{DREADY}$ pin of the first ADE7912/ADE7913 device. This pin has $\overline{DREADY}$

functionality enabled by default. In Figure 35, Figure 37, and Figure 38, the ADE7912/ADE7913 device on Phase A is clocked from the crystal, and the CLKOUT/DREADY pin generates the DREADY signal. The other ADE7912/ADE7913 devices are clocked by the DREADY signal because the CLKOUT signal has not yet been received by their XTAL1 pins. The microcontroller enables CLKOUT functionality when Bit 0 (CLKOUT_EN) is set to 1 in the CONFIG register. This operation ensures that the other ADE7912/ ADE7913 devices in the system receive the same clock as the ADE7912/ADE7913 on Phase A and that all ADCs within all ADE7912/ADE7913 devices in the system sample data at the same exact moment.

As an alternative to using one crystal, the microcontroller can generate a clock signal to the XTAL1 pins of every ADE7912/ ADE7913, ensuring precise ADC sampling synchronization (see Figure 36).

To configure all ADE7912/ADE7913 devices in an energy meter to provide coherent ADC output samples, that is, samples obtained in the same output cycle, all ADE7912/ADE7913 devices must have the same ADC output frequency and the outputs must be synchronized. Bits[5:4] (ADC_FREQ) in the CONFIG register select the ADC output frequency; therefore, they must be initialized to the same value (see the ADC Output Values section for more details).

To synchronize the ADC outputs, that is, to set all ADE7912/ADE7913 devices to generate ADC outputs at the same exact moment, after power-up, the microcontroller must broadcast a write to the 8-bit SYNC_SNAP register with the value 0x01. All ADE7912/ADE7913 devices then start a new ADC output period simultaneously when Bit 0 (sync) of the SYNC_SNAP register is written. The sync bit clears itself to 0 after one CLKIN cycle.

As shown in Figure 35, Figure 37, and Figure 38, the CLKOUT/ DREADY pin of one ADE7912/ADE7913 is connected to an I/O input of the microcontroller. This ADE7912/ADE7913 device has Bit 0 (CLKOUT_EN) in the CONFIG register set to the default value, 0, to enable the DREADY functionality. When the ADC output period starts, the CLKOUT/DREADY pin goes low for 64 CLKIN cycles (15.625 μs when CLKIN = 4.096 MHz), signaling that all ADC outputs from all ADE7912/ADE7913 devices are available and the microcontroller must start reading them. It is recommended that the SPI read in burst mode be used to ensure that all data is read in the shortest amount of time.

The ADE7912/ADE7913 contain an internal 12-bit counter that functions at the CLKIN frequency. The counter is synchronized with the ADC output period and the CLKOUT/DREADY pin. When a new output period starts, the counter starts decreasing from a value determined by Bits[5:4] (ADC_FREQ) in the CONFIG register. Table 12 shows these values.

Table 12. Counter Initial Values as a Function of ADC_FREQ Bits

Bits[5:4] (ADC_FREQ) in CONFIG Register	ADC Output Frequency (kHz)	Counter C_0 Initial Value (CLKIN = 4.096 MHz)	Counter C_0 Initial Value as a Function of CLKIN
00	8	511	$\frac{CLKIN}{8000} - 1$
01	4	1023	$\frac{CLKIN}{4000} - 1$
10	2	2047	$\frac{CLKIN}{2000} - 1$
11	1	4095	$\frac{CLKIN}{1000} - 1$

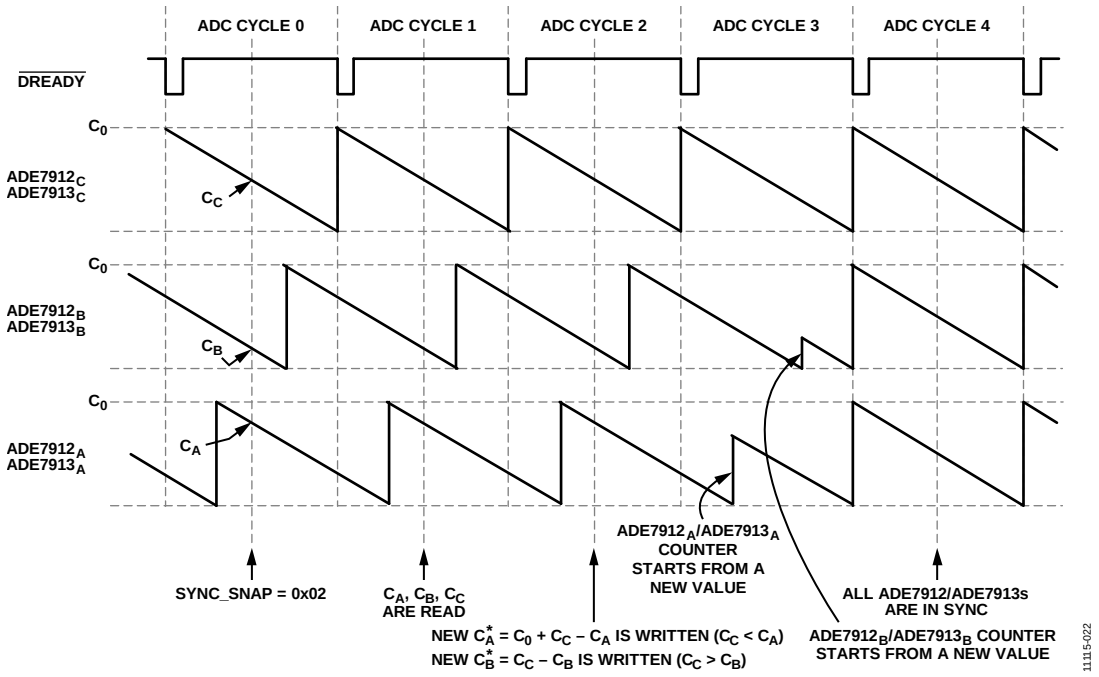


Figure 44. Synchronizing Phase A and Phase B ADE7912/ADE7913 Devices with Phase C ADE7912/ADE7913

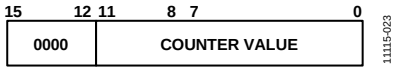


Figure 45. CNT_SNAPSHOT Register

The 8-bit SYNC_SNAP register latches the value of the counter when it is written with 0x02, that is, Bit 1 (snap) set to 1. A broadcast write to all ADE7912/ADE7913 devices ensures that all the counters of every ADE7912/ADE7913 are latched at the same moment. The snap bit clears itself to 0 after one CLKIN cycle. The values of the counters offer a measure of the ADC output synchronization across all ADE7912/ADE7913 devices. Ideally, the values should be perfectly equal, indicating that all ADE7912/ADE7913 devices are fully synchronized. In reality, due to the uncertainty between the SPI clock generated by the microcontroller and the ADE7912/ADE7913 CLKIN, a ±1 count difference between counters is acceptable. The 12-bit counter is accessed via the 16-bit CNT_SNAPSHOT register (see Figure 45).

If the internal counter of one ADE7912/ADE7913 device does not have a value correlated with the values of the counters of the other ADE7912/ADE7913 devices, this means that the ADC outputs of one phase are no longer synchronized with the ADC outputs from the other phases. The ADE7912/ADE7913 provide two options to resynchronize all the ADE7912/ADE7913 devices: one is to broadcast a write to the 8-bit SYNC_SNAP register with the value 0x01. This action immediately forces all ADE7912/ADE7913 devices to start an ADC output cycle simultaneously. However, all phases present ADC output distortions of various degrees, a function of when a SYNC_SNAP = 0x01 write is executed within the current output period. Therefore, it is recommended that this command be executed at power-up or after a hardware or software reset.

The other option is to compute a new starting value for the internal counter of the ADE7912/ADE7913 device that is out of synchronization. This value forces the internal counter to start a new ADC output cycle, counting down from it, and end simultaneously with the other counters of the other ADE7912/ADE7913 devices. The 12-bit value is stored in two 8-bit registers, COUNTER1 and COUNTER0 (see Figure 46). COUNTER0 contains the least significant eight bits and must be written first. COUNTER1 contains the four most significant bits and must be written after COUNTER0. The advantage of this option compared to writing SYNC_SNAP = 0x01 is that only the ADC outputs of out of sync phases are affected. The other phases already in synchronization remain unaffected. As a general rule, it is recommended that the synchronization of the ADE7912/ ADE7913 devices be verified every couple of seconds.

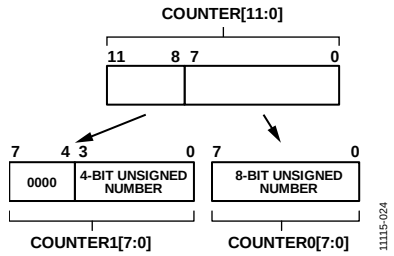


Figure 46. Counter Start Value Communicated Using Two 8-Bit Registers

Consider the example shown in Figure 44: the Phase A, Phase B, and Phase C counters of three ADE7912/ADE7913 devices are shown for the meter configuration shown in Figure 35. All three phases are out of synchronization. It is desirable to synchronize the Phase A and Phase B ADE7912/ADE7913 devices with the Phase C ADE7912/ADE7913, which is considered the reference because it generates the $\overline{\text{DREADY}}$ signal.

When the $\overline{\text{DREADY}}$ active low pulses are generated, execute the following steps immediately after the output registers (IWV, V1WV, V2WV, ADC_CRC, STATUS0, and CNT_SNAPSHOT) are read:

1. ADC Cycle 0. Disable the protection of the configuration registers by setting the lock register to 0x9C (see the Protecting the Integrity of Configuration Registers section).
   Set the 8-bit register SYNC_SNAP to 0x02 using a write broadcast command. The C_A, C_B, and C_C values of the three counters are latched and stored in the CNT_SNAPSHOT register of each device.
2. ADC Cycle 1. The ADE7912/ADE7913 counters (C_A, C_B, and C_C) latched at Cycle 0 are read in burst mode from the CNT_SNAPSHOT register together with the IWV, V1WV, V2WV, ADC_CRC, and STATUS0 registers.
3. ADC Cycle 2. Because $C_A > C_C$, the following equation can be written:

$$C_C + C_0 = C_A + C_A^*$$

   where C_A^* is the new value that must be determined.

   The new initial counter value, $C_A^* = C_C + C_0 - C_A$, is written into the Phase A ADE7912/ADE7913 (labeled ADE7912$_A$/ADE7913$_A$ in Figure 44) in two consecutive 8-bit writes to the COUNTER0 and COUNTER1 registers. The Phase A ADE7912/ADE7913 device is in synchronization with the Phase C ADE7912/ADE7913 starting with ADC Cycle 4.
   Because $C_B < C_C$, the following equation can be written:

$$C_C = C_B + C_B^*$$

   where C_B^* is the new value that must be determined.

   The new initial counter value, $C_B^* = C_C - C_B$, is written into the Phase B ADE7912/ADE7913 in two consecutive 8-bit writes to the COUNTER0 and COUNTER1 registers. Phase B ADE7912/ADE7913 is in synchronization with the Phase C ADE7912/ADE7913 starting with ADC Cycle 4.

   As demonstrated, if the latched value of the counter on the reference Phase X is C_X and the initial value of the counter is C_0 (see Table 10), the new value of the counter on Phase Y that is required to bring Phase Y in synchronization to Phase X is as follows:

$$\text{If } C_Y > C_X, \text{ then } C_Y^* = C_X + C_0 - C_Y \quad (10)$$

$$\text{If } C_Y \le C_X, \text{ then } C_Y^* = C_X - C_Y \quad (11)$$

4. ADC Cycle 3. The Phase A and Phase B ADE7912/ADE7913 counters start counting down based on the COUNTER1 and COUNTER0 values written during ADC Cycle 2.
5. ADC Cycle 4. All ADE7912/ADE7913 devices generate ADC outputs synchronously. To verify this, as a good programming practice, read the counters again so that the SYNC_SNAP = 0x02 command is executed one more time.
6. ADC Cycle 5. The ADE7912/ADE7913 counters (C_A, C_B, and C_C), latched after the SYNC_SNAP = 0x02 command, are stored in the CNT_SNAPSHOT register and are read in burst mode. They show the same value, ±1 LSB, which means ±1 CLKIN cycle (±244 ns for CLKIN = 4.096 MHz).

$$C_C = C_A \pm 1 = C_B \pm 1$$

7. Reenable protection of the configuration registers by setting the lock register to 0xCA (see the Protecting the Integrity of Configuration Registers section).

The ±1 LSB error may appear because CLKIN, the internal clock of the ADE7912/ADE7913, is asynchronous to the serial port clock generated by the microcontroller and is used to write the COUNTER1 and COUNTER0 values during ADC Cycle 2.

The EMI reduction scheme managed by the EMI_CTRL register (see the DC-to-DC Converter section for details) requires that the ADE7912/ADE7913 devices of the meter system provide coherent samples. This EMI reduction scheme ensures that one ADE7912/ADE7913 device does not generate the PWM signals required to manage the dc-to-dc converter at the same moment as another ADE7912/ADE7913. The ±1 LSB error in the counter synchronization means that at least two ADE7912/ ADE7913 devices generate PWM signals simultaneously for one CLKIN cycle and the EMI reduction scheme may be affected. Although there are no guarantees, both synchronization procedures outlined in this section can be repeated until $C_C = C_A = C_B$.

POWER MANAGEMENT

DC-TO-DC CONVERTER

The dc-to-dc converter section of the ADE7912/ADE7913 works on principles that are common to most modern power supply designs. VDD power is supplied to an oscillating circuit that drives the primary side of a chip scale air core transformer. Power is transferred to the secondary side, where it is rectified to a 3.3 V dc voltage. This voltage is then supplied to the ADC side section through a 2.5 V LDO regulator.

The internal dc-to-dc converter state of the ADE7912/ADE7913 is controlled by the input, VDD. In normal operation mode, maintain V_{DD} between 2.97 V and 3.63 V.

The block diagram of the isolated dc-to-dc converter is shown in Figure 47. The ADE7912/ADE7913 primary supply voltage VDD input supplies an alternative current (ac) source. The ac signal passes through a chip scale air core transformer, and it is transferred to the secondary side. A rectifier then produces the isolated power supply, VDD_{ISO}. Using another chip scale air core transformer, a feedback circuit measures VDD_{ISO} and passes the information back into the VDD domain, where a PWM control block controls the ac source to maintain VDD_{ISO} at 3.3 V.

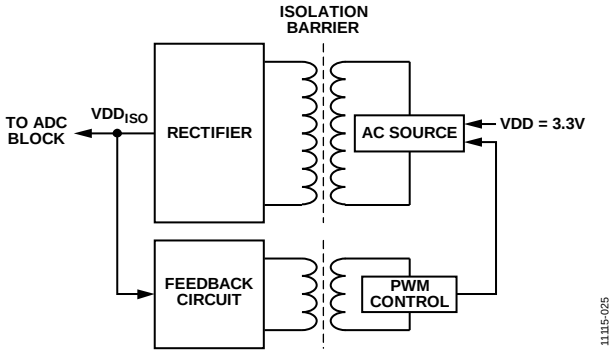


Figure 47. Isolated DC-to-DC Converter Block Diagram

The PWM control block works at a CLKIN/4 (1.024 MHz) clock, and every half period generates a PWM pulse to the ac source (see Figure 48).

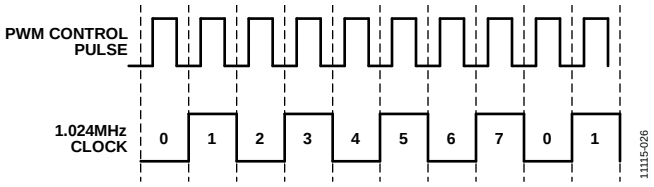


Figure 48. PWM Control Block Generates Pulses Based on a 1.024 MHz Clock

Every time a PWM pulse is generated, the ac source transmits very high frequency signals across the isolation barrier to allow efficient power transfer through the small chip scale transformers. This transfer creates high frequency currents that can propagate in the circuit board ground and power planes, causing edge and dipole radiation. The Layout Guidelines section describes the best PCB layout approach to manage the electromagnetic interference (EMI) issues. In addition to the layout approach, the 8-bit EMI_CTRL register helps to reduce the emissions generated by the ADE7912/ADE7913 dc-to-dc converter.

The clock that manages the PWM control block is divided into eight periodical slots, 0 to 7, as shown in Figure 48. Each bit of the EMI_CTRL register controls one slot: Bit 0 controls Slot 0, Bit 1 controls Slot 1, …, Bit 7 controls Slot 7. When the bit is 1, the default value, the PWM control block generates a pulse. When the bit is 0, the PWM control block does not generate a pulse. The recommendation is to have only four of these bits set to 1 while keeping the others at 0 for every ADE7912/ADE7913 used in the system to further reduce the emissions generated by the ADE7912/ADE7913 dc-to-dc converter.

If the 3-phase energy meter contains four ADE7912/ADE7913 devices, the ADE7912/ADE7913 devices must first be synchronized (see the Synchronizing Multiple ADE7912/ADE7913 Devices section). Then the EMI_CTRL register of every ADE7912/ADE7913 must be initialized. The dc-to-dc converters of only two ADE7912/ADE7913 devices generate EMI at the same moment, lowering the overall EMI level of the meter. Initialize the EMI_CTRL register of the Phase A ADE7912/ADE7913 (EMI_CTRL_A) to 0x55, EMI_CTRL_B to 0xAA, EMI_CTRL_C to 0x55, and EMI_CTRL_N to 0xAA (see Figure 49).

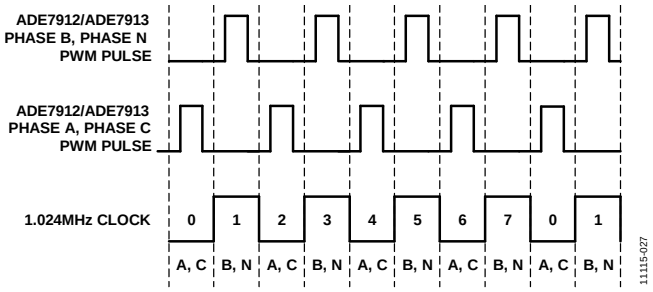


Figure 49. EMI Management of a 3-Phase Meter with Four ADE7912/ADE7913 Devices

If the system contains one, two, or three ADE7912/ADE7913 devices, set four bits to 1 in the EMI_ CTRL register according to the approach shown in Figure 49, while leaving some of the slots unused.

MAGNETIC FIELD IMMUNITY

The ADE7912/ADE7913 are immune to dc magnetic fields because they use air core transformers. The limitation on the ADE7912/ADE7913 ac magnetic field immunity is set by the condition in which the induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition is examined because it is the nominal supply of the ADE7912/ADE7913.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = \left(-\frac{dB}{dt}\right)\sum_{n=1}^{N}\pi r_n^2 \quad (12)$$

where:
B is the ac magnetic field: $B(t) = B \times \sin(\omega t)$.
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil.

Given the geometry of the receiving coil in the ADE7912/ADE7913 and an imposed requirement that the induced voltage, V_{THR}, be at most 50% of the 0.5 V margin at the decoder, a maximum allowable external magnetic field, B, is calculated, as shown in Equation 13 and Figure 50.

$$B = \frac{V_{THR}}{2\pi f \times \sum_{n=1}^{N}\pi r_n^2} \quad (13)$$

where:
f is the frequency of the magnetic field.
B is the amplitude of the ac magnetic field.

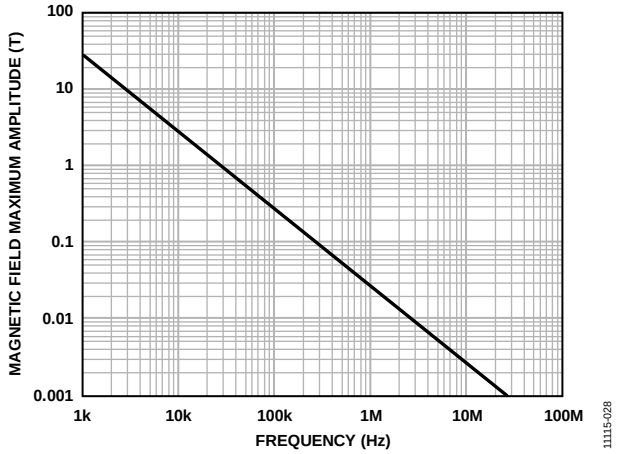


Figure 50. Maximum Allowable External Magnetic Field

For example, at a magnetic field frequency of 10 kHz, the maximum allowable magnetic field of 2.8 T induces a voltage of 0.25 V at the receiving coil. This voltage is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from more than 1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic field values correspond to specific current magnitudes at given distances from the ADE7912/ADE7913 transformers.

$$I = \frac{B}{\mu_0} \times 2\pi d = \frac{V \times d}{\mu_0 \times f \times \sum_{n=1}^{N}\pi r_n^2} \quad (14)$$

where μ_0 is $4\pi \times 10^{-7}$ H/m, the magnetic permeability of the air.

Figure 51 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 51, the ADE7912/ADE7913 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 10 kHz example previously noted, a current with an amplitude of 69 kA placed 3 mm from the ADE7912/ADE7913 is required to affect component operation.

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility (see the Layout Guidelines section).

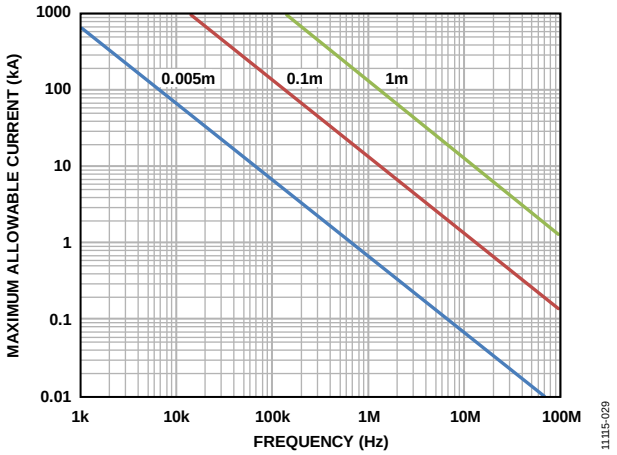


Figure 51. Maximum Allowable Current for Various Current-to-ADE7912/ADE7913 Spacings

POWER-UP AND INITIALIZATION PROCEDURES

At power-up or after a hardware or software reset, the following steps must be executed for a microcontroller managing a system formed by one or multiple ADE7912/ADE7913 devices.

Power-Up Procedure for Systems with a Single ADE7912/ADE7913

For one standalone ADE7912/ADE7913 device managed by a microcontroller, the power-up procedure is as follows (see Figure 52):

1. Connect a crystal between the XTAL1 and XTAL2 pins.
2. Supply V_{DD} to the ADE7912/ADE7913 device. To ensure that the ADE7912/ADE7913 device starts functioning correctly, the supply must reach 3.3 V − 10% in less than 23 ms from approximately a 2.6 V level. The ADE7912/ADE7913 device starts to function.
3. The dc-to-dc converter powers up and supplies the isolated side of the ADE7912/ADE7913. The Σ-Δ modulators become functional. This process takes approximately 100 ms to execute when the recommended capacitors on the VDD_{ISO}, LDO, and REF pins described in Table 9 are used. After this time, the isolated side of the ADE7912/ADE7913 is fully functional.
4. To determine when the ADE7912/ADE7913 device is ready to accept commands, read the STATUS0 register until Bit 0 (RESET_ON) is cleared to 0. This happens approximately 20 ms after the ADE7912/ADE7913 start to function and indicates that the nonisolated side of the ADE7912/ADE7913 is fully functional using the default settings.
5. Initialize the CONFIG register and the EMI_CTRL emissions control register.
6. Protect the user accessible and internal configuration registers by setting the lock register to 0xCA. See the Protecting the Integrity of Configuration Registers section.
7. When the ADC conversion data is available, the ADE7912/ADE7913 device begins generating a signal that is active low at the CLKOUT/$\overline{\text{DREADY}}$ pin for 64 CLKIN cycles (15.625 µs for CLKIN = 4.096 MHz). $\overline{\text{DREADY}}$ functionality is enabled by default at the CLKOUT/$\overline{\text{DREADY}}$ pin.
8. The microcontroller reads the IWV, V1WV, V2WV, ADC_CRC, and STATUS0 registers in SPI burst mode (see the SPI Read Operation in Burst Mode section for more information).

Note that this power-up procedure also applies in the same way to systems that have multiple ADE7912/ADE7913 devices, each clocked from its own crystal. Every ADE7912/ADE7913 device is powered up and started independently.

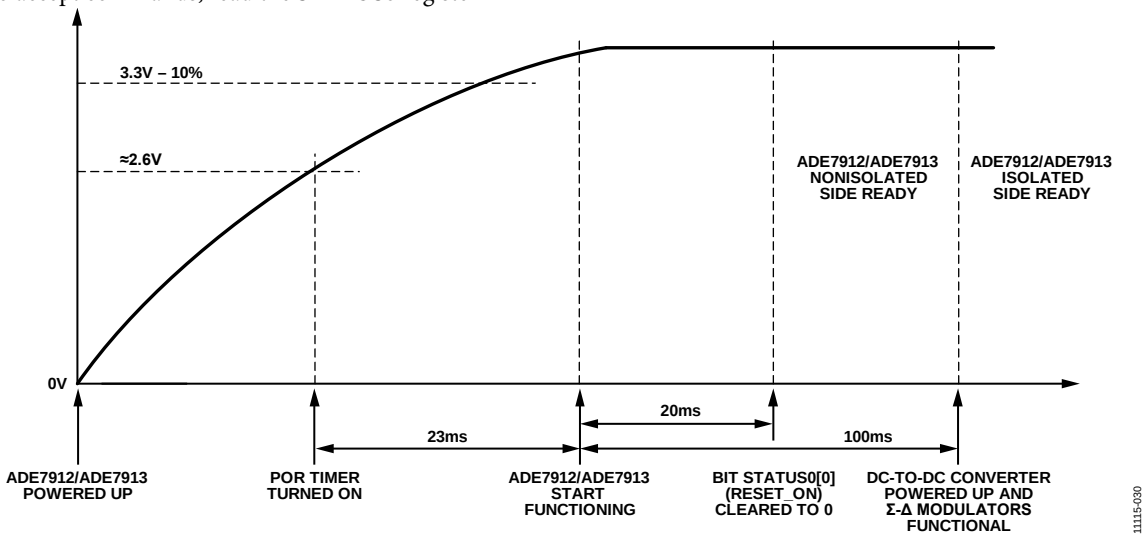


Figure 52. Power-Up Procedure for Systems with One or Multiple ADE7912/ADE7913 Devices, Each Clocked from Its Own Crystal

Power-Up Procedure for Systems with Multiple Devices That Use a Single Crystal

For the polyphase energy meters shown in Figure 35, Figure 37, and Figure 38, in which one single crystal is used, the power-up procedure is as follows (see Figure 53):

1. Supply V_{DD} to the ADE7912/ADE7913 devices. To ensure that the Phase A ADE7912/ADE7913 (labeled $ADE7912_A$/$ADE7913_A$ in Figure 53) device starts functioning correctly, the supply must reach 3.3 V − 10% in less than 23 ms from approximately a 2.6 V level. The $ADE7912_A$/$ADE7913_A$ device is clocked by the 4.096 MHz crystal and starts functioning. The other ADE7912/ADE7913 devices are not clocked yet.
2. The dc-to-dc converter powers up and supplies the isolated side of the $ADE7912_A$/$ADE7913_A$. The Σ-Δ modulators become functional. This process takes approximately 100 ms to execute when the recommended capacitors on the VDD_{ISO}, LDO, and REF pins described in Table 9 are used. After this time, the isolated side of the $ADE7912_A$/$ADE7913_A$ is fully functional.
3. To determine when the $ADE7912_A$/$ADE7913_A$ device is ready to accept commands, the STATUS0 register is read until Bit 0 (RESET_ON) is cleared to 0. This happens approximately 20 ms after the $ADE7912_A$/$ADE7913_A$ start to function and indicates that the nonisolated side of the $ADE7912_A$/$ADE7913_A$ is fully functional using the default settings.
4. Initialize the CONFIG register of the $ADE7912_A$/$ADE7913_A$ with Bit 0 (CLKOUT_EN) set to 1. The CLKOUT signal is provided at the CLKOUT/$\overline{\text{DREADY}}$ pin, and the ADE7912/ADE7913 devices on the other phases are now clocked.
5. Initialize EMI_CTRL, the emissions control register, of the $ADE7912_A$/$ADE7913_A$.
6. The dc-to-dc converters of the other ADE7912/ADE7913 devices power up and supply their isolated sides. The Σ-Δ modulators become functional. This process takes approximately 100 ms to execute when the recommended capacitors on the VDD_{ISO}, LDO, and REF pins described in Table 9 are used. The isolated sides of the ADE7912/ADE7913 devices are now fully functional.
7. Read the STATUS0 registers of the other ADE7912/ADE7913 devices until Bit 0 (RESET_ON) is cleared to 0, indicating that their nonisolated sides are fully functional with default settings. This happens approximately 20 ms after the clock signal is provided.
8. Initialize the CONFIG register of all remaining ADE7912/ADE7913 devices. Select one ADE7912/ADE7913 device (Phase C ADE7912/ADE7913 in Figure 35, Figure 37, and Figure 38 examples; labeled $ADE7912_C$/$ADE7913_C$ in Figure 53) and connect its CLKOUT/$\overline{\text{DREADY}}$ pin to an external interrupt I/O pin of the microcontroller. $ADE7912_C$/$ADE7913_C$ must have Bit 0 (CLKOUT_EN) in the CONFIG register left at the default value of 0 to use the $\overline{\text{DREADY}}$ functionality of the CLKOUT/$\overline{\text{DREADY}}$ pin.
9. Initialize EMI_CTRL, the emissions control register, of all remaining ADE7912/ADE7913 devices.
10. Execute a SYNC_SNAP = 0x01 write broadcast to synchronize all the ADE7912/ADE7913 devices of the meter (see the Synchronizing Multiple ADE7912/ADE7913 Devices sections).
11. Execute a lock = 0xCA write broadcast to protect the configuration registers of all ADE7912/ADE7913 devices. See the Protecting the Integrity of Configuration Registers section.
12. Every couple of seconds, disable the protection of the configuration registers, execute a SYNC_SNAP = 0x02 write broadcast to read the CNT_SNAPSHOT register of every ADE7912/ADE7913, and verify if resynchronization is necessary. Resynchronize the ADE7912/ADE7913 devices that are out of synchronization (see the Synchronizing Multiple ADE7912/ADE7913 Devices section) and then reenable the protection of the configuration registers.

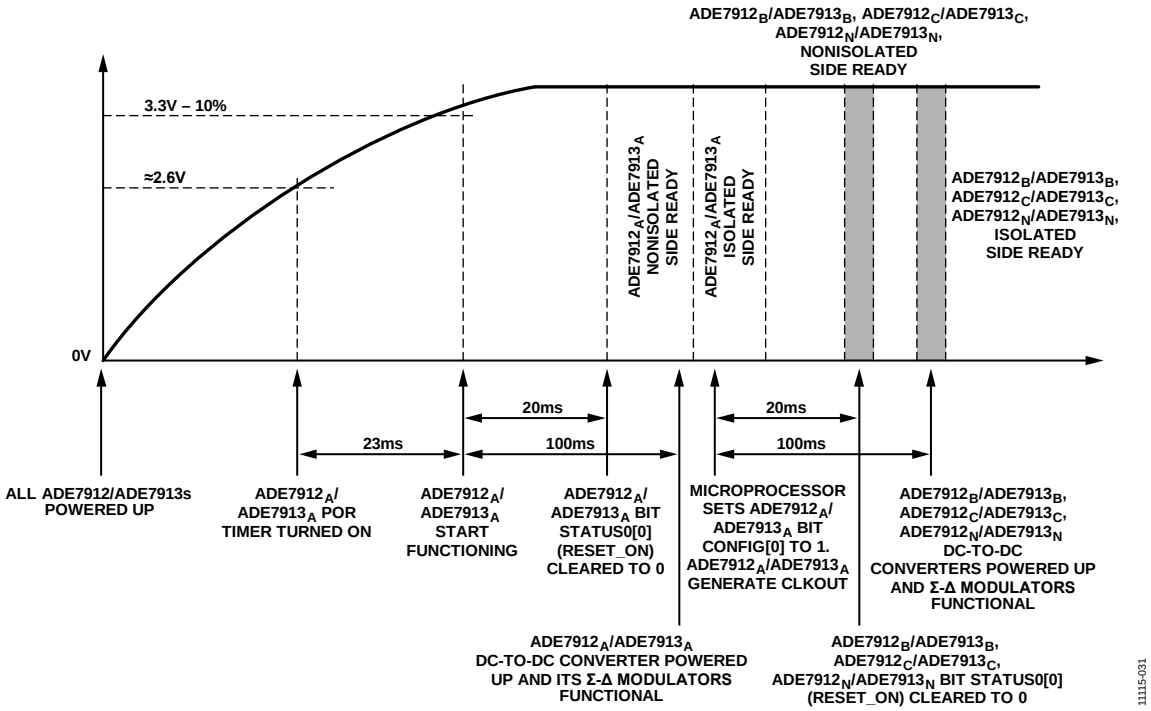


Figure 53. Power-Up Procedure for Systems with Multiple ADE7912/ADE7913 Devices; Only Phase A ADE7912/ADE7913 Are Clocked from a Crystal

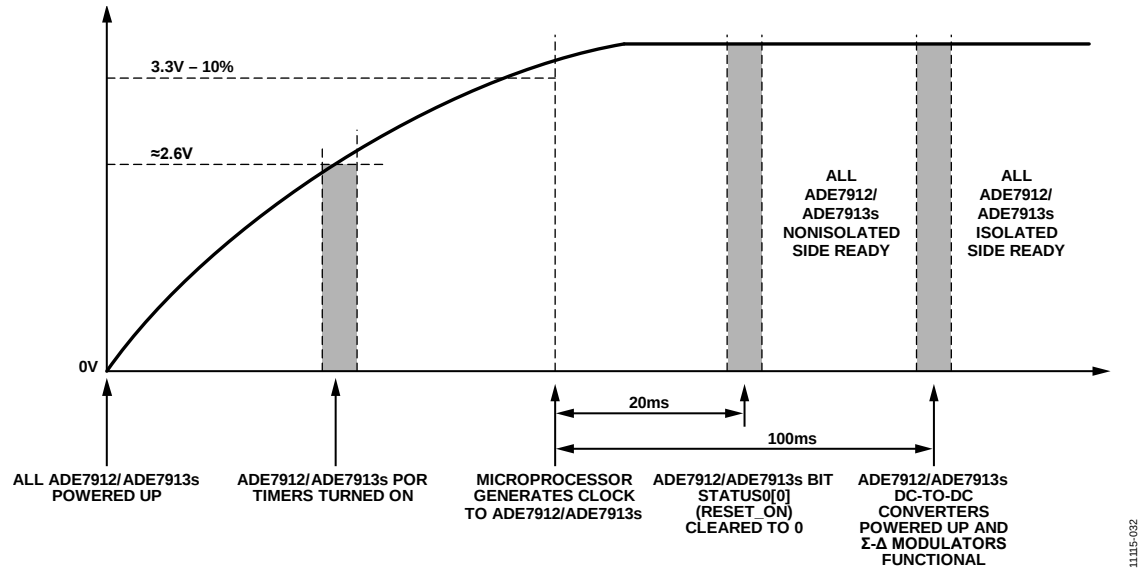


Figure 54. Power-Up Procedure for Systems with Multiple ADE7912/ADE7913 Devices Clocked from a Microcontroller

Power-Up Procedure for Systems with Multiple Devices That Use Clock Generated from Microcontroller

For polyphase energy meters in which the microcontroller generates the clock signal used by all ADE7912/ADE7913 devices (see Figure 36), the power-up procedure is as follows:

1. Supply V_{DD} to the ADE7912/ADE7913 devices. To ensure that the ADE7912/ADE7913 devices start functioning correctly, the supply must reach 3.3 V − 10% in less than 23 ms from approximately a 2.6 V level.
2. Generate the clock signal from the microcontroller to all ADE7912/ADE7913 devices.
3. The dc-to-dc converters power up and supply the isolated side of the ADE7912/ADE7913 devices. The Σ-Δ modulators become functional. This process takes approximately 100 ms to execute when the recommended capacitors on the VDD_{ISO}, LDO, and REF pins described in Table 9 are used. After this time, the isolated sides of the ADE7912/ADE7913 devices are fully functional.
4. Read the STATUS0 registers of the ADE7912/ADE7913 devices until Bit 0 (RESET_ON) is cleared to 0, indicating that the nonisolated side of the ADE7912/ADE7913 devices is fully functional with default settings. This happens approximately 20 ms after the clock signal is provided.
5. Initialize the CONFIG register of the ADE7912/ADE7913 devices with Bit 0 (CLKOUT_EN) cleared to 0 to avoid generating an unnecessary clock at the CLKOUT/$\overline{\text{DREADY}}$ pin. Select one ADE7912/ADE7913 device (Phase C ADE7912/ADE7913 in Figure 36, for example) and connect its CLKOUT/$\overline{\text{DREADY}}$ pin to an external interrupt I/O pin of the microcontroller.
6. Initialize EMI_CTRL, the emissions control register, of all ADE7912/ADE7913 devices.
7. Execute a SYNC_SNAP = 0x01 write broadcast to synchronize all the ADE7912/ADE7913 devices of the meter (see the Synchronizing Multiple ADE7912/ADE7913 Devices sections for details).
8. Execute a lock = 0xCA write broadcast to protect the configuration registers of all ADE7912/ADE7913 devices. See the Protecting the Integrity of Configuration Registers section.
9. Every couple of seconds, disable the registers protection, execute a SYNC_SNAP = 0x02 write broadcast to read the COUNTER1 and COUNTER0 registers of every ADE7912/ADE7913, and verify if resynchronization is necessary. Resynchronize the ADE7912/ADE7913 devices that are out of synchronization (see the Synchronizing Multiple ADE7912/ADE7913 Devices section) and then reenable protection of the configuration registers.

HARDWARE RESET

The ADE7912/ADE7913 do not have a dedicated reset pin. Instead, while the SCLK pin is receiving the serial clock, the $\overline{\text{CS}}$ and MOSI pins can be kept low by executing a SPI broadcast write operation in which the lines are kept low for 64 SCLK cycles. This is equivalent to sending eight bytes equal to 0x00 to the ADE7912/ADE7913 to accomplish a hardware reset.

During a hardware reset, all the registers are set to their default values and the dc-to-dc converter is shut down. This procedure can be done simultaneously for all ADE7912/ADE7913 devices in a polyphase energy meter. At the end of the reset period, the ADE7912/ADE7913 clears Bit 0 (RESET_ON) to 0 in the STATUS0 register. At this point, one of the procedures described in the Power-Up and Initialization Procedures section must be followed to initialize the ADE7912/ADE7913 devices correctly.

SOFTWARE RESET

Bit 6 (SWRST) in the CONFIG register manages the software reset functionality. The default value of this bit is 0. If this bit is set to 1, the ADE7912/ADE7913 enter the software reset state. In this state, all the internal registers are reset to their default values. The dc-to-dc converter continues to function. When the software reset ends, Bit 6 (SWRST) in the CONFIG register clears automatically to 0 and Bit 0 (RESET_ON) in the STATUS0 register is cleared to 0. If the configuration registers are protected using a lock = 0xCA register write, first unlock the registers by writing lock = 0x9C and then write to the CONFIG register by setting Bit 6 (SWRST) to 1 to start a software reset. At this point, one of the procedures described in the Power-Up and Initialization Procedures section must be followed to initialize the ADE7912/ADE7913 correctly.

POWER-DOWN MODE

There are situations in which the ADCs of the ADE7912/ADE7913 do not need to function and it is desirable to lower the current consumption of the device. When set to 1, Bit 2 (PWRDWN_EN) in the CONFIG register turns off the dc-to-dc converter and shuts down the Σ-Δ modulators. Although the ADE7912/ADE7913 configuration registers maintain their values, the IWV, V1WV, and V2WV ADC output registers are in an undefined state. If PWRDWN_EN is cleared to 0, the default value, the dc-to-dc converter is functional and the Σ-Δ modulators are active.

If the microcontroller generates the clock to all ADE7912/ADE7913 devices (the configuration shown in Figure 36), the current consumption can be further reduced by shutting down the clock. The ADE7912/ADE7913 stop functioning. When the clock is restarted, as a good programming practice, execute a hardware reset to restart the ADE7912/ADE7913.

In systems in which the CLKOUT/$\overline{\text{DREADY}}$ pin of one ADE7912/ADE7913 device is used to clock other ADE7912/ADE7913 devices (the configuration shown in Figure 35, Figure 37, and Figure 38), lower current consumption of the ADE7912/ADE7913 devices can be achieved by clearing Bit 0 (CLKOUT_EN) to 0 in the CONFIG register.

LAYOUT GUIDELINES

Figure 20 shows the test circuit of the ADE7912/ADE7913. The test circuit contains three ADE7912/ADE7913 devices together with the surrounding circuitry required to sense the phase currents and voltages in a 3-phase system. The ADE7912/ADE7913 devices are managed by a microcontroller using the SPI interface. The microcontroller is not shown in the schematic. Figure 20 replicates the schematic of the ADE7913 evaluation board (see the ADE7913 Evaluation Board section).

Figure 55 and Figure 56 show a proposed layout of a printed circuit board (PCB) with two layers that have the components placed on the top of the board only. Follow these layout guidelines to create a low noise design with higher immunity to EMC influences. Note that the layout is cropped from a board containing other circuitry besides the three ADE7913 devices.

The layout of an ADE7912-based meter is very similar to the one designed for the ADE7913. The only difference is the absence of the V2P voltage channel, which means the absence of the related circuitry: the resistor divider and the protection diodes.

The primary supply voltage is supplied at VDD, Pin 19. Place a 10 µF decoupling capacitor and a 100 nF ceramic decoupling capacitor between the VDD pin and GND, Pin 20. The 10 µF capacitor must be placed in close proximity to the part, but the ceramic capacitor must be placed closer to the ADE7912/ADE7913 because it decouples the high frequency noise.

Use a 10 µF capacitor and a 100 nF ceramic capacitor to decouple VDD_{ISO}, Pin 1, from GND_{ISO}, Pin 2. Apply the same rules in the placement of these capacitors as for the VDD pin.

Use a 4.7 µF capacitor and a 100 nF, ceramic capacitor to decouple LDO, Pin 8, and REF, Pin 9, from GND_{ISO}, Pin 10. Use the same rules in the placement of these capacitors as for the VDD pin.

Note that the ADE7912/ADE7913 isolated ground point is one of the shunt poles. This point is directly connected to GND_{ISO}, Pin 10. There is no need to connect the shunt ground pole to GND_{ISO}, Pin 2. Pin 2 is internally connected to Pin 10.

The crystal load capacitors must be placed closest to the ADE7912/ADE7913, whereas the crystal can be placed in close proximity.

Note that the bottom layer extends the ground of the primary side below the ADE7912/ADE7913 and the related circuitry. A distance of at least 8 mm is maintained on the bottom layer between the input pins on the board and the primary side ground plane.

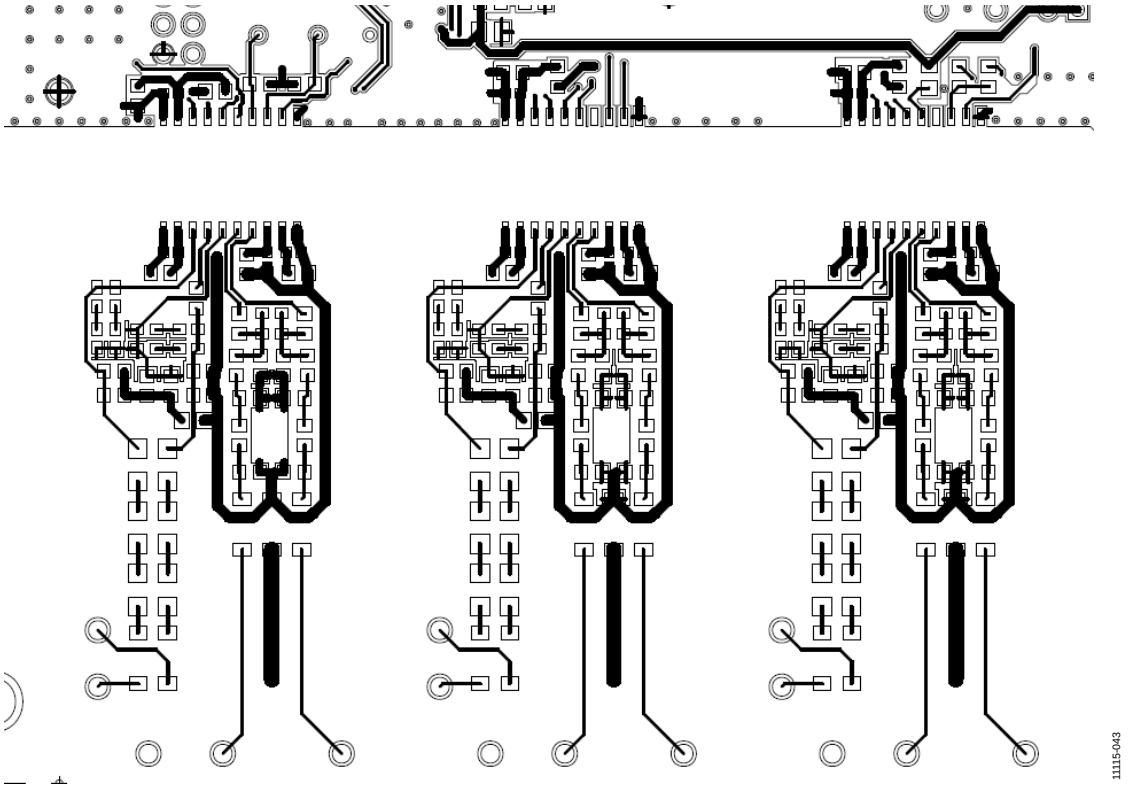


Figure 55. 2-Layer Circuit Board: Top Layer

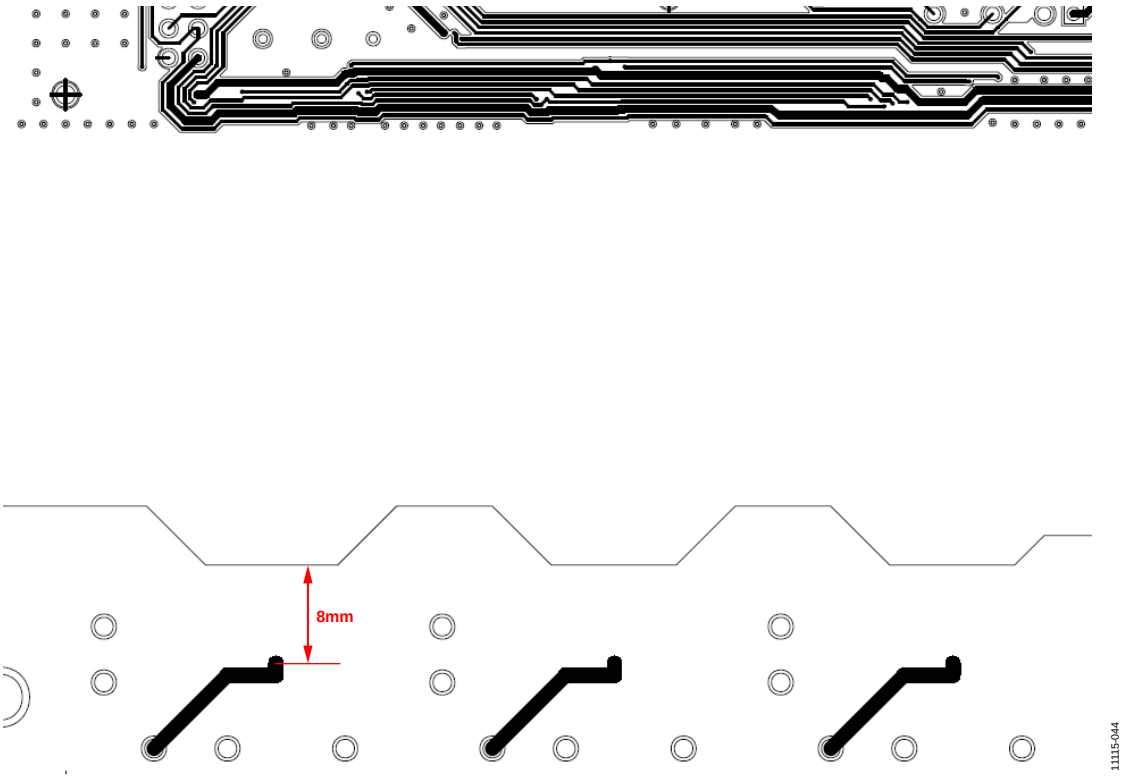


Figure 56. 2-Layer Circuit Board: Bottom Layer

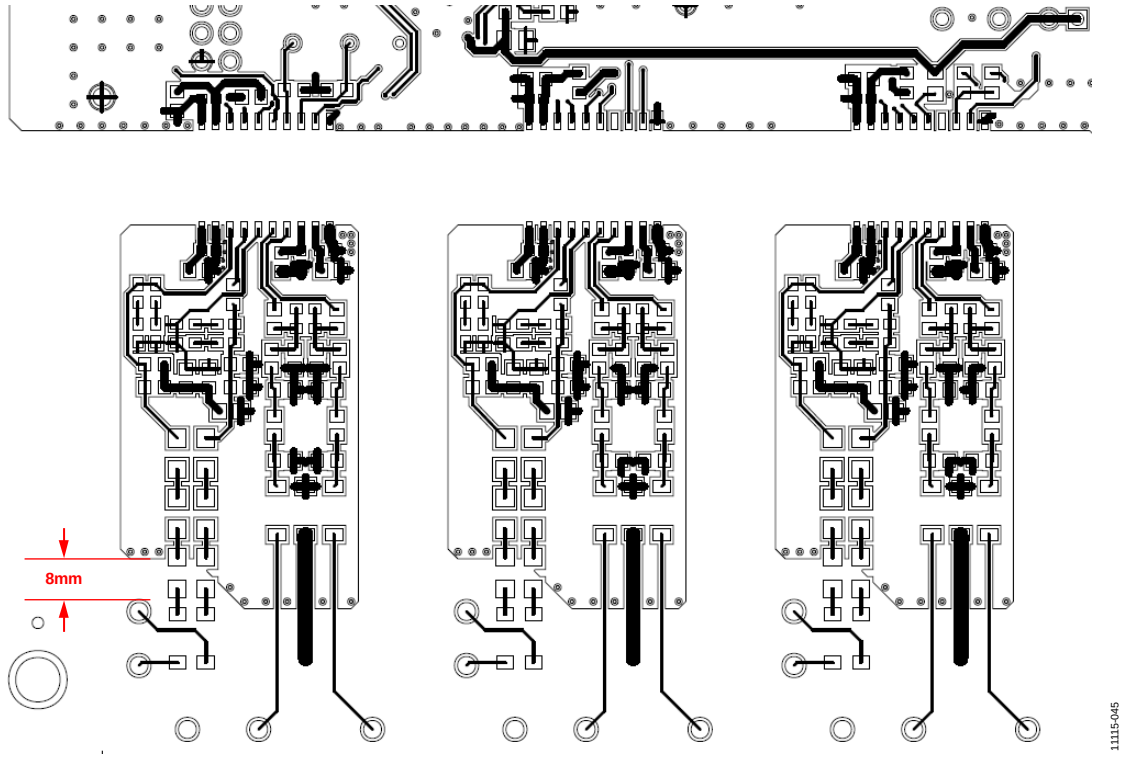


Figure 57. 4-Layer Circuit Board: Top Layer

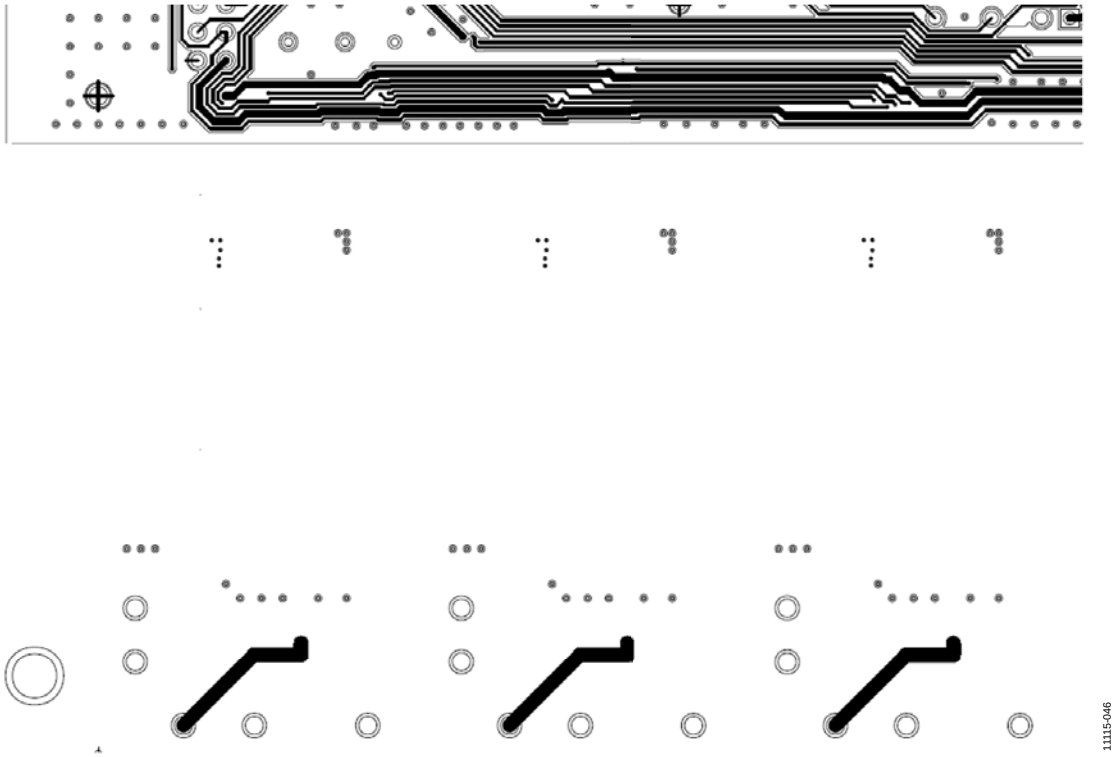


Figure 58. 4-Layer Circuit Board: Bottom Layer

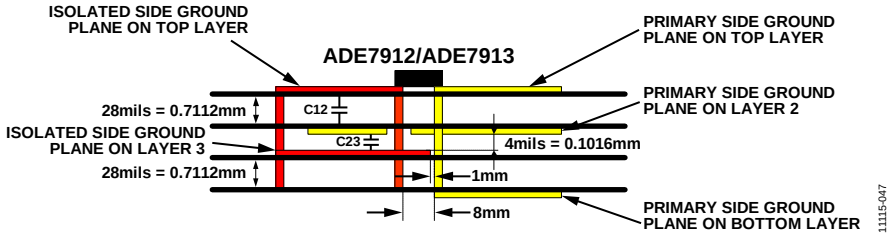


Figure 59. Stitching Capacitors Created by 4-Layer PCB

If a 4-layer PCB is used, additional stitching capacitors can be created. On the top layer, all components placed on the isolated secondary side are surrounded by a ground plane connected to GND_{ISO}, Pin 10 (see Figure 57). Layer 2 (see Figure 60) replicates the bottom layer of the 2-layer circuit board approach, extending the ground of the primary side below the ADE7912/ADE7913 and the related circuitry. Layer 3 (see Figure 61) replicates the ground plane of the top layer. The bottom layer does not have the ground of the primary side below the ADE7912/ADE7913 and the related circuitry as in the 2-layer circuit board approach because the corresponding stitching capacitor created with Layer 3 does not have any effect in reducing the emissions.

The structure of the stitching capacitors created by a 4-layer PCB is shown in Figure 59. The isolated ground plane of the top layer creates the 10 pF capacitor (C12) with the primary side ground plane placed on Layer 2. In a similar manner, the 400 pF (C23) capacitor is created between Layer 2 and Layer 3.

These capacitances have an important role in reducing the emissions generated by the ADE7912/ADE7913 dc-to-dc converter.

ADE7913 EVALUATION BOARD

An evaluation board built upon the ADE7913 allows users to quickly evaluate this IC. It is used in conjunction with the system demonstration platform (EVAL-SDP-CB1Z). Order both the ADE7913 evaluation board and the system demonstration platform to evaluate the ADE7913. Visit www.analog.com/ADE7913 for details.

ADE7912/ADE7913 VERSION

Bits[2:0] (version) in the STATUS1 register identify the version of the ADE7912/ADE7913.

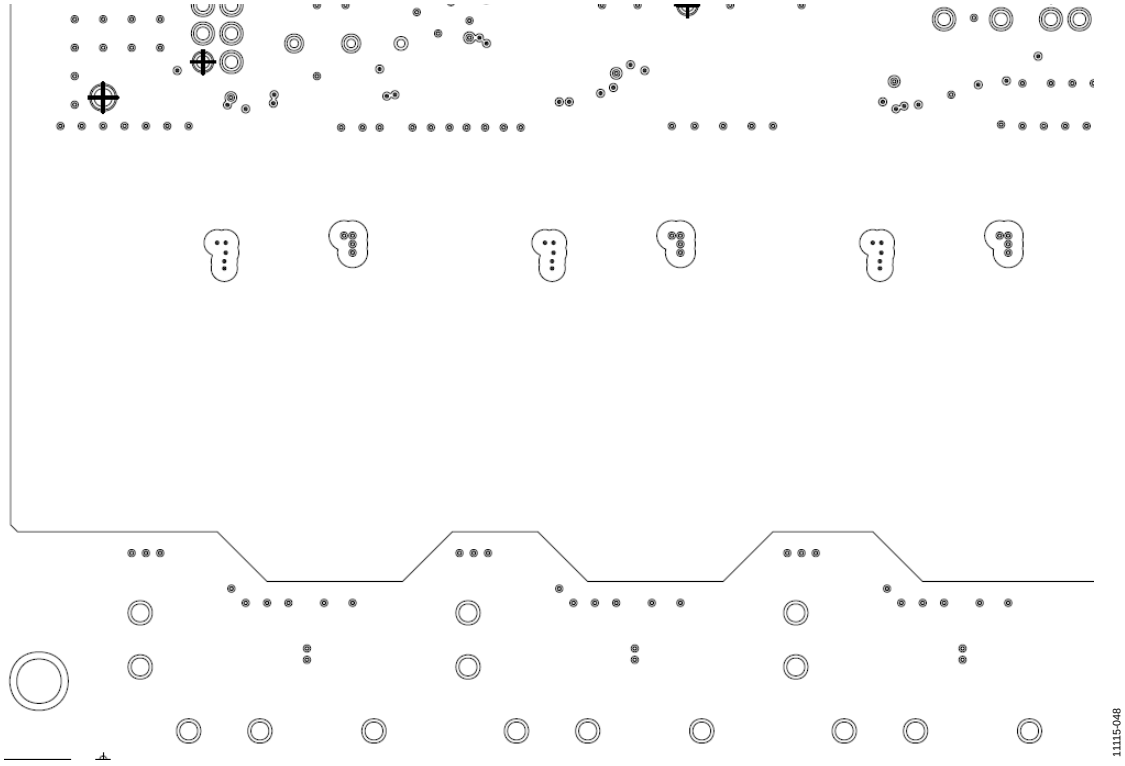


Figure 60. 4-Layer Circuit Board: Layer 2

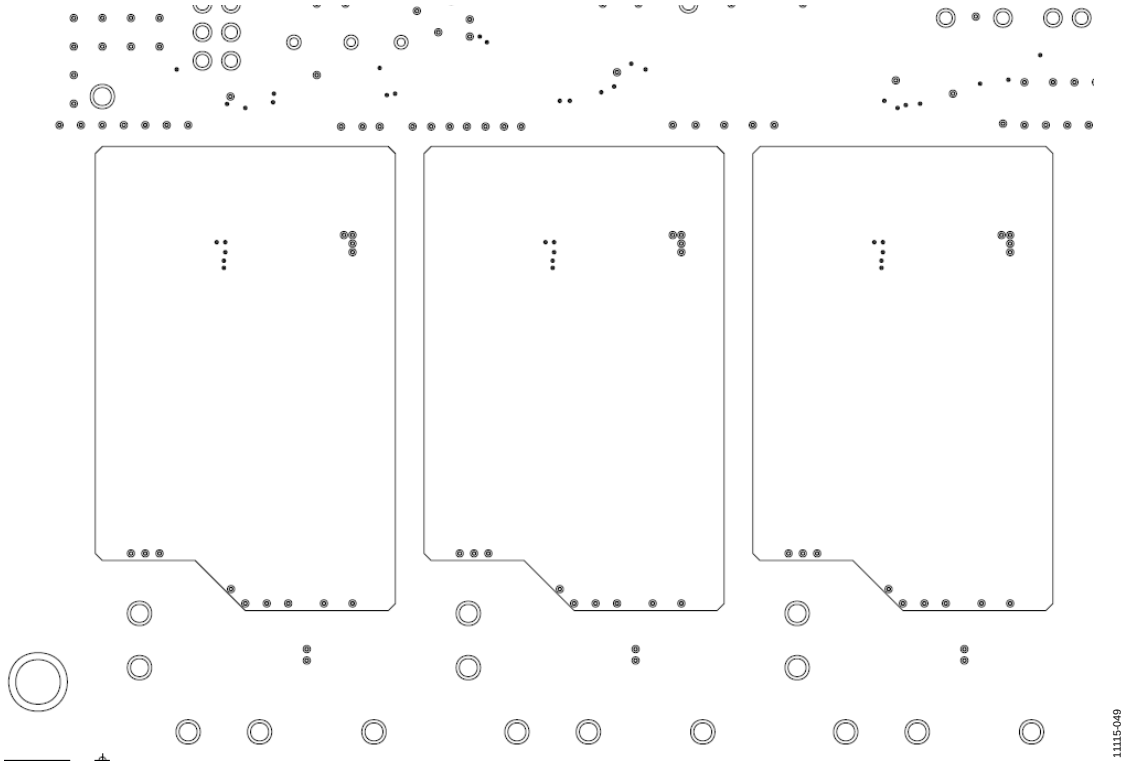


Figure 61. 4-layer Circuit Board: Layer 3

REGISTER LIST

In Table 13 to Table 20, R means a register can be read, and W means a register can be written. U means an unsigned register, and S means a signed register in twos complement format.

Table 13. Register List

Address	Register Name	R/W	Bit Length	Type	Default Value	Description
0x0	IWV	R	24	S	0x000000	Instantaneous value of Current I.
0x1	V1WV	R	24	S	0x000000	Instantaneous value of Voltage V1.
0x2	V2WV	R	24	S	0x000000	Instantaneous value of Voltage V2.
0x3	Reserved	R	24	S	0x000000	Reserved. This location always reads 0x000000.
0x4	ADC_CRC	R	16	U	N/A	CRC value of IWV, V1WV, and V2WV registers. See the ADC Output Values CRC section for details.
0x5	CTRL_CRC	R	16	U	N/A	CRC value of configuration registers. See the CRC of Configuration Registers for details.
0x6	Reserved	R	16	S	0x0000	Reserved. This location always reads 0x0000.
0x7	CNT_SNAPSHOT	R	16	U	0x00	Snapshot value of the counter used in synchronization operation. See Table 14 and the Synchronizing Multiple ADE7912/ADE7913 Devices section for details.
0x8	CONFIG	R/W	8	U	0	Configuration register. See Table 15 for details.
0x9	STATUS0	R	8	U	0x01	Status register. See Table 16 for details.
0xA	Lock	W	8	U	0x00	Memory protection register. See the Protecting the Integrity of Configuration Registers section and Table 17 for details.
0xB	SYNC_SNAP	W	8	U	0x00	Synchronization register. See Table 18 for details.
0xC	COUNTER0	R/W	8	U	N/A	Contains the least significant eight bits of the internal synchronization counter.
0xD	COUNTER1	R/W	8	U	N/A	COUNTER1[3:0] bits contain the most significant four bits of the internal synchronization counter. See the Synchronizing Multiple ADE7912/ADE7913 Devices section for details.
0xE	EMI_CTRL	R/W	8	U	0xFF	EMI control register. Manages the PWM control block of the isolated dc-to-dc converter to reduce EMI emissions (see Table 19 and the DC-to-DC Converter section for details).
0xF	STATUS1	R	8	U	0x00	Status register. See Table 20 for details.
0x10, 0x11	Reserved	R/W	8	U	0x00	For proper operation, do not write to these registers.
0x12, 0x13	Reserved	R	8	U	0x00	Reserved registers.
0x14	Reserved					No functionality assigned at this address.
0x15, 0x16, 0x17	Reserved	R	8	U	0x00	Reserved registers.
0x18	TEMPOS	R	8	S	N/A	Temperature sensor offset. See the Temperature Sensor section for more information.

Table 14. CNT_SNAPSHOT Register (Address 0x7)

Bit Location	Bit Name	Default Value	Description
11:0	Counter	0x000	Snapshot value of the counter used in synchronization operation.
15:12	Reserved	0000	Reserved. These bits do not represent any functionality.

Table 15. CONFIG Register (Address 0x8)

Bit Location	Bit Name	Default Value	Description
0	CLKOUT_EN	0	Enables CLKOUT functionality at the CLKOUT/$\overline{\text{DREADY}}$ pin. When CLKOUT_EN = 0, the default value, $\overline{\text{DREADY}}$ functionality is enabled. When CLKOUT_EN = 1, CLKOUT functionality is enabled.
1	Reserved	0	Reserved. This bit does not manage any functionality.
2	PWRDWN_EN	0	Shuts down the dc-to-dc converter. When PWRDWN_EN = 0, the default value, the dc-to-dc converter is functional and the Σ-Δ modulators are active. When PWRDWN_EN = 1, the dc-to-dc converter is turned off and the Σ-Δ modulators are shut down.
3	TEMP_EN	0	This bit selects the second voltage channel measurement. When the TEMP_EN bit is set to 0, the default value, the voltage between the V2P and VM pins is measured. When this bit is 1, the internal temperature sensor is measured (see the Temperature Sensor section for more information). In the case of the ADE7912, the internal temperature sensor is always measured, and this bit does not have any significance.
5:4	ADC_FREQ	00	These bits select the ADC output frequency. 00 = 8 kHz, 125 µs period. 01 = 4 kHz, 250 µs period. 10 = 2 kHz, 500 µs period. 11 = 1 kHz, 1 ms period.
6	SWRST	0	When this bit is set to 1, a software reset is initiated. This bit clears itself to 0 after one CLKIN cycle.
7	BW	0	Selects the bandwidth of the digital low-pass filter of the ADC. When BW = 0, the default value, the bandwidth is 3.3 kHz. When BW = 1, the bandwidth is 2 kHz. The bandwidth data is for CLKIN = 4.096 MHz and an ADC output frequency of 8 kHz. See the Analog-to-Digital Conversion section for details on how CLKIN and the ADC output frequency influence the bandwidth selection.

Table 16. STATUS0 Register (Address 0x9)

Bit Location	Bit Name	Default Value	Description
0	RESET_ON	1	During reset, the RESET_ON bit is set to 1. When the reset ends and the ADE7912/ADE7913 are ready to be configured, the RESET_ON bit is cleared to 0.
1	CRC_STAT	0	If the CRC of the configuration registers changes value, CRC_STAT bit is set to 1.
2	IC_PROT	0	If the configuration registers are not protected, this bit is 0. After the configuration registers are protected (lock register = 0xCA), this bit is set to 1.
7:3	Reserved	0	Reserved. These bits do not represent any functionality.

Table 17. Lock Register (Address 0xA)

Bit Location	Bit Name	Default Value	Description
7:0	LOCK_KEY	00000000	When the LOCK_KEY bits are equal to 0xCA, protection of the configuration registers is enabled. When the LOCK_KEY bits are equal to 0x9C, the protection is disabled and the configuration registers can be written. This is a write only register. If the address location is read, the value is 0x00.

Table 18. SYNC_SNAP Register (Address 0xB)

Bit Location	Bit Name	Default Value	Description
0	Sync	0	When the sync bit is set to 1 via a broadcast SPI write operation, the ADE7912/ADE7913 devices in the system generate ADC outputs in the same exact moment. The bit clears itself back to 0 after one CLKIN cycle. See the Synchronizing Multiple ADE7912/ADE7913 Devices section for more details.
1	Snap	0	When snap is set to 1 via a broadcast SPI write operation, the internal counters of the ADE7912/ADE7913 devices in the system are latched. The bit clears itself back to 0 after one CLKIN cycle. See the Synchronizing Multiple ADE7912/ADE7913 Devices section for more details.
7:2	Reserved	0	Reserved. These bits do not represent any functionality.

Table 19. EMI_CTRL Register (Address 0xE)

Bit Location	Bit Name	Default Value	Description
0	SLOT0	1	Controls the PWM control block pulse during Slot 0 of the CLKIN/4 clock (see the DC-to-DC Converter section for details).
1	SLOT1	1	Controls the PWM control block pulse during Slot 1 of the CLKIN/4 clock.
2	SLOT2	1	Controls the PWM control block pulse during Slot 2 of the CLKIN/4 clock.
3	SLOT3	1	Controls the PWM control block pulse during Slot 3 of the CLKIN/4 clock.
4	SLOT4	1	Controls the PWM control block pulse during Slot 4 of the CLKIN/4 clock.
5	SLOT5	1	Controls the PWM control block pulse during Slot 5 of the CLKIN/4 clock.
6	SLOT6	1	Controls the PWM control block pulse during Slot 6 of the CLKIN/4 clock.
7	SLOT7	1	Controls the PWM control block pulse during Slot 7 of the CLKIN/4 clock.

Table 20. STATUS1 Register (Address 0xF)

Bit Location	Bit Name	Default Value	Description
2:0	Version	0	The ADE7912/ADE7913 version number.
3	ADC_NA	0	If the ADC outputs are not accessed during one ADC output period, the ADC_NA bit is set to 1. When the STATUS1 register is read, the bit is cleared to 0.
6:4	Reserved	0	Reserved. These bits do not represent any functionality.
7	Reserved	0	Reserved. Internal functionality is associated with this bit.

OUTLINE DIMENSIONS

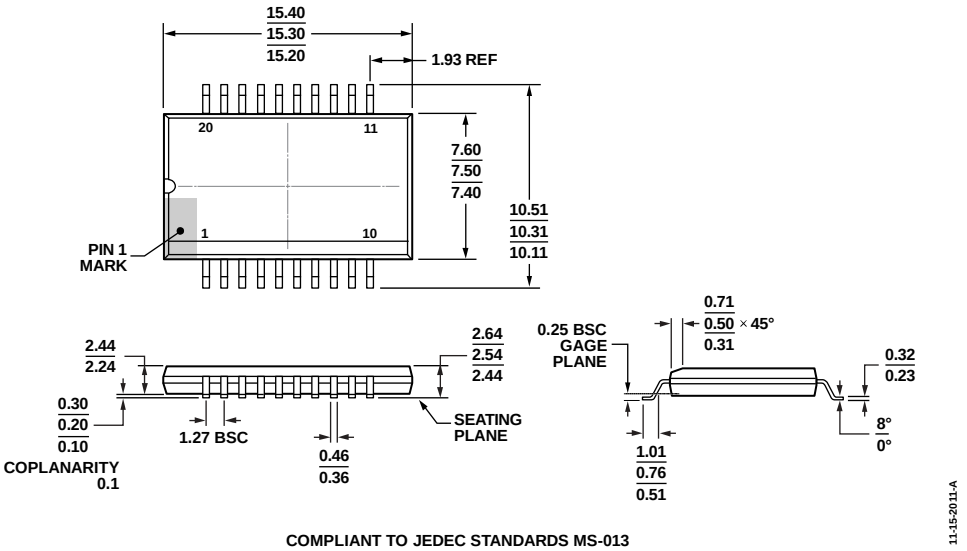


Figure 62. 20-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADE7912ARIZ	−40°C to +85°C	20-Lead SOIC_IC	RI-20-1
ADE7912ARIZ-RL	−40°C to +85°C	20-Lead SOIC_IC, 13″ Tape and Reel	RI-20-1
ADE7913ARIZ	−40°C to +85°C	20-Lead SOIC_IC	RI-20-1
ADE7913ARIZ-RL	−40°C to +85°C	20-Lead SOIC_IC, 13″ Tape and Reel	RI-20-1
EVAL-ADE7913EBZ		Evaluation Board	
EVAL-SDP-CB1Z		Evaluation System Controller Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-SDP-CB1Z is the controller board that manages the EVAL-ADE7913EBZ evaluation board. Both boards must be ordered together.

D11115-0-11/13(0)