16M x 4-Bit Dynamic RAM
(4k & 8k Refresh, EDO-version)

HYB 3164405J/T(L) -50/-60
HYB 3165405J/T(L) -50/-60

Preliminary Information

- 16 777 216 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  $\overline{RAS}$ access time:
  50 ns (-50 version)
  60 ns (-60 version)
  Cycle time:
  84 ns (-50 version)
  104 ns (-60 version)
  $\overline{CAS}$ access time:
  13 ns (-50 version)
  15 ns (-60 version)
- Hyper page mode (EDO) cycle time
  20 ns (-50 version)
  25 ns (-60 version)
- Single + 3.3 V (± 0.3V) power supply
- Low power dissipation
  max. 396 active mW (HYB 3164405J/T(L)-50)
  max. 360 active mW (HYB 3164405J/T(L)-60)
  max. 504 active mW (HYB 3165405J/T(L)-50)
  max. 432 active mW (HYB 3165405J/T(L)-60)
  7.2 mW standby (TTL)
  720 W standby (MOS)
  14.4 mW Self Refresh (L-version only)
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR), $\overline{RAS}$-only refresh, hidden refresh and self refresh modes
- Hyper page mode (EDO) capability
- 8192 refresh cycles/128 ms , 13 R/ 11C addresses (HYB 3164405J/T(L))
- 4096 refresh cycles/ 64 ms , 12 R/ 12C addresses (HYB 3165405J/T(L))
- Plastic Package:

P-SOJ-34-1	500 mil	HYB 3164(5)400J
P-TSOPII-34-1	500 mil	HYB 3164(5)400T

This HYB3164(5)405 is a 64 MBit dynamic RAM organized 16 777 216 by 4 bits. The device is fabricated in SIEMENS/IBM most advanced first generation 64Mbit CMOS silicon gate process technology. The circuit and process design allow this device to achieve high performance and low power dissipation. The HYB3164(5)405 operates with a single 3.3 +/-0.3V power supply and interfaces with either LVTTL or LVCMOS levels. Multiplexed address inputs permit the HYB 3164(5)400J/T to be packaged in a 500mil wide SOJ-34 or TSOP-34 plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment.The HYB3164(5)405TL parts have a very low power „sleep mode" supported by Self Refresh.

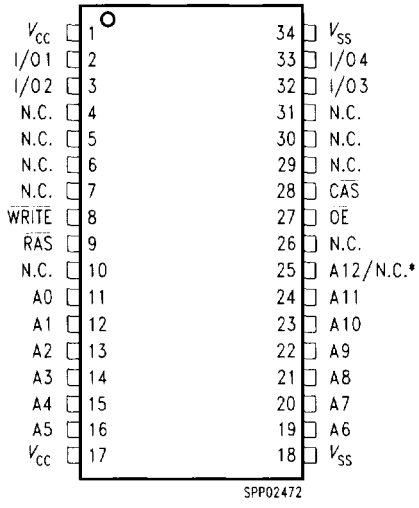
Ordering Information

Type	Ordering Code	Package		Descriptions
HYB 3164405J-50	on request	P-SOJ-34-1	500 mil	DRAM (access time 50 ns)
HYB 3164405J-60	on request	P-SOJ-34-1	500 mil	DRAM (access time 60 ns)
HYB 3164405T-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3164405T-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)
HYB 3164405TL-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3164405TL-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)
HYB 3165405J-50	on request	P-SOJ-34-1	500 mil	DRAM (access time 50 ns)
HYB 3165405J-60	on request	P-SOJ-34-1	500 mil	DRAM (access time 60 ns)
HYB 3165405T-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3165405T-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)
HYB 3165405TL-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3165405TL-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)

Pin Names

A0-A12	Address Inputs for HYB 3164405J/T(L)
A0-A11	Address Inputs for HYB 3165405J/T(L)
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
Vcc	Power Supply (+ 3.3V)
Vss	Ground

P-SOJ-34-1 (500 mil)
P-TSOPII-34-1 (500 mil)

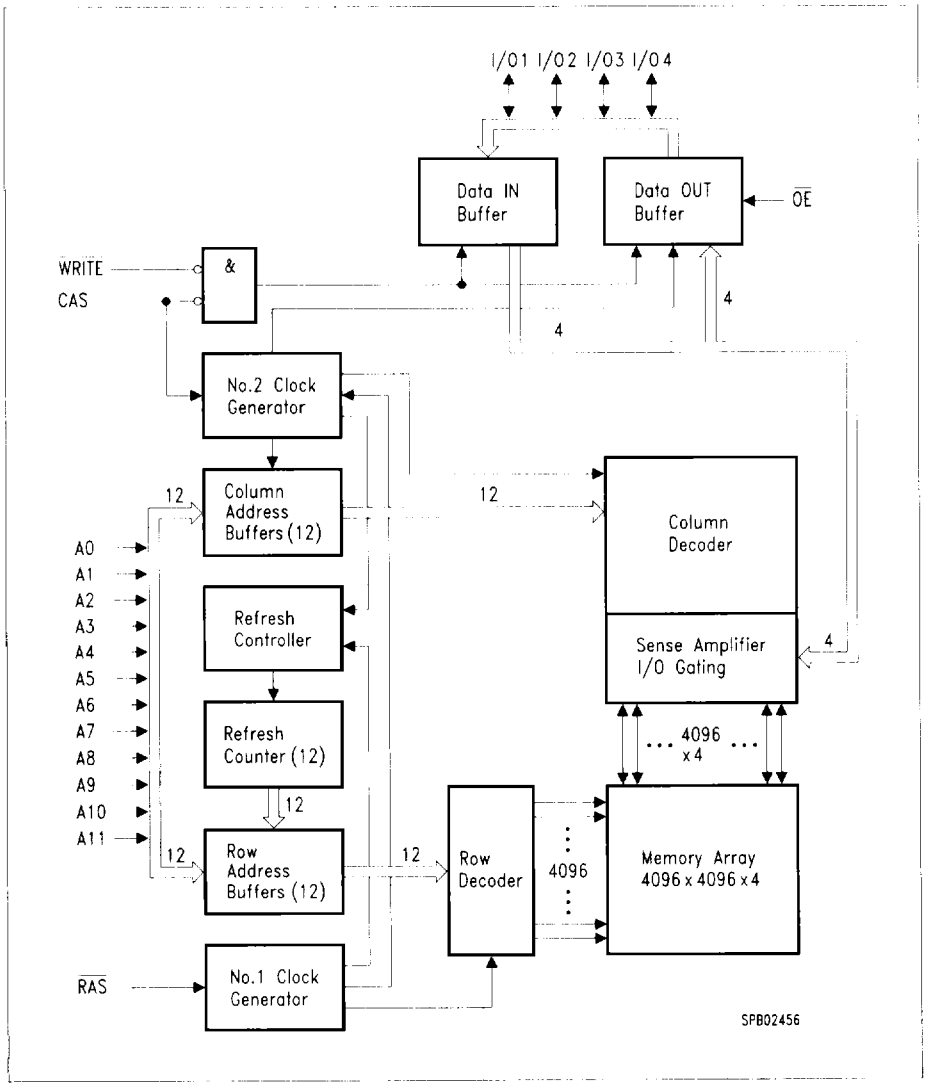


* Pin 25 is A12 for HYB 3164400J/T and N.C. for HYB 3165400J/T

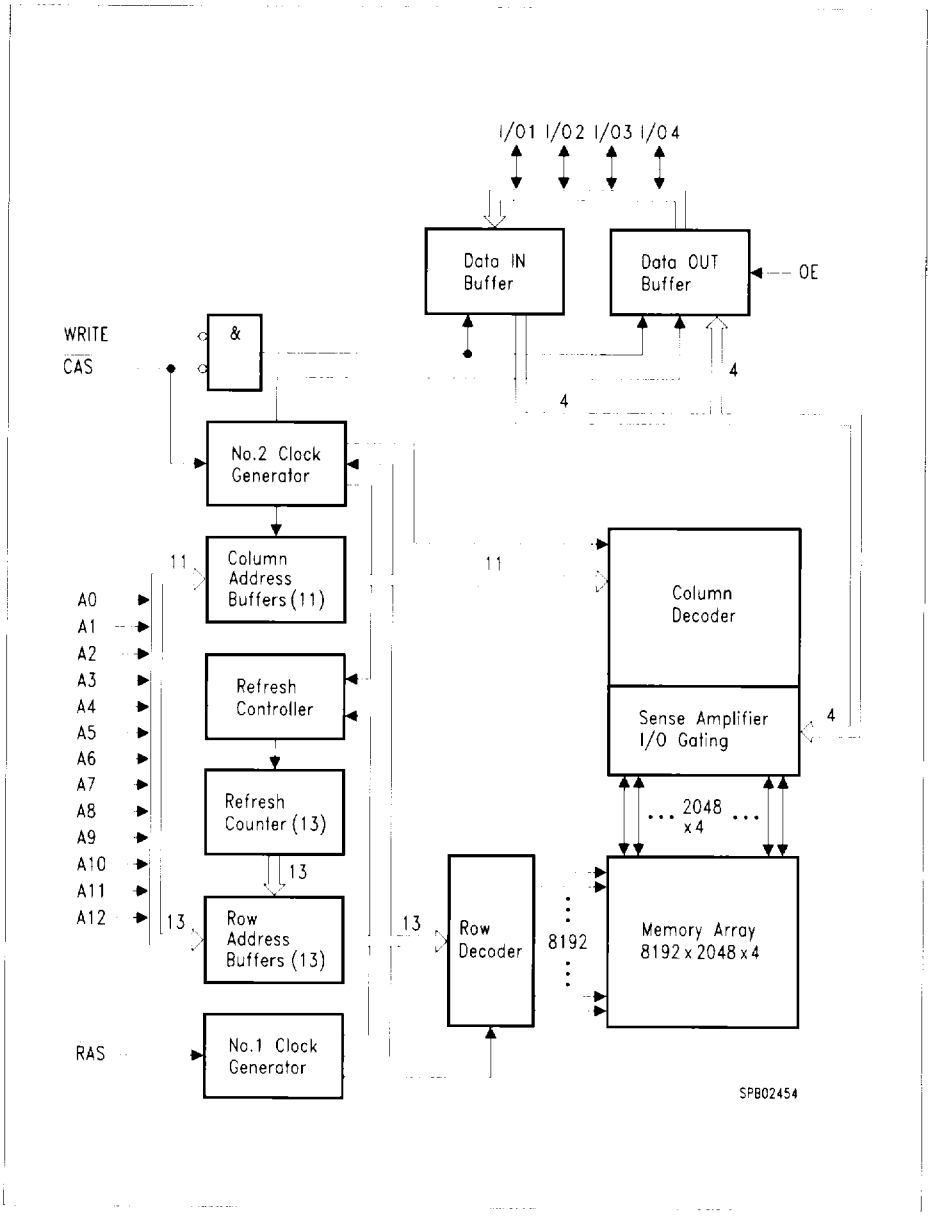
Pin Configuration

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WRITE}$	$\overline{OE}$	ROW ADDR	COL ADDR	I/O1-I/O4
Standby		H	H - X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Delayed-Write		L	L	H - L	H	ROW	COL	Data In
Read-Modify-Write		L	L	H - L	L - H	ROW	COL	Data Out, Data In
Hyper Page Mode Read	1st Cycle	L	H - L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H - L	H	L	n/a	COL	Data Out
Hyper Page Mode Write	1st Cycle	L	H - L	L	X	ROW	COL	Data In
	2nd Cycle	L	H - L	L	X	n/a	COL	Data In
Hyper Page Mode RMW	1st Cycle	L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
	2st Cycle	L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
$\overline{RAS}$ only refresh		L	H	X	X	ROW	n/a	High Impedance
$\overline{CAS}$-before-$\overline{RAS}$ refresh		H - L	L	H	X	X	n/a	High Impedance
Test Mode Entry		H - L	L	L	X	X	n/a	High Impedance
Hidden Refresh	READ	L-H-L	L	H	L	ROW	COL	Data Out
	WRITE	L-H-L	L	L	X	ROW	COL	Data In
Self Refresh (L-version only)		H - L	L	H	X	X	X	High Impedance



Block Diagram for HYB 3164405J/T(L)



Block Diagram for HYB 3165405J/T(L)

Absolute Maximum Ratings

Operating temperature range.....0 to 70 °C

Storage temperature range.....– 55 to 150 °C

Input/output voltage.....-0.5 to min (Vcc+0.5,4.6) V

Power supply voltage.....-0.5V to 4.6 V

Power dissipation.....1.0 W

Data out current (short circuit).....50 mA

Note

Stresses above those listed under „Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, (values in brackets for HYB 3165405J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	1)
Input low voltage	V_{IL}	– 0.3	0.8	V	1)
Output high voltage (LVTTL) Output „H" level voltage (Iout = -2mA)	V_{OH}	2.4	–	V	
Output low voltage (LVTTL) Output „L"level voltage (Iout = +2mA)	V_{OL}	–	0.4	V	
Output high voltage (LVCMOS) Output „H" level voltage (Iout = -100uA)	V_{OH}	Vcc-0.2	-	V	
Ouput low voltage (LVCMOS) Output „L" level voltage (Iout = +100uA)	V_{OL}	-	0.2	V	
Input leakage current,any input (0 V < Vin < Vcc , all other pins = 0 V	$I_{I(L)}$	– 2	2	µA	
Output leakage current (DO is disabled, 0 V < Vout < Vcc)	$I_{O(L)}$	– 2	2	µA	
Average Vcc supply current:	I_{CC1}				
-50 ns version		–	110 (140)	mA	2) 3) 4)
-60 ns version		–	100 (120)	mA	
($\overline{RAS}$, $\overline{CAS}$, address cycling: tRC = tRC min.)					
Standby Vcc supply current ($\overline{RAS}$=$\overline{CAS}$= Vih)	I_{CC2}	–	2	mA	–

DC Characteristics *(cont'd)*

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, (values in brackets for HYB 3165405J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average Vcc supply current, during RAS-only refresh cycles: -50 ns version	I_{CC3}	–	110 (140)	mA	2) 4)
-60 ns version		–	100 (120)	mA	
(RAS cycling: CAS = VIH: tRC = tRC min.)					
Average Vcc supply current, during hyperpage mode (EDO): -50 ns version	I_{CC4}	–	115 (150)	mA	2) 3) 4)
-60 ns version		–	100 (120)	mA	
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: tHPC=tHPC min.)					
Standby Vcc supply current ($\overline{RAS}$=$\overline{CAS}$= Vcc-0.2V)	I_{CC5}	–	200	A	–
Average Vcc supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -50 ns version	I_{CC6}	–	110 (140)	mA	2) 4)
-60 ns version		–	100 (120)	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling: tRC = tRC min.)					
Self Refresh Current (L-version only) Average Power Supply Current during Self Refresh. ($\overline{CBR}$ cycle with tRAS>TRASSmin, $\overline{CAS}$ held low, $\overline{WE}$ = Vcc-0.2V, Address and Din=Vcc-0.2V or 0.2V)	I_{CC7}	–	400	A	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,A12)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O4)	C_{IO}	–	7	pF

AC Characteristics 5)6)

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V , t_T = 2 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
common parameters							
Random read or write cycle time	t_{RC}	84	–	104	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	–	40	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	100k	60	100k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10k	10	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	8	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	12	30	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	45		50	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	7
Refresh period for HYB3164405	t_{REF}	–	128	–	128	ms	
Refresh period for HYB3165405	t_{REF}	–	64	–	64	ms	
Read Cycle							
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	ns	8,10
$\overline{OE}$ access time	t_{OEA}	–	13	–	15	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	11

AC Characteristics *(cont'd)* 5)6)

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V , t_T = 2 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	12
Data to $\overline{CAS}$ low delay	t_{DZC}	0	–	0	–	ns	13
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	t_{CDD}	13	–	15	–	ns	14
$\overline{OE}$ high to data delay	t_{ODD}	13	–	15	–	ns	14
Write Cycle							
Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	7	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	8	–	10	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8	–	10	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	16
Data hold time	t_{DH}	7	–	10	–	ns	16
Read-modify-Write Cycle							
Read-write cycle time	t_{RWC}	111	–	135	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	67	–	79	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	–	34	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	42	–	49	–	ns	15
$\overline{OE}$ command hold time	t_{OEH}	7	–	10	–	ns	
Hyper Page Mode (EDO) Cycle							
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	27	–	35	ns	7
Output data hold time	t_{COH}	5	–	5	–	ns	
$\overline{RAS}$ pulse width in hyper page mode	t_{RAS}	50	200k	60	200k	ns	

AC Characteristics *(cont'd)* 5)6)

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V , t_T = 2 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	27	–	35	–	ns	
$\overline{OE}$ pulse width	t_{OEP}	7	–	10	–	ns	
$\overline{OE}$ hold time from $\overline{CAS}$ high	t_{OEHC}	7	–	10	–	ns	
$\overline{WE}$ pulse width to output disable at $\overline{CAS}$ high	t_{WPZ}	7	–	10	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WPZ}	0	10	0	10	ns	
Hyper Page Mode (EDO) Read-modify-Write Cycle							
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	51	–	66	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	41	–	49	–	ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle							
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	8	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	8	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	8	–	10	–	ns	
CAS-before-RAS counter test cycle							
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	ns	
Self Refresh Cycle							
$\overline{RAS}$ pulse width during self refresh	t_{RASS}	100k	–	100k	–	ns	17
$\overline{RAS}$ precharge time during self refresh	t_{RPS}	84	–	104	–	ns	17
$\overline{CAS}$ hold time during self refresh	t_{CHS}	-50	–	-50	–	ns	17

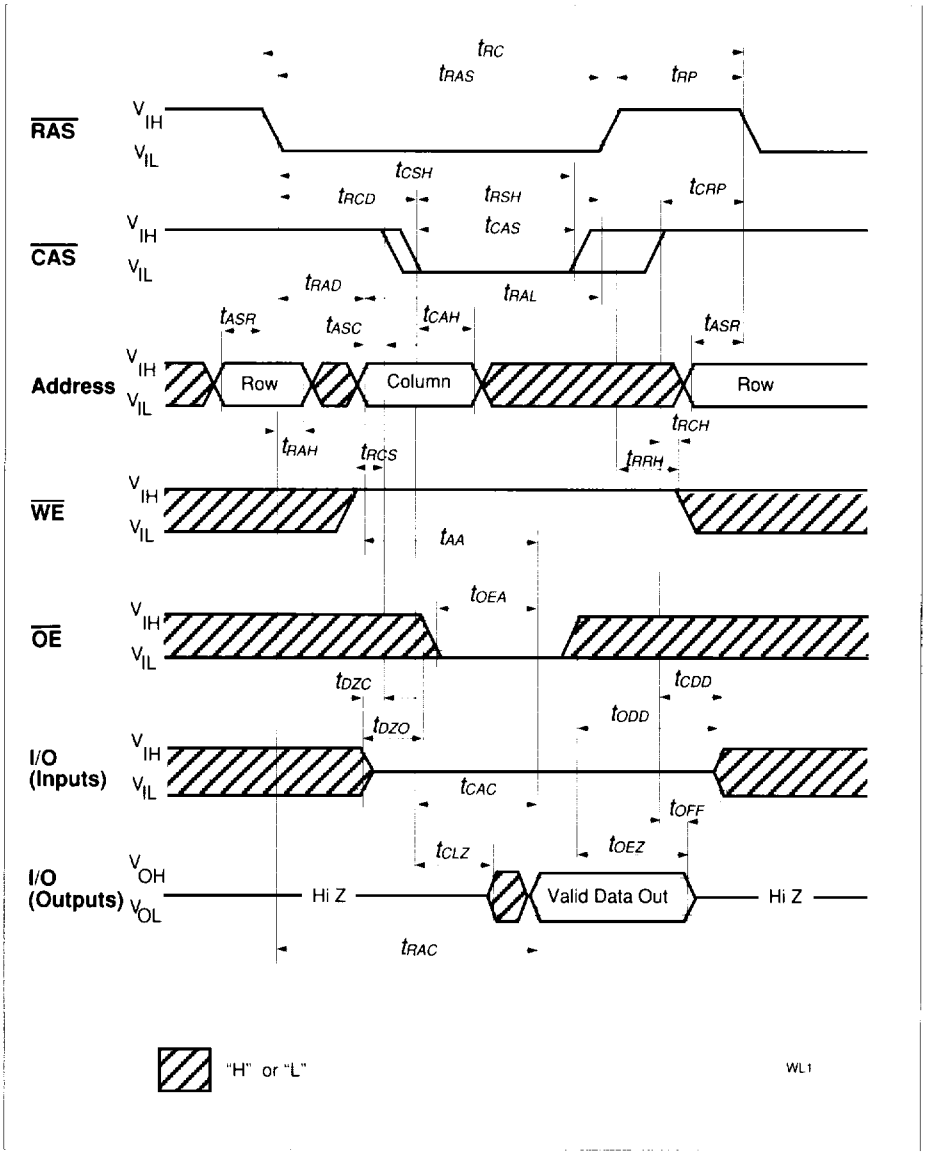
AC Characteristics *(cont'd)* 5)6)

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3V , t_T = 2 ns

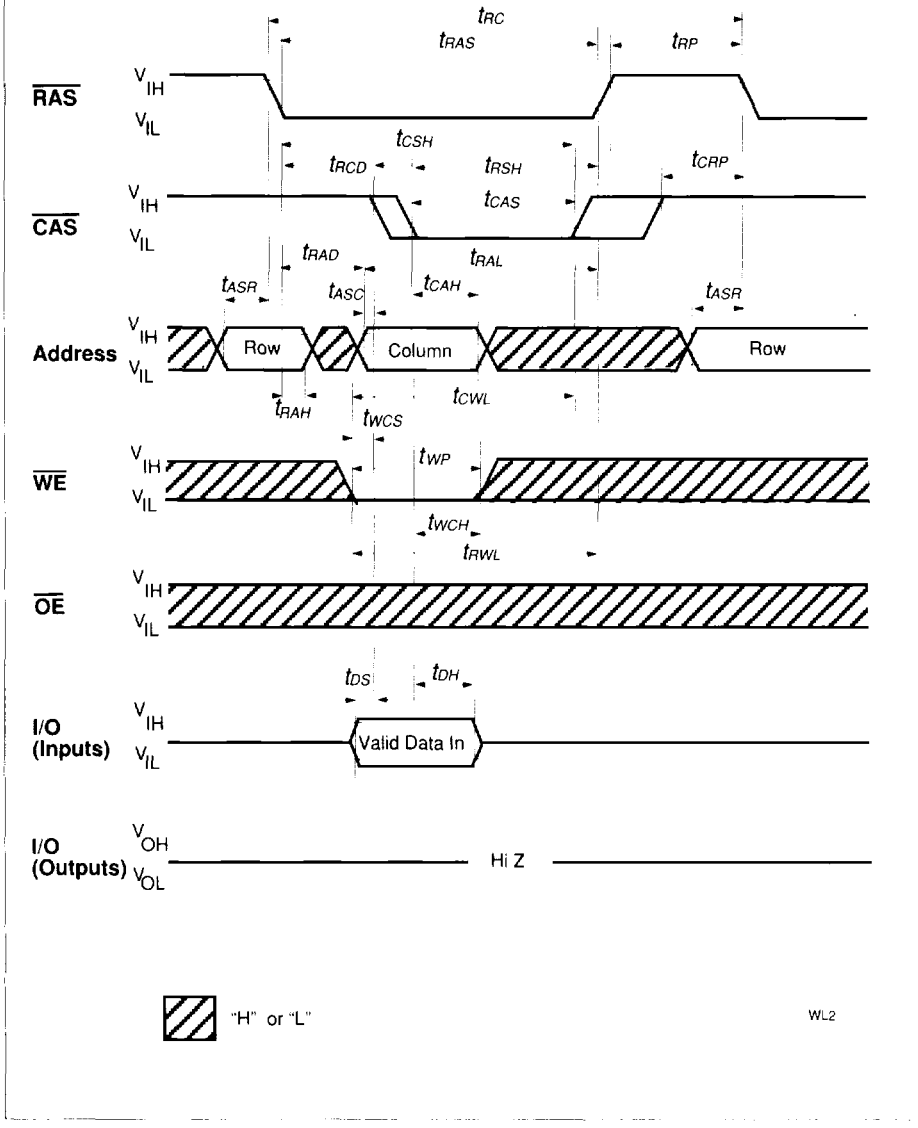
Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Test Mode							
Write command setup time	t_{WTS}	10	–	10	–	ns	18)
Write command hold time	t_{WTH}	10	–	10	–	ns	18)

Notes:

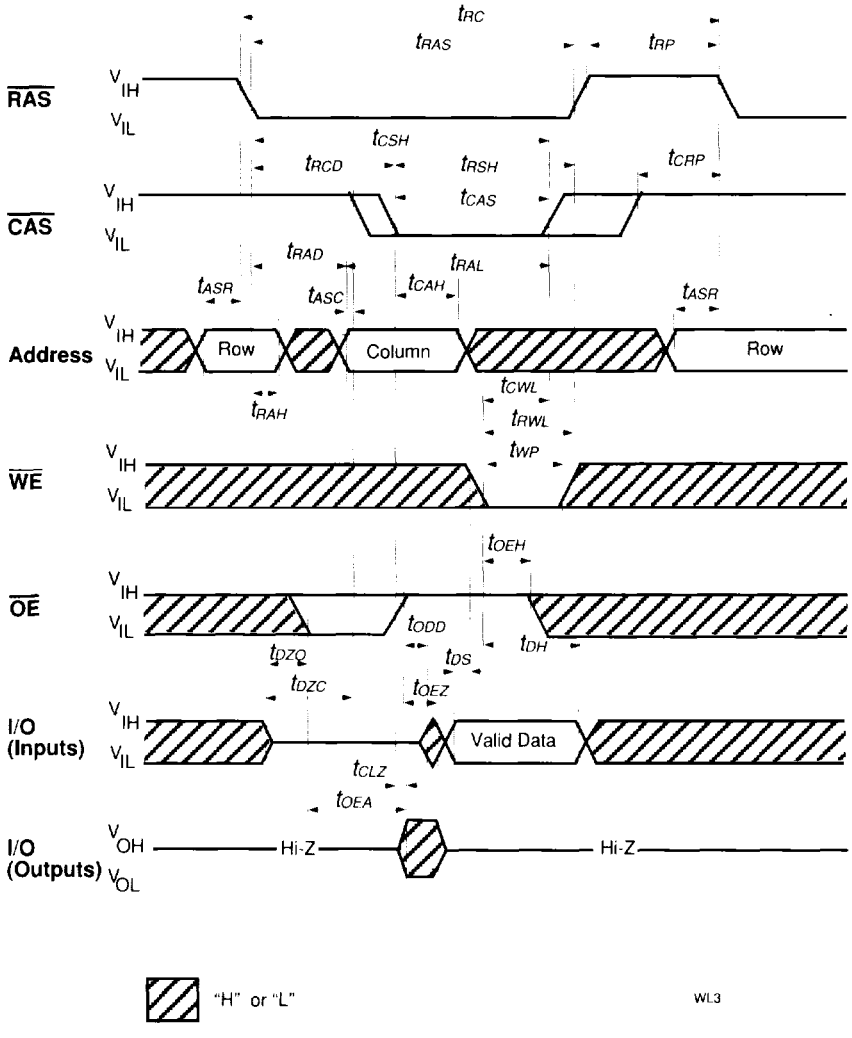
1) All voltages are referenced to VSS.
   Vih may overshoot to VV + 0.2V for pulse widths of < 4ns with 3.3V. Vil may undershoot to -2.0V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.
2) ICC1, ICC3, ICC4 and ICC6 and ICC7 depend on cycle rate.
3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
4) Address can be changed once or less while $\overline{RAS}$ = Vil.In the case of ICC4 it can be changed once or less during a hyper page mode cycle (thpc).
5) An initial pause of 100 s is required after power-up followed by 8 $\overline{RAS}$-only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6) AC measurements assume tT = 2 ns.
7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.
8) Measured with the specified current load and 100 pF at Voh = 2.0 V and Vol = 0.8 V.
9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
11) Either tRCH or tRRH must be satisfied for a read cycle.
12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
13) Either tDZC or tDZO must be satisfied.
14) Either tCDD or tODD must be satisfied.
15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if tRWD > tRWD (min.), tCWD > tCWD (min.), tAWD > tAWD (min.) and tCPWD > tCPWD (min.) , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
16) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
   If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediatly after exit from Self Refresh.
   If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediatey after exit from Self Refresh
18) In a Test Mode Read Cycle, the value of trac, taa, tcac and tcpa are delayed by 5 ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must be adjusted by 5 ns.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row
Column
Row
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O
(Inputs)
tCAC
tOFF
tCLZ
tOEZ
I/O
(Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"
WL1

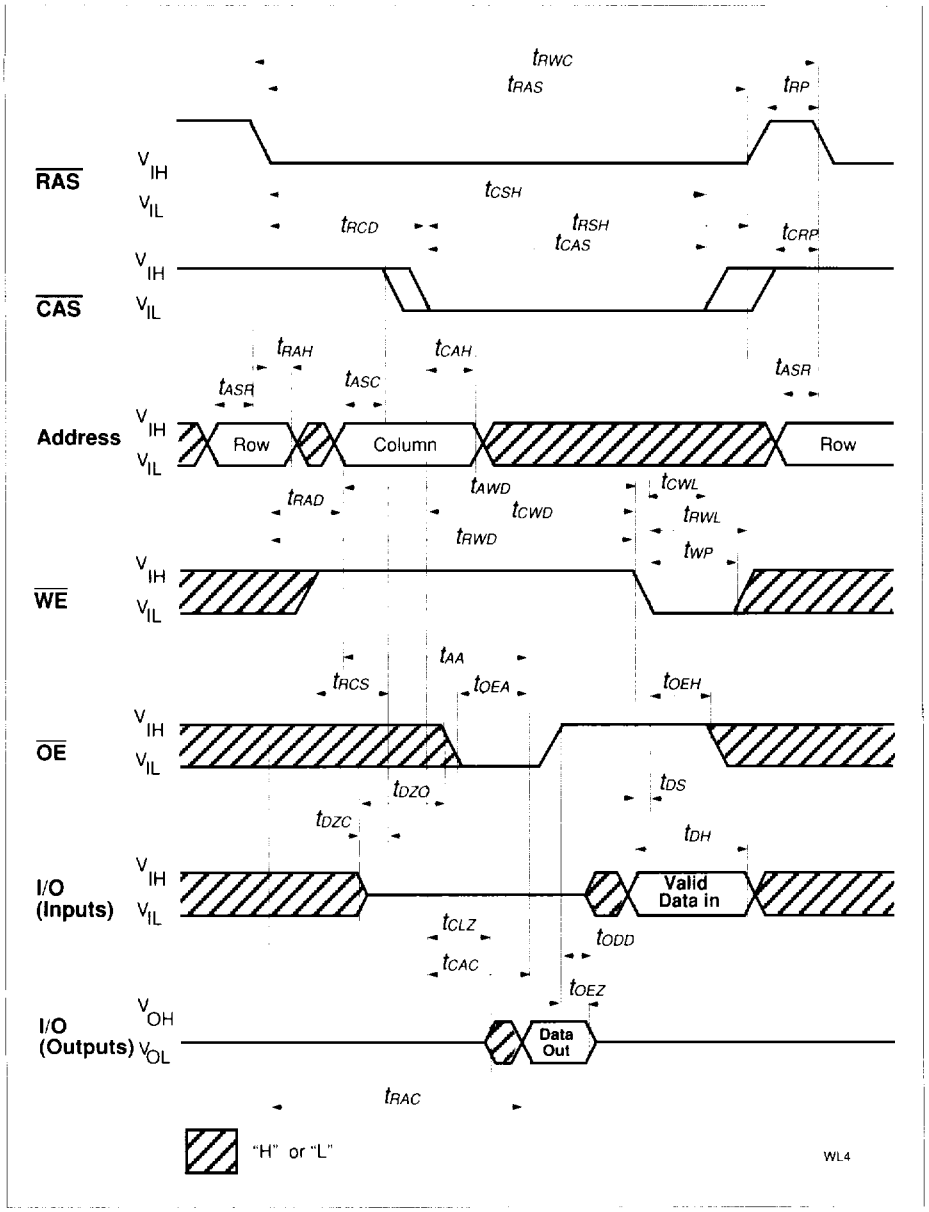
Read Cycle



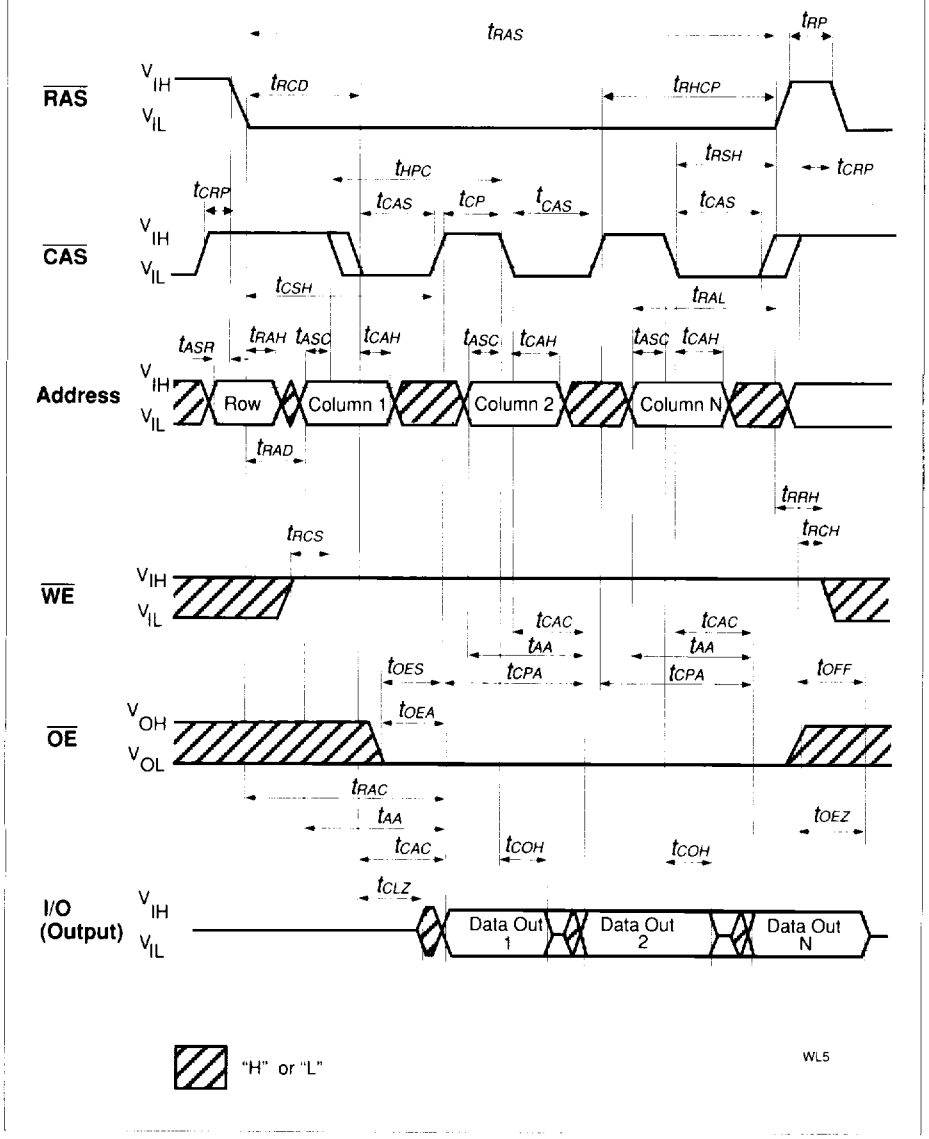
Write Cycle (Early Write)



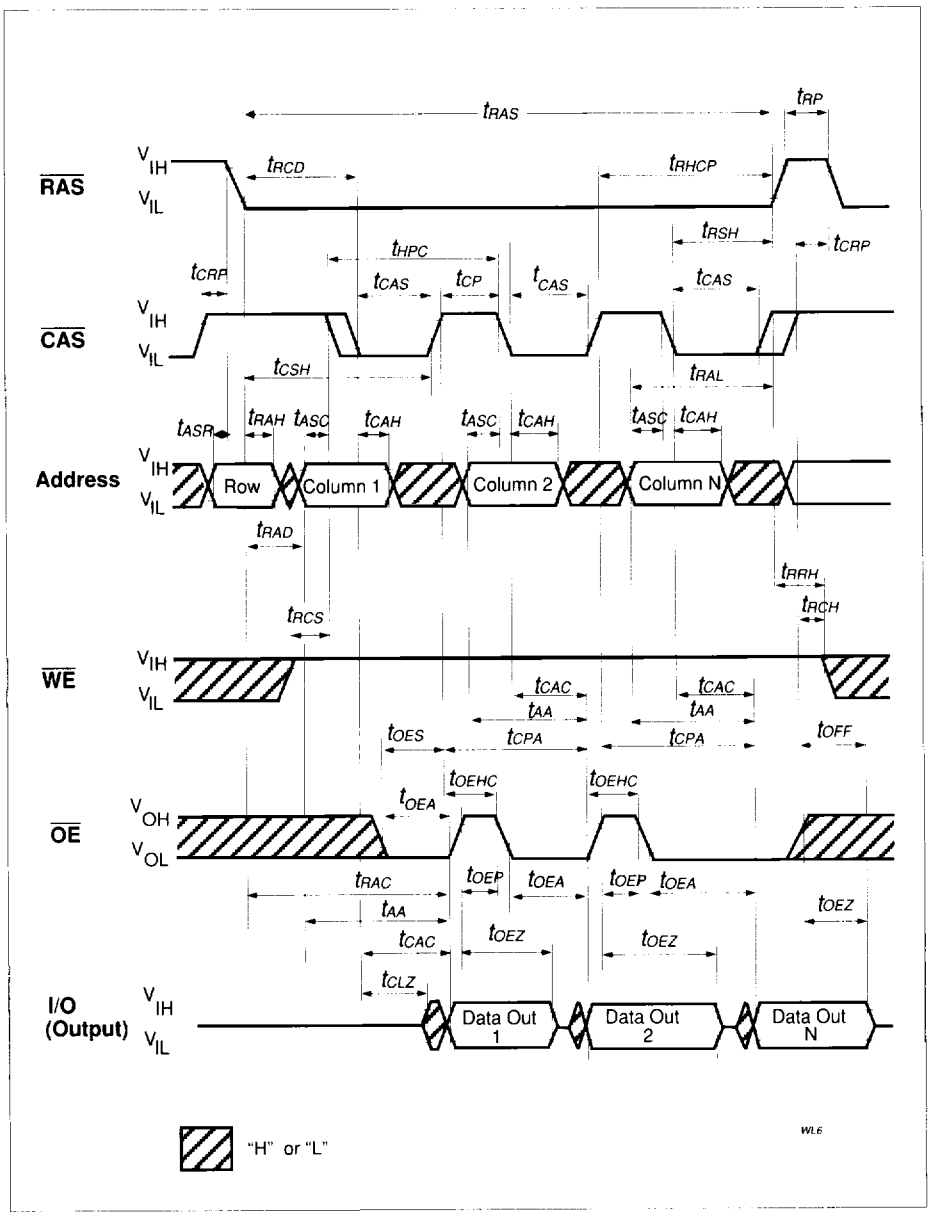
Write Cycle ($\overline{OE}$ Controlled Write)



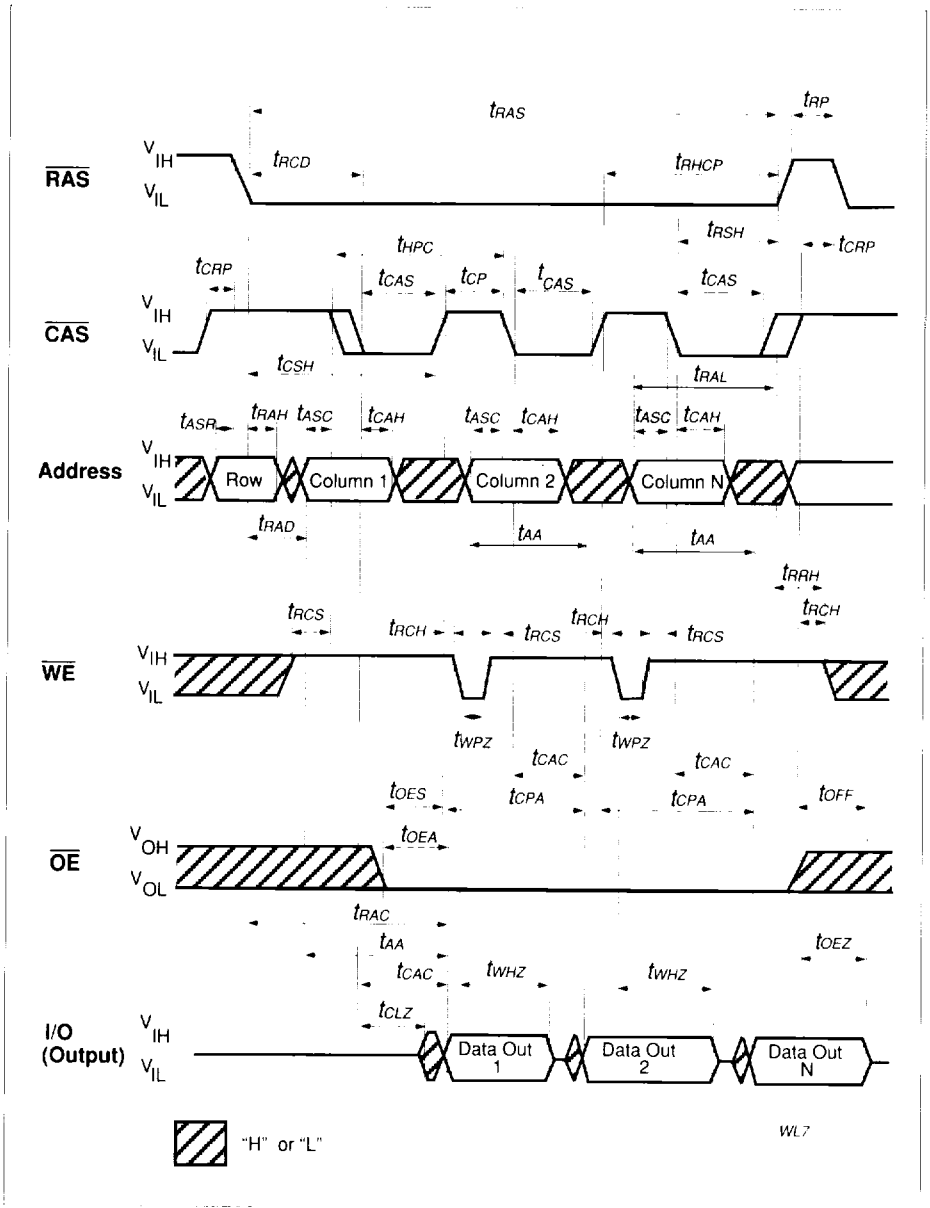
Read-Write (Read-Modify-Write) Cycle



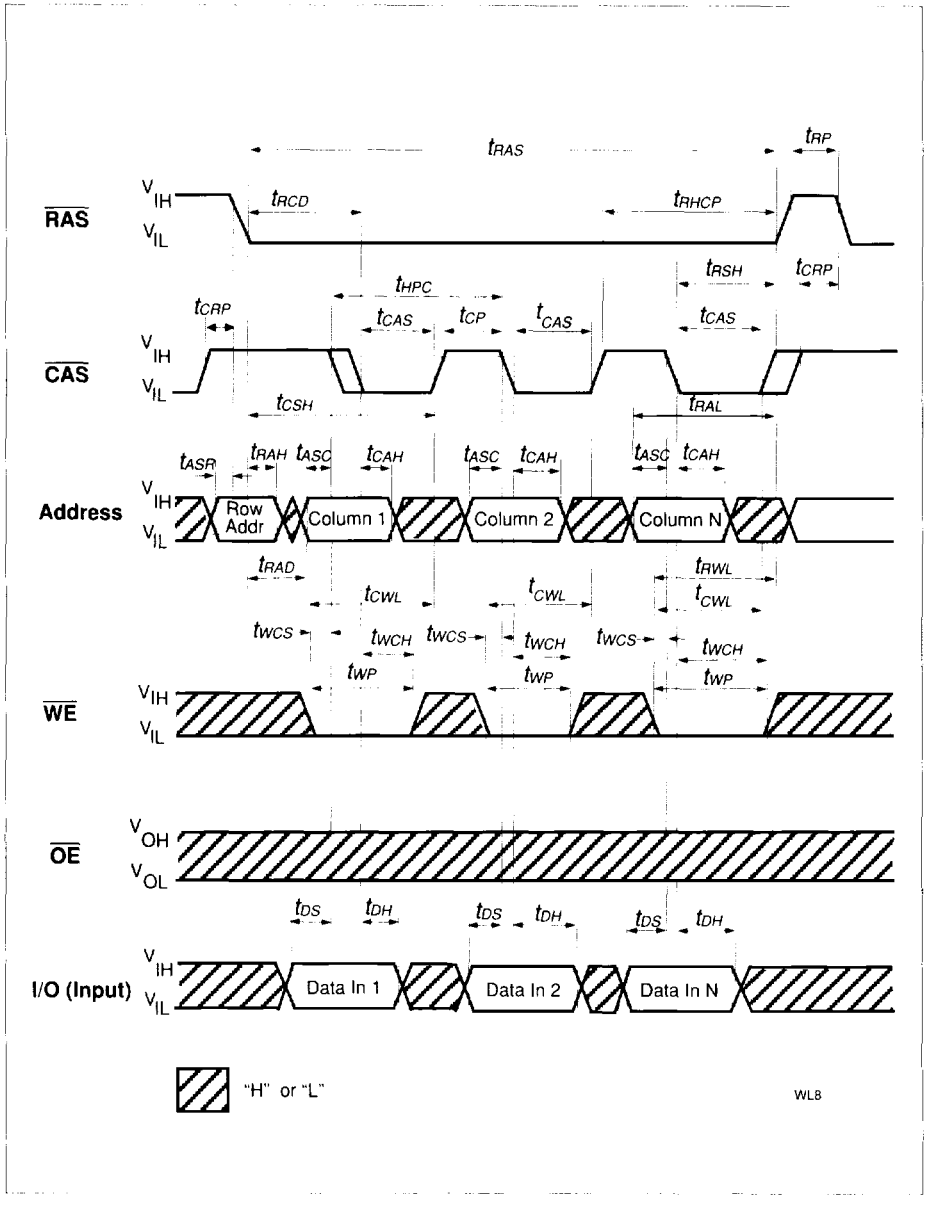
Hyper Page Mode (EDO) Read Cycle



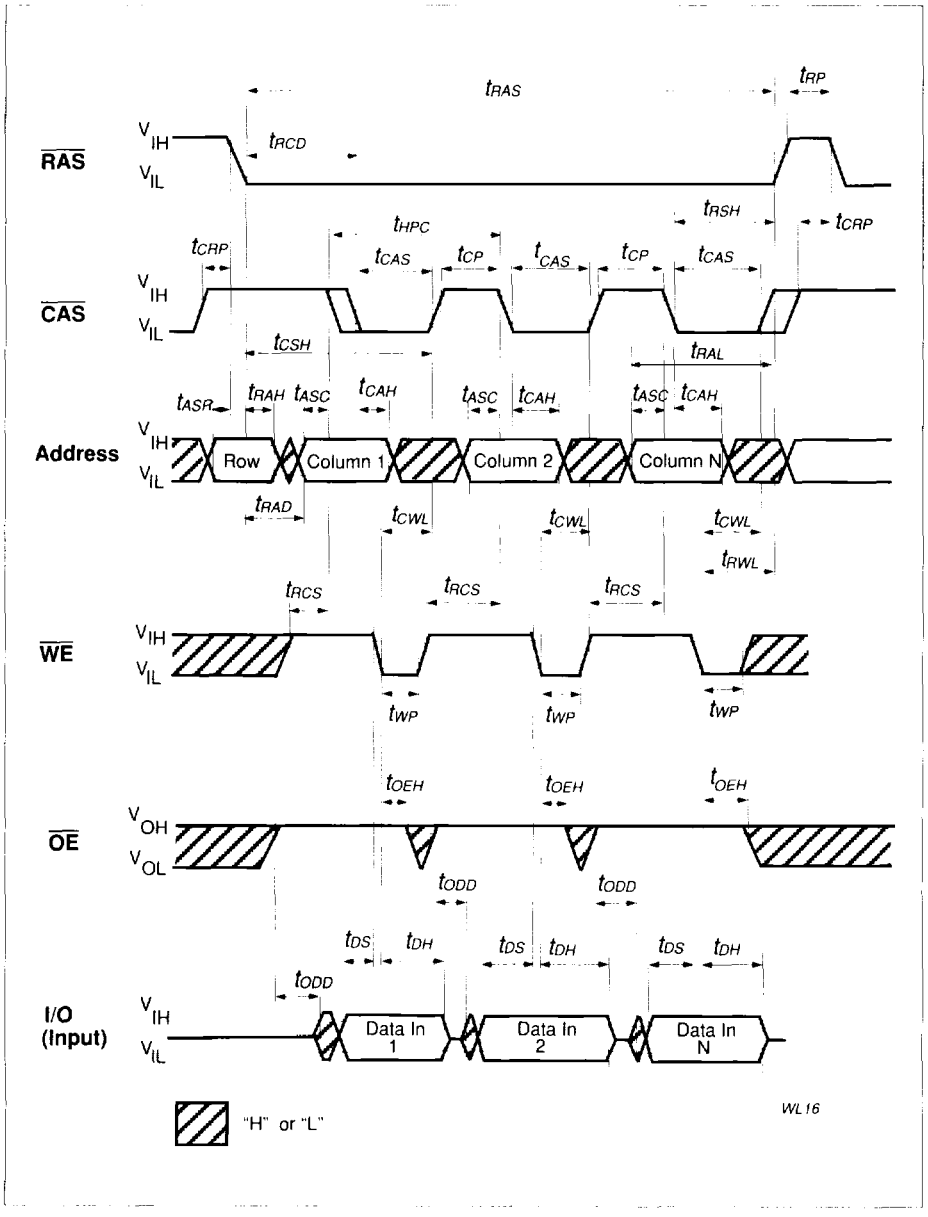
Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



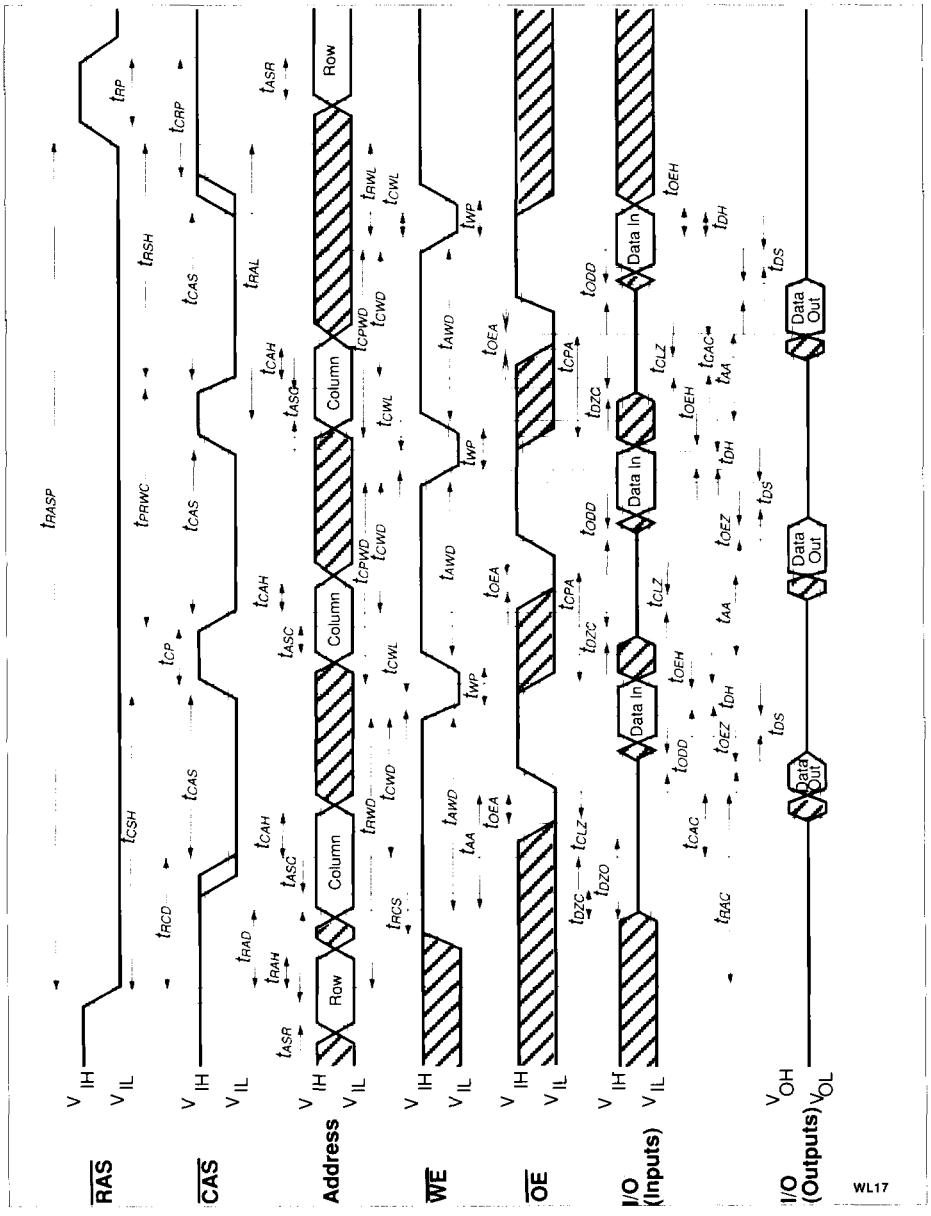
Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



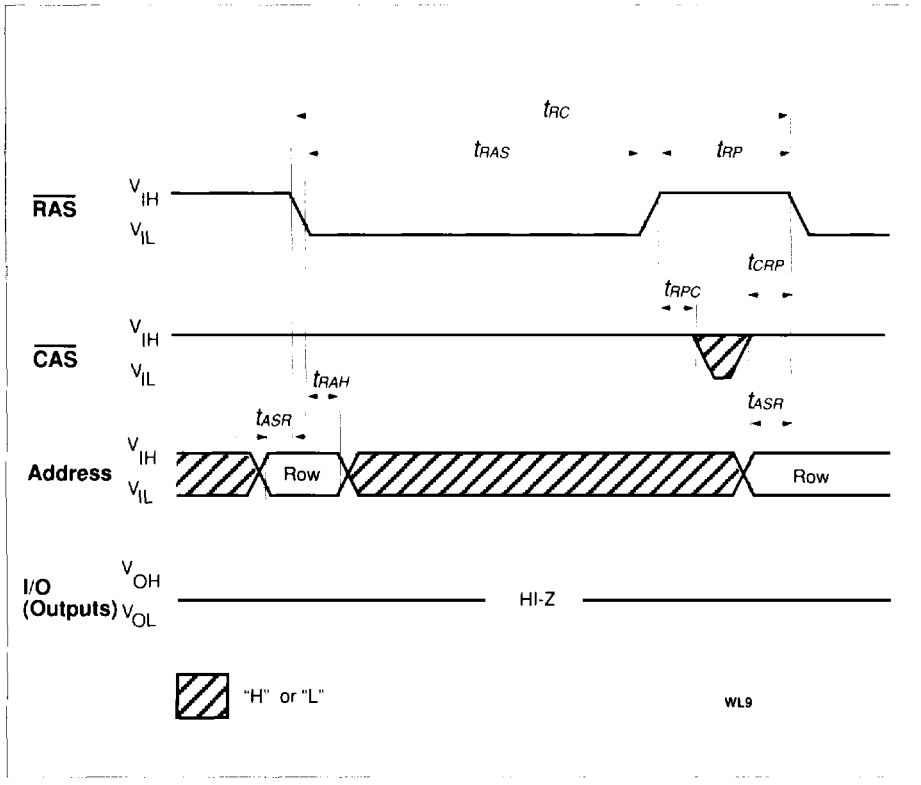
Hyper Page Mode (EDO) Early Write Cycle



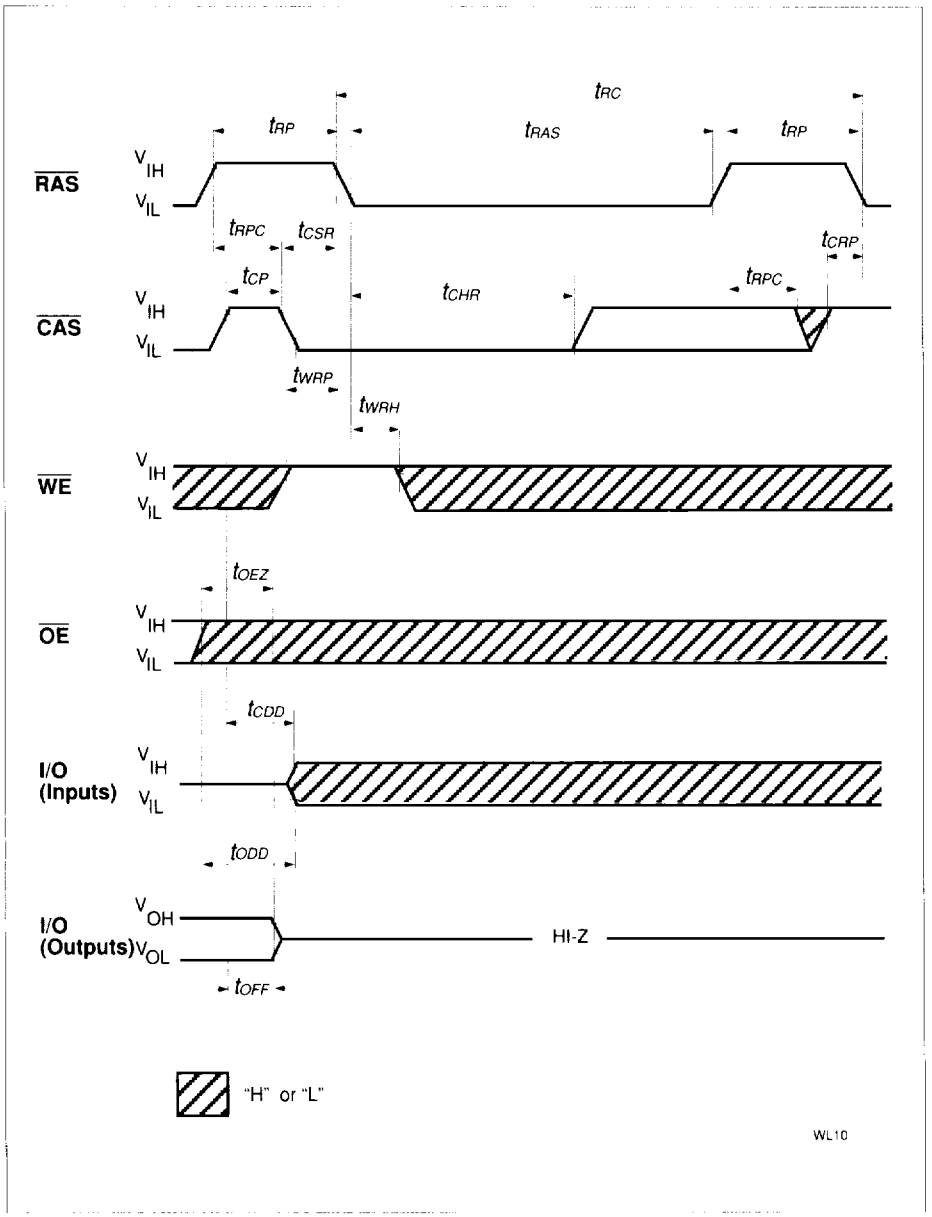
Hyper Page Mode (EDO) Late Write Cycle



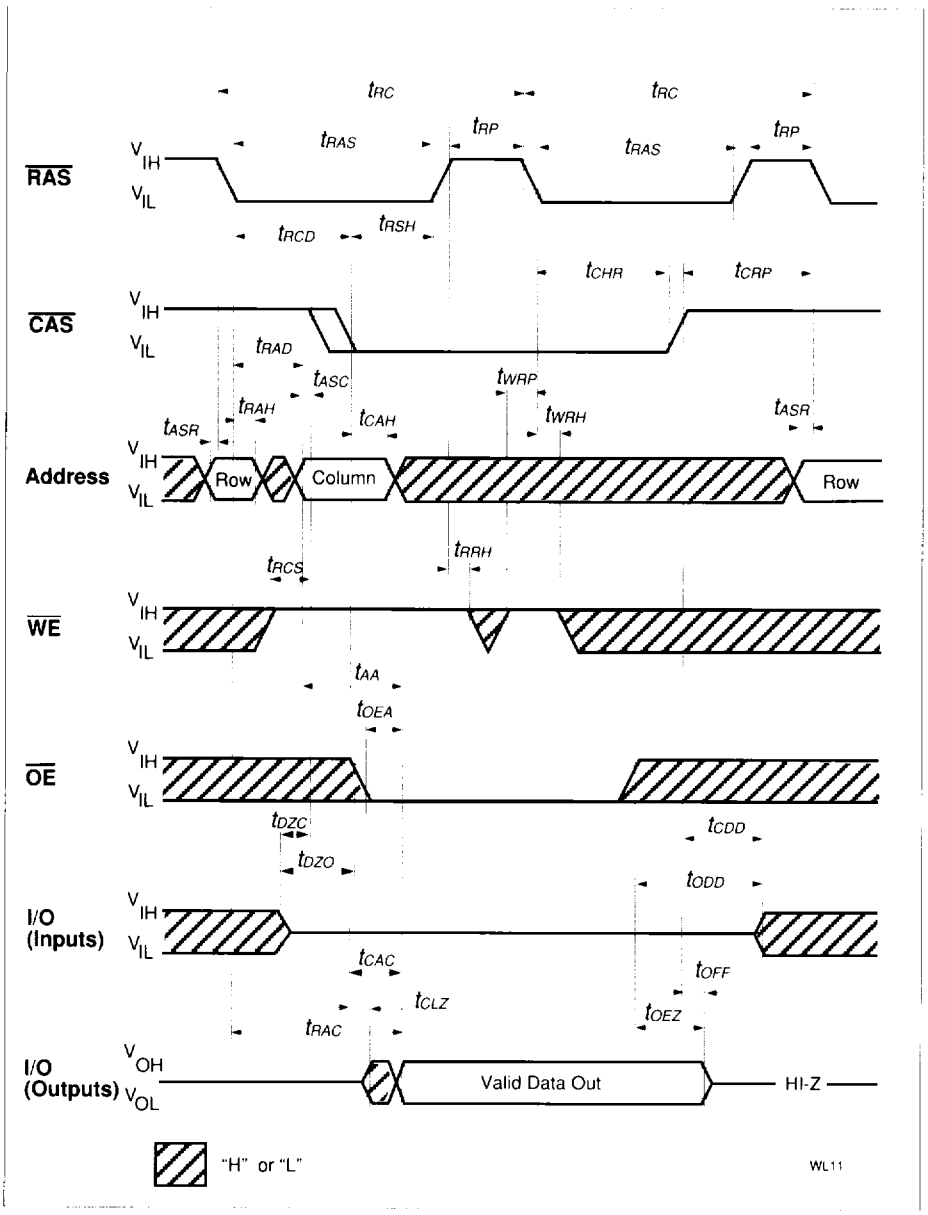
Hyper Page Mode (EDO) Read-Modify-Write Cycle



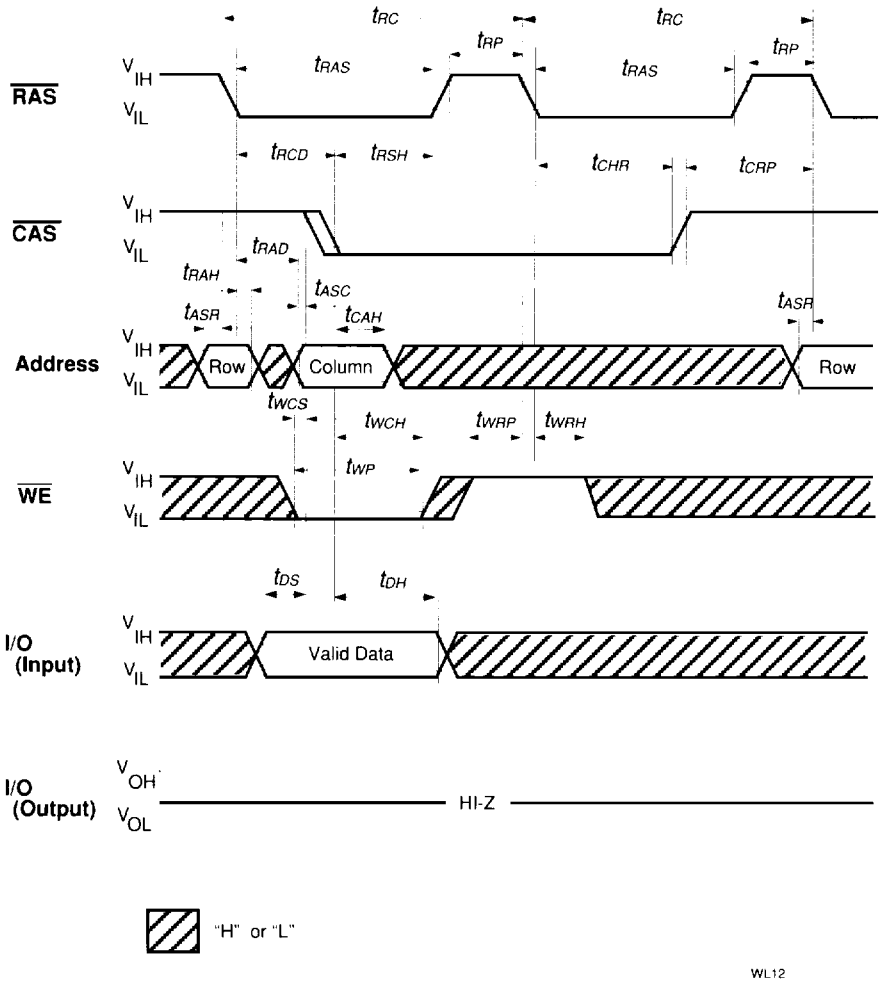
$\overline{\text{RAS}}$ Only Refresh Cycle



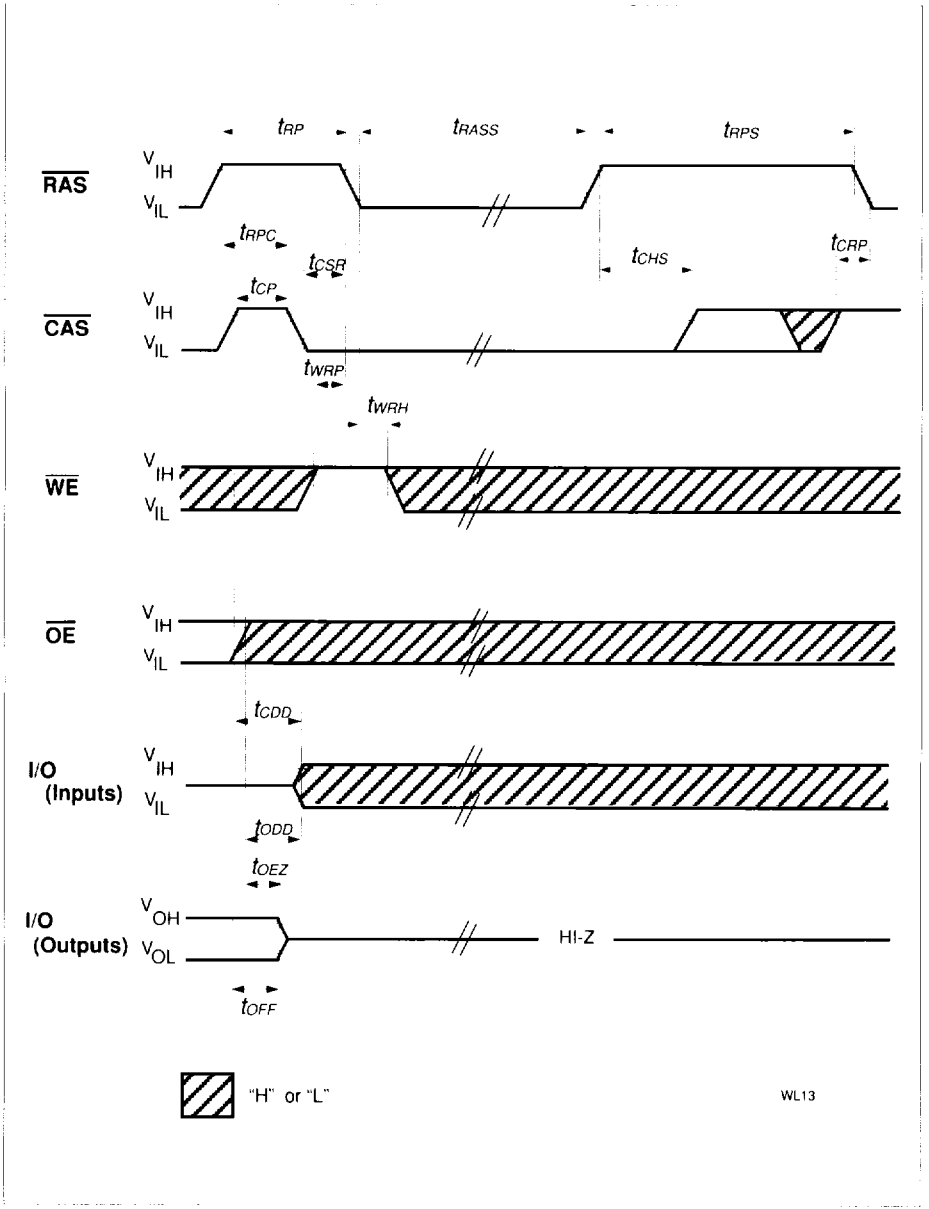
CAS-before-RAS Refresh Cycle



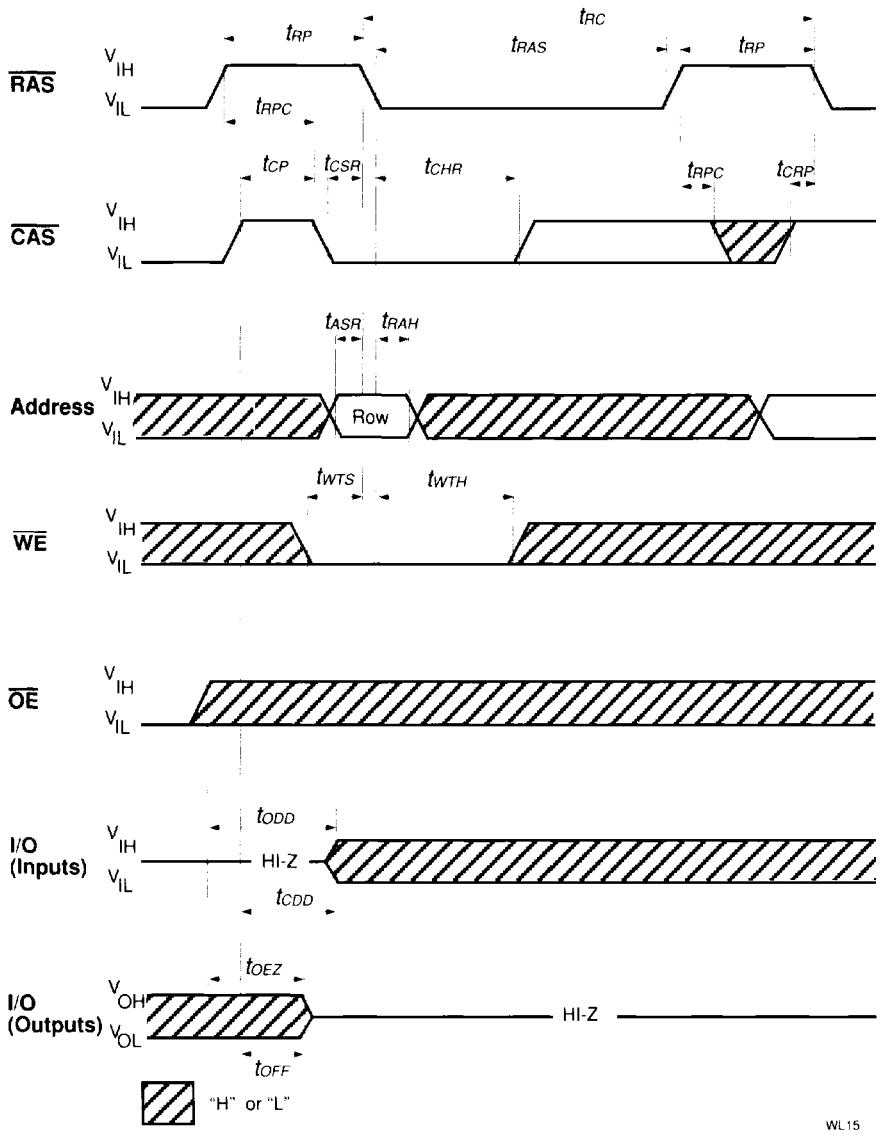
Hidden Refresh Read Cycle



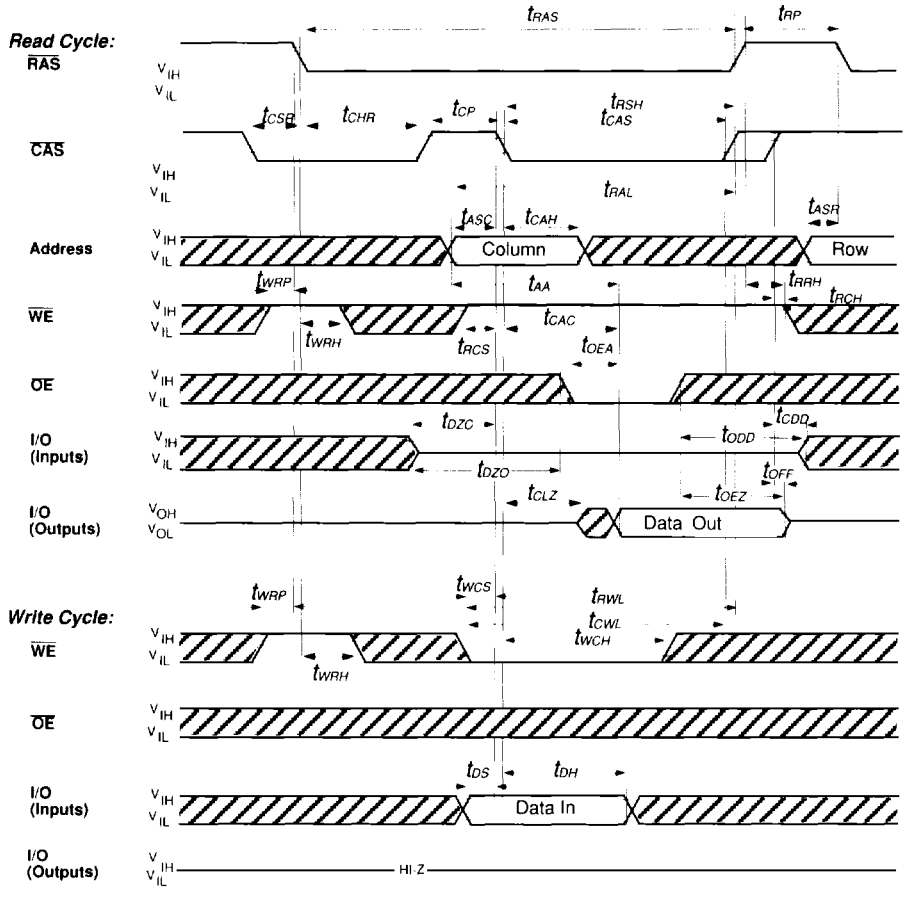
Hidden Refresh Early Write Cycle



Self Refresh (Sleep Mode)



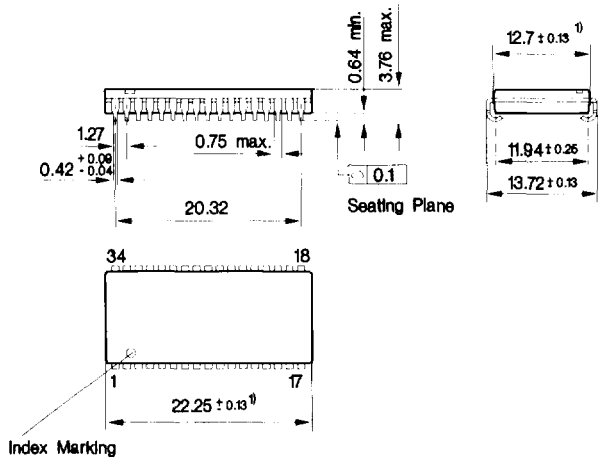
Test Mode Entry Cycle



CAS-before-RAS Refresh Counter Test Cycle

Package Outlines

P-SOJ-34-1 (500 mil)
(Plastic Small Outline J-leaded Package)

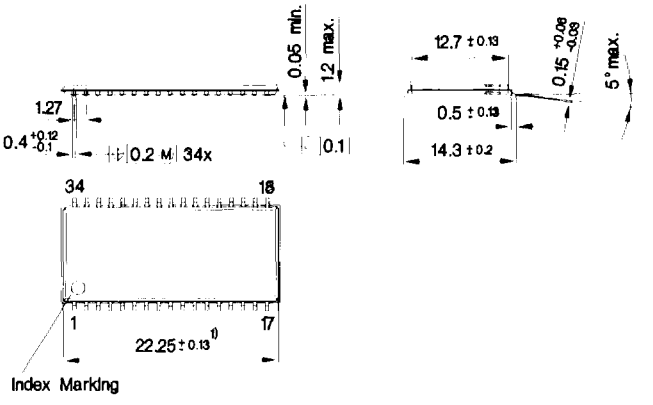


1) Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm

P-TSOPII-34-1 (500 mil)
(Plastic Thin Small Outline Package Type II



1) Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm