T-52-30-90

注文コードNo. EN3743

No. 3743

LC8900,LC8900Q

CMOS LSI

Digital Audio Interface Receiver

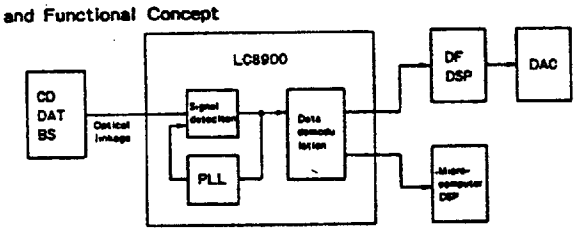
Overview:

The LC8900/8900Q is a CMOS LSI circuit chip that can be used to enable the EIAJ formatted data transmission between digital audio equipment. It is used by the receiving end and operates synchronously with input signals. This chip demodulates input signals into normally-formatted signals.

Features

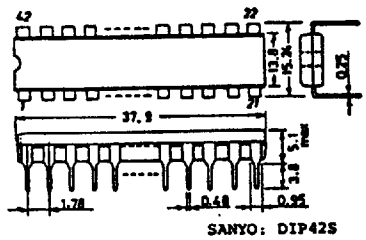
1) On-chip PLL circuit: enables the LSI operation to be synchronous to the transmitted EIAJ format input signals.
2) Four input pins and One output pin: The output pin enables the input data to be sent as they are.
3) Two data output function modes: 20-bit data LSB first mode and 16-bit data MSB first mode.
4) Four output clocks: Bit clock, LRCK, 384Fs and 256Fs. All these clocks are synchronized to the data.
5) Various signal outputs: Copy inhibit, Emphasis On:Off control, User's bit, Validity flag and sampling frequency.
6) LPF time constant select mode: This function can be used in the PLL lock-up state.
7) Error detect signal output: If an input data error is detected, this LSI circuit chip outputs the error signal. In this case, the previous data will be output by the chip.
8) Lock-up signal output: this signal is output when the internal PLL (Phase Locked Loop) block of the LSI circuit chip is locked.
9) The chip has the pin to receive a signal for stopping the PLL operation.
10) Control and Processing mode via microcomputer interface: Input pin select, copy information and sampling frequency output
11) Each input pin has an internal amplifier circuit.
12) Si gate, CMOS process technology and Single 5V power supply Applicational and functional concept

Applicational and Functional Concept



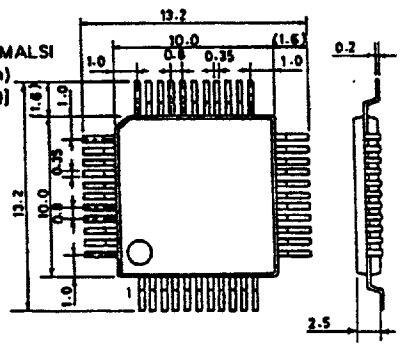
Case Outline

3025B-D42SIC [LC8900]
(unit: mm)



SANYO: DIP42S

3148-Q44MALSI
(unit: mm)
[LC8900Q]



SANYO: QIP44MA

Specifications and information herein are subject to change without notice.

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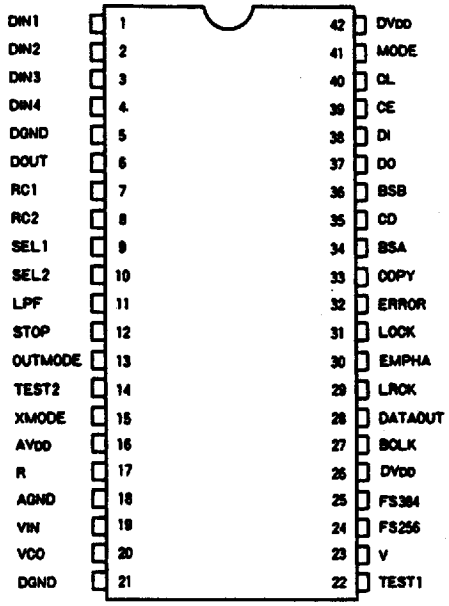
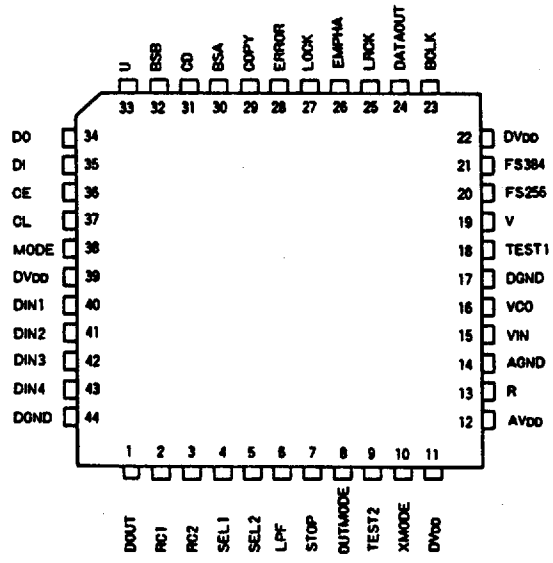
Pin Assignment

1) LC8900(DIP-42S)



2) LC8900Q(QIP-44M)



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LC8900 (DIP-42S) Pin Description

Pin No.	Pin Name	I/O Type	Functional Description
1	DIN1	I	Data input pin
2	DIN2	I	Data input pin
3	DIN3	I	Data input pin
4	DIN4	I	Data input pin
5	DGND		Digital Ground
6	DOUT	O	Input data output pin. However, its output is fixed at the 'L' level if the DIN 4 input pin is selected.
7	RC1	I	RC oscillation pin
8	RC2	O	RC oscillation pin
9	SEL1	I	Input pin select pin
10	SEL2	I	Input pin select pin
11	LPF	I	'H' level=LPF time constant select mode. 'L' level=LPF time constant fixed mode.
12	STOP	I	'H' level:Forces the VCO operation to stop.
13	OUTMODE	I	Output data format select. 'H'=20-bit LSB first data format. 'L'=16-bit MSB first data format.
14	TEST2	I	Test pin:Connected to the GND in most cases.
15	XMODE	I	Input pin to start the PLL operation immediately after the LSI chip is powered on.
16	AVDD		Analog power supply
17	R	I	VCO oscillation bandwidth adjust pin
18	AGND		Analog Ground
19	VIN	I	VCO self oscillation frequency setting pin
20	VCO	O	PLL LPF pin
21	DGND		Digital Ground
22	TEST1	I	Test pin:Connected to the DGND in most cases.
23	V	O	Validity flag output pin
24	FS256	O	256Fs clock output pin
25	FS384	O	384Fs clock output pin
26	DVDD		Digital Power Supply
27	BCLK	O	Bit clock output pin
28	DATAOUT	O	Audio data output pin
29	LRCK	O	L/R clock output pin
30	EMPHA	O	Emphasis control (On/Off) output pin:'H'=Emphasis mode. 'L'=None-Emphasis mode.
31	LOCK	O	PLL lock state output pin:'H'=PLL locked state. 'L'=PLL unlocked state.
32	ERROR	O	Input data error detect signal output:'H'=Error detected.
33	COPY	O	Copy information output pin
34	BSA	O	Input data sampling frequency indication:'H'=32kHz.
35	CD	O	Input data sampling frequency indication:'H'=44.1kHz.
36	BSB	O	Input data sampling frequency indication:'H'=48kHz.
37	DO	O	Microcomputer interface output pin
38	DI	I	Microcomputer interface input pin
39	CE	I	Microcomputer interface chip enable input pin
40	CL	I	Microcomputer interface clock input pin
41	MODE	I	Microcomputer interface control input:'H'=microcomputer interface active mode. 'L'=microcomputer interface inactive mode.
42	DVDD		Digital Power Supply

*:The DIP-42S chip does not have the user's bit output function.

LC8900Q (QIP-44) Pin Description

Pin No.	Pin Name	I/O Type	Functional Description
1	DOUT	O	Input data output pin. However, its output is fixed at the 'L' level if the DIN4 input pin is selected.
2	RC1	I	RC oscillation pin
3	RC2	O	RC oscillation pin
4	SEL1	I	Input pin select pin
5	SEL2	I	Input pin select pin
6	LPF	I	'H' level=LPF time constant select mode. 'L' level=LPF time constant fixed mode.
7	STOP	I	'H'= level:Forces the VCO operation to stop.
8	OUTMODE	I	Output data format select pin. 'H'=20-bit LSB first data format. 'L'=16-bit MSB first data format
9	TEST2	I	Test pin:Connected to the GND in most cases.
10	XMODE	I	Input pin to start the PLL operation immediately after the LSI chip is powered on.
11	DV_{DD}		Digital power supply
12	AV_{DD}		Analog power supply
13	R	I	VCO oscillation bandwidth adjust pin
14	AGND		Analog Ground
15	VIN	I	VCO self oscillation frequency setting pin
16	VCO	O	PLL LPF pin
17	DGND		Digital Ground
18	TEST1	I	Test pin:Connected to the DGND in most cases.
19	V	O	Validity flag output pin
20	FS256	O	256Fs clock output pin
21	FS384	O	384Fs clock output pin
22	DV_{DD}		Digital Power Supply
23	BCLK	O	Bit clock output pin
24	DATAOUT	O	Audio data output pin
25	LRCK	O	L/R clock output pin
26	EMPHA	O	Emphasis control (On/Off) output pin:'H'=Emphasis mode. 'L'=None-Emphasis mode.
27	LOCK	O	PLL lock state output pin:'H'=PLL locked state. 'L'=PLL unlocked state.
28	ERROR	O	Input data error detect signal output:'H'=Error detected.
29	COPY	O	Copy information output pin
30	BSA	O	Input data sampling frequency indication:'H'=32kHz.
31	CD	O	Input data sampling frequency indication:'H'=44.1kHz.
32	BSB	O	Input data sampling frequency indication:'H'=48kHz.
33	U	O	User's bit output pin
34	DO	O	Microcomputer interface output pin
35	DI	I	Microcomputer interface input pin
36	CE	O	Microcomputer interface chip enable input pin
37	CL	O	Microcomputer interface clock input pin
38	MODE	I	Microcomputer interface control input:'H'=microcomputer interface active mode. 'L'=microcomputer interface inactive mode.
39	DV_{DD}		Digital Power Supply
40	DIN1	I	Data input pin
41	DIN2	I	Data input pin
42	DIN3	I	Data input pin
43	DIN4	I	Data input pin
44	DGND		Digital Ground

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Absolute Maximum Ratings

				Unit
Maximum Supply Voltage	V_{DD} max	Ta=25℃	−0.3 to +7.0	V
Input/Output Voltage	V_I · V_O	Ta=25℃	−0.3 to V_{DD}+0.3	V
Ambient Storage Temperature	Tstg		−55 to +125	℃
Ambient Operating Temperature	Topg		−30 to +75	℃

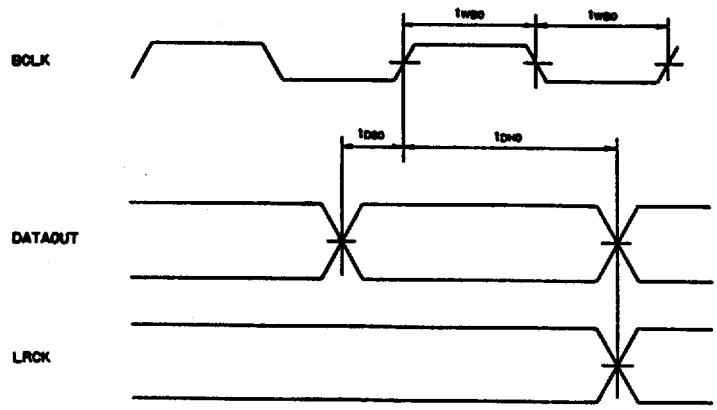
Operating Range

		min	typ	max	unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Operating Temperature	Topg	−30		+75	℃

DC Characteristics at Ta=-30 ℃ to +75 ℃. V_{DD}=4.5V to 5.5V

			Min	Typ	Max	Unit
Input High Level Voltage	V_{IH}		2.2		V_{DD}+0.3	V
Input Low Level Voltage	V_{IL}		−0.3		0.8	V
Output High Level Voltage	V_{OH}	I_{OH}=−1 μA	V_{DD}−0.05			V
Output Low Level Voltage	V_{OL}	I_{OL}=1 μA			Vss+0.05	V
Current Dissipation	I_{DD}	V_{DD}=5.0V		20		mA

AC Characteristics

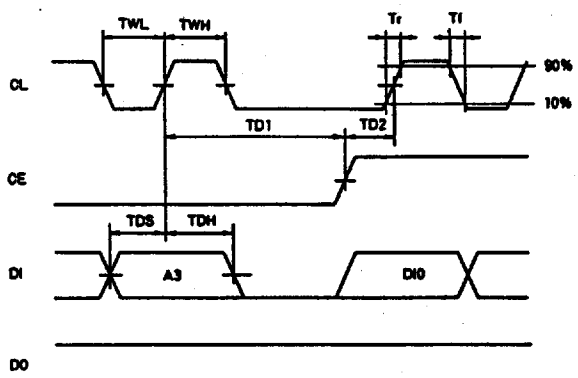


AC Characteristics at Ta=-30 ℃ to 75 ℃. V_{DD}=4.5V to 5.5V.

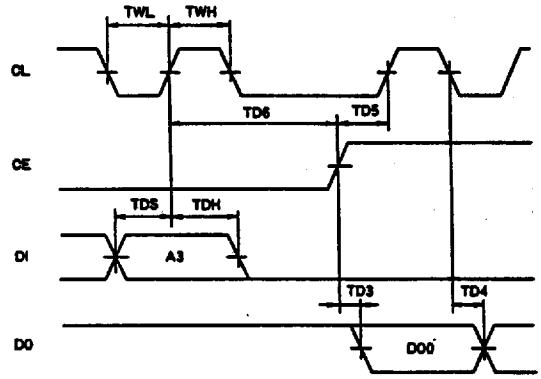
			Min	Typ	Max	Unit
Output Pulse Width	tWBO	Fs=48kHz	160			ns
Output Set-up Time	tDSO		80			ns
Output Data Hold Time	tDHO		80			ns

AC characteristics at the microcomputer interface block

Input mode operation



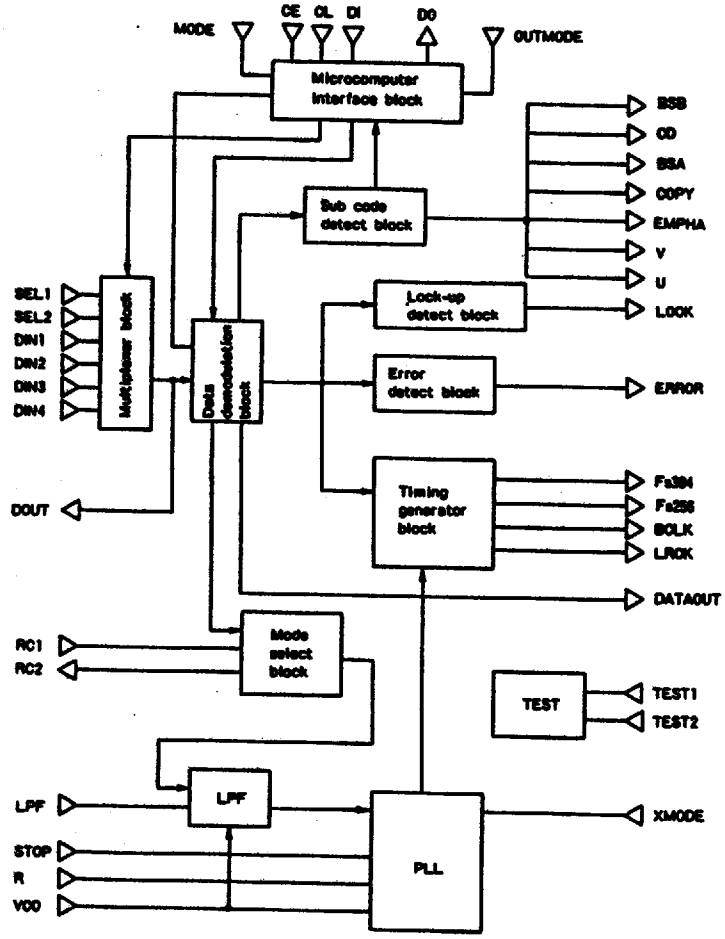
Output mode operation



AC Characteristics at Ta=-30°C to +75°C, VDD=4.5V to 5.5V.

		Min	Typ	Max	Unit
TWL		100			ns
TWH		100			ns
TDS		50			ns
TDH		50			ns
Tr	CL, CE, DI			30	ns
Tf	CL, CE, DI			30	ns
TD1		1.0			μs
TD2		50			ns
TD3	Load capacitance=30pF.			25	ns
TD4	Load capacitance=30pF.			50	ns
TD5		100			ns
TD6		1.0			μs

LC8900 Block Diagram



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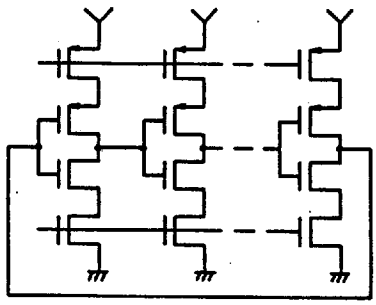
PLL functional circuit block

VCO

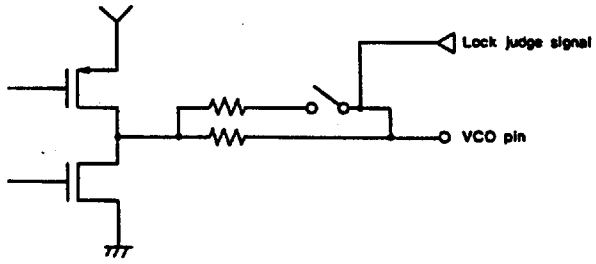


- The VCO (Voltage Controlled Oscillator) functional block consists of multiple Ring Oscillator ad shown above.
- The Ring oscillator produces the frequencies from 3MHz to 40MHz according to the VCO pin voltages 0V to 3V.
- The self oscillation frequency by the VCO is determined by the VIN pin voltage level.

Phase Detector

- The phase detector circuit operates on the rising edge of the incoming signals. It compares the clock generated from the input signal with the VCO clock.

LPF (Low Pass Filter)



- The charge pump and the LPF are shown above. The LPF time constant varies depending on the Lock judge signal.

DATA

1) The relationship between the data input pins and the data select pins are shown in the table below.

	SEL1	SEL2	DOUT
DIN1	L	L	DIN1 data output
DIN2	L	H	DIN2 data output
DIN3	H	L	DIN3 data output
DIN4	H	H	'L' level signal output (fixed level output)

- Each input pin has an internal amplification circuit. This means that the signal with the amplitude of 400mVpp can be input to this LSI chip.

2) The relationship between the OUTMODE pin and the output data format is shown in the table below.

OUTMODE pin	H	20-bit LSB first data output format
	L	16-bit MSB first data output format

- IF an error is detected in an input data, that input data is not output. Instead, the previous data will be output.
- The data output is synchronized with falling edge of the bit clock.
- IF the PLL is in the Lock state, the 384Fs or 256Fs clock that is synchronized with the output data will be output. Note that the duty is of the 256Fs clock is 'H:L=2:1'. It is not 'H:L=1:1'.

Sub codes

The sub code output consists of the copy inhibit signal, emphasis mode signal, sampling frequency signal, validity flag signal and user's bit. The table below details these sub code outputs.

COPY inhibit signal	COPY pin level='H':Copy not inhibited. COPY pin level='L':Copy inhibited.
Emphasis mode signal	EMPHA pin level='H':Emphasis mode. EMPHA pin level='L':Non emphasis mode.
Sampling frequency	BSA pin level='H':32kHz sampling frequency CD pin level='H':44.1kHz sampling frequency BSB pin level='H':48kHz sampling frequency
Validity flag signal	This signal is output from the V pin in sub frame unit.
User's bit	This signal is output from the U pin in sub frame unit. Note that this signal is not output by the DIP-42S chip.

Clock modes

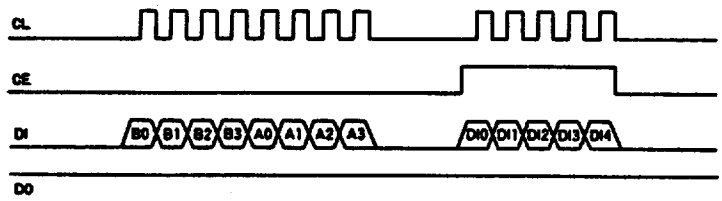
Self oscillation mode	•XMODE pin level='L' •No data input	•The VCO continues its oscillation according to the VIN pin potential. This means that the output data is not effective.
PLL mode	•Data input with the XMODE pin level='H'	•The PLL block and the entire circuit are in the normal operation state.

- When the STOP pin is changed to the 'H' level, the PLL functional circuit block stops its operation and the entire circuit operation is then forced to stop. The entire circuit will start the normal operation again when the STOP pin is changed to the 'L' level.
- If the LOCK operation is not activated in a certain fixed time period after the PLL enters the lock-up state:
  Reinitialize the PLL functional circuit block to active the lock-up mode. This should be done to prevent the PLL lock error.

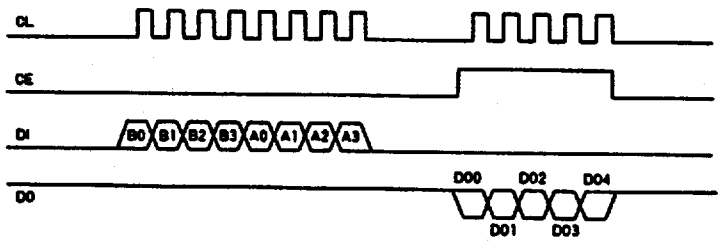
Microcomputer interface

The microcomputer interface function can be used by setting the MODE pin level to the 'H'. In this function mode, the pins CE, CL, DI and DO can be used to allow the interface between the LSI chip and a microcomputer. This microcomputer interface allows the microcomputer to control and process the input pin selection, output data format, copy information and sampling frequency output.

Input data format



Output data format



Bits B0 to A3 of the DI signal in the format are used to specify an 8-bit address. These 8-bits are used to specify the addresses both in the input and output operations.

	B0	B1	B2	B3	A0	A1	A2	A3
Data input mode	1	0	1	0	0	1	1	0
Data output mode	0	1	1	0	0	1	1	0

1) Data input mode
Bits DI0 to DI4 of the DI signal are used to select the operation modes shown in the tables below.

DI1=L	16-bit data MSB first output mode
DI1=H	20-bit data LSB first output mode

DI2	DI3	Input pin selection	DOUT
L	L	DIN1	DIN1 data output
L	H	DIN2	DIN2 data output
H	L	DIN3	DIN3 data output
H	H	DIN4	'L' level signal output (fixed level output)

- When the MODE pin level is set to the 'H', the input pins and output data format are selected by the microcomputer. This means that the selection data input to the SEL1, SEL2 and OUTMODE pins has no significance.

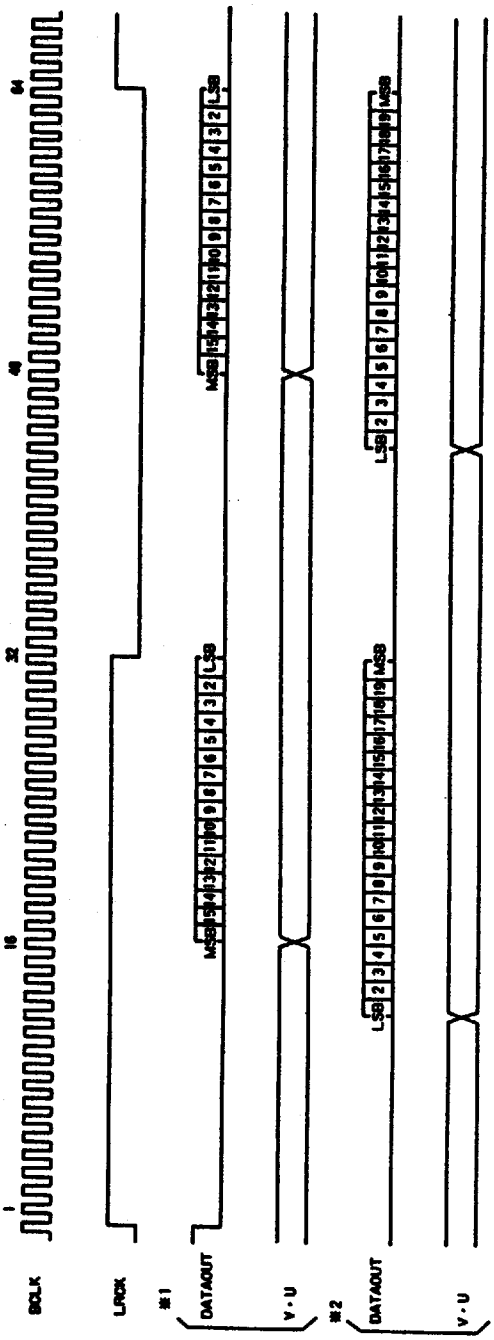
2) Data output mode
Bits DO0 to DO4 of the DO signal have the following meanings shown in the tables below.

DO3=L	Copy inhibited
DO3=H	Copy not inhibited

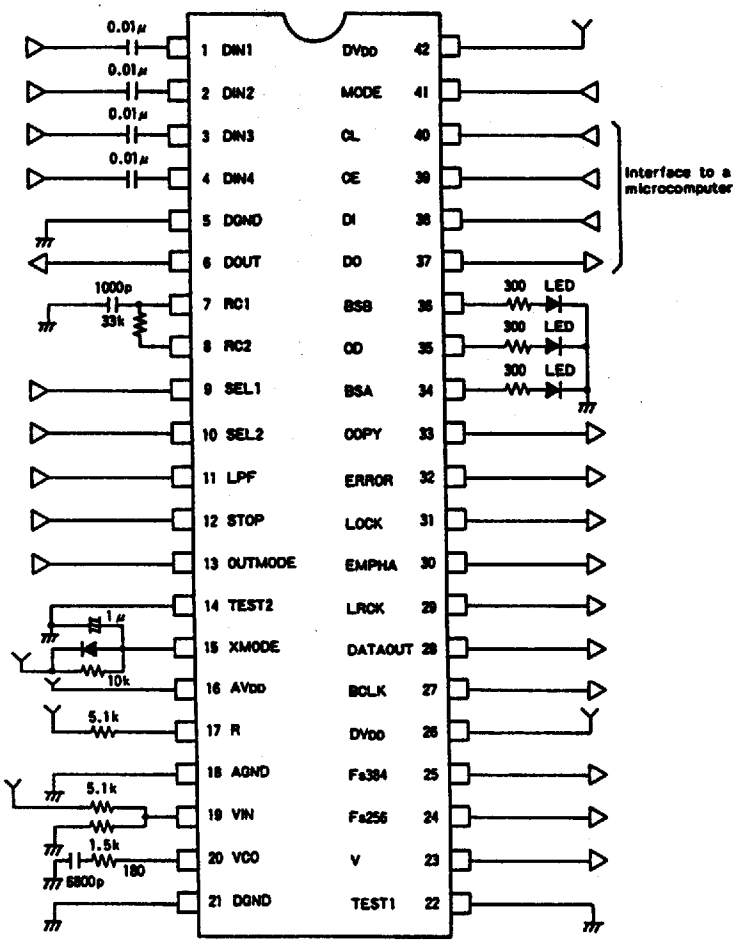
DO1	DO2	Sampling frequency selection
L	L	44.1kHz
L	H	48kHz
H	H	32kHz

- When the LOCK pin level is 'H', the PLL circuit block is already in the lock-up state. In this case, each sub code data has been already set up.

Timing Chart



Example application circuit



※Note:These constants are temporal values.