OKI Semiconductor

PEDL87V3116-02
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ML87V3116 Preliminary

Display Controller with Built-in Display Memory and JPEG

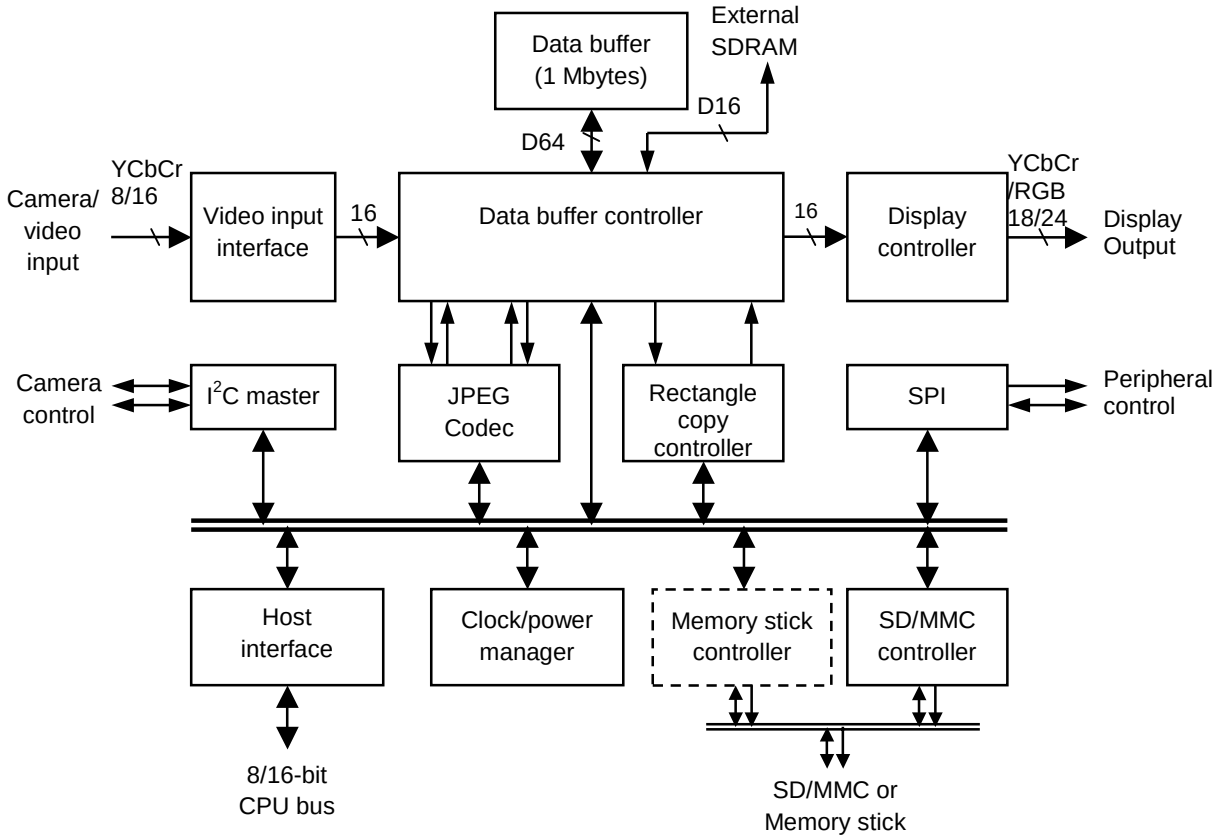
GENERAL DESCRIPTION

The ML87V3116 is a multi-function image processor LSI for small imaging devices.
Imaging functions, such as image input, temporary storage, processing and display output, are integrated into a single chip. The ML87V3116 has functions includuing camera or video input image capture, display control in LCD or TV format, compression and decompression of still pictures and moving pictures (Motion-JPEG) using a JPEG engine, and image copying with the size reduction and the rotation.
DRAM is embedded inside the chip to improve the performance of memory access and realize simultaneous operations of multiple functions. Furthermore, by adding external memory, large-sized images can be processed and the moving pictures recording time can be extended.

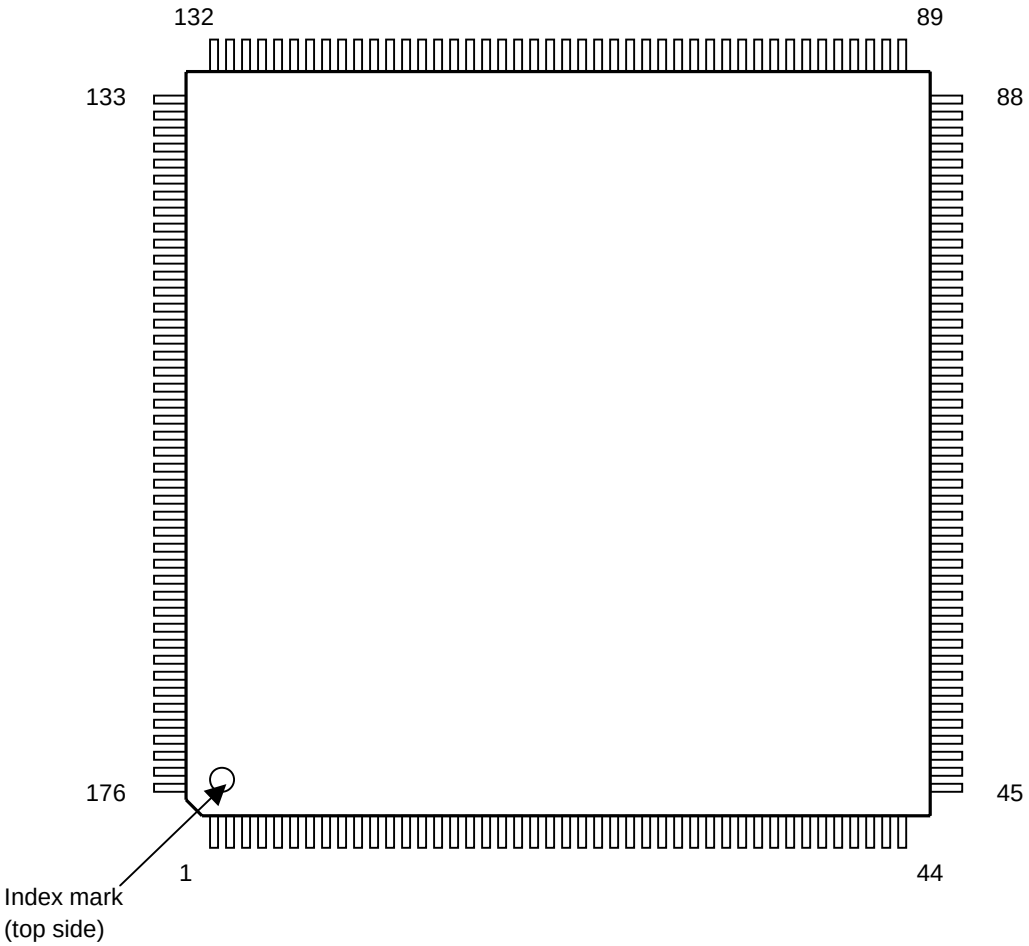
MAIN FEATURES

- Camera imaging : Maximum 4 million pixels, 30 frames/sec at VGA resolution (350,000 pixels)
- Image compression/decompression : Base line JPEG and Motion-JPEG
- Display controller : Color TFT-LCD up to VGA, or TV format
- Rectangle copy : Magnification and reduction x1/2 to 1/32, rotation 0/90/180/270°
- Built-in memory. : 8-Mbit SDRAM
- External memory (optional) : SDRAM, 16/64/128/256/512 Mbits, x16 types, 0 to 3 memory
- Video input : YCbCr (4:2:2) 16-bit format x 1, or ITU-R BT.656 (8-bit) format x 2
- Display output : 18/24 bits, RGB/YCbCr, 65536 colors
- Operating frequency : Maximum 28 MHz (internal 56 MHz)
- Host interface : 8/16-bit bus (compatible with various microcontrollers)
- Peripheral control interface : I^2C bus master, SPI master controller
- Memory card controller : SD card/MMC, or MEMORY STICK™ (only in serial mode)
- Power supply voltage : Core section 2.5 V ±0.15 V, I/O section 3.3 V ±0.3 V
- Standby current : 2 mA or less (target value when displaying partially on a small-sized LCD)
- Package : 176-pin LQFP, 0.5 mm pitch, 24 mm (LQFP176-P-2424-0.50-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



176-Pin Plastic LQFP

PIN DESCRIPTIONS

Table-P1 Pin List (1/7): Video Input Related

Pin No.	Symbol	I/O	Type	Description
139-144, 146, 147	VY7-0	I	LVTTL, pull-up	Video input data Y/port 0
148-151, 153-156	VC7-0	I	LVTTL, pull-up	Video input data C/port 1
159	VHS	I	LVTTL, pull-up	Video input horizontal synchronous signal
158	VVS	I	LVTTL, pull-up	Video input vertical synchronous signal
161	VFID	I	LVTTL, pull-up	Video input field ID signal
160	VCLK	I	LVTTL, pull-down Schmitt trigger	Video input clock

Table-P2 Pin List (2/7): Display Output Related

Pin No.	Symbol	I/O	Type	Description
78, 77, 75-72	DG7-2	O	4mA drive	Display data G, bits 7-2
71	DG1LDP2	I/O	Input LVTTL	Display data G, bit 1 or line drive pulse 2
70	DG0LDP3	I/O	Input LVTTL	Display data G, bit 0 or line drive pulse 3
68-65, 63, 62	DB7-2	O	4mA drive	Display data G, bits 7-2
61	DB1LDP4	I/O	Input LVTTL	Display data B, bit 1 or line drive pulse 4
60	DB0HST2	I/O	Input LVTTL	Display data B, bit 0 or horizontal start signal 2
87-82	DR7-2	O	4mA drive	Display data G, bits 7-2
80	DR1FDP2	I/O	Input LVTTL	Display data R, bit 1 or line drive pulse 2
79	DR0FDP3	I/O	Input LVTTL	Display data R, bit 0 or frame drive pulse 3
59	CP	O	4mA drive	Data clock
57	LDP1	O	4mA drive	Line drive pulse 1 (HSYNC)
56	HST1	I/O	Input LVTTL	Horizontal start signal 1 (GPIO3)
55	FDP1	O	4mA drive	Frame drive pulse 1 (VSYNC)
54	FIDF	O	4mA drive	Current-alternating signal/field ID signal
53	DISP	O	4mA drive	Display enable

Table-P3 Pin List (3/7): SDRAM Interface Related

Pin	Symbol	I/O	Type	Description
137-134, 131-128, 118, 119, 121-126	MDQ15-00	I/O	Input LVTTL Output 8mA drive	Memory data
104, 102-97, 95-90	MA12-00	O	8mA drive	Memory address
106,105	MBA1-0	O	8mA drive	Memory bank address
109	MWEN	O	8mA drive	Write enable
111	MDQM	O	8mA drive	Data mask
107	MRASN	O	8mA drive	Row address strobe
108	MCASN	O	8mA drive	Column address strobe
115-117	MCSN1-3	O	8mA drive	Memory chip select
112	MCKE	O	8mA drive	Memory clock enable
113	MCLK	O	8mA drive	Memory clock

Table-P4 Pin List (4/7): Host Interface Related

Pin	Symbol	I/O	Type	Description
165-168, 170-173	D7-0	I/O	Input LVTTL Output 4mA drive	Host data bus
174, 175, 2-7, 9-12	AD11-00	I/O	Input LVTTL Output 4mA drive	Host address/data bus
13	CSN	I	LVTTL	Host access chip select
19	REN	I	LVTTL	Host read enable
18	WEN	I	LVTTL	Host write enable
14	BSN	I	LVTTL	Host bus strobe
17	DSN	I	LVTTL	Host data strobe
20	BSYN	O	4mA drive 3 states	Bus busy/wait
16	BCLK	I	LVTTL	Bus clock
21	INT	O	4mA drive	Interrupt
23-26	HMOD3-0	I	LVTTL	Host bus mode select

Table-P5 Pin List (5/7): Peripheral Interface Related

Pin	Symbol	I/O	Type	Description
164	SDA	I/O	Input LVTTL Output 4mA drive Open drain	I^2C bus serial data
163	SCL	O	Input LVTTL Output 4mA drive Open drain	I^2C bus serial clock
50	SSDO	O	4mA drive 3-state	Synchronous serial interface output data
49	SSDIO	I/O	Input LVTTL Output 4mA drive	Synchronous serial interface input/input-output data
48	SSCK	O	4mA drive	Synchronous serial interface clock
47	SSCE	O	4mA drive	Synchronous serial interface chip enable
29	SDCD3	I/O	Input LVTTL Output 4mA drive	SD card interface data 3
30	SDCD2	I/O	Input LVTTL Output 4mA drive	SD card interface data 2
31	SDCD1	I/O	Input LVTTL Output 4mA drive	SD card interface data 1
32	SDMSCD0	I/O	Input LVTTL Output 4mA drive	SD card interface data 0 Memory stick interface serial data
33	SDMSCMD	I/O	Input LVTTL Output 4mA drive	SD card interface command Memory stick interface bus state
34	SDMSCLK	O	4mA drive	SD card interface clock Memory stick interface serial clock
36	SDMSDTN	I	LVTTL	SD card interface insertion/extraction detection (active low) Memory stick interface insertion/extraction detection
37	SDWP	I	LVTTL	SD card interface write protect
46	SDPWR	O	4mA drive	SD card interface power control

Table-P6 Pin List (6/7): System Control

Pin	Symbol	I/O	Type	Description
42	REFCLK	I	LVTTL	Reference clock
27	RESETN	I	LVTTL	System reset
39-41	TMOD2-0	I	LVTTL	Test mode (all fixed to "L")
51	TOUT	O	4mA drive	Test output (open)
38	SCAN	I	LVTTL	Test mode (fixed to "L")

Table-P7 Pin List (7/7): Power Supply

Pin	Symbol	Description
35, 52, 76, 88, 103, 127, 138, 176	VDD1	I/O power supply (3.3V)
28, 45, 69, 81, 110, 132, 133, 169	VSS1	I/O ground
8, 22, 64, 89, 114, 152, 162	VDD2	Core power supply (2.0V)
1, 15, 58, 96, 120, 145, 157	VSS2	Core ground
44	VDDP	PLL power supply
43	VSSP	PLL ground

FUNCTIONAL DESCRIPTION

1. General Description

The ML87V3116 is comprised of the following blocks.

1.1 Video Input Interface

The video input interface has two video input ports, and stores image data input from either port into the Data Buffer.

1.2 Display Interface

The display interface outputs image data written into the Data Buffer to the external display unit.
Either color TFT-LCD or TV format can be selected as an output format.

1.3 JPEG Codec

JPEG Codec compresses image data using the JPEG method or decompresses a JPEG file into image data
Furthermore, JPEG Codec can perform a Motion-JPEG operation by repeating the above. JPEG Codec manages the address of each frame using an index during a Motion-JPEG operation.
As the storage location of image data and JPEG files, both internal and external Data Buffers can be selected.

1.4 Rectangle Copy Controller

The rectangle copy controller copies the data in the specified rectangle area into another rectangle area within the Data Buffer. It can reduce the size or rotate images when copying them.

1.5 Data Buffer + Data Buffer Controller

This memory buffer stores video input data, display data and other image data. It is virtually handled as two-dimensional 16-bit deep memory.
This memory supports images with more pixels than the memory capacity by varying the aspect ratio.
Furthermore, external memory can be added as an address extension of this memory. By storing multiple JPEG files into an extension data buffer during a Motion-JPEG operation, for instance, the moving picture recoding/playback time can be extended.

1.6 Host Interface

The host interface allows access to the control register of each block and two memory buffers, including external memory. A type of an interface that is compatible with various CPU buses can be selected by mode pin (HMOD3-0) setting.

1.7 Clock/Power Manager

The clock/power manager controls the generation and stopping of the operating clocks of each block.

2. Function of Each Block

2.1 Video Input Interface

2.1.1 Video Input Ports

There are three types of video input formats.

- BT.656 format : An 8-bit format defined in ITU-R Rec. BT.656
- 8-bit format : A format that deletes the synchronous reference code (EAV/SAV) from BT.656 format, and inputs the horizontal synchronous signal, vertical synchronous signal and field ID separately
- 16-bit format : A format that inputs 8 bits of brightness Y data, 8 bits of color difference C data into which Cb/Cr data are multiplexed, horizontal synchronous signal, vertical synchronous signal and field ID

Either one of two inputs, Y port (VY7-0) and C port (VC7-0), can be selected in BT.656 format.
8-bit format data uses only the Y port.

[Control Registers]

- VMDSEL : Input video format selection, 2 bits (write/read)
  "00": BT.656 format/ "01": 8-bit format/ "10": 16-bit format
- VPTSEL : Port selection in BT.656 mode, 1 bit (write/read)

2.1.2 Synchronous Signal Format for Video Input

Synchronous signals of video input include the horizontal synchronous signal (VHS), vertical synchronous signal (VVS), field ID signal (FID) and data clock (VCLK). A pulse polarity can be selected for each of the synchronous signals.
The FID signal can be used only at the time of interlace input. When the FID input does not operate, whether the input is an interlace input or a progressive input is automatically determined based on the pulse phase relationship between the VHS signal and the VVS signal. In the case of interlace input, an internal field ID signal is generated.
When VHS or VVS signal does not operate, it is determined as an ITU-R Rec. BT.656 input. Then, an internal horizontal synchronous signal and vertical synchronous signal are generated from the synchronous reference code (EAV/SAV) included in the data.
ITU-R BT.656 format is based on the video data interface standard for TV format. However, if data is within the designated data range and uses the synchronous reference code (EAV/SAV), it can be input as a signal that conforms to the standard even if the image size is different.

[Control Registers]

- HSPOL : Horizontal synchronous signal polarity, 1 bit (write/read)
- VSPOL : Vertical synchronous signal polarity, 1 bit (write/read)
- FIDPOL : Field ID polarity, 1 bit (write/read)
- HSCYC : Horizontal synchronous signal cycle, 12 bits (read only)
- VSCYC : Vertical synchronous signal cycle, 12 bits (read only)
- HVDET : VHS signal, VVS signal detection, 1 bit (read only)
- IPDET : Interlace/progressive detection, 1 bit (read only)

2.1.3 Input Image Format

Specify the image area to be loaded into the data buffer for video input.
Specify the start position and size of the effective image area for input synchronous signals using the control register. Furthermore, specify the position on the data buffer where that image area is to be written using the address of the upper left origin.
Store the image area into the picture buffer using the data format of 16 BPP (bit per pixel) and YCbCr 4:2:2: (Y 8 bits, Cb/Cr multiplexed 8 bits).

In the case of interlace input, construct a single frame image with consecutive two fields.

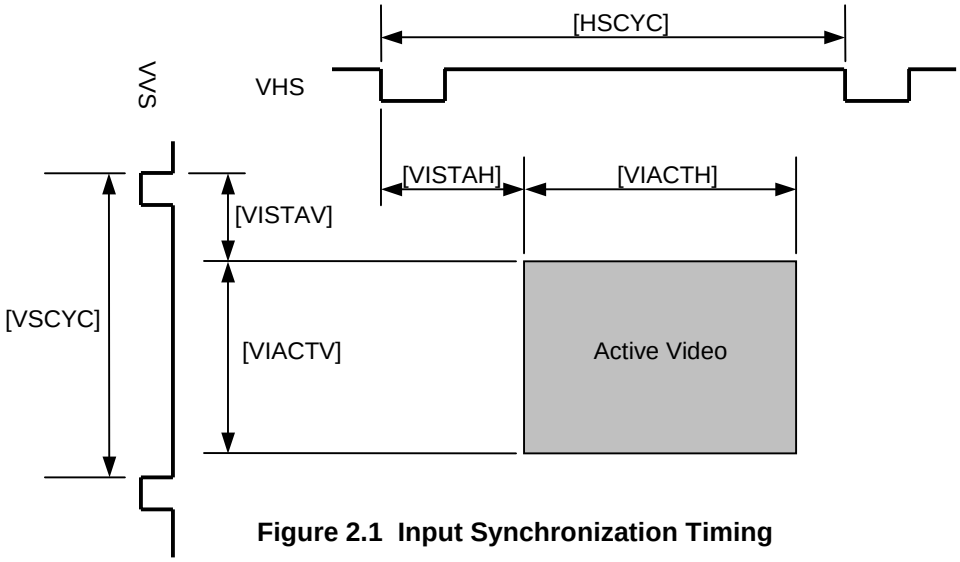


Figure 2.1 Input Synchronization Timing

There are two capture modes in capture operation: 1-frame capture mode and continuous capture mode. In the 1-frame capture mode, one frame of data is written into the Data Buffer after starting a capture operation and then exits. In the continuous capture mode, after capturing one frame of image after starting a capture operation, the data of the next frame is captured from the successive vertical address again. The continuous capture mode can be ended by forced stop.
Images can be captured by thinning the number of input pixels and the number of frames. If images are captured by thinning the number of pixels, the size of an image to be captured gets smaller than the setting value according to that thinning rate. Thinning the number of frames is effective when in the continuous capture mode, and the interval of frames to be captured can be specified.

Use the following frames rate as a guide in the continuous capture mode.

- Up to 720 x 480 pixels: 30 frames/sec max.
- Up to 1 million pixels: 15 frames/sec max.
- Up to 2 million pixels: 10 frames/sec max.
- Up to 4 million pixels: 3 frames/sec max.

[Control Registers]

- VITRIG : Starts image capture/status, 1 bit (write/read)
  At a write, starts image capture when “1” is written, and stops forcibly when “0” is written.
  At a read, “1” indicates capturing, and “0” indicates the completion of capture.
- VIMOD : Image capture mode, 1 bit (write/read)
  “0”: 1 frame capture
  “1”: Continuous frame capture
- VISTAH : Horizontal effective image start position, 12 bits (write/read)
- VISTAV : Vertical effective image start position, 12 bits (write/read)
- VIACTH : Horizontal effective image size, 12 bits (write/read)
- VIACTV : Vertical effective image size, 12 bits (write/read)
- VIDECH : Horizontal direction pixel thinning rate, 3 bits (write/read)
  “000”: 1/1, “001”: 1/2, “010”: 1/4, “011”: 1/8, “100”: 1/16
- VIDECV : Vertical direction pixel thinning rate, 3 bits (write/read)
  “000”: 1/1, “001”: 1/2, “010”: 1/4, “011”: 1/8, “100”: 1/16
- VIFITV : Frame thinning rate, 4 bits (write/read)
  “0000”: 1/1, “0001”: 1/2, …, “1110”: 1/15, “1111”: 1/16
- VCAPAX : Data buffer X address, 8-pixel unit
  12 bits (write/read)
- VCAPAY : Data buffer Y address, 1- (or 8-) line unit
  12 bits (write/read)

2.2 Display Interface

2.2.1 Display Output Format

The TFT-LCD mode or TV mode can be selected as a display output format.

- TFT-LCD mode : Progressive scan, output synchronization, variable number of pixels
- TV mode : Interlace scan, fixed to 525i or 625i

[Control Registers]

- DOFMT : Display format, 1 bit (write/read)
  "0": TFT-LCD mode
  "1": TV mode
- TVSTD : TV format selection, 3 bits (write/read)
  "000" : 525i, 27.0 MHz (NTSC equivalent, BT.656)
  "001" : 525i, 13.5 MHz (NTSC equivalent, BT.601)
  "010" : 525i, 12.272727 MHz (NTSC equivalent, square pixels)
  "011" : 525i, 14.31818 MHz (NTSC equivalent, 4fsc)
  "100" : 625i, 27.0 MHz (PAL equivalent, BT.656)
  "101" : 625i, 13.5 MHz (PAL equivalent, BT.601)
  "110" : 625i, 14.75 MHz (PAL equivalent, square pixels)
  Note: It is necessary to set the system clock to each frequency described above.

2.2.2 Output Synchronous Signals

The functions of the output synchronous signals partially vary with the display output format.

Sync. signal	Function		Remarks
	TFT-LCD mode	TV mode	
CP	Data clock	Data clock	
LDP1	Line drive pulse 1	HSYNC (horizontal synchronous signal)	
LDP2	Line drive pulse 2	(Not used)	
LDP3	Line drive pulse 3	(Not used)	
LDP4	Line drive pulse 4	(Not used)	
HST1	Horizontal start signal 1	(Not used)	Pulse width: 1 CP
HST2	Horizontal start signal 2	(Not used)	Pulse width: 1 CP
FDP1	Frame drive pulse 1	VSYNC (vertical synchronous signal)	
FDP2	Frame drive pulse 2	(Not used)	Possible to AND with LDP4
FDP3	Frame drive pulse 3	(Not used)	Possible to OR with LDP2
FIDF	Current-alternating signal	Field ID signal	
DISP	Display enable	Display enable	

- CP : Data clock
  The polarity of CP can be selected.
- LDP1-4 : Line drive pulse (4 types)
  The pulse cycle is common to LDP1-4, and the pulse width, pulse phase and pulse polarity can be specified in units of the number of CP clocks.
  When in the TV mode, LDP1 is automatically set and used as a HSYNC.
- HST1, 2 : Horizontal start signal (2 types)
  The pulse width is 1 CP clock, and the pulse cycle (common to two types), pulse phase and pulse polarity can be specified.
- FDP1-3 : Frame drive pulse (3 types)
  The frame cycle (common to 3 types), pulse width, pulse phase and pulse polarity can be specified in units of the number of lines.
  By ANDing FDP2 with LDP4, a frame cycle pulse with a pulse width narrower than one line can be set.
  By ORing FDP3 with FDP2, a drive pulse can be set twice in one frame.
  When in the TV mode, FDP1 is automatically set and used as a VSYNC.
- FIDF : Current-alternating drive signal, or field ID signal
  A signal that inverts for each frame, or a signal that inverts for each number of specified lines. In the latter case, the logic at the beginning of a frame is inverted for each frame.
  When in the TV mode, FIDF is automatically set so as to invert for each frame, and used as a field ID signal.
- DISP : Display enable signal
  A signal that specifies display ON/OFF

Set the pulse phases of the “HST1, 2” and “LDP1-4” signals using an internal, virtual horizontal synchronous signal as a reference.
The “FDP1-3” signals are synchronized with this virtual horizontal synchronous signal. Set the pulse phases of the “FDP1-3” signals using an internal, virtual vertical synchronous signal as a reference.
Set the horizontal and vertical effective periods of output data in the same manner.
These settings can be changed in the TFT-LCD mode. However, the values set are held even after switching to the TV mode; thus, display can be performed in the original state when returning to the TFT-LCD mode again.
The “LDP2-4,” “HST1, 2” and “FDP2-3” signals can be used as GPIOs if they are not used as synchronous signals.

[Control Registers]

- CPPOL : Synchronous polarity selection for CP and output data, 1 bit (write/read)
  "0": Synchronizes on the rising edge of CP, "1": Synchronizes on the falling edge of CP
- HLCYC : HST/LDP cycle (units of the number of CP clocks), 11 bits (write/read)
- HST1POL : HST1 pulse polarity selection, 1 bit (write/read)
  "0": Positive pulse, "1": Negative pulse (same for the following)
- HST1POS : HST1 pulse position, 11 bits (write/read)
- HST2POL : HST2 pulse polarity selection, 1 bits (write/read)
- HST2POS : HST2 pulse position, 11 bits (write/read)
- LDP1POL : LDP1 pulse polarity selection, 1 bits (write/read)
- LDP1ST : LDP1 pulse's front edge position, 11 bits (write/read)
- LDP1ED : LDP1 pulse's rear edge position, 11 bits (write/read)
- LDP2POL : LDP2 pulse polarity selection, 1 bits (write/read)
- LDP2ST : LDP2 pulse's front edge position, 11 bits (write/read)
- LDP2ED : LDP2 pulse's rear edge position, 11 bits (write/read)
- LDP3POL : LDP3 pulse polarity selection, 1 bits (write/read)
- LDP3ST : LDP3 pulse's front edge position, 11 bits (write/read)
- LDP3ED : LDP3 pulse's rear edge position, 11 bits (write/read)
- LDP4POL : LDP4 pulse polarity selection, 1 bits (write/read)
- LDP4ST : LDP4 pulse's front edge position, 11 bits (write/read)
- LDP4ED : LDP4 pulse's rear edge position, 11 bits (write/read)
- VFCYC : FDP cycle (units of the number of lines), 10 bits (write/read)
- FDP1POL : FDP1 pulse polarity selection, 1 bits (write/read)
- FDP1ST : FDP1 pulse's front edge position, 10 bits (write/read)
- FDP1ED : FDP1 pulse's rear edge position, 10 bits (write/read)
- FDP2POL : FDP2 pulse polarity selection, 1 bits (write/read)
- FDP2ST : FDP2 pulse's front edge position, 10 bits (write/read)
- FDP2ED : FDP2 pulse's rear edge position, 10 bits (write/read)
- FDP3POL : FDP3 pulse polarity selection, 1 bits (write/read)
- FDP3ST : FDP3 pulse's front edge position, 10 bits (write/read)
- FDP3ED : FDP3 pulse's rear edge position, 10 bits (write/read)
- FDP2MIX : Positive pulse AND synthesis between FDP2 and LDP4, 1 bit (write/read)
  "0": Without synthesis, "1": With synthesis
- FDP3MIX : Positive pulse OR synthesis between FDP3 and LDP2 bit (write/read)
  "0": Without synthesis, "1": With synthesis
- ACTHST : Horizontal start position of effective image data, 11 bits (write/read)
- ACTHED : Horizontal end position of effective image data, 11 bits (write/read)
- ACTVST : Vertical start position of effective image data, 10 bits (write/read)
- ACTVED : Vertical end position of effective image data, 10 bits (write/read)

- LDP2IO : Specify the LDP2 signal in GPIO6, 1 bit (write/read)
  "0": Synchronous signal, "1": GPIO (same for the following)
- LDP3IO : Specify the LDP3 signal in GPIO5, 1 bit (write/read)
- LDP4IO : Specify the LDP4 signal in GPIO4, 1 bit (write/read)
- HST1IO : Specify the HST1 signal in GPIO3, 1 bit (write/read)
- HST2IO : Specify the HST2 signal in GPIO2, 1 bit (write/read)
- FDP2IO : Specify the FDP2 signal in GPIO1, 1 bit (write/read)
- FDP3IO : Specify the FDP3 signal in GPIO0, 1 bit (write/read)
- GPIN6-0 : GPIO6-0 input/output mode, 7 bits (write/read)
- GPIOD6-0 : GPIO6-0 data, 7 bits (write/read)
  At a write, data is output to the GPIO that corresponds to the bits of the output mode. At a read, the signal level of the GPIO that corresponds to the bits of the input mode is read. Reading the bits of the output mode and writing to the bits of the input mode are disabled.

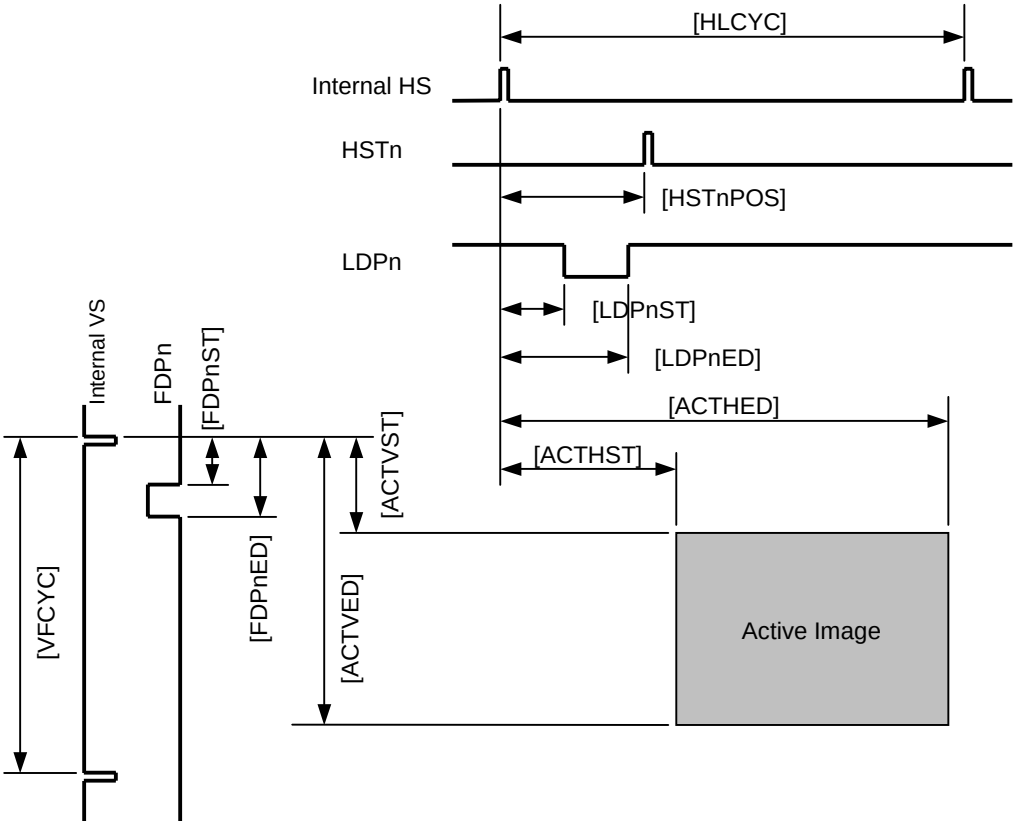


Figure 2.2 Output Synchronization Timing

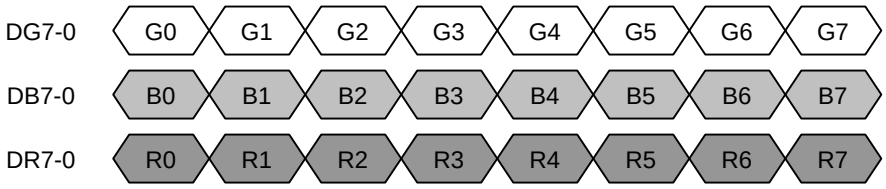
2.2.3 Display Data Formats

The RGB format or YCbCr format can be selected as a display data format.
Because the data in a data buffer is in 16-bit YCbCr, 4:2:2 format, color space conversion is performed after expanding into 24-bit, 4:4:4 format first.
Cb/Cr data is interpolated when expanding from 4:2:2 format to 4:4:4 format.
The color space conversion formula is in accordance with ITU-R Rec. BT-601.

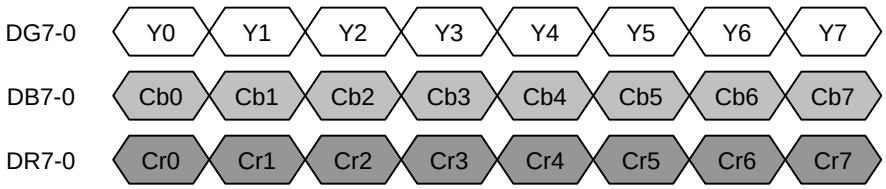
[Control Registers]

- DOFMT : Output data format, 2 bits (write/read)
  "00": RGB. 4:4:4, 24 bits
  "01": YCbCr 4:4:4, 24 bits
  "10": YCbCr 4:2:2, 16 bits (no conversion)
  "11": YCbCr 4:2:2, 8 bits, BT.656
- DCINTP : Cb/Cr interpolation method, 1 bit (write/read)
  "0": Linear interpolation (average of preceding and succeeding data)
  "1": Repeat of the previous data

DOFMT="00": RGB, 4:4:4, 24 bits



DOFMT="01": YCbCr, 4:4:4, 24 bits



DOFMT="10": YCbCr, 4:2:2, 16 bits

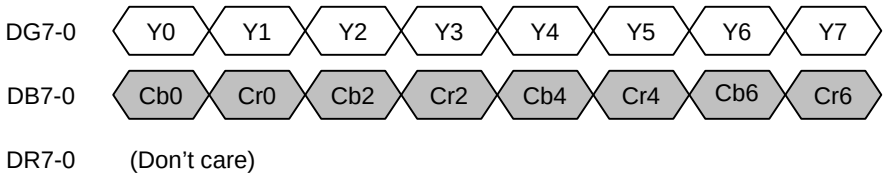


Figure 2.3 Display Data Formats

2.2.4 Display Data Area Partition, Display/Hide

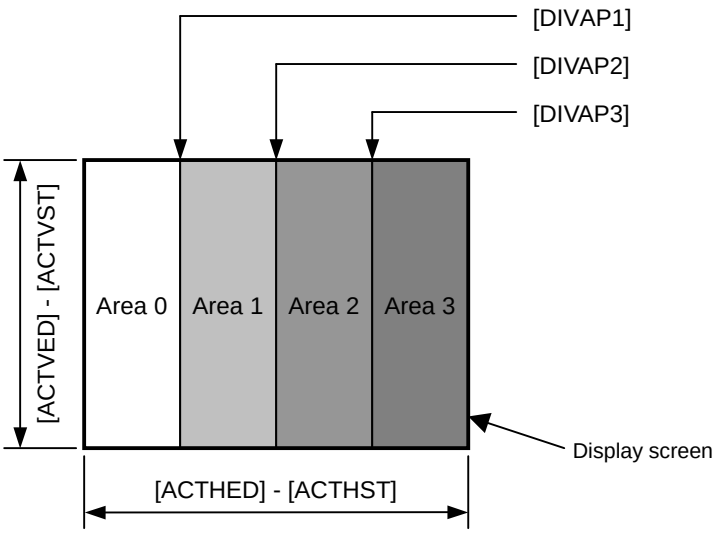
The effective data area of the display output can be divided into four partitions. Horizontal division or vertical division can be selected, and the data buffer address of data to be displayed in each of the four areas can be specified individually.

Also, the specified area can be hidden. Hidden areas are not used to read the data buffers.

[Control Registers]

- DASMOD : Display area partition mode, 1 bit (write/read)
  "0": Horizontal partition, "1": Vertical partition
- DIVAP1 : Display area 0-1 partition point, 10 bits (write/read)
- DIVAP2 : Display area 1-2 partition point, 10 bits (write/read)
- DIVAP3 : Display area 2-3 partition point, 10 bits (write/read)
- DA0SAX : Data buffer read start X address for display area 0, 8-pixel units
  12 bits (write/read)
- DA0SAY : Data buffer read start Y address for display area 0, 8-line units
  12 bits (write/read)
- DA1SAX : Data buffer read start X address for display area 1, 8-pixel units
  12 bits (write/read)
- DA1SAY : Data buffer read start Y address for display area 1, 8-line units
  12 bits (write/read)
- DA2SAX : Data buffer read start X address for display area 2, 8-pixel units
  12 bits (write/read)
- DA2SAY : Data buffer read start Y address for display area 2, 8-line units
  12 bits (write/read)
- DA3SAX : Data buffer read start X address for display area 3, 8-pixel units
  12 bits (write/read)
- DA3SAY : Data buffer read start Y address for display area 3, 8-line units
  12 bits (write/read)
- DPENB0-3 : Partition area display enable, 4 bits (write/read)
  "0": Display, "1": Hide (each bit)
- BLKCOL : Output data in hidden area, 1 bit (write/read)
  "0": All "L", "1": All "H"
- DOPSNG : Positive/negative mode of output data, 4 bits (write/read)
  "0": Normal mode (positive), "1": All bits reversed (negative)
- DISP : DISP signal output level, 1 bit (write/read)
  "0": "L" level, "1": "H" level

Horizontal Partition Mode



Vertical Partition Mode

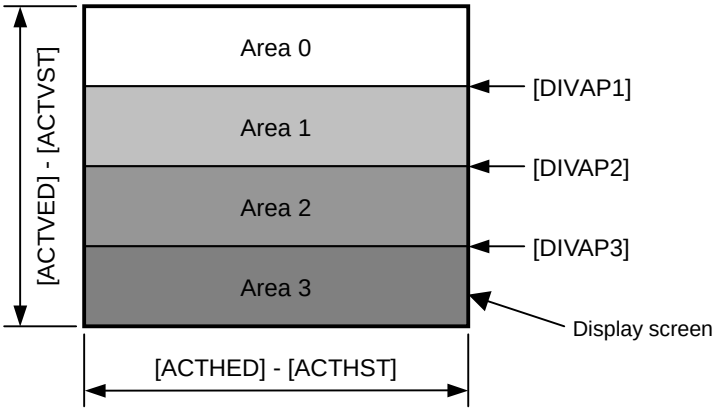


Figure 2.4 Display Area Partitioning

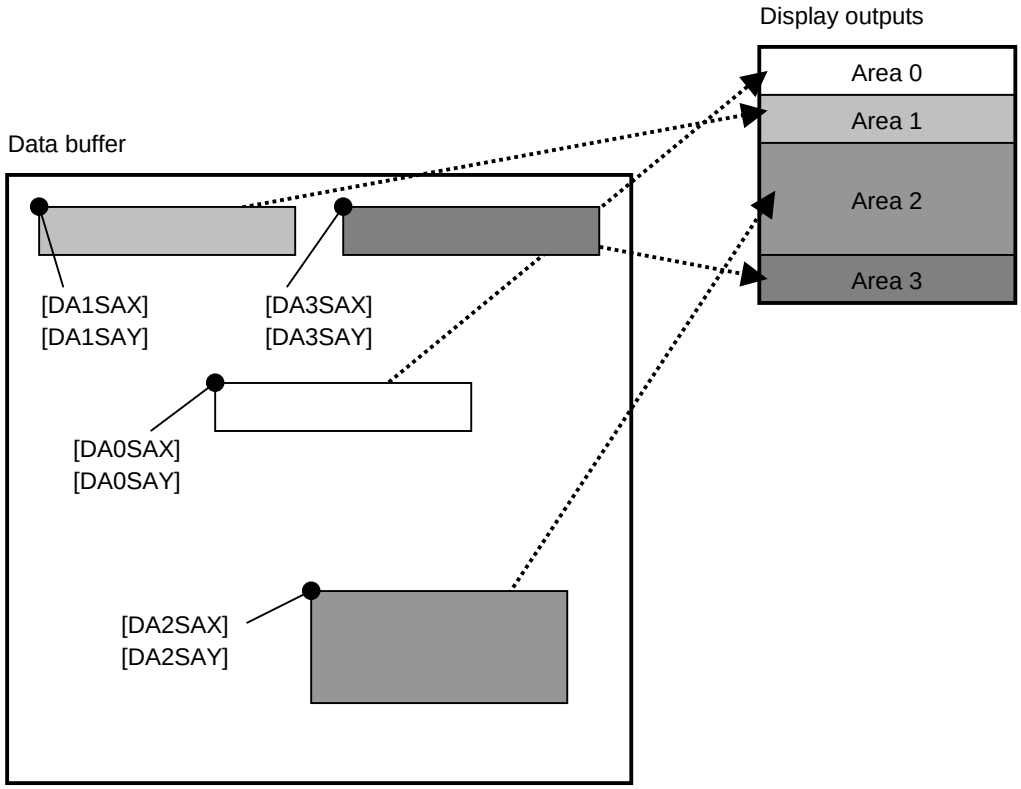


Figure 2.5 Display Address Specification (Example in Vertical Partition Mode)

2.3 JPEG Codec

2.3.1 General Description

JPEG Codec compresses and decompresses image data.
When compressing images, JPEG Codec uses a rectangle area specified in the Data Buffer as the source image, sequentially reads data into block forms, compresses data using the JPEG method, and then converts the compressed data to a compressed data file in the JFIF format. This compressed data file is written in the rectangle area from the start address specified in the Data Buffer. Compression formats such as block interleave are in accordance with the JPEG baseline standard. Set the source image size, quantization table and Huffman table using control registers in advance. Color components only support the 2:1:1 format equivalent to 4:2:2 of video. For image compression, the sequential compression of input image data can be performed by conducting an operation simultaneously with image input.

When decompressing images, JPEG Codec sequentially reads a compressed data file from the start address specified in the Data Buffer, decompresses data using the JPEG method, placing restored data block again, and reconstructing images. Decompressed images are sequentially written from the start address specified in the Data Buffer in block units. The image size, quantization table and Huffman table are extracted from a compressed data file in the JFIF format.

2.3.2 Still Picture Mode and Moving Picture Mode

Compression and decompression operations are available in two modes: still picture mode and moving picture mode.

In the still picture mode, an operation starts by writing to the startup register, and ends when the processing of one image “frame” completes. Also, an operation can temporarily be stopped for each number of specified lines. This makes it possible to process images having the number of pixels larger than the memory buffer capacity. It does not relate to the restart marker RSTm.

The moving picture mode is a repetition of operations in the still picture mode. By automatically managing the addresses of compressed data files, multiple files can sequentially be compressed or decompressed. An operation in the moving picture mode is started by writing to the startup register, and ended after the completion of a series of specified operations, or the same operation is repeated.
When recording (compressing) moving pictures, the operation is synchronized with the frame timing of video input. When playing back (decompressing) moving pictures, the operation is synchronized with the frame timing of video output.
During an moving picture recording operation, the same image size, quantization table and Huffman table are used for all frames. They cannot be changed during recording.

2.3.3 Moving Picture Mode

The size of a compressed data file in each frame is restricted by the segment size specification. For the segment size, any of 256/512/1K/2K/4K/8K/16K/32K/64K bytes can be selected according to the image size.
(Be careful so that the compressed data file size does not exceed the segment size.)

The addresses of compressed data files are managed using index pointers.
An index pointer is 16 bits in size, and indicates the number of a frame to be compressed or decompressed. A frame number is equivalent to the upper bit of the start address of a compressed data file. An actual address is a value that is shifted to the left by the number of bits for the segment size.

An index pointer is a sort of a counter.
When recording moving pictures, the value of an index pointer is incremented from 0 to the specified number of frames for each input frame.
When playing back moving pictures, various playback operations can be performed, such as “normal play” that increments an index pointer for each display frame, “reverse play” that decrements an index pointer, “slow play” that increments an index pointer for 2/4/8/15/30/60 display frames, and "fast forward play" that skips an index pointer at intervals of specified numbers.

One or two locations can be specified as the source image read addresses when compressing and playback image write addresses when decompressing. If two locations are specified at the same time, they can alternately be switched for each frame. When playing back moving pictures, a double-buffer operation can be performed, achieving smooth moving picture display.

2.4 Rectangle Copy Controller

2.4.1 General Description

The rectangle copy controller reads data from the specified rectangle area (copy source), reduces and/or rotates it, and writes it into another specified area (copy destination).
Specify the start addresses (X start, Y start) (upper left coordinates) of the copy source and copy destination and the rectangle size (X size, Y size), and perform a copy operation using a startup command.
When copying, either reduction or rotation can be specified.
For the reduction magnification, x1 (no reduction), x1/2, x1/8, x1/16, or x1/32 can be selected.
For rotation, 0 deg. (no rotation), 90 deg., 180 deg. or 270 deg. (all clockwise rotations) can be selected.
The rectangle size of the copy destination is set as the size calculated from the rectangle size of the copy source according to the reduction/rotation function.
Reduction and rotation cannot be specified at the same time.

Also, data buffer access from the host CPU goes through this rectangle copy controller.
When writing from the host, specify the host as the copy source, and also specify the start address of the copy destination and the rectangle size. When continuous writes are performed from the host, data is sequentially written into the specified rectangle area.
When reading from the host, specify the host as the copy destination, and also specify the start address of the copy source and the rectangle size. When continuous reads are performed from the host, data is sequentially read from the specified rectangle area.

Table 2.4.1 Copy Function List

No.	Function name	Functional description	Note
1	Rotate	Rotate data in a rectangle area in the Data Buffer, and copy it into an area of the copy destination. <<Rotation angles>> Clockwise rotation: 0°, 90°, 180°, 270°	
2	Reduce	Reduce data in a rectangle area in the Data Buffer in both the horizontal and vertical directions, and copy it into an area of the copy destination. <<Reduction rates>> Horizontal: x1/2, x1/4, x1/8, x1/16, x1/32 Vertical: x1/2, x1/4, x1/8, x1/16, x1/32	
3	Fill	Fill a rectangle area in the Data Buffer with the color data (Y, Cb, Cr) specified from the host CPU.	
4	Host Access	Read data in a rectangle area in the Data Buffer by the host CPU. Also, write data sent from the host CPU into a rectangle area in the Data Buffer .	

2.4.2 Specifying a Rectangle Area

Specify a rectangle area using the start address (Xadrs, Yadrs) and size (Xsize, Ysize).
For the start address, specify the start addresses using an upper left point of a rectangle area even when copying by rotating.
Be sure to specify a rectangle area within the range of the buffer memory size in use.

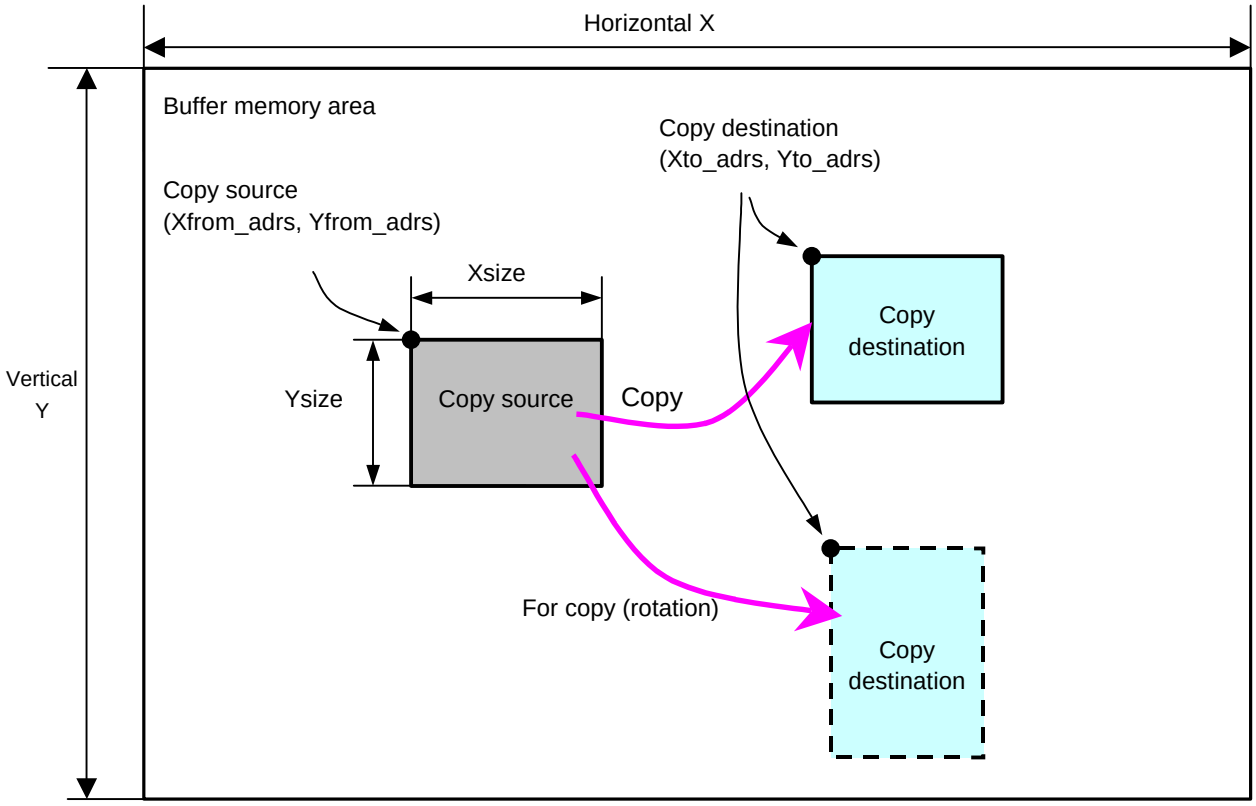


Figure 2.4.2 Image of Rectangle Area Specification

2.4.3 Rotation Processing in Block

The copy controller rotates the rectangle area specified by the host CPU, and copies it into an area of the copy destination.

C data when rotating 90° or 270° is thinned out and its position is adjusted.

<<Rotation angles>>

Clockwise rotation: 0°, 90°, 180°, 270°

<<Host CPU specification contents>>

Rectangle area start address of copy source (Xfrom_adrs, Yfrom_adrs)
Rectangle area size of copy source (Xsize, Ysize)
Rotation angle (Angle)
Start address of copy destination (Xto_adrs, Yto_adrs)

<<Rectangle specification restriction items>>

Minimum pixel unit for rotation processing: 16 pixels x 16 lines
Rectangle area start address unit of copy source:
Horizontal direction: 16 pixels
Vertical direction: 4 lines
Rectangle area start address unit of copy destination:
Horizontal direction: 16 pixels
Vertical direction: 4 lines

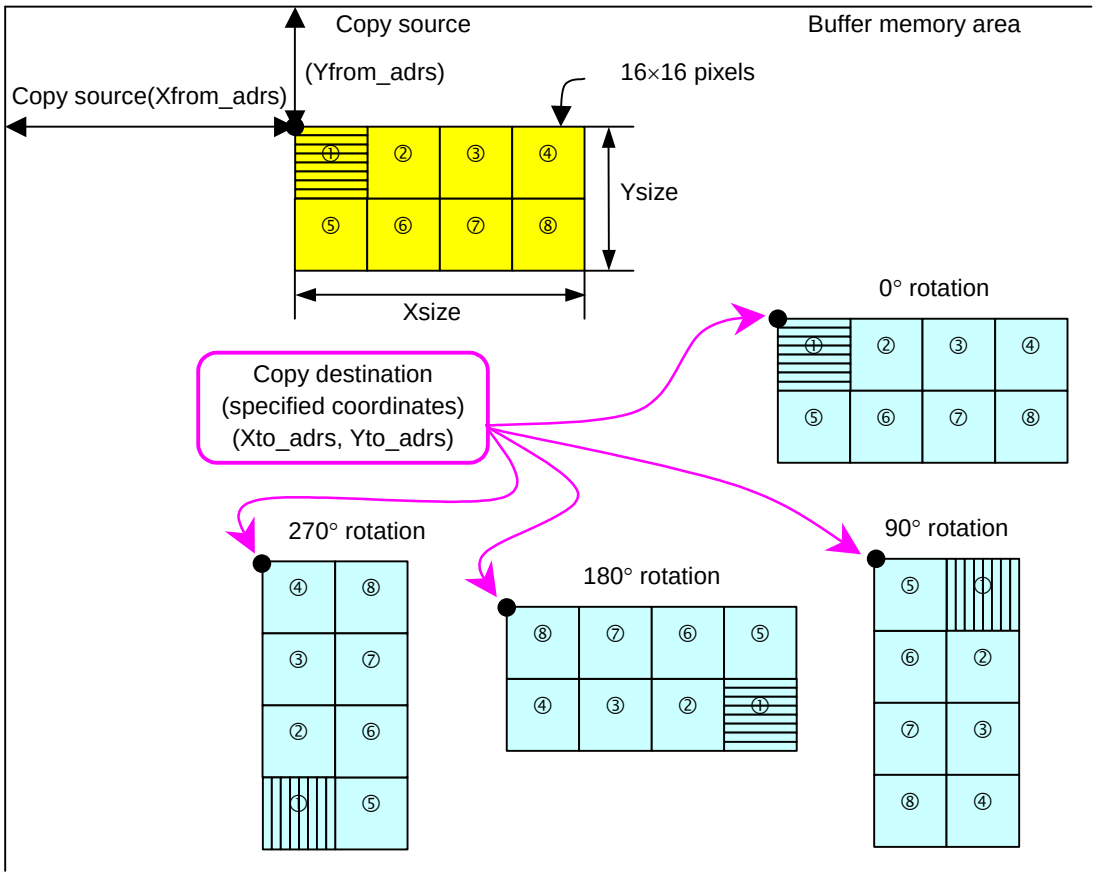


Figure 2.4.3 Example of Copy Destination Coordinate Specification and Processing Sequence for Copy by Rotating

2.5 Data Buffer and Controller

2.5.1 General Description

A data buffer is a memory buffer having two-dimensional addresses. The memory size is 1 Mbyte and the depth is 1 pixel (16 bits).
Write/read access to the Data Buffer is always performed via block access.
External SDRAM is called an extension Data Buffer, which is assumed as an address extension area of the internal Data Buffer. However, there are restrictions on access to extension Data Buffers.

If the internal data buffer is used two-dimensionally, the X size (horizontal direction) and Y size (vertical direction) of the memory size can be changed.

- Data buffer size variations (X size × Y size)
  4096 × 128 pixels
  2048 × 256 pixels
  1024 × 512 pixels
  512 × 1024 pixels

The following types of sources are available for access to data buffers:

a) Video input write
b) Display output read
c) JPEG block access read/write
d) JPEG compressed data file read/write
e) Copy source read
f) Copy destination write
g) Host access read/write
h) Refresh

For access to the internal Data Buffer, up to four access sources can simultaneously (time sharing) be used among the access sources listed above. However, JPEG accesses of c) and d) are always carried out simultaneously in pair. Also, during the operations of the copy functions e) and f), the host access g) cannot be carried out simultaneously.
For access to an extension data buffer, always only one access source can be used.

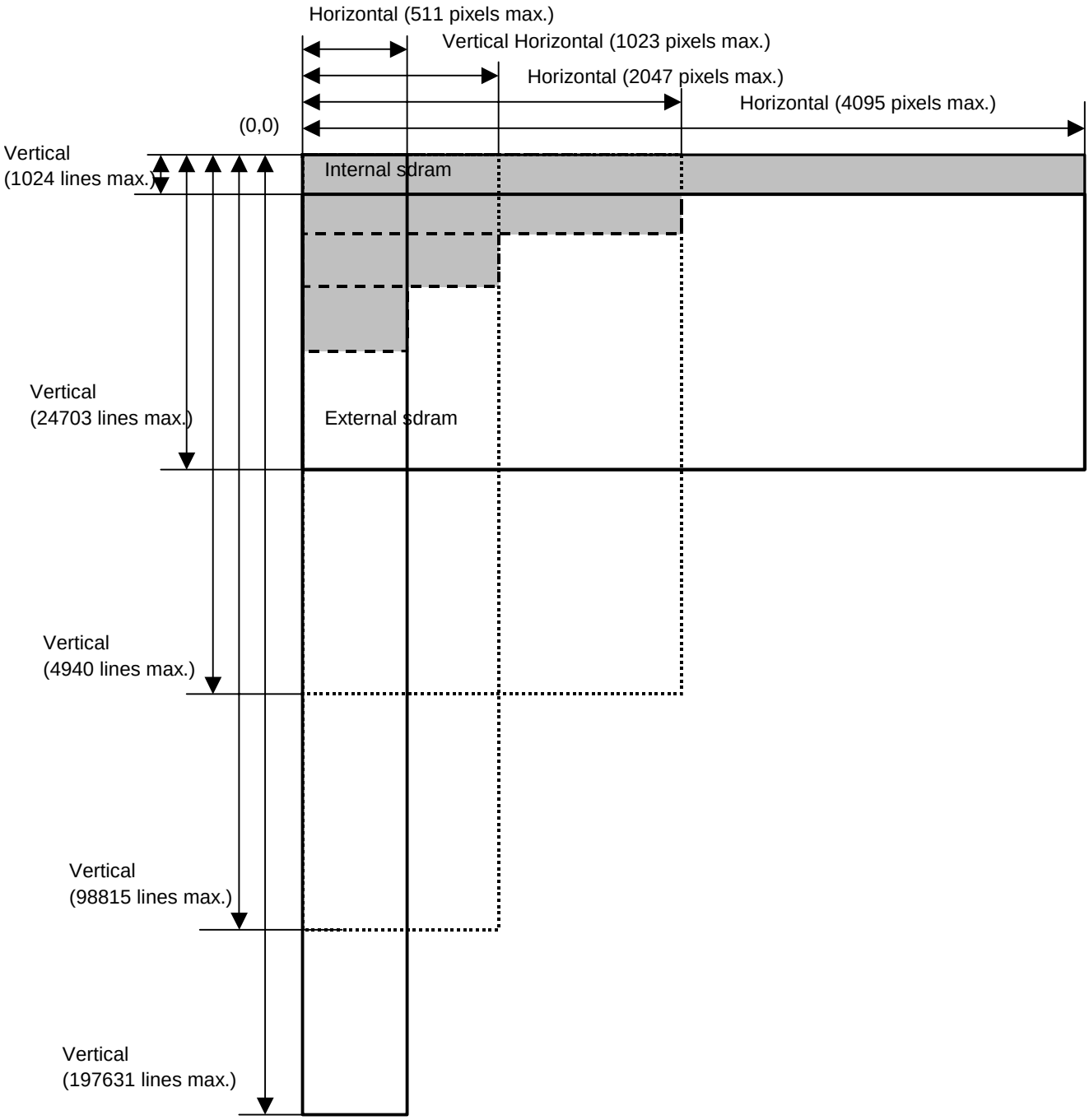


Figure 2.5.1 Image of Buffer Memory Size

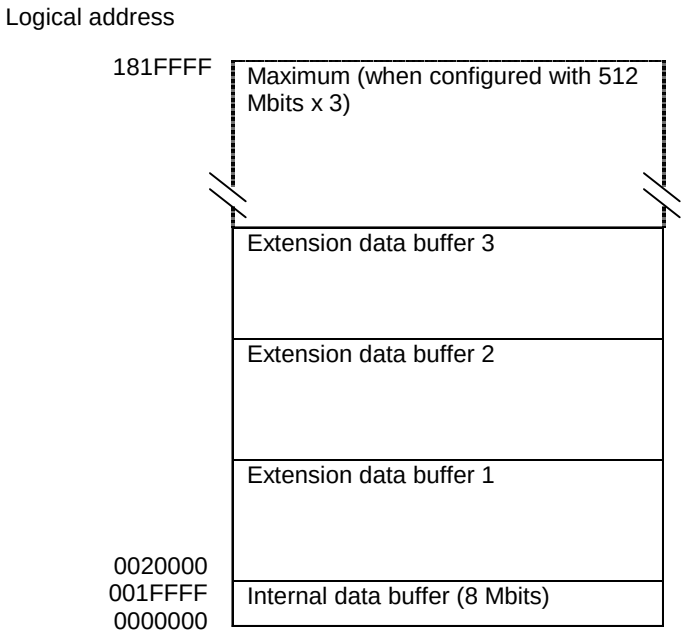


Figure 2.5.2 Data Buffer Memory Map

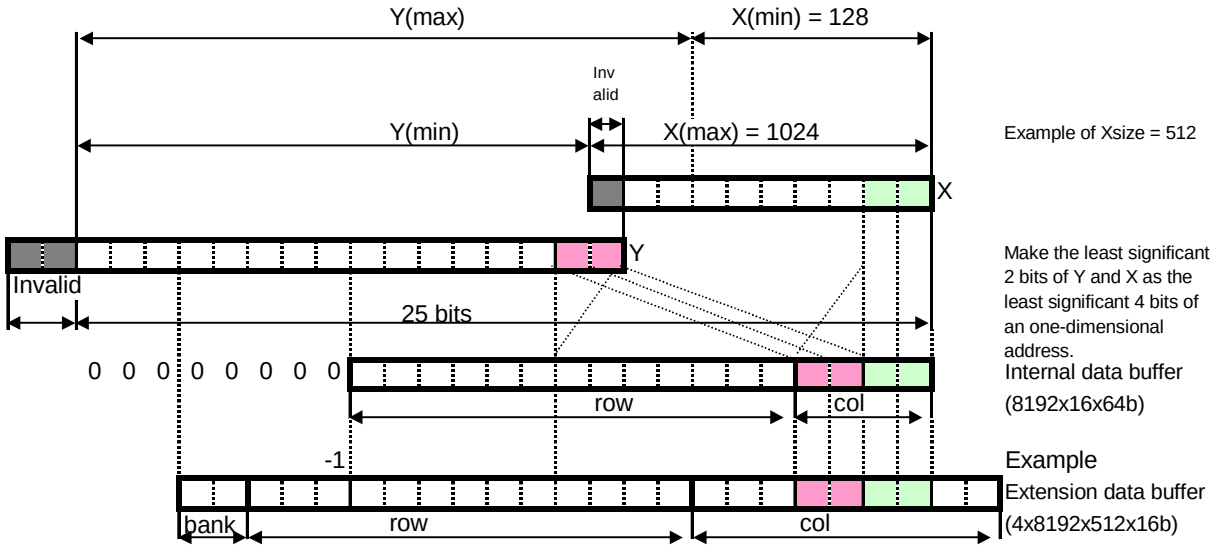


Figure 2.5.3 Address Conversion

2.6 Host Interface

2.6.1 General Description

The host interface allows access to the control register of each block and the internal/external Data Buffers. A type of an interface that is compatible with various CPU buses can be selected by mode pin (HMOD3-0) setting.

Also, there are an I^2C bus master and synchronous serial interface master that can directly be controlled by the host interface.

Table-F5.1 Host Interface Bus Modes

HMOD [3:0]	Bus type	Address/ data bus	Bus control	Reference CPU *1)
0 0 0 0	A0	Separate A[18:00] D[07:00]	CSN, WEN, REN, Busy	Renesas SH-1, SH-2, H8S Fujitsu F^2MC-16F, FR30 Toshiba TLCS-900/H2
0 0 0 1	A1		AS, WEN, REN, Busy	Renesas SH-4, SH-3 *2)
0 0 1 0	A2		BSN, WEN, REN, ACK	Motorola MCF5204 Toshiba TX39
0 0 1 1	—		(Reserved)	—
0 1 0 0	A4		BSN, RWN, DSN, ACK	Toshiba TX19 Motorola MCF5206 MPC801/850, M68K
0 1 0 1	A5		BSN, RWN, DSN, Busy	Renesas M32R, NEC V830 Intel SA-110
0 1 1 X	—		(Reserved)	—
1 0 0 0	B0	Multiplex A[18:16] AD[15:00]	ASN, WEN, REN, Busy	Renesas SH-1, SH-2 NEC V850, 78K/IV Renesas M16C Oki MSM66K, 80C51
1 0 0 1	B1		AS, WEN, REN, Busy	Fujitsu F^2MC-16L Toshiba TLCS-900 Renesas M16C Oki MSM66K, 80C51
1 0 1 X	—		(Reserved)	—
1 1 X X	—			

*1) The CPUs listed above are reference models. Upon verifying the specification of the CPU bus you are using, select a setting mode.

*2) In the case of the SH-3, invert the bus strobe signal and input to the BSN pin.

2.6.2 Bus Control Signals

The assignment of the bus control signals to the input/output pins is determined by the host interface bus mode.

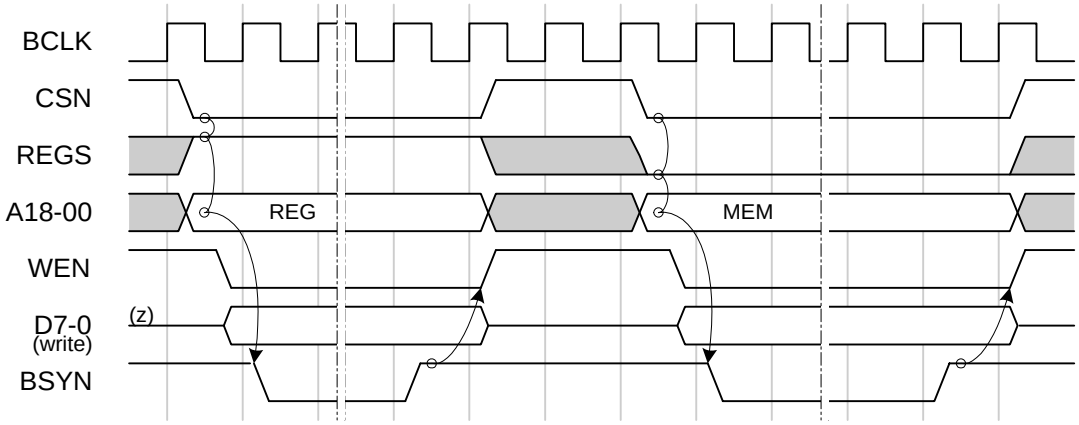
Table-F5.5.1 Bus Control Signals

Pin name	Bus type						
	A0	A1	A2	A4	A5	B0	B1
A18-16	A18-16	A18-16	A18-16	A18-16	A18-16	A18-16	A18-16
AD15-00	A15-00	A15-00	A15-00	A15-00	A15-00	AD15-00	AD15-00
D07-00	D07-00	D07-00	D07-00	D07-00	D07-00	—	—
REGS	REGS	REGS	REGS	REGS	REGS	REGS	REGS
CSN	CSN	CSN	CSN	CSN	CSN	CSN	CSN
REN	REN	REN	REN	RWN	RWN	REN	REN
WEN	WEN	WEN	WEN	—	—	WELN	WELN
BSN	—	BS	BSN	BSN	BSN	ASN	AS
DSN	—	—	—	—	—	WEHN	WEHN
BSYN	BSYN	BSYN	ACK	ACK	BSYN	BSYN	BSYN
BCLK	BCLK	BCLK	BCLK	BCLK	BCLK	BCLK	BCLK

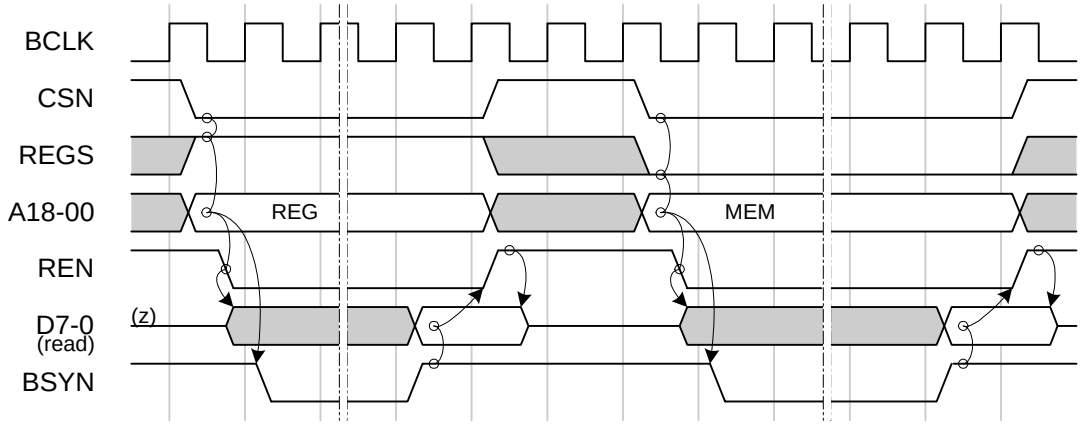
REGS : Memory/register address space selection: “L”: Memory, “H”: Register
CSN : Chip select (active “L”)
REN : Read enable (active “L”)
WEN : Write enable (active “L”)
WEHN : Upper byte write enable (active “L”)
WELN : Lower byte write enable (active “L”)
RWN : Read/write selection: “L”: Write, “H”: Read
BSN : Bus start (active “L”)
ASN : Address strobe (active “L”)
DSN : Data strobe (active “L”)
BSYN : Bus busy or wait, variable width according to wait time (active “L”)
ACK : Data acknowledge, 1 clock width (active “L”)
BCLK : Bus clock

[Bus Interface Timing]

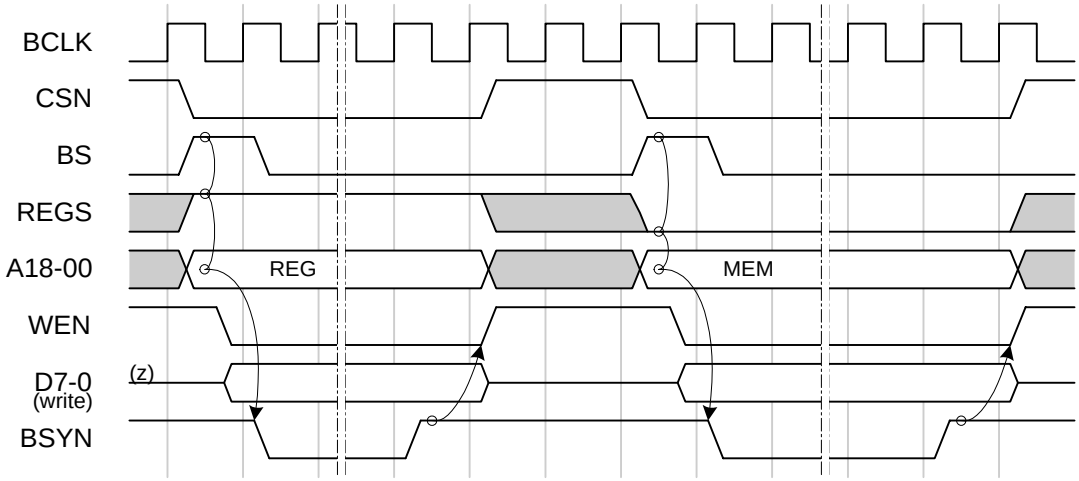
(1) A0-Type Write



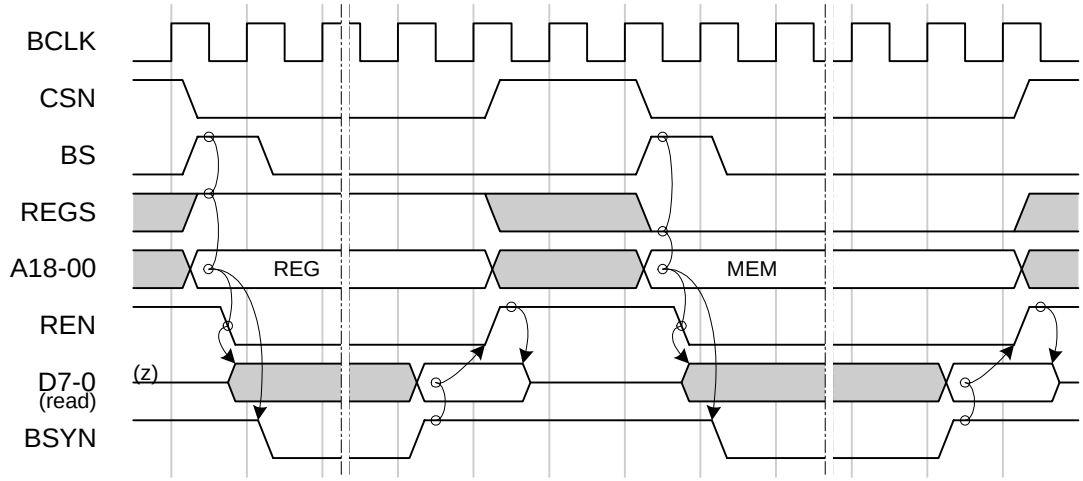
(2) A0-Type Read



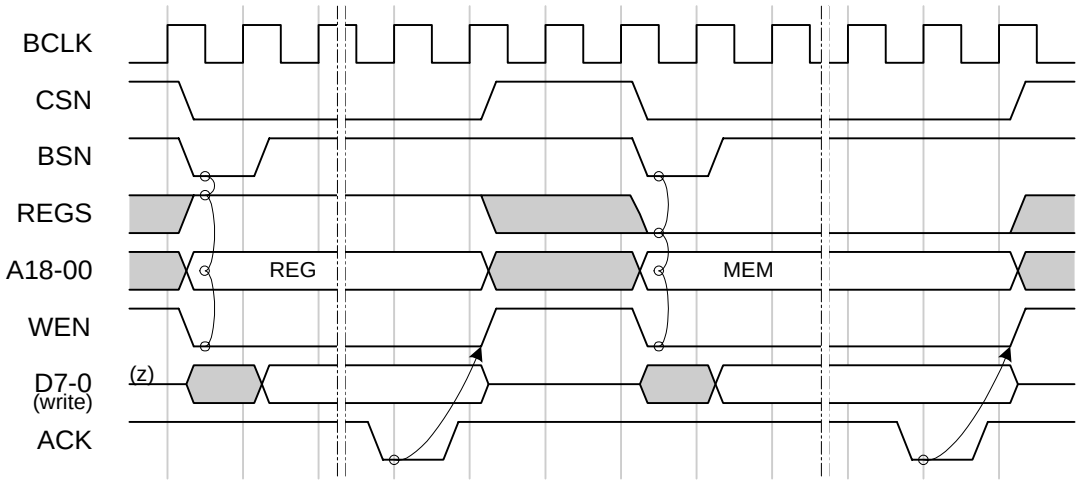
(3) A1-Type Write



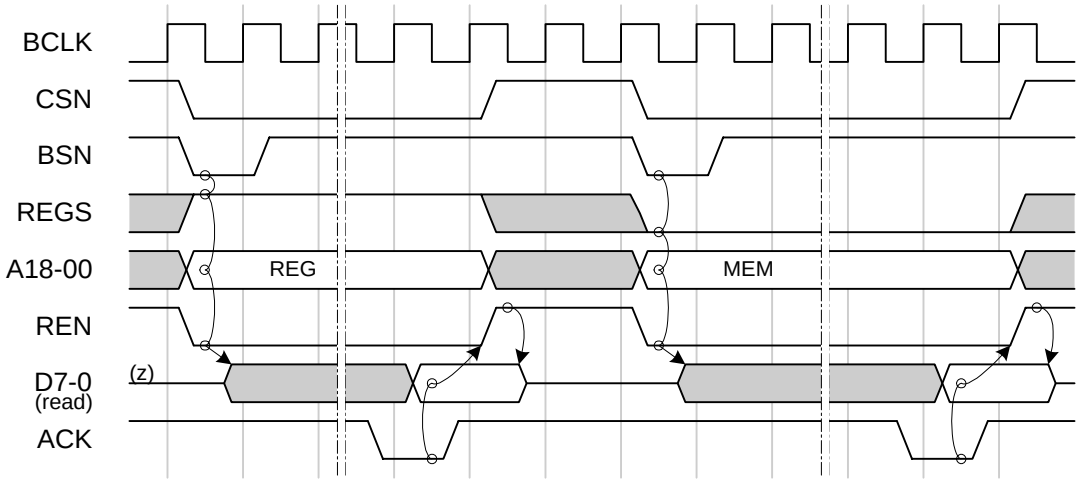
(4) A1-Type Read



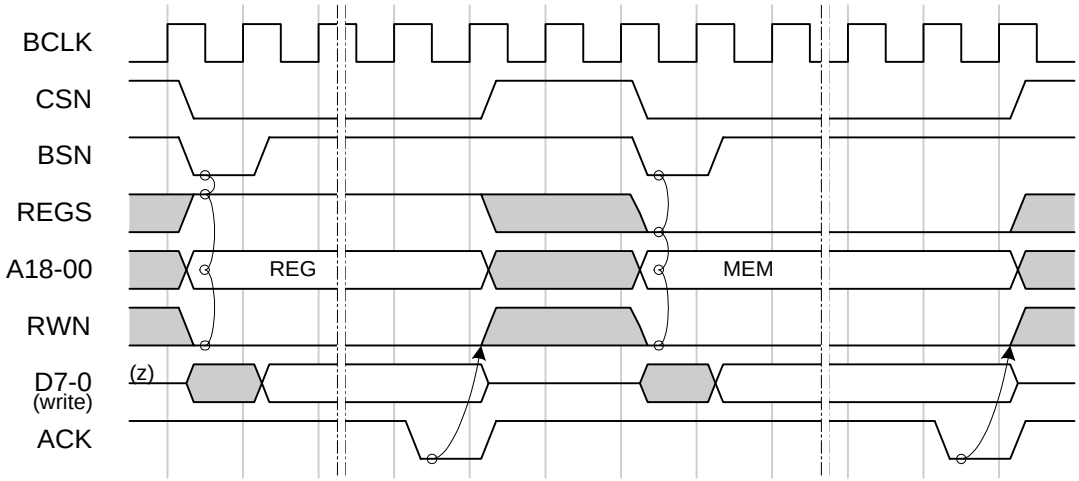
(5) A2-Type Write



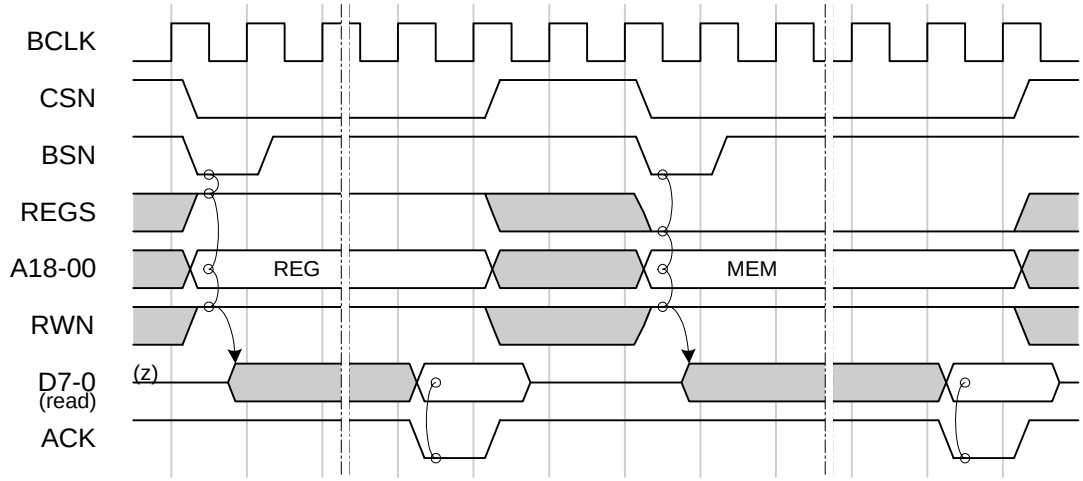
(6) A2-Type Read



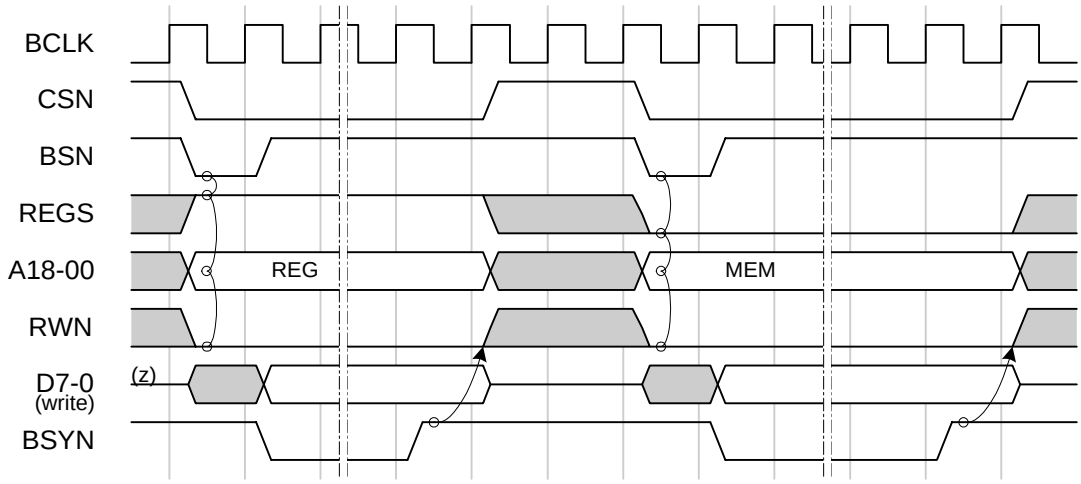
(7) A4-Type Write



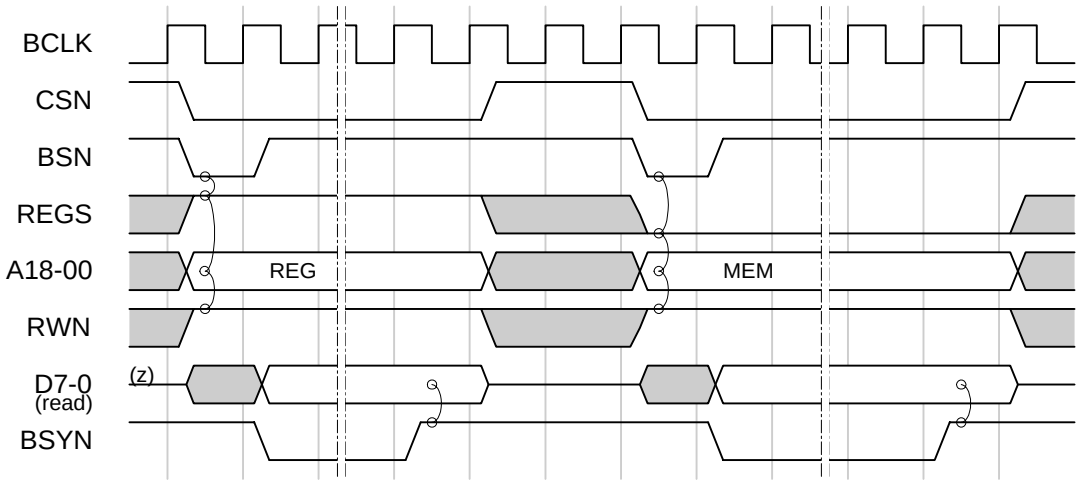
(8) A4-Type Read



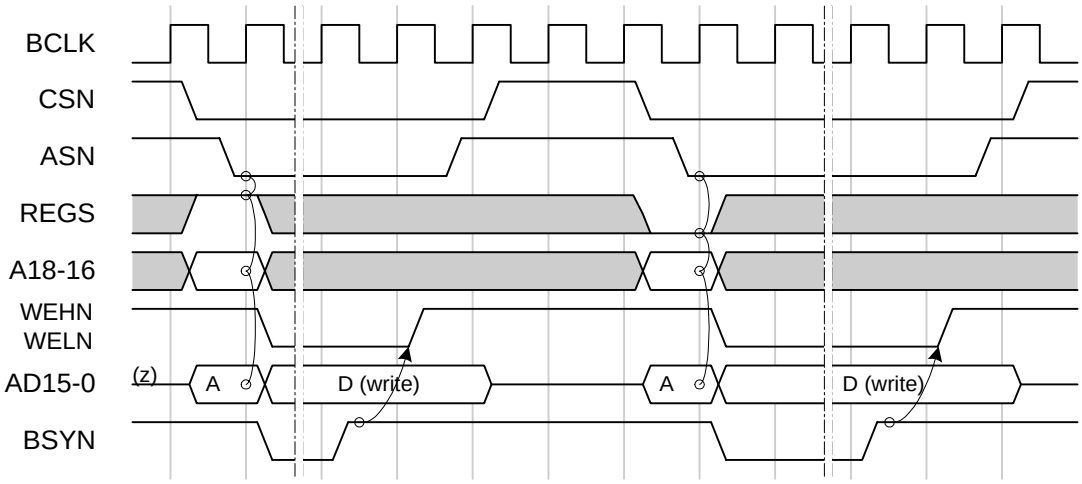
(9) A5-Type Write



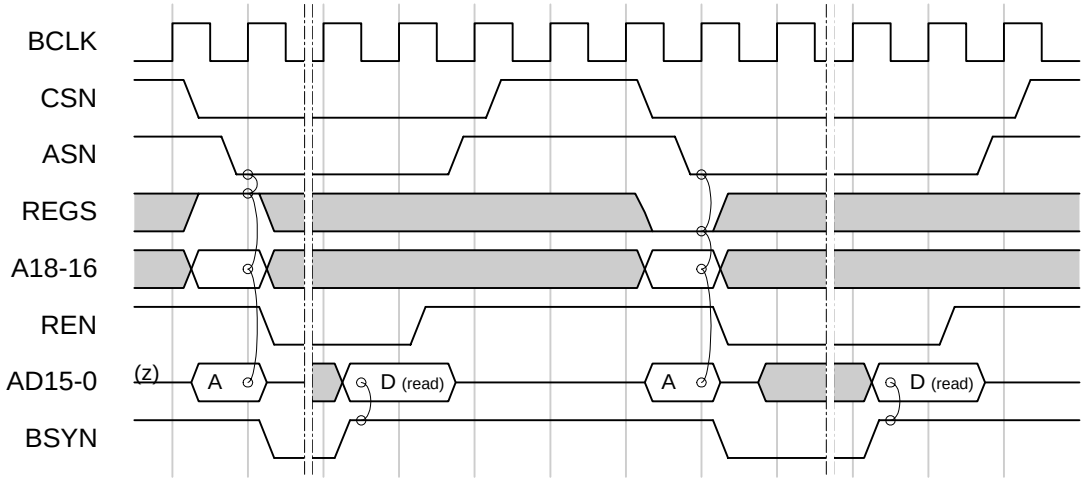
(10) A5-Type Read



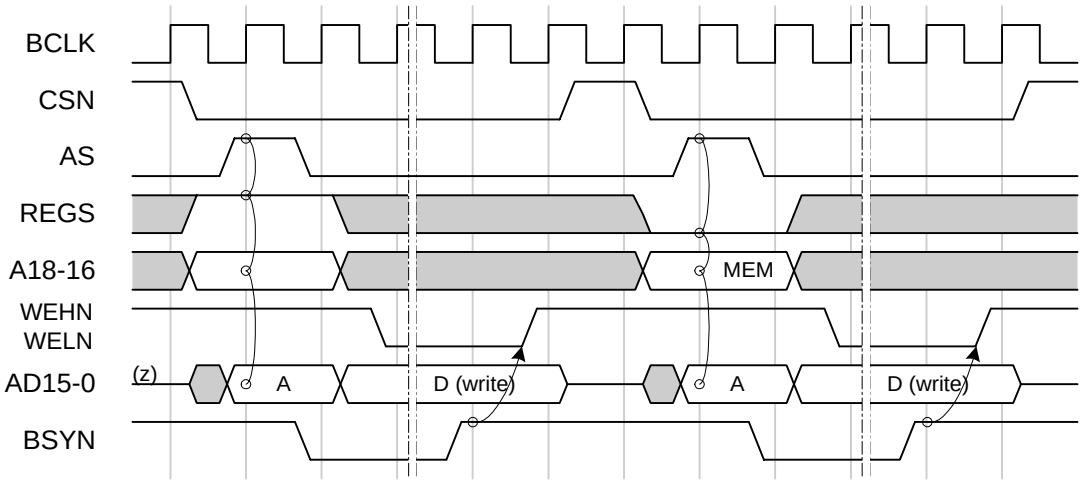
(11) B0-Type Write



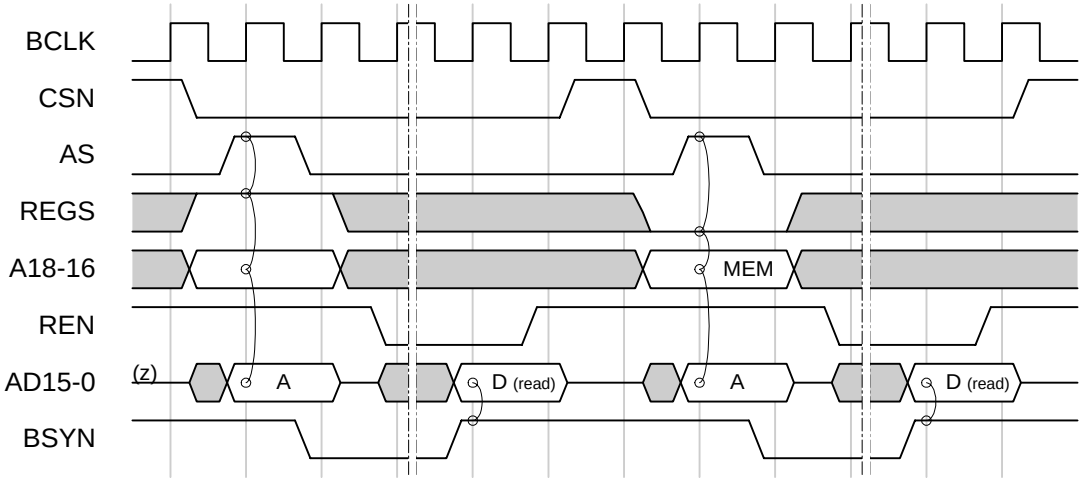
(12) B0-Type Read



(13) B1-Type Write



(14) B1-Type Read



2.7 Clock/Power Manager

2.7.1 General Description

The system clock of the ML87V3116 uses the same pixel clock frequency as display output or a frequency of x2, x4 or x8. This clock generates the REFCLK input by a built-in PLL using simple integer ratio n/m (n and m are 1 to 255) as a reference. Power saving can be achieved by setting to a slower system clock frequency at standby.
The video input clock VCLK and host interface bus clock BCLK are asynchronous with the system clock. The frequency ratio to the system clock can be set in a range of 1:10 to 10:1.

The system clock is distributed to each function block and its ON/OFF can be controlled individually.
The types of a clock to be distributed are:

- Video input interface
- Display output interface
- JPEG Codec
- Rectangle copy controller
- Data buffer controller and internal SDRAM
- External SDRAM clock for extension data buffers
- I^2C bus master
- Synchronous serial interface (SPI) master
- SD card controller
- Memory stick controller

2.7.2 Clock Generation

The system clock of the ML87V3116 uses x2, x4 or x8 of the pixel clock frequency of display output. This clock generates the REFCLK input by a built-in PLL using simple integer ratio n/m (n and m are 1 to 255) as a reference. (System clock = n/m•REFCLK)
The clock for JPEG is generated by the frequency divider of another system, and can be operated even at a slower speed than the system clock.
The system clock is distributed to internal modules. The clock for each module can control a clock enable individually by register control, so that it can be used for the purpose of reducing power consumption.

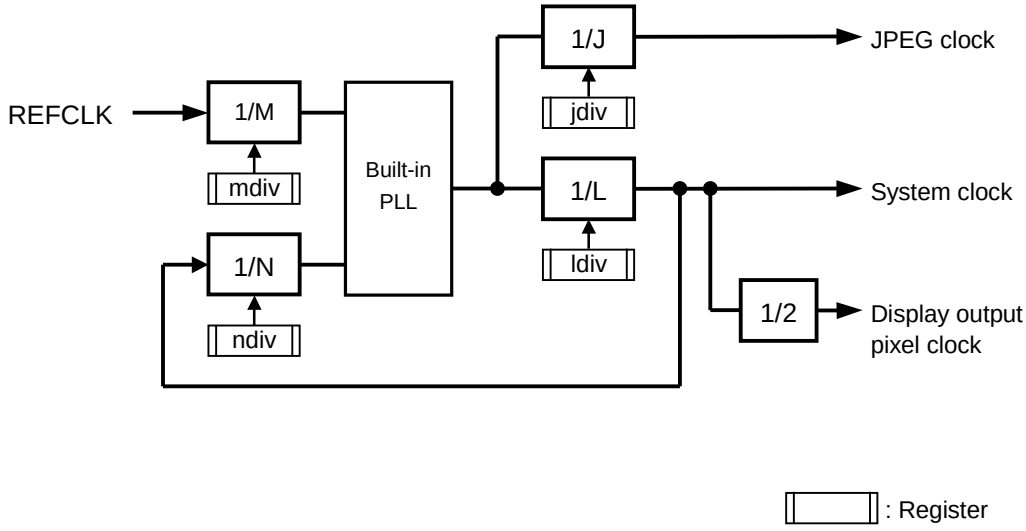


Figure 2.7.1 Clock Generation

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
I/O power supply	VDD1	Ta = 25°C	–0.3 to +4.6	V
Core power supply	VDD2	Ta = 25°C	–0.3 to +3.6	V
PLL power supply	VDDP	Ta = 25°C	–0.3 to +3.6	V
Input voltage	VI	Ta = 25°C	–0.3 to VDD1+0.3	V
Output voltage	VO	Ta = 25°C	–0.3 to VDD1+0.3	V
Output short-circuit current	IOS	—	50	mA
Power dissipation	PD	Ta = 25°C	1.0	W
Storage temperature	TSTG	—	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
I/O power supply	VDD1	VSS1 = VSS2 = 0 V	3.0 to 3.6	V
Core power supply	VDD2	VSS1 = VSS2 = 0 V	2.35 to 2.65	V
PLL power supply	VDDP	VSSP = 0 V	2.35 to 2.65	V
Operating temperature	TOP	—	0 to 70	°C

Note: Turn on the power in the order of VDD1, VDD2, and then VDDP. To shut down the power, use the reverse order.

PIN CAPACITANCE

(VDD1= 3.3V±0.3V, VDD2=VDDP= 2.5V±0.15V, VSS= 0V, f = 1 MHz, Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance	C_i	-	7	pF
Input/Output Capacitance	C_{io1}	-	7	pF
Output Capacitance	C_o	-	7	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics

(VDD1 = 3.3 V ±0.3 V, VDD2 = VDDP = 2.0 V ±0.15 V, VSS = 0 V, Ta = 0 to 70°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
"H" level input voltage		VIH1	—	2.0	-	VDD1+0.3	V
"L" level input voltage		VIL1	—	VSS-0.3	-	0.8	V
"H" level output voltage	For SDRAM	VOH1	IOH = 8mA	0.8 VDD1	—	—	V
"L" level output voltage		VOL1	IOL = 8mA	—	—	0.2 VDD1	V
"H" level output voltage	Others	VOH2	IOH = 4mA	0.8 VDD1	—	—	V
"L" level output voltage		VOL2	IOL = 4mA	—	—	0.2 VDD1	V
Input leakage current		ILI	—	−10	—	+10	μA
Output leakage current		ILO	—	−10	—	+10	μA
"H" level output current (Pull-down)		IIH	VI=VDD1	20	-	200	μA
"L" level output current (Pull-Up)		IIL	VI=0V	-200	-	-20	μA
Power supply current (internal core)*1	Dynamic	IDD1	fope = 54MHz Outputs open	—	—	200	mA
	When in the nondisplay state	IDD2		—	—	10	mA
	Standby	IDDS	VI=0V	—	—	5	mA

*1 Power supply current mentioned here does not include the supply current for the I/O buffer.

AC Characteristics

(VDD1 = 3.3 V ±0.3 V, VDD2 = VDDP = 2.0 V ±0.15 V, VSS = 0 V, Ta = 0 to 70°C)

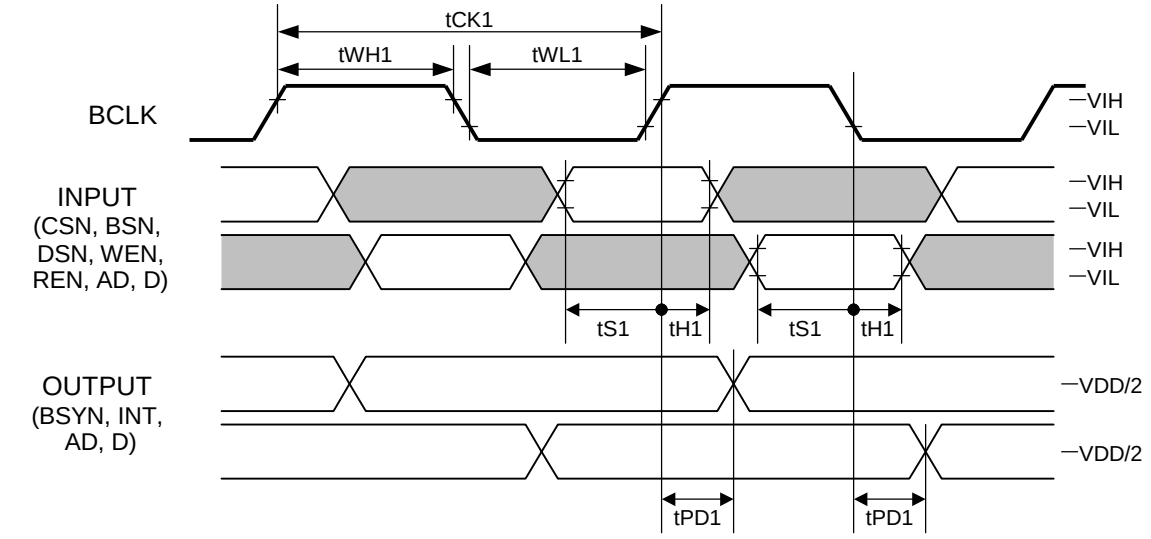
Parameter		Symbol	Condition	Min.	Max.	Unit
Operating frequency (internal clock)		fope	—	—	56.0	MHz
BCLK clock period		tCK1	—	30	—	ns
BCLK "H" level pulse width		tWH1	—	12	—	ns
BCLK "L" level pulse width		tWL1	—	12	—	ns
Input setup time (→BCLK)		tS1	—	5	—	ns
Input hold time (→BCLK)		tH1	—	5	—	ns
Output delay time (BCLK→)*1		tPD1	CL = 15pF	5	15	ns
REFCLK clock period		tCK2	—	36	—	ns
REFCLK "H" level pulse width		tWH2	—	14	—	ns
REFCLK "L" level pulse width		tWL2	—	14	—	ns
Output hold time (CP→)	CP period = tCK2	tHCP	CL = 15pF tCK2 = tCK2(max)	0	10	ns

*1 Values for the output signal timing characteristics have been measured at the VDD1/VDD2 points.

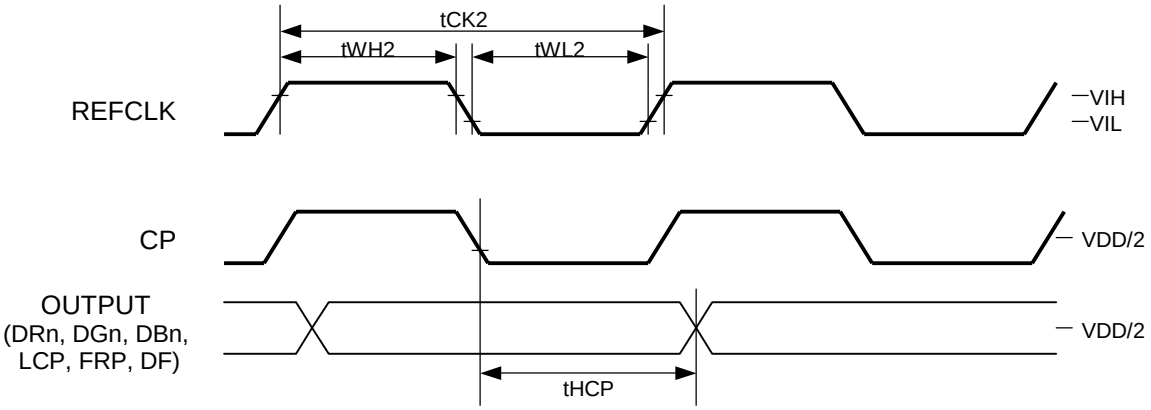
*2 Activate the clock signal to be input to the REFCLK pin by the time the specified voltage is reached after power is turned on.

TIMING DIAGRAMS

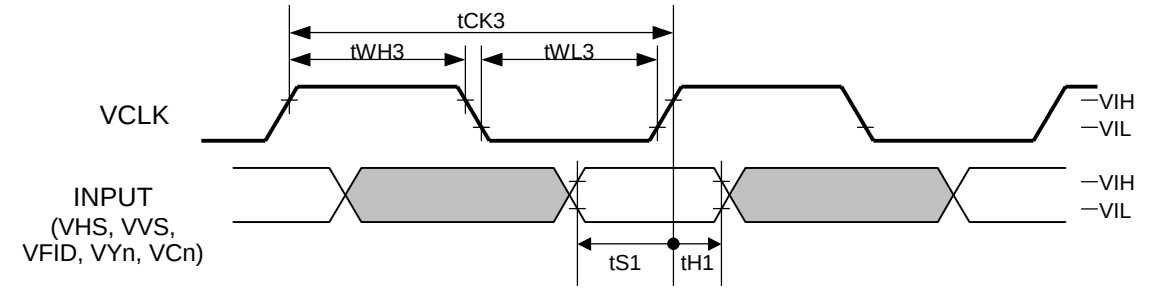
(1) AC Characteristics



(a) Host Interface



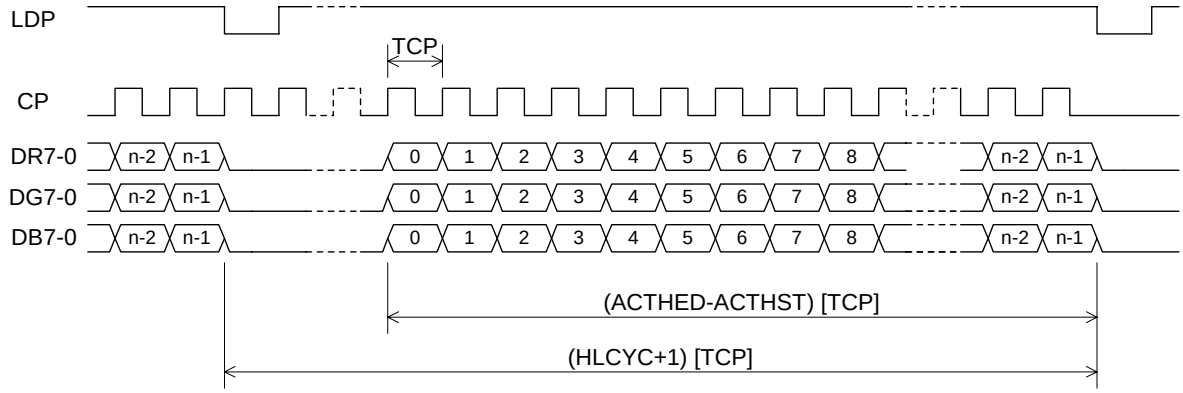
(b) LCD Interface



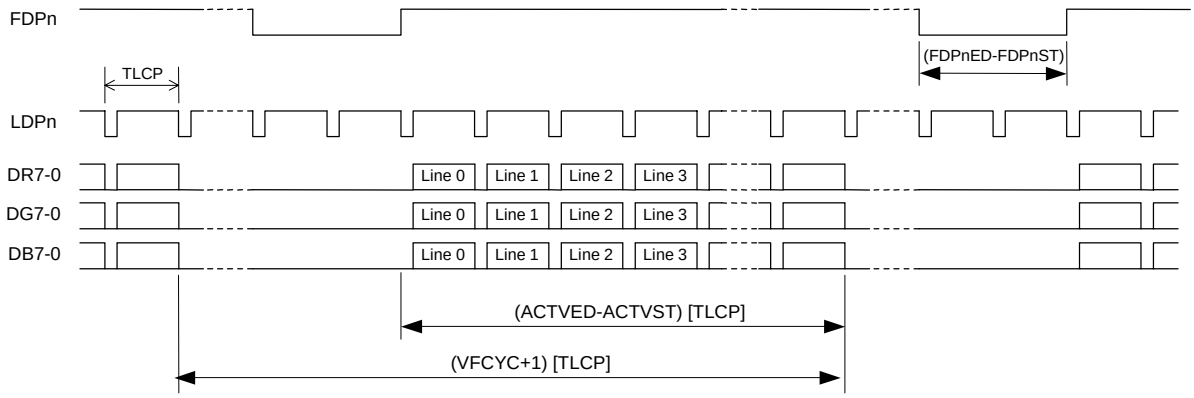
(c) Video Interface

Fig. A-1 AC Characteristics

(2) Color TFT, horizontal timing



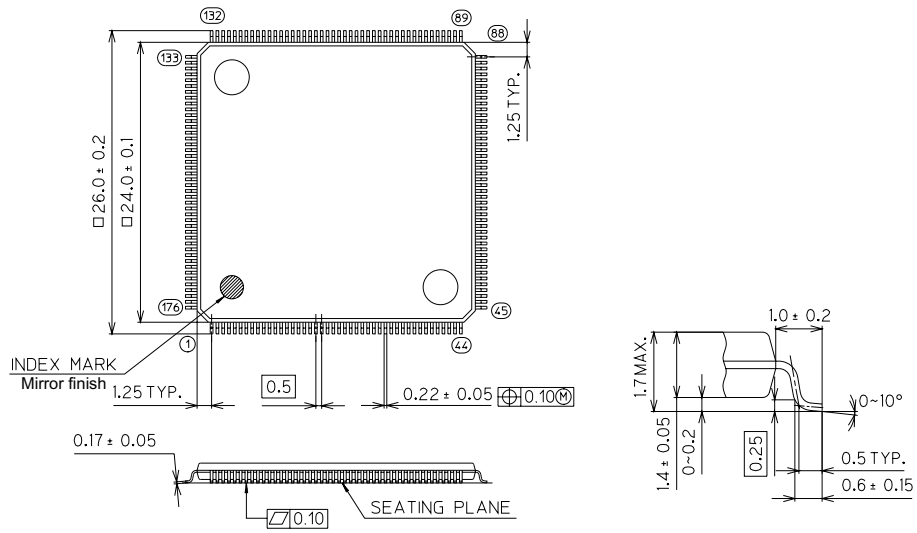
(3) Color TFT, vertical timing



PACKAGE DIMENSIONS

(Unit: mm)

LQFP176-P-2424-0.50-BK



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Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.87 TYP.
Rev. No./Last Revised	3/Nov. 28, 1996

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL87V3116-01	Jan. 30, 2004	–	–	Preliminary edition 1
PEDL87V3116-02	Sep. 21, 2004	–	–	

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