S1C33L27

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CMOS 32-bit Application Specific Controller

- 32-bit RISC CPU-Core (EPSON S1C33PE core) Max.60MHz
- Built-in 54KB RAM (with cache, VRAM)
- Built-in PLL (Multiplication rate: ×1 to ×16)
- Built-in Calculation Module (CALC)
  (Multiply and accumulation (MAC)、Matrix computation、Affine transformation、Butterfly computation and more)
- Built-in LCD Controller with 32KB IVRAM
  Supports STN LCD panels with 4/8-bit data lines or TFT LCD panels with up to 24-bit data lines.
  Supports various panel resolutions, such as 640 × 480 pixels (VGA) and 320 × 240 pixels (QVGA) (can be configured according to the panel used).
  Supports up to 16M-color (for color TFT), 4K-color (for color STN), and 16-level gray scale (for monochrome STN) display modes.
  Two-image overlay display via the Picture-in-Picture Plus function
- interface to communicate with a built-in RAM type LCD driver
- Eight channels of table DMA
- Two channels of 16-bit Audio PWM Timer
- Three channels of multi-serial interface that can be used as a UART, SPI, or I2C module
- One channel of UART (Conforms to IrDA 1.0.)
- General-purpose I2S audio bus interface with one input and one output channels
  Resolution: 16 bits and 24 bits (PCM data output format)
- Built-in Infrared Remote Controller function
- MMC/SD/SDHC card interface
- Support an EDC (Error Detection Code) and an ECC (Error Correction Code) functions
- 8ch.(max) ADC for Analog Input
- Support USB interface with FIFO
- Isolated power supply
- Boot function(NOR/NAND/SPI/RS232C/HIF)

■ DESCRIPTIONS

The S1C33L27 is a 32-bit application specific RISC controller. It is suitable for applications that require an abundance of input/output ports and serial interfaces, USB, ADC, and a display panel, such as electronic dictionaries and control panels on OA/FA equipment.
The S1C33L27 incorporates an LCD controller and VRAM supporting QVGA display in single-chip. Adding an external SDRAM expands this capability into more higher resolution and displayable colors (e.g., VGA display, 16M-color display). It provides an interface to communicate with a built-in RAM type LCD driver.

■ FEATURES

CPU
- EPSON original C33 PE 32-bit RISC CPU-Core
- Maximum operating frequency: 60 MHz
- Internal two-stage pipeline
- Instruction set: 128 instructions (16-bit fixed length)

Internal Memories
- A0RAM (general-purpose RAM)
  - 20K bytes (including 1K-byte instruction cache and 1K-byte data cache)
  - Usable as a general-purpose RAM when not used as cache RAM
- IVRAM (internal VRAM)
  - 32K bytes
  - Configurable as a general-purpose RAM in Area 0 or a RAM for the calculation module
- DSTRAM (DMA descriptor table RAM)
  - 2K bytes
  - Configurable as a RAM for the calculation module
- BBRAM (battery backup RAM)
  - 16 bytes
  - The RAM contents can be maintained while the system power is off using the separated power supply for RTC.

Input clock

- High-speed clock (OSC3)
  - Maximum input clock frequency: 48 MHz
  - Generated by the oscillator circuit (using an external crystal or ceramic resonator) or an external clock is input.
- Low-speed clock (OSC1)
  - 32.768 kHz (typ.) clock for RTC and low-power operations
  - Generated by the oscillator circuit (using an external crystal resonator) or an external clock is input.

Cache Controller (CCU)
- 1K-byte instruction cache and 1K-byte data cache that adopts a four-way associative method
- LRU replacement algorithm
- Automatic lock function during debug mode and the interrupt process of specified priority
- Write through function with a 1-word write buffer

DMA Controller (DMAC)
- Eight channels of table DMA
- Supports table reloading and low-priority channel pausing functions.
- 24 hardware trigger sources and 8 software trigger sources

SRAM Controller (SRAMC)
- Allows connection of SRAM, ROM, and Flash memories.
- 26-bit address bus and 8/16-bit selectable data bus
- Up to six chip enable signals are available to connect external devices.
- Up to 64M-byte (A[25:0]) address space can be accessible with each chip enable signal.
- Programmable bus access wait cycle (0 to 15 cycles)
- Little endian access
- Memory mapped I/O
- Supports both A0 and BS (Bus Strobe) type devices.
- Supports external wait request via the #WAIT pin.

SDRAM Controller (SDRAMC)
- Supports SDRAM interface.
- Supports only SDRAM devices with 8/16-bit data bus.
  - Minimum configuration: 16M bits (2MB), 16-bit SDRAM × 1
  - Maximum configuration: 512M bits (64MB), 16-bit SDRAM × 1
- CAS latency: one, two, or three programmable
- Supports two-burst read and single write operations.
- Equipped with a four-stage × 16-bit DQB (Data Queue Buffer).
- Supports up to four SDRAM banks and bank active mode.
- Built-in 12-bit auto-refresh counter
- Intelligent self-refresh function for low power operation
- Arbitrates external bus accesses by AHB-1 (CPU, DMAC, HIF) and AHB-2 (LCDC).

Host Processor Interface (HIF)
- 8- or 16-bit asynchronous parallel interface to control the S1C33L27 by an external host processor
- Provides semaphore registers.

Clock Management Unit/Oscillators/PLL (CMU)
- Selects the system clock source (OSC3, PLL, or OSC1).
- Turns the OSC3 and OSC1 oscillator circuits on and off.
- Controls frequency multiplication rate of the PLL (×1 to ×16).
- Controls clocks according to the standby mode (SLEEP and HALT).
- Controls the external clock.
- Controls clock supply to the core and peripheral modules.
- OSC3 oscillator circuit
  - Crystal oscillation: 5 MHz min. to 48 MHz max.
  - Ceramic oscillation: 5 MHz min. to 48 MHz max.
  - External clock input: 2 MHz min. to 48 MHz max.

* A 48 MHz clock source with 0.25% of accuracy should be connected for using the USB function.

* Before using a ceramic resonator, please be sure to contact Murata Manufacturing Co., Ltd. for further information on conditions of use for ceramic resonators.

- PLL
  - PLL input frequency: 5 MHz min. to 48 MHz max. (OSC3 ×1, ×1/2, ×1/3, ... ×1/9, ×1/10)
  - PLL output frequency: 20 MHz min. to 60 MHz max.
  - Multiplication rate: ×1, ×2, ×3, ... ×15, ×16
- OSC1 oscillator circuit
  - Crystal oscillation: 32.768 kHz typ.
  - External clock input: 32.768 kHz typ.

Interrupt Controller (ITC)
- Five non-maskable interrupts
- 34 maskable interrupts (including four software exceptions)

16-bit Audio PWM Timer (T16P)
- Two channels of 16-bit timer/counter with PWM output function
- Three bit division modes are provided. (10 bits + 6 bits, 9 bits + 7 bits, 8 bits + 8 bits)
- Can support 8, 16, 22.05, 32, 44.1, and 48 kHz sampling rates.

- PWM function that can handle 8-bit and 16-bit PCM data with 8 k to 48 kbps sampling rates
- Provides fine mode to improve the precision of the pulse width.
- Supports a digital volume control function.
- Can generate two types of compare-match interrupts.
- Supports DMA transfer.

Fine Mode 8-bit Timers (T8F)

- Six channels of 8-bit timer with fine mode (presettable down counter)
- Clocks generated with the counter underflow can be output to internal devices (USI, USIL, ADC, and UART).
- Each timer can generate underflow interrupts.

16-bit PWM Timer (T16A6)

- Four channels of 16-bit timer with a counter capture/comparison functions
- Each channel has built-in two comparison/capture data buffers.
- Can generate compare/capture interrupts.
- The counter clock can be selected from the system clock, OSC3 clock, and OSC1 clock.
- Supports DMA transfer.

Watchdog Timer (WDT)

- 30-bit watchdog timer to generate an NMI or a reset
- Programmable watchdog timer overflow period (NMI or reset interrupt period)
- The watchdog timer overflow signal can be output outside the IC.

Real Time Clock (RTC)

- Contains time counters (seconds, minutes, and hours) and calendar counters (days, days of the week, months, and year).
- 24-hour or 12-hour mode can be selected.
- Operates with an independent power supply (RTCVDD) separated from system power (operable while the system power is off).
- Provides the WAKEUP output pin and #STBY input pin to control standby mode.
- Can generate clock interrupts.

Universal Serial Interface (USI)

- Three channels of multi-serial interface that can be used as a UART, SPI, or I2C module
- Contains 1-byte receive data buffer and 1-byte transmit data buffer.
- UART mode
  - Character length: 7 or 8 bits
  - Parity mode: even, odd, or no parity
  - Stop bit: 1 or 2 bits (start bit: 1 bit fixed)
  - Supports both MSB first and LSB first modes.
  - Parity error, framing error, and overrun error detectable
  - Can generate receive buffer full, transmit buffer empty, and receive error interrupts.
  - Supports DMA transfer.
- SPI mode
  - Supports both master and slave modes.
  - Data length: 8 or 9 bits (master mode), 8 bits fixed (slave mode)
  - Supports both MSB first and LSB first modes.
  - Data transfer timing (clock phase and polarity variations) is selectable from among 4 types.
  - Can generate receive buffer full, transmit buffer empty, and overrun error interrupts.
  - Supports DMA transfer.
- I2C mode
  - Supports both master (single master only) and slave modes.
  - 7-bit addressing mode (10-bit addressing is possible by software control.)
  - Supports clock stretch/wait functions.
  - Can generate start/stop, data transfer, ACK/NAK transfer, and overrun error interrupts.

Universal Serial Interface with Built-in RAM LCD interface (USIL)

- Multi-serial interface that can be used as a UART, SPI, I2C, or built-in RAM LCD interface module
- Contains 1-byte receive data buffer and 1-byte transmit data buffer.
- UART mode
  - Same features as USI
- SPI mode
  - Data length: 8 bits fixed
  - Other features are the same as USI.
- I2C mode
  - Same features as USI
- LCD SPI mode
  - Data length is configurable for 8 bits, 16 bits, 18 bits (4 data format) and 24 bits + CMD bit.
  - CMD bit or A0 is selectable.
  - Data transfer timing (clock phase and polarity variations) is selectable from among 4 types.
  - Can generate transmit buffer empty interrupts.
  - Supports DMA transfer.
- LCD parallel interface mode
  - Provides 8-bit data bus, #CS, #RD, #WR and A0 control signals.

- Supports byte read/write access mode only.
- Can generate transmit buffer empty and receive buffer full interrupts.
- Supports DMA transfer for both data transmission and reception.

UART

- One channel of UART is available.
- Conforms to IrDA 1.0.
- Two-byte receive data buffer and one-byte transmit buffer are built in to support full-duplex communication.
- Transfer rate: 150 to 460800 bps, character length: 7 or 8 bits, parity mode: even, odd, or no parity, stop bit: 1 or 2 bits
- Parity error, framing error, and overrun error detectable
- Can generate receive buffer full, transmit buffer empty, and receive error interrupts.

I2S Bus Interface (I2S)

- General-purpose I2S audio bus interface with one input and one output channels
- Contains a 24-byte FIFO (24 bits × 2 channels (L & R) × 4).
- Resolution: 16 bits and 24 bits (PCM data output format)
- Clock polarity and data shift direction (MSB first/LSB first) are software configurable.
- Can generate FIFO empty interrupts for the output channel (half empty, whole empty, or one empty) and FIFO full interrupts for the input channel (whole full or one data).
- Supports DMA transfer.

Card Interface (CARD)

- Generates 8-bit SLC/MLC NAND Flash interface signals.
- Includes a Reed-Solomon codec to support an EDC (Error Detection Code) and an ECC (Error Correction Code) functions.
- A #CE area can be selected to connect a NAND Flash.

MMC/SD/SDHC Card Interface (SD_MMC)

- SD/SDHC card controller compatible with SD Memory Card Physical Layer Specification Version 2.00.
- MMC controller compatible with MultiMediaCard System Specification Version 2.2.
- Variable clock rate up to 30 MHz.
- Supports 4-bit (wide bus) and 1-bit SD bus interface.
- CRC7 and CRC16 generators
- Supports DMA transfer.

Note: Please join the SD Association (SDA) when handling SD and SDHC cards.

Infrared Remote Controller (REMC)

- Outputs a modulated carrier signal and inputs remote control pulses.
- Embedded carrier signal generator and data length counter
- Can generate counter underflow interrupts for data transmission and input rising/falling edge detection interrupts for data reception.

LCD Controller (LCDC)

- Supports STN LCD panels with 4/8-bit data lines or TFT LCD panels with up to 24-bit data lines.
- Supports various panel resolutions, such as 640 × 480 pixels (VGA) and 320 × 240 pixels (QVGA) (can be configured according to the panel used).
- Supports up to 16M-color (for color TFT), 4K-color (for color STN), and 16-level gray scale (for monochrome STN) display modes.
- Typical display configuration when the internal VRAM (20KB) is used
  - 320 × 240 pixels, 2 bpp (4-level gray scale display)
- Display configuration when an external memory is used
  - 320 × 240 pixels, 16 bpp (QVGA 64K-colors display)
  - 400 × 240 pixels, 16 bpp (WQVGA 64K-colors display)
  - 640 × 480 pixels, 16 bpp (VGA 64K-colors display)
- Two-image overlay display via the Picture-in-Picture Plus function
- Virtual display function to handle images with a different resolution from the LCD panel (any area in the virtual screen can be displayed on the LCD.)

A/D Converter (ADC10)

- 10-bit successive approximation type A/D converter
- Up to eight analog input channels (chip and PFBGA12U-180 package)
- Up to four analog input channels (TQFP24/QFP20-144pin and TQFP15-128pin packages)
- Conversion time: 10 µs min. (when 2 MHz input clock is selected) 1,250 µs max. (when 16 kHz input clock is selected)
- Can generate conversion completion and data overwrite error interrupts.

USB Function Controller (USB)

- Supports USB2.0 full speed (12M bps) mode.
- Provides auto negotiation function.
- Supports control, bulk, isochronous and interrupt transfers.
- Supports four general-purpose endpoints and endpoint 0 (control).
- Embedded 1K-byte programmable FIFO
- Can generate USB interrupts.
- Supports DMA transfer.

General-purpose I/O Ports (GPIO)

- Maximum 91 I/O ports and eight input ports are available (chip and PFBGA12U-180 package).

- Maximum 72 I/O ports and four input ports are available (TQFP24/QFP20-144pin package).
- Maximum 56 I/O ports and four input ports are available (TQFP15-128pin package).
- Can generate maximum 8 port input interrupts from the 64 I/O ports selected and key input interrupts from the predefined 32 ports.

* The GPIO ports are shared with other peripheral function pins (USI, PWM etc.). Therefore, the number of GPIO ports depends on the peripheral functions used.

Calculation Module (CALC)

- Multiply and accumulation (MAC)
- Matrix computation
- Affine transformation
- Butterfly computation
- Supports signed/unsigned 32-bit integer operation mode and signed 16-bit fixed-point values operation mode with saturation processing.

Operating Voltage

- HVDD (I/O power voltage)
  2.7 V to 3.6 V (3.3 V typ.)
  or 3.0 V to 3.6 V (3.3 V typ.) when the USB module is used.
- AVDD (analog power voltage)
  2.7 V to 3.6 V (3.3 V typ.)
- LVDD (internal logic/internal memory power voltage)
  1.65 V to 1.95 V (1.8 V typ.)
  or 1.7 V to 1.9 V (1.8 V typ.) when a ceramic resonator is used.
- PLLVDD (PLL power voltage)
  1.65 V to 1.95 V (1.8 V typ.)
  or 1.7 V to 1.9 V (1.8 V typ.) when a ceramic resonator is used.
- RTCVDD (RTC/BBRAM power voltage)
  1.65 V to 1.95 V (1.8 V typ.)
  or 1.7 V to 1.9 V (1.8 V typ.) when a ceramic resonator is used.

* LVDD = PLLVDD = RTCVDD, HVDD = AVDD
The S1C33L27 does not support 5 V tolerant I/O.

Operating Temperatures

- -40 to 85°C
- 0 to 70°C when the USB module is used or when a ceramic resonator is used.

Power Consumption

(No I/O current is included.)

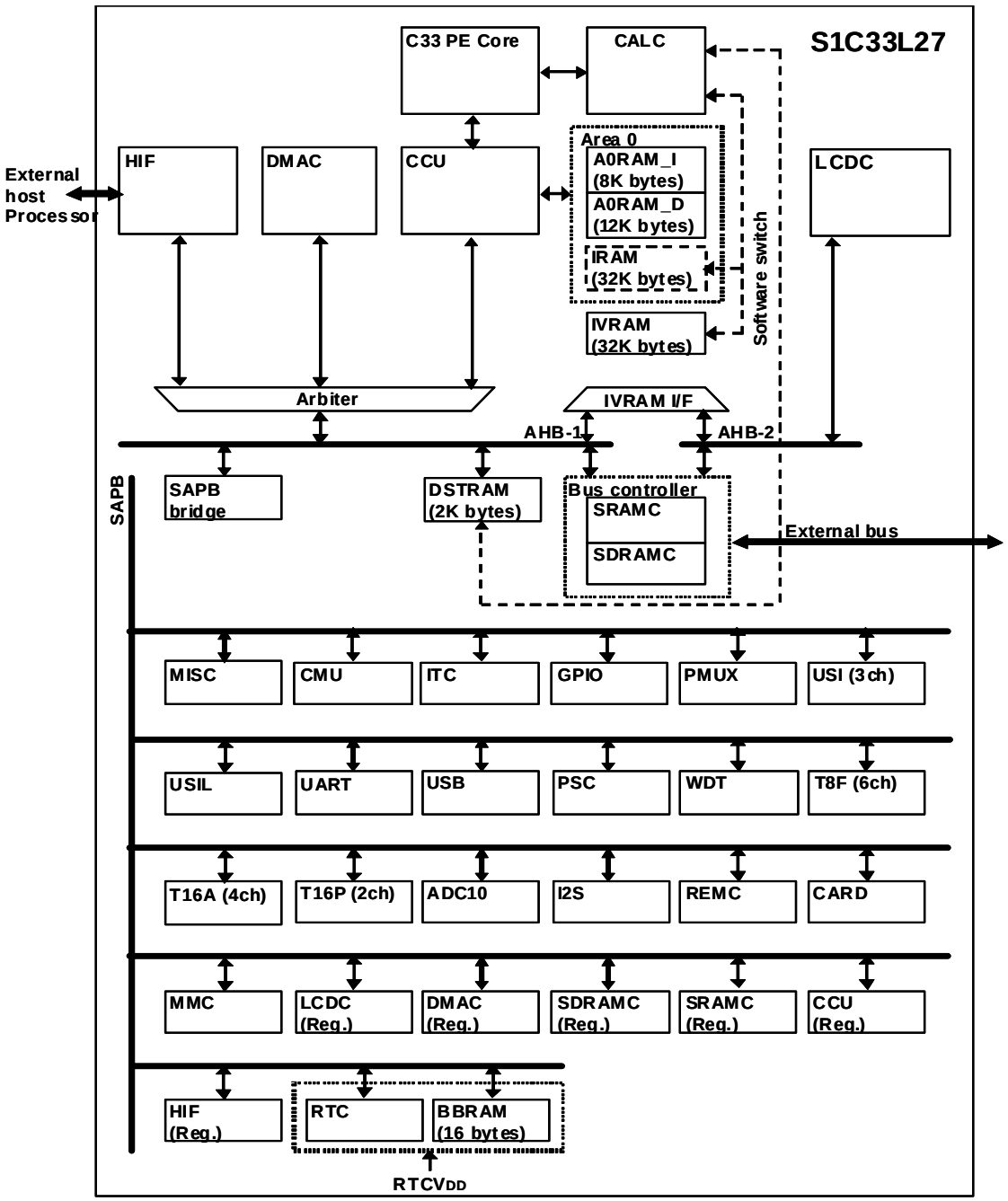
- During SLEEP: 2.3 µA typ. when RTC is running.
  1.0 µA typ. when RTC is not used.
- During HALT: 4.3 mA typ. when 48 MHz OSC3 clock is used as the system clock,
  all peripheral clocks = Off.
- During execution: 18 mA typ. when 48 MHz OSC3 clock is used as the system clock,
  CPU is running, all peripheral clocks = Off.

* Power consumption can be reduced by controlling the clocks through the clock management unit (CMU).

Shipping Form

• Die form:	200 pads	(5.213 mm × 5.213 mm, pad pitch: 90 µm)
• Plastic package:	TQFP15-128pin	(14 mm × 14 mm × 1.0 mm, lead pitch: 0.4 mm)
	TQFP24-144pin	(16 mm × 16 mm × 1.0 mm, lead pitch: 0.4 mm)
	QFP20-144pin	(20 mm × 20 mm × 1.4 mm, lead pitch: 0.5 mm)
	PFBGA12U-180	(12 mm × 12 mm × 1.2 mm, ball pitch: 0.8 mm)

■ BLOCK DIAGRAM



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