AN6398, AN6398S

VTR SECAM Color Killer Circuits

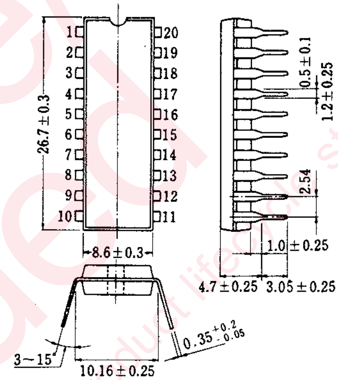
■ Outline

The AN6398 and the AN6398S are integrated circuit designed for VTR SECAM killer and constitute a VTR SECAM-system color signal processing circuit by combining with the AN6397 or the AN5397S.

■ Features

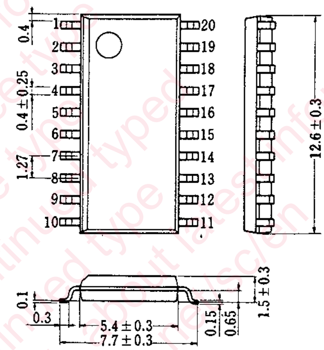
- The functions consist of :
  - Noise-gate circuit
  - SECAM-killer circuit
- Supply voltage : 5V

AN6398 Unit : mm



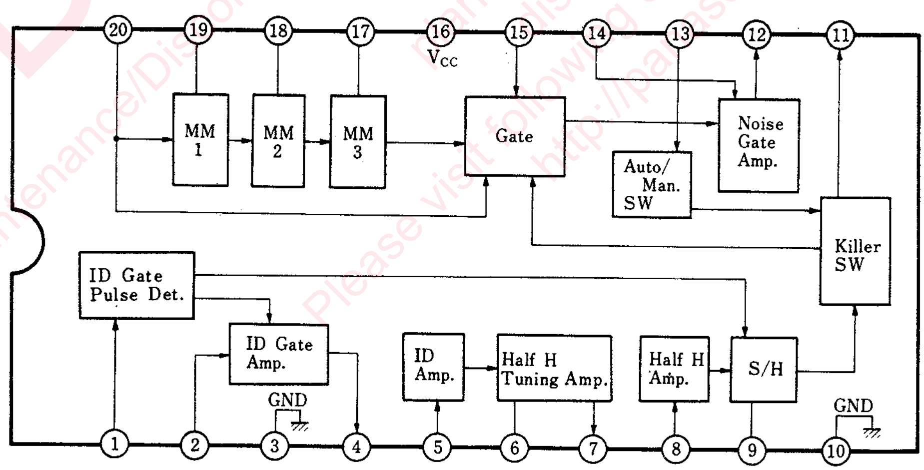
20-Lead DIL Plastic Package

AN6398S Unit : mm



20-Lead PANAFLAT Package (SO-20D)

■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	ID Gate Pulse	11	Killer Output
2	Chroma Input (Ⅱ)	12	Chroma Output
3	GND	13	Auto/Manual SW
4	ID Gate Output	14	Chroma Input (Ⅰ)
5	Trap Filter Output	15	V Blank Pulse Input
6	Filter	16	V_{CC}
7	Half f_H Tuning Amp. Output	17	MM3 Control
8	Half f_H Input	18	MM2 Control
9	S & H	19	MM1 Control
10	GND	20	H Sync. Pulse Input

■ Absolute Maximum Ratings (Ta=25℃)

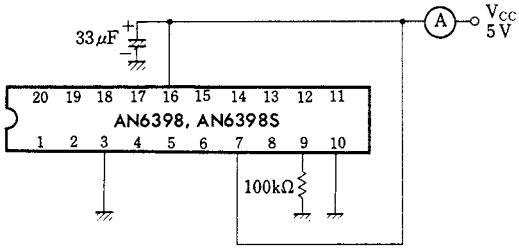
Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	6.0	V
Power dissipation (Ta=70℃)	P_D	250	mW
Operating ambient temperature	T_{opr}	−20～+70	℃
Storage temperature	T_{stg}	−40～+125	℃

■ Electrical Characteristics (V_{CC}=5V, Ta=25℃±2℃)

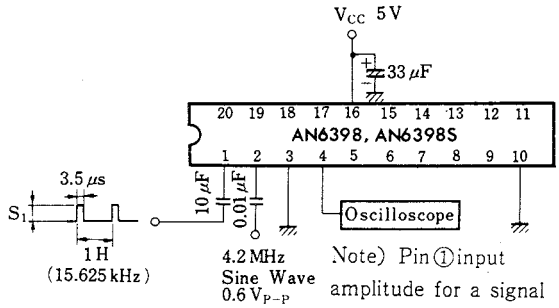
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Total circuit current	I_{tot}	1		22		43	mA
ID gate pulse input sensitivity	S_1	2		2			V_{P-P}
Forced color input voltage	$V_{I(H-13)}$	3		4.5		5	V
Forced monochrome input voltage	$V_{I(L-13)}$	4		0		0.5	V
Lead-in current (Killer mode)	I_{O-11}	4	Pin⑪ 0.3V	0.5		2	mA
Monochrome evaluation level (Killer mode)	$S_{(B/W-9)}$	5				1.3	V
Color evaluation level (Killer mode)	$S_{(Color-9)}$	5		2.2			V
H Sync. pulse input voltage (High)	V_{IH-20}	6		3.5		5	V
H Sync. pulse input voltage (Low)	V_{IL-20}	6		0		0.5	V
V blank pulse input voltage (High)	V_{IH-15}	7		3		5	V
V blank pulse input voltage (Low)	V_{IL-15}	7		0		0.3	V
Gate amp. gain	G_{V-12}	8	Pin⑭ input 400 mV_{P-P}	1		6	dB
Gate amp. cross talk	CT_{12}	8				−30	dB
Gate amp. offset voltage	V_{offset}	9		−50		+50	mV

Note) Operating supply voltage range $V_{CC(opr)}$=4.5～5.5V

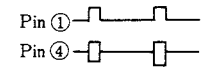
Test Circuit 1 (I_{tot})



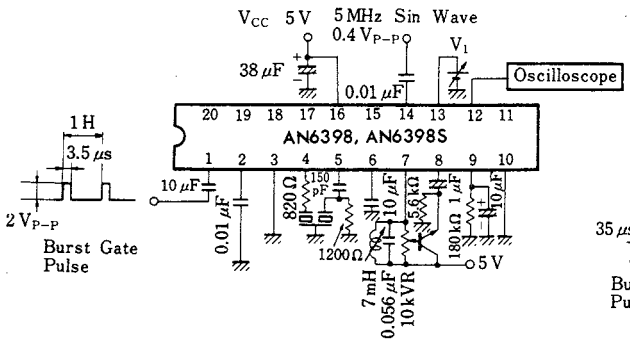
Test Circuit 2 (S_1)



Note) Pin①input amplitude for a signal to be output to the Pin④ as shown below



Test Circuit 3 ($V_{I(H-13)}$)

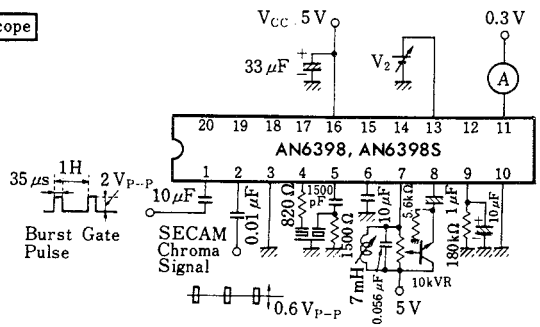


V 14−13 is a Pin ⑬ DC voltage when a sine wave of about $0.4V_{P-P}$ is output to the Pin⑫.

Note) Adjust Pin⑦ external L properly so that the following relations with Pin⑦ external C will be met : (about 7.1mH)

$$\frac{f_H}{2} = \frac{1}{2 \times \sqrt{LC}}$$

Test Circuit 4 ($V_{I(L-13)}$, I_{0-11})



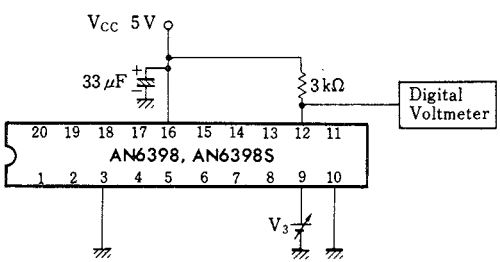
$V_{I(L-13)}$: Pin⑬ voltage when the Pin⑪ leads in a current of about 1mA.

I_{0-11} : Pin⑪ lead-in current when a Pin⑬ voltage is 0V

Note 1) Pin⑦ external L-C relations should be $\frac{f_H}{2} = \frac{1}{2\pi\sqrt{LC}}$

Note 2) Adjust the Pin⑦ external variable resistor so that a Pin⑧ amplitude will be $0.9V_{P-P}$.

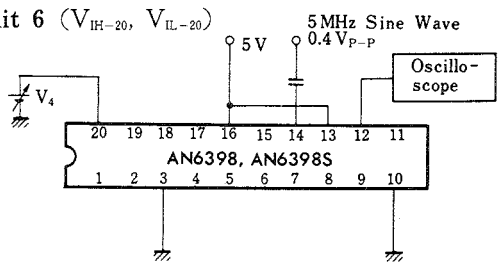
Test Circuit 5 ($S_{(B/W-9)}$, $S_{(Color-9)}$)



$S_{(B/W-9)}$: Pin⑨ voltage when a Pin⑫ voltage comes Low (about 0.4V)

$S_{(Color-9)}$: Pin⑨ voltage when the Pin⑫ voltage comes High (about 5V)

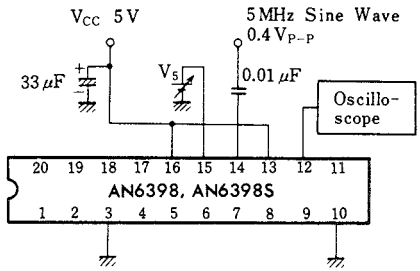
Test Circuit 6 (V_{IH-20}, V_{IL-20})



V_{IL-20} : Pin⑳ voltage to output a sine wave of about $0.6V_{P-P}$ to the Pin⑫

V_{IH-20} : Pin⑳ voltage not to output the level signal above to the Pin⑫

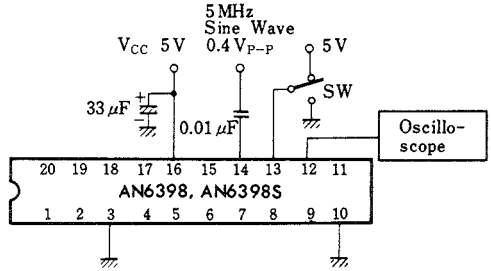
Test Circuit 7 (V_{IH-15}, V_{IL-15})



V_{IL-15} : Pin⑮ voltage to output a sine wave of about 0.6V_{P-P} to the Pin⑫

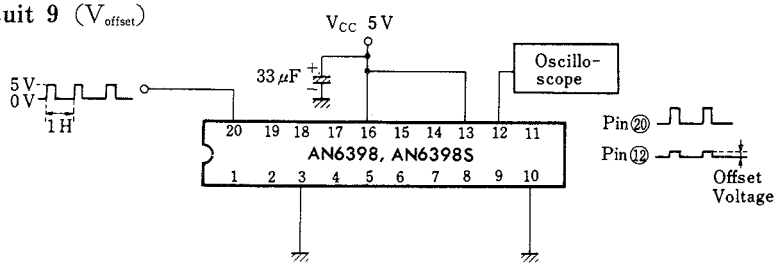
V_{IH-15} : Pin⑮ voltage not to output the signal of the level above to the Pin⑫

Test Circuit 8 (G_{V-12}, CT_{12})

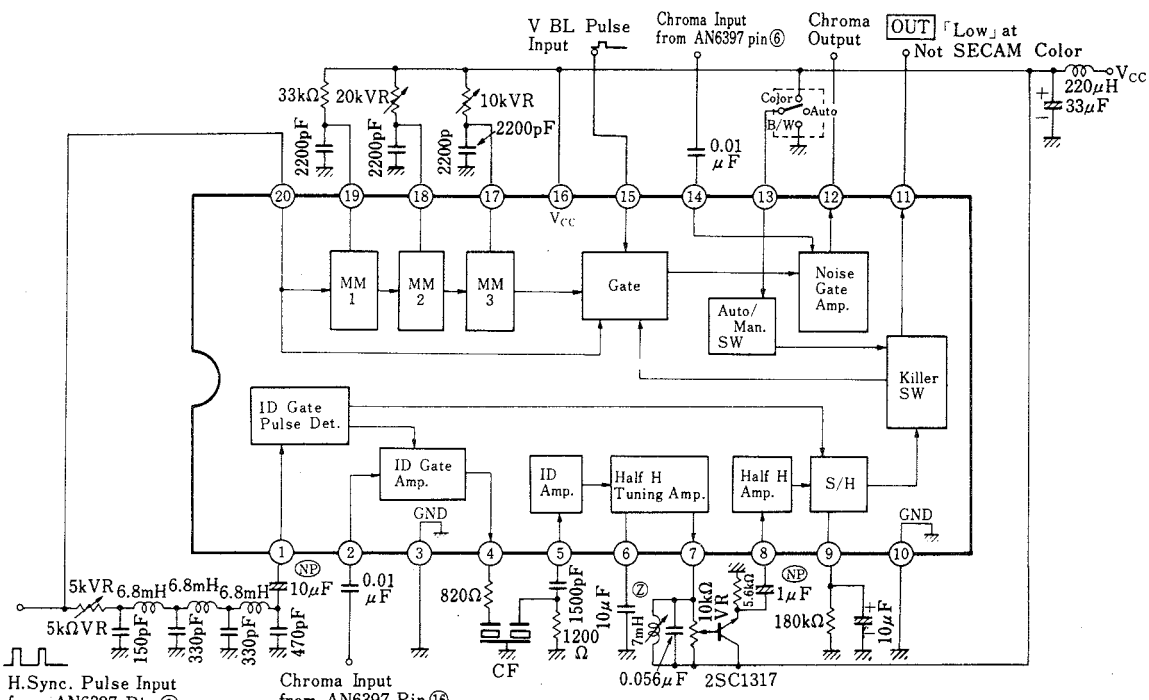


G_{V-12} : Ratio of Pin⑫ output amplitude and Pin⑭ input amplitude when the Pin⑬ is set to 5V

Test Circuit 9 (V_{offset})



■ Application Circuit



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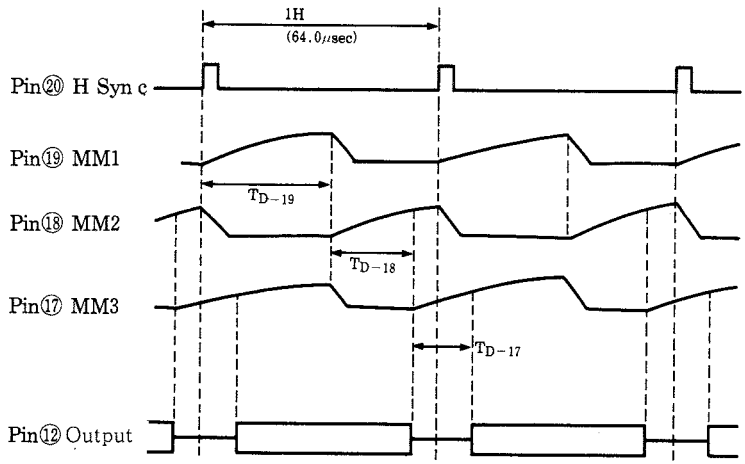
Precautions for Use

1) MM1, MM2 and MM3 delay times

$T_D = C_X \cdot R_X \cdot \ln 2$ C_X ▲ (C_X and R_X are external constant ▼ values for each MM)

2) MM1 through MM3 standard setting



*1H− ($T_{D-19}+T_{D18}$) 1.5μ s

* ($T_{D-18}+T_{D-18}+T_{D-17}$) −H 5.3μ s

*A lead-in current for each MM is 0.3 to 4.0mA.

3) Half H frequency adjustment

Use LC so that a value of Pin⑦ external LC will be $\frac{f_H}{2}=\frac{1}{2\pi\sqrt{LC}}$

4) Half H level adjustment

For a value the Pin⑦external variable reststor, make adjustment so that Pin⑧input signal level will be $0.90V_{P-P}$ when inputting a standard-standard-level signal to combined AN6397 and inputting the standard-level signal to the Pins①and②of AN6398.

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