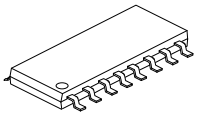
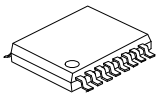
U74HC4094

CMOS IC

8-STAGE SHIFT & STORE BUS REGISTER



SOP-16



TSSOP-16

■ DESCRIPTION

The **U74HC4094** consists of an 8-stage shift register and an 8-stage D-type latch with 3-stage parallel outputs. Data is shifted serially through the shift register on the positive-going clock transition of the input singal. The output of the last stage QS1 can be used to cascade several devices.

The output of QS1 is transferred to a second output(QS2) on the following negative-going clock transition of the input singal. The data of each stage of the shift register is provided with a latch whose data on the negative going transition of the Strobe input signal. When the strobe input is held high, data propagates through the latch to a 3-state output buffer.

The buffer is enabled when Output Enable input is taken high.

■ FEATURES

* Operate from 2.0V to 6.0V
* Low Power Dissipation I_{CC}=4μA(Max)
* High Noise Immunity Characteristic of CMOS Devices

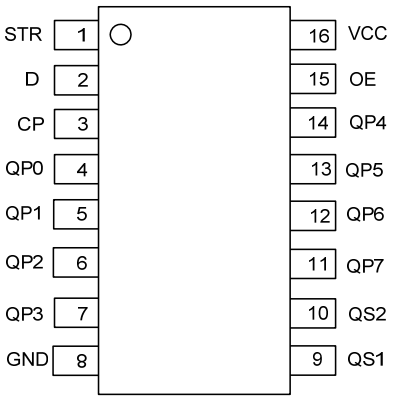
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC4094L-S16-R	U74HC4094G-S16-R	SOP-16	Tape Reel
U74HC4094L-P16-R	U74HC4094G-P16-R	TSSOP-16	Tape Reel
U74HC4094L-P16-T	U74HC4094G-P16-T	TSSOP-16	Tube

U74HC4094L-P16-R
(1)Packing Type
(2)Package Type
(3)Lead Free

(1) R: Tape Reel, T: Tube
(2) P16: TSSOP-16, S16: SOP-16
(3) G: Halogen Free, L: Lead Free

■ PIN CONFIGURATION

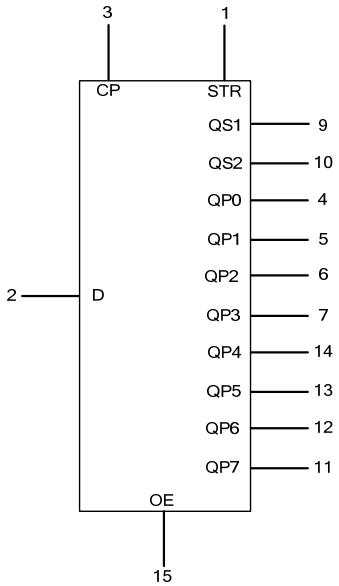


■ FUNCTION TABLE

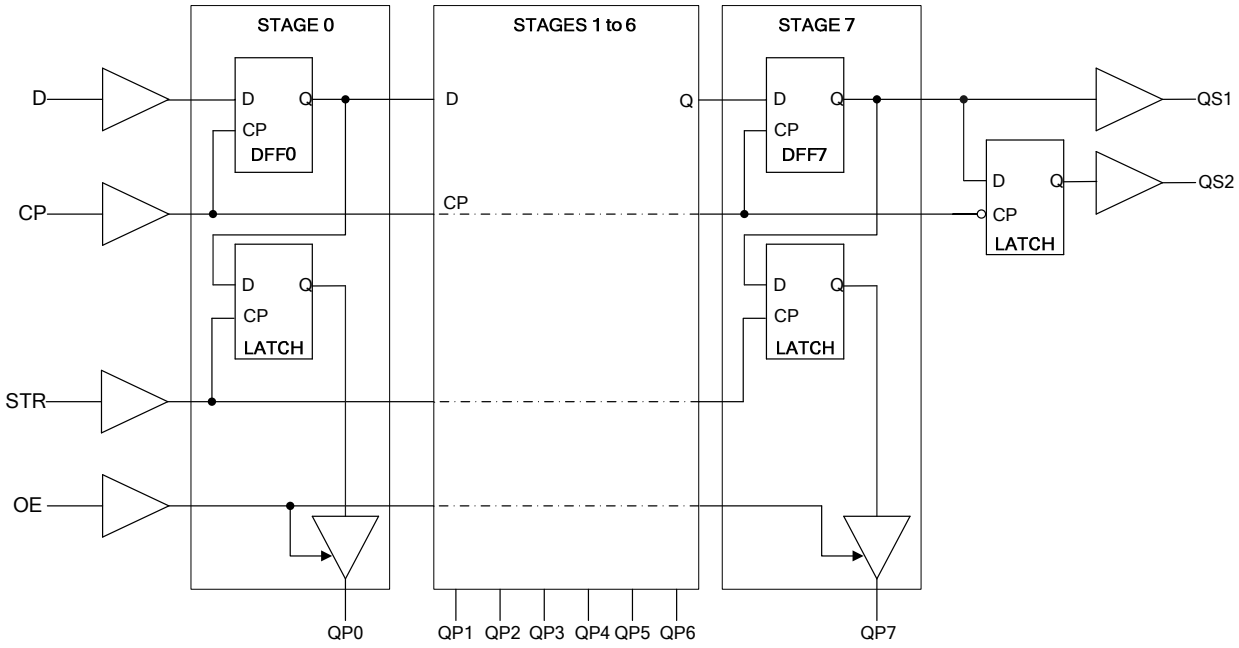
INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q'6	NC
↓	L	X	X	Z	Z	NC	QP7
↑	H	L	X	NC	NC	Q'6	NC
↑	H	H	L	L	QPn-1	Q'6	NC
↑	H	H	H	H	QPn-1	Q'6	NC
↓	H	H	H	NC	NC	NC	QP7

Note:H : HIGH voltage level;
L : LOW voltage level.
X : Don't care.High impedance OFF-state.
NC: No change.
Z : High impedance OFF-state.
↑ : Low-to-High CP transition.
↓ : High-to-Low CP transition.
Q'6: the information in the seventh register stage is transferred to the 8th register stage and QSn output at the positive clock edge

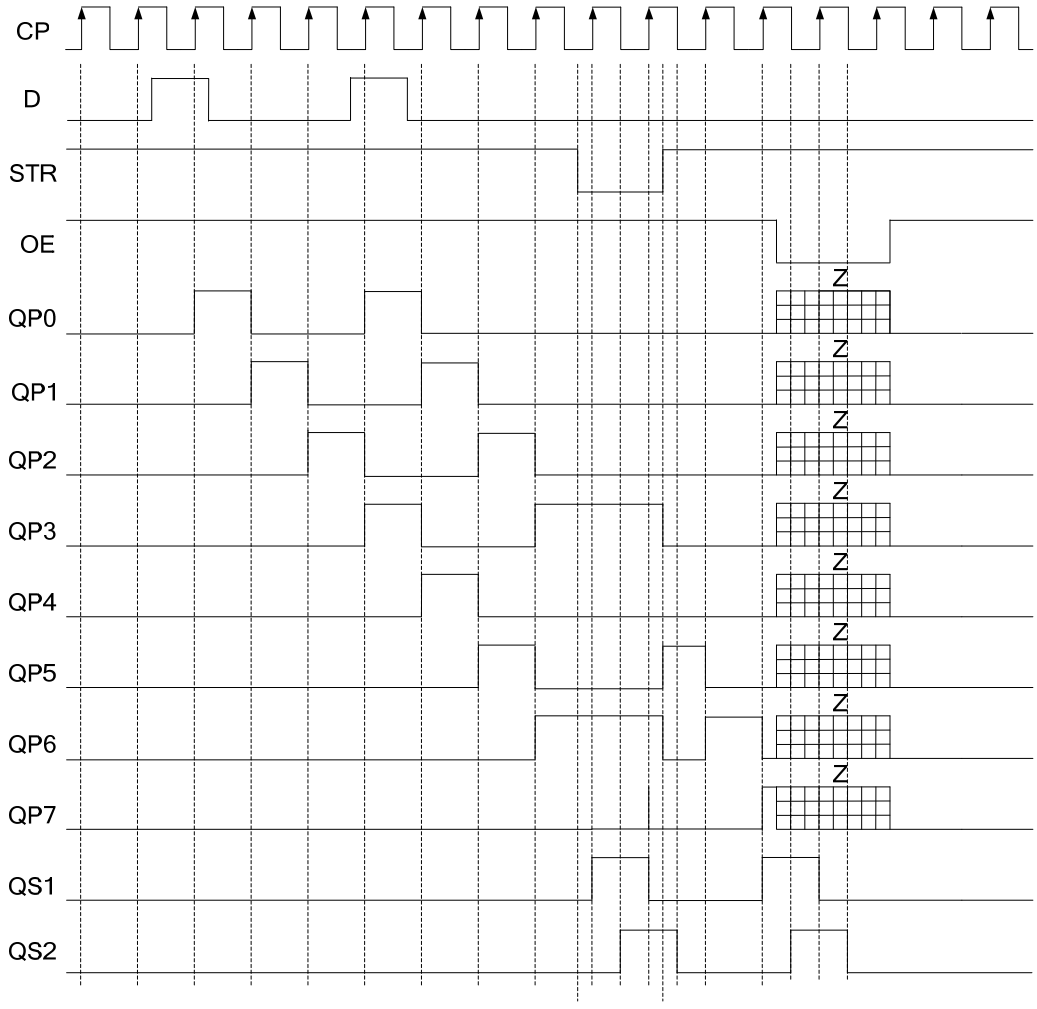
■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ V_{CC} +0.5	V
Output Voltage	V_{OUT}	-0.5 ~ V_{CC} +0.5	V
V_{CC} or GND Current	I_{CC}	±50	mA
Input Current	I_{IN}	±20	mA
Output Current	I_{OUT}	±25	mA
Storage Temperature	T_{STG}	-65 ~ + 150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	2.0		6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		+125	℃
Input Rise or Fall Times	t_R, t_F	V_{CC}=2.0V			1000	ns
		V_{CC}=4.5V			500	
		V_{CC}=6.0V			400	

■ ELECTRICAL CHARACTERISTICS(T_A=25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=4.5V	3.15			V
		V_{CC}=6V	4.2			V
Lowever output voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=4.5V			1.35	V
		V_{CC}=6V			1.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9			V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4			V
		V_{CC}=6V, I_{OH}=-20μA	5.9			V
		V_{CC}=4.5V, I_{OH}=-4.0mA	3.98			V
		V_{CC}=6V, I_{OH}=-5.2mA	5.48			V
Low-Level Output Voltage	V_{OL}	V_{CC}=2V, I_{OL}=20μA			0.1	V
		V_{CC}=4.5V, I_{OL}=20μA			0.1	V
		V_{CC}=6V, I_{OL}=20μA			0.1	V
		V_{CC}=4.5V, I_{OH}=4mA			0.26	V
		V_{CC}=6V, I_{OL}=5.2mA			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}= V_{CC} or GND			±0.1	μA
Output OFF -state current	I_{OZ}	V_{CC}=6V, V_{OUT}=V_{CC} or GND			±0.5	μA
Quiescent Supply Current	I_Q	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			4	μA

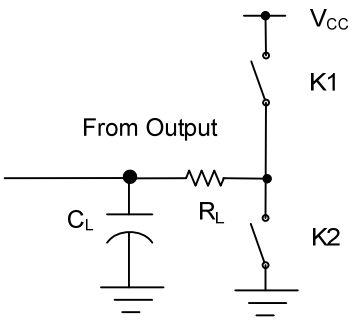
■ SWITCHING CHARACTERISTICS(T_A=25℃,see TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (CP) to output(QS1)	t_{PHL}/t_{PLH}	V_{CC}=2V		50	150	ns
		V_{CC}=4.5V		18	30	ns
		V_{CC}=6V		14	26	ns
Propagation delay from input (CP) to output(QS2)	t_{PHL}/t_{PLH}	V_{CC}=2V		44	135	ns
		V_{CC}=4.5V		16	27	ns
		V_{CC}=6V		13	23	ns
Propagation delay from input (CP) to output(QPn)	t_{PHL}/t_{PLH}	V_{CC}=2V		63	195	ns
		V_{CC}=4.5V		23	39	ns
		V_{CC}=6V		18	33	ns
Propagation delay from input (STR) to output(QPn)	t_{PHL}/t_{PLH}	V_{CC}=2V		58	180	ns
		V_{CC}=4.5V		21	36	ns
		V_{CC}=6V		17	31	ns
3-state output enable time from input (OE) to output(QPn)	t_{PZH}/t_{PZL}	V_{CC}=2V		55	175	ns
		V_{CC}=4.5V		20	35	ns
		V_{CC}=6V		16	30	ns
3-state output disable time from input (OE) to output(QPn)	t_{PHZ}/t_{PLZ}	V_{CC}=2V		41	125	ns
		V_{CC}=4.5V		15	25	ns
		V_{CC}=6V		12	21	ns
Output transition time(QSn、QPn)	t_{TLH}/t_{THL}	V_{CC}=2V		19	75	ns
		V_{CC}=4.5V		7	15	ns
		V_{CC}=6V		6	13	ns
Clock pulse width HIGH or LOW(CP)	t_W	V_{CC}=2V	80	14		ns
		V_{CC}=4.5V	16	5		ns
		V_{CC}=6V	14	4		ns
Strobe pulse width HIGH(STR)	t_W	V_{CC}=2V	80	14		ns
		V_{CC}=4.5V	16	5		ns
		V_{CC}=6V	14	4		ns
Set-up time(D to CP)	t_{SU}	V_{CC}=2V	50	14		ns
		V_{CC}=4.5V	10	5		ns
		V_{CC}=6V	9	4		ns
Set-up time(D to STR)	t_{SU}	V_{CC}=2V	100	28		ns
		V_{CC}=4.5V	20	10		ns
		V_{CC}=6V	17	8		ns
Hold time(D to CP)	t_H	V_{CC}=2V	3	-6		ns
		V_{CC}=4.5V	3	-2		ns
		V_{CC}=6V	3	-2		ns
Hold time(D to STR)	t_H	V_{CC}=2V	0	-14		ns
		V_{CC}=4.5V	0	-5		ns
		V_{CC}=6V	0	-4		ns
Maximum clock pulse frequency	f_{MAX}	V_{CC}=2V	6	28		MHz
		V_{CC}=4.5V	30	87		MHz
		V_{CC}=6V	35	103		MHz

■ OPERATING CHARACTERISTICS

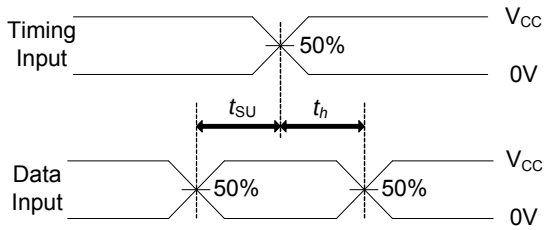
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		300		pF

■ TEST CIRCUIT AND WAVEFORMS

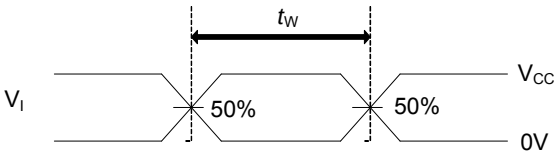


TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

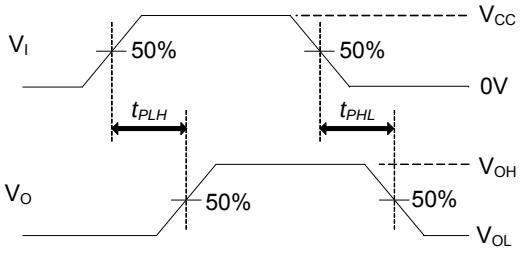
Note: C_L =50pF, R_L =1kΩ



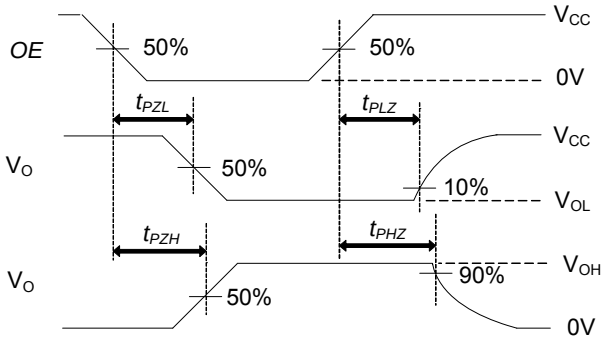
Setup Time and Hold Time



Pulse Width



Propagation Delay Times



Enable and Disable Times

Note: CL includes probe and jig capacitance.
PRR ≤10MHz, Zo = 50Ω, tr ≤6ns, tf ≤6ns.