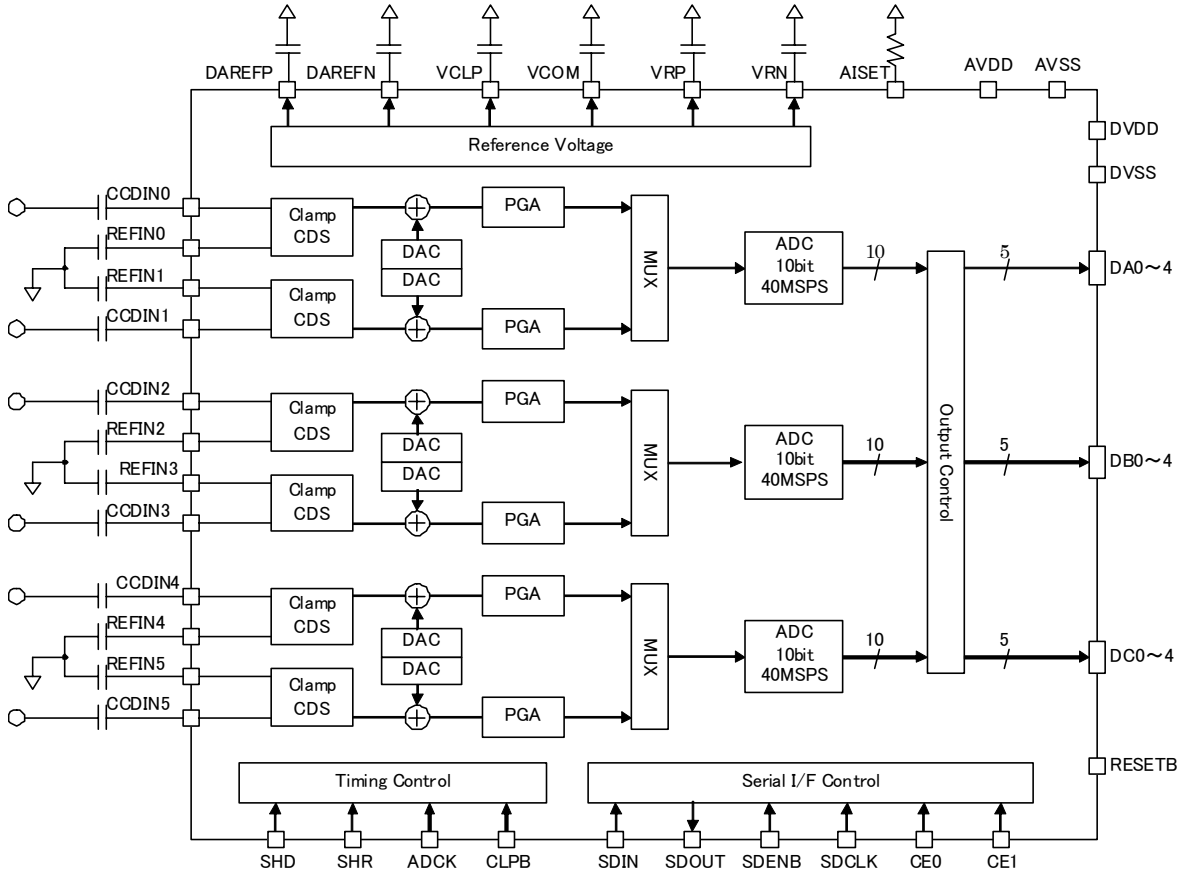
AK8448

6-Channel Linear Sensor compatible

10 Bit 40 MSPS x 3 Analog Pre-Processor

Features

- ☐ Maximum Processing Speed
  - In CDS mode and Clamp mode
    - 1ch, 2ch and 3ch mode: 40M samples/sec per channel
    - 4ch and 6ch mode: 20M sample/sec per channel
  - In DC Direct-coupled mode
    - 1ch, 2ch and 3ch mode: 15M sample/sec per channel
    - 4ch and 6ch mode: 15M sample/sec per channel
- ☐ Maximum Input Level: 1.35Vpp (typ.)@CDS mode and DC connection mode
  1.19Vpp (typ.)@Clamp mode
- ☐ Compatible with both CCD and CIS Signal Polarities
- ☐ Simultaneously Sampling 6-Channel CDS circuits (Correlated Double Sampling)
- ☐ Offset DACs: Adjustable Range : ±298.7 mV (typ.), Independent 6-channel 8 Bit DACs
- ☐ PGA: Adjustable Gain Range : 0 dB ~ 18.75 dB (typ.)
  Independently adjustable 6-channel 8 Bit PGAs.
- ☐ Linearity: DNL = -1LSB (min.), +1LSB (max.) with guaranteed no missing code.
- ☐ 5 bit Output Bus: Enables to output 10 Bit Data in 5 Bit x 2 cycles
- ☐ 4-Wire Serial Interface
- ☐ Supply: 3.3V±0.3V
- ☐ Power Dissipation: T.B.D(typ.)@6ch mode, at 20M samples/sec per channel
- ☐ Package: 64 Pin LQFP, Pin pitch 0.5 mm, Mold size 10 mm x 10 mm



Functional Description of Each Block

☐ Clamp / CDS Sensor Interface Circuit

It samples the Image signal level from the sensor.

The AK8448 has 3 sampling modes – CDS mode, Clamp mode and DC direct-coupled mode.

There are 5 ,number of channel select modes – 1, 2, 3, 4 and 6 channels. Channel(s) to be used is selected by the number of channel mode.

CDS circuits, DACs, PGAs and ADCs of the un-used channels are automatically powered-down.

☐ DAC Offset addition D/A converter

This is a D/A converter to generate an offset voltage which is added to the sampled signal level at the Sensor Interface part. Voltage range of DAC is ±298.7mV (typ.) and its resolution is 8 Bit. An independent offset voltage can be set to each channel by register setting.

☐ PGA (Programmable Gain Amplifier)

This is a programmable Gain amplifier to adjust signal amplitude of each channel. Adjustable range is from 0 dB to 18.75 dB (typ.), and its resolution is 8 Bit.

An independent gain can be set to each channel by register setting.

☐ MUX Channel Multiplexer

This is an Analog Switch to input in the time-division-multiplexed fashion the simultaneously-sampled 2 channel signals to an ADC, in 4 channel mode and 6 channel mode.

In 4 channel mode and 6 channel mode, 10 Bit ADCs process dual channels in time-division-multiplexed method.

☐ ADC A/D Converter

This is a 10 Bit, 40 MSPS A/D converter to convert an Image signal level into digital data after offset adjustment and gain adjustment are made. There are 3 ADCs and 2 channels are connected to each ADC through a channel multiplexer.

☐ Output Control ADC Output Data Control

Digital circuit to control the Output Form of ADC data. ADC data can be output in either 5 Bit-wide or 10 Bit-wide by register setting.

In case of 5 Bit-wide data operation, the upper 5 Bit of the ADC data is output at the rising edge of ACDK clock, and the lower 5 Bit data ,at the falling edge of ADCK.

In case of 10 Bit-wide data operation, ADC data from two different data channels are output at the rising edge and at the falling edge of ADCK respectively.

It is also possible to output ADC data at only the falling edge of ADCK clock by register setting in 10 Bit-wide data operation.

☐ Reference Voltage Reference Voltage Generation Circuit

Circuit to generate internal Clamp level VCLP, Analog Common Level VCOM, ADC Reference Voltages VRP & VRN and DAC Reference Voltages DAREFP & DAREFN.

☐ Timing Control Timing Generating Circuit

Digital circuit to generate internal timing pulses from those input clocks, ADCK, SHR, SHD and CLPB.

ADCK is a clock which is used for ADC operation and for operation of ADC Output Data Control part.

SHR is a timing pulse which is used to sample Reference level of Sensor signal.

SHD is a timing pulse which is used to sample Data level of Sensor signal.

CLPB is a timing pulse to show Clamp period.

☐ Serial I/F Control Serial Register Interface Circuit

A 4-Wire Interface to set values at the Control registers.

Control registers also can be read out.

By assigning specific address to individual devices by chip enable pins CE0 and CE1, up to 4. AK8448 devices can be connected on the same, 4-wires.

Pin Assignment

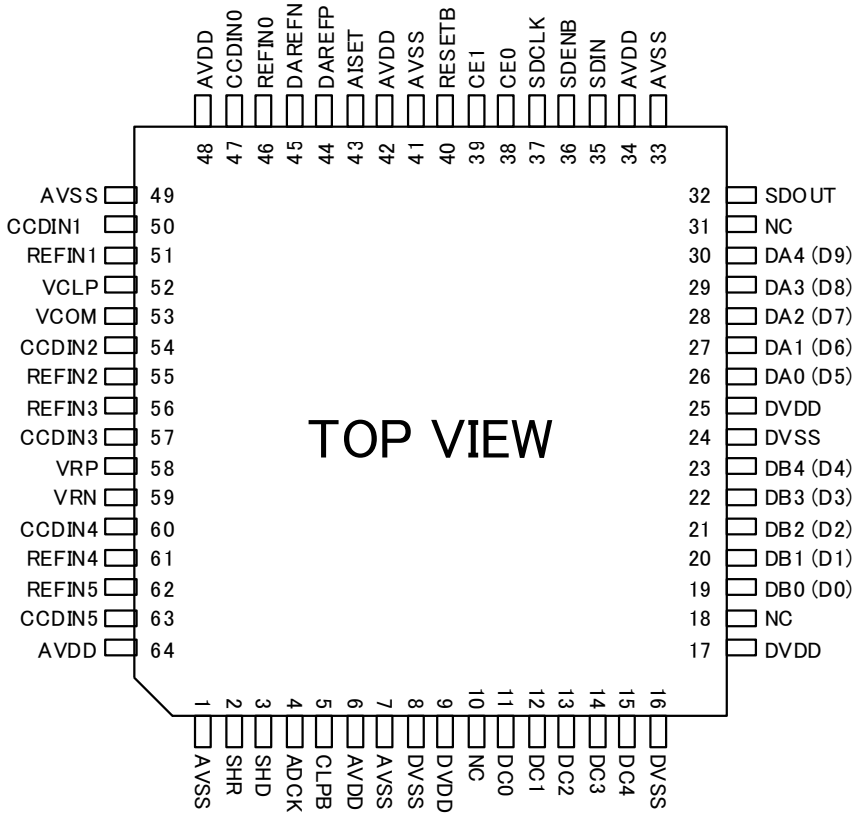


Figure 1 Pin Layout

Pin Function

No.	Name	Type	Description
1	AVSS	PWR	Analog ground
2	SHR	I	Reference level sampling pulse input
3	SHD	I	Data level sampling pulse input
4	ADCK	I	ADC sampling clock input
5	CLPB	I	Clamp control input Low : Clamp operation “ON” High : Clamp operation “OFF” This should be fixed to Low during CDS mode
6	AVDD	PWR	Analog power supply
7	AVSS	PWR	Analog ground
8	DVSS	PWR	Digital ground
9	DVDD	PWR	Digital power supply
10	NC		left open or should be connected to VSS
11 12 13 14 15	DC0 DC1 DC2 DC3 DC4	O O O O O	ADC output in a straight binary code(DC0 : LSB side , DC4 : MSB side) In 5 Bit-wide output operation in 3-channel and 6 channel modes, Data output corresponds to CCDIN4 and CCDIN5. In 10 Bit-wide output operation and in 5 Bit-wide output operation in 1 channel, 2 channel and 4 channel modes, these outputs are not used. When these modes are selected, low level is output in normal operation and either low level or high-Z output is programmable in power-down mode by register setting.
16	DVSS	PWR	Digital ground
17	DVDD	PWR	Digital power supply
18	NC		left open or should be connected to AVSS
19 20 21 22 23	DB0 (D0) DB1 (D1) DB2 (D2) DB3 (D3) DB4 (D4)	O O O O O	ADC output in a straight binary code. Signal name with parenthesis means a signal name in 10 Bit-wide output operation (in 5 Bit-wide output operation, DB0 : LSB side, DB4 : MSB side and in 10 Bit-wide output operation, D0 : LSB). When in 5 Bit-wide output operation in 1 channel mode, these outputs are not used. They become low level output in normal operation and either low level or high-Z output is programmable by register setting in power-down mode.
24	DVSS	PWR	Digital ground
25	DVDD	PWR	Digital power supply

No.	Name	Type	Description
26 27 28 29 30	DA0 (D5) DA1 (D6) DA2 (D7) DA3 (D8) DA4 (D9)	O O O O O	ADC output in a straight binary code. Signal name with parenthesis means a signal name in 10 Bit-wide output operation (in 5 Bit-wide output operation, DA0 : LSB side, DA4 : MSB side and in 10 Bit-wide output operation, D9 : MSB).
31	NC		left open or should be connected to AVSS.
32	SDOUT	O	Serial I/F Data output, Pull up or pull down please.
33	AVSS	PWR	Analog ground
34	AVDD	PWR	Analog power supply
35	SDIN	I	Serial I/F Data input
36	SDENB	I	Serial I/F Data enable
37	SDCLK	I	Serial I/F clock
38 39	CE0 CE1	I I	Chip Enable
40	RESETB	I	Reset
41	AVSS	PWR	Analog ground
42	AVDD	PWR	Analog power supply
43	AISET	I	Internal Bias current Connect a 8.2Kohm resistor between AVSS and this pin.
44	NC		left open or should be connected to AVSS.
45	TEST	I	For test , connect to AVSS.
46	REFIN0	I	Reference input Connect a same value capacitor as CCDIN0 input capacitor between AVSS and this pin. In DC direct-coupled mode, an externally-fed signal reference level should be input.
47	CCDIN0	I	Sensor signal input
48	AVDD	PWR	Analog power supply
49	AVSS	PWR	Analog ground
50	CCDIN1	I	Sensor signal input
51	REFIN1	I	Reference input Connect a same value capacitor as CCDIN1 input capacitor between AVSS and this pin. In DC direct-coupled mode, an externally-fed signal reference level should be input.
52	VCLP	O	Clamp level output Connect a stabilizing capacitor between AVSS and this pin.

No.	Name	Type	Description
53	VCOM	O	Internal Reference voltage Connect a stabilizing capacitor between AVSS and this pin
54	CCDIN2	I	Sensor signal input
55	REFIN2	I	Reference input Connect a same value capacitor as CCDIN2 input capacitor between AVSS and this pin. In DC direct-coupled mode, an externally-fed signal reference level should be input.
56	REFIN3	I	Reference input Connect a same value capacitor as CCDIN3 input capacitor between AVSS and this pin. IN DC direct-coupled mode, an externally-fed signal reference level should be input.
57	CCDIN3	I	Sensor signal input
58	VRP	O	ADC reference voltage positive side Connect a stabilizing capacitor between AVSS and this pin.
59	VRN	O	ADC reference voltage negative side Connect a stabilizing capacitor between AVSS and this pin.
60	CCDIN4	I	Sensor signal input
61	REFIN4	I	Reference input Connect a same value capacitor as CCDIN4 input capacitor between AVSS and this pin. In DC direct-coupled mode, an externally-fed signal reference level should be input.
62	REFIN5	I	Reference input Connect a same value capacitor as CCDIN5 input capacitor between AVSS and this pin. In DC direct-coupled mode, an externally-fed signal reference level should be input.
63	CCDIN5	I	Sensor signal input
64	AVDD	PWR	Analog power supply

Type description I : input pin O : output pin PWR : power supply pin

Note) AVDD is a power supply for Analog part and Digital part.
DVDD is a power supply for the Digital output bufferes.

Absolute Maximum Ratings

AVSS = DVSS = 0 V. All voltages are referenced to ground.

Parameter	Symbol	Min.	Max.	Unit	Notes
Power Supplies	AVDD DVDD	−0.3 −0.3	4.5 4.5	V V	
Input Current	IIN	−10	10	mA	Except Supply Pins
Analog Input Voltage	VINA	−0.3	AVDD+0.3	V	
Digital Input Voltage (Input Pins)	VINL	−0.3	AVDD+0.3	V	
Digital Input Voltage (Output Pins)	VONL	−0.3	DVDD+0.3	V	Restriction on the over input
Ambient Operating Temperature	Ta	0	70	°C	
Storage Temperature	Tstg	−65	150	°C	

Operation under a condition exceeding above limits may cause permanent damage to the device. Normal operation is not guaranteed under the above extreme conditions.

Recommended Operating Conditions

AVSS = DVSS = 0 V. All voltages are referenced to ground.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supplies Analog Output buffer	 AVDD DVDD	 3.0 3.0	 3.3 3.3	 3.6 3.6	 V V	
REFINn (n = 0 ~ 5) Input voltage at DC direct-coupled mode	VREFIN	0		AVDD−1.3	V	Positive Polarity

Electrical Characteristics

■ DC Characteristics

(AVDD = 3.0 ~ 3.6 V, DVDD = 3.0 ~ 3.6 V, Ta = 0 ~ 70 °C)

Parameter	Symbol	Pin	Min.	Max.	Unit	Notes
High level input voltage	VIH	Note 1	0.7AVDD		V	
Low level input voltage	VIL	Note 1		0.3AVDD	V	
High level output voltage 1	VOH1	Note 2	0.8DVDD		V	IOH= −1mA
Low level output voltage 1	VOL1	Note 2		0.2DVDD	V	IOL= 1mA
High level output voltage 2	VOH2	Note 3	0.8DVDD		V	IOH= −0.25mA
Low level output voltage 2	VOL2	Note 3		0.2DVDD	V	IOL= 0.25mA
Input leakage current	ILIKG	Note 1	−10	10	μA	
High-Z leakage current	IOZ	Note 2	−10	10	μA	

(note 1) SHD, SHR, ADCK, CLPB, SDCLK, SDENB, SDIN, CE0, CE1,RESETB

(note 2) DA0 ~ DA4, DB0 ~ DB4, DC0 ~ DC4

(note 3) SDOUT

■ Analog Characteristics

(AVDD = 3.3 V, DVDD = 3.3 V, Ta = 25 °C, ADCK at 40MHz unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reference Voltage part						
Clamp Voltage	VCLP	Positive Polarity Negative Polarity	0.94 2.15	1.04 2.3	1.14 2.45	V
Common Voltage	VCOM		1.1	1.2	1.3	V
ADC Reference Voltage Positive Negative	 VRP VRN		 1.5 0.7	 1.6 0.8	 1.7 0.9	V
Clamp / CDS part						
Input Range	VI	At PGA Gain= 0dB CDS mode Clamp mode DC direct-coupled mode	 1.20 1.04 1.20	 1.35 1.19 1.35	 1.50 1.34 1.50	Vpp
Input Capacitance	CIN	CCDIN		10		pF
Input Bandwidth (note 1)	CBW	CCDIN~ADC At PGA Gain= 0dB		1		 pixel
CDS Effect	CDS	noise 0.4Vpp 150kHz signal 0.8Vpp 1MHz		-35		dB
Offset Adjust DAC						
Resolution	DRES				8	Bit
Range	DRNG	Input referred value	±252.0	±298.7	±366.6	mV
Differential Non-Linearity	DNL	Guaranteed monotonicity	−1.0		+1.5	LSB
PGA						
Maximum Gain	GMAX	CCDIN~ADC Relative value to 0dB	18.25	18.75	19.25	dB
Step Width	GSTA	Guaranteed monotonicity	0.001	0.03 ～0.26		dB
ADC						
Resolution	RES				10	bit
Differential Non-Linearity	DNL	CCDIN~ADC Guaranteed no-missing code	−1.0		+1.0	LSB
Noise, Internal Offset, Cross-talk						
Input Idle State Noise (note 2)	NI	At PGA Gain=0dB At PGA Gain=18dB		0.4 1.0		LSB_{rms}
Internal Offset (note 3)	VOFST	At PGA Gain=0dB	−50		50	mV
Cross-Talk	XTALK1 XTALK2	(note 4) (note 5)	 −3	±1	 +3	LSB

(AVDD = 3.3 V, DVDD = 3.3 V, Ta = 25 °C, ADCK at 40MHz unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current Consumption						
Analog Part In Normal Operation	IA	6 channel mode		160	202	mA
Digital Output Part	ID	6 channel mode, a full scale minus 2 dB 1 MHz sine-wave input signal, CL = 10 pF		14.5	30	mA
At Power-Down	IPD	Analog part + Digital part			0.1	mA

Characteristics above are when same external components and time-constant are used as shown in the recommended , external circuit configuration examples.

(note 1)

Time till the ADC output settles within +/– 1 LSB of the final value when a full-scale minus 2 dB step signal is input.

(note 2)

Defined as a sigma of ADC output code variations.

(note 3)

It defines that the Offset DAC setting value in no input signal condition exists between Offset DAC setting value of A0h (equivalent to an input-referred, – 50 mV) and 60h (equivalent to an input-referred, + 50 mV) where ADC output code changes from 000h to 001h.

Since a total adjustable range of Offset Adjust DAC includes this internal Offset adjust range, a practical adjustable range of input signal is reduced by the internal Offset amount.

(note 4)

Definition at ADCK = 40 MHz, A/D conversion rate mode, 6 channels, CDS mode. PGA gain of the channel to be measured is set at its maximum value, all other channels' PGA gains are set at minimum values.

Then measure how much the output code of the target channel to be measured fluctuates when input to the measured channel is fixed and a full-scale minus 1 dB step signal is input on all other channels.

(note 5)

Definition at ADCK = 10 MHz, A/D conversion rate mode, all channels' PGA gains at minimum values.

Then measure how much the output code of the target channel to be measured fluctuates when input to the measured channel is fixed and a full-scale minus 1 dB step signal is input on all other channels.

■ Switching Characteristics 1 : in ADC conversion rate mode, DC direct-coupled mode

- Timing Diagrams (1) 5 Bit wide, 1 channel, 2 channel, 3 channel modes
- Timing Diagrams (3) 5 Bit wide, 4 channel, 6 channel modes
- Timing Diagrams (5) 10 Bit wide, 1 channel mode
- Timing Diagrams (7) 10 Bit wide, 2 channel mode
- Timing Diagrams (9) 10 Bit wide, 4 channel mode

(AVDD = 3.0 ~ 3.6 V, DVDD = 3.0 ~ 3.6 V, Ta = 0 ~ 70 °C)

No.	Parameter	Pin	Min.	Typ.	Max.	Unit	Condition
1	ADCK Cycle Time (T)	ADCK	33.3		2000	ns	4, 6ch mode
			66.6		2000		1, 2, 3 ch mode
2	ADCK Low Level Width	ADCK	15.0			ns	4, 6 ch mode
			31.7				1, 2, 3 ch mode
3	ADCK High Level Width	ADCK	15.0			ns	4, 6 ch mode
			31.7				1, 2, 3 ch mode
4	ADCK Rise Time	ADCK			6	ns	
5	ADCK Fall Time	ADCK			6	ns	
6	SHD Cycle Time	SHD		2T		ns	4, 6 ch mode
				T			1, 2, 3 ch mode
7	SHD Pulse Width	SHD	12			ns	
8	SHD Set-up Time (time to ADCK to rise)	SHD	0			ns	
9	SHD Delay Time (time from ADCK to fall)	SHD	14			ns	
10	SHD Aperture Delay	SHD		2.5		ns	
11	Output Data Delay Time (time from ADCK edge)	DA4~DA0 DB4~DB0 DC4~DC0	1		9	ns	C=10pF
12	Pipe Line Delay	DA4~DA0 DB4~DB0 DC4~DC0		9		unit: # of ADCK cycles	2, 3, 4, 6 ch mode and 1 ch 5 bits Width mode
				8.5			1 ch 10 bits Width mode
13	SHD = “ H “ inhibit period (time till the first ADCK to rise after SHD to fall)	SHD	T+1			ns	4, 6ch mode

■ Switching Characteristics 2 : in ADC conversion rate mode, CDS, Clamp modes

- Timing Diagrams (2) 5 Bit wide,1 channel, 2 channel, 3 channel modes
- Timing Diagrams (4) 5 Bit wide, 4 channel, 6 channel modes
- Timing Diagrams (6) 10 Bit wide, 1 channel mode
- Timing Diagrams (8) 10 Bit wide, 2 channel mode
- Timing Diagrams (10) 10 Bit wide, 4 channel mode

(AVDD = 3.0 ~ 3.6 V, DVDD = 3.0 ~ 3.6 V, Ta = 0 ~ 70 °C)

No.	Parameter	Pin	Min.	Typ.	Max.	Unit	Condition
1	ADCK Cycle Time (T)	ADCK	25		2000	ns	
2	ADCK Low Level Width	ADCK	10.9			ns	
3	ADCK High Level Width	ADCK	10.9			ns	
4	SHR, SHD Cycle Time	SHR, SHD		2T		ns	4, 6ch mode
				T			1, 2, 3ch mode
5	SHR Pulse Width	SHR	8			ns	
6	SHD Pulse Width	SHD	8			ns	
7	SHD Set-up Time (time to ADCK to rise)	SHD	0			ns	
8	SHD Delay Time (time from ADCK to fall)	SHD	10			ns	
9	SHR Aperture Delay	SHR		3.0		ns	
10	SHD Aperture Delay	SHD		2.5		ns	
11	Output Data Delay Time (time from ADCK edge)	DA4~DA0 DB4~DB0 DC4~DC0	1		9	ns	C=10pF
12	Pipe Line Delay	DA4~DA0 DB4~DB0 DC4~DC0		9		unit: # of ADCK cycles	2, 3, 4, 6ch mode and 1CH 5 bits Width mode
				8.5			1CH 10 bits Width mode
13	SHD = " H " inhibit period (time till the first ADCK to rise after SHD to fall)	SHD	T+1			ns	4, 6ch mode

■ Switching Characteristics 3 : in total pixel rate mode, DC direct-coupled mode

- Timing Diagrams (11) 10 Bit wide, 2 channel mode
- Timing Diagrams (13) 10 Bit wide, 3 channel mode
- Timing Diagrams (15) 10 Bit wide, 4 channel mode
- Timing Diagrams (17) 10 Bit wide, 6 channel mode

(AVDD = 3.0 ~ 3.6 V, DVDD = 3.0 ~ 3.6 V, Ta = 0 ~ 70°C)

No.	Parameter	Pin	Min.	Typ.	Max.	Unit	Condition
1	ADCK Cycle Time (T)	ADCK	12.5		333	ns	6ch mode
			16.6		500		4ch mode
			22.2		666		3ch mode
			33.3		1000		2ch mode
2	ADCK Low Level Width	ADCK	4.6			ns	6ch mode
			6.7				4ch mode
			9.5				3ch mode
			15.0				2ch mode
3	ADCK High Level Width	ADCK	4.6			ns	6ch mode
			6.7				4ch mode
			9.5				3ch mode
			15.0				2ch mode
4	SHD Cycle Time	SHD		6T		ns	6ch mode
				4T			4ch mode
				3T			3ch mode
				2T			2ch mode
6	SHD Pulse Width	SHD	12			ns	
7	SHD Set-up Time (time to ADCK to rise)	SHD	0		T/2-2	ns	
8	SHD Delay Time (note 1)	SHD	14			ns	
9	SHD Aperture Delay	SHD		2.5		ns	
10	Output Data Delay Time (time from ADCK edge)	DA4~DA0 DB4~DB0	1		9	ns	C=10pF
11	Pipe Line Delay	DA4~DA0 DB4~DB0		30		unit: # of ADCK cycles	3ch,6ch mode
				20			2ch,4ch mode
12	SHD = " H " inhibit period (time till the first ADCK to rise after SHD to fall)	SHD	3T+1			ns	6ch mode
			2T+1				4ch mode

(note 1)

Time from the ADCK edge where a falling edge of the internal A / D clock is generated.

In 2 channel, 4 channel modes, it is from ADCK to rise.

In 3 channel, 6 channel modes, it is from ADCK to fall.

■ Switching Characteristics 4 : in total pixel rate mode, CDS, Clamp modes

- Timing Diagrams (12) 10 Bit wide, 2 channel mode
- Timing Diagrams (14) 10 Bit wide, 3 channel mode
- Timing Diagrams (16) 10 Bit wide, 4 channel mode
- Timing Diagrams (18) 10 Bit wide, 6 channel mode

(AVDD = 3.0 ~ 3.6 V, DVDD = 3.0 ~ 3.6 V, Ta = 0 ~ 70°C)

No.	Parameter	Pin	Min.	Typ.	Max.	Unit	Condition
1	ADCK Cycle Time (T)	ADCK	12.5		333	ns	6ch mode
			12.5		500		4ch mode
			12.5		666		3ch mode
			12.5		1000		2ch mode
2	ADCK Low Level Width	ADCK	4.6			ns	
3	ADCK High Level Width	ADCK	4.6			ns	
4	SHR, SHD Cycle Time	SHR, SHD		6T		ns	6ch mode
				4T			4ch mode
				3T			3ch mode
				2T			2ch mode
5	SHR Pulse Width	SHR	8			ns	
6	SHD Pulse Width	SHD	8			ns	
7	SHD Set-up Time (time to ADCK to rise)	SHD	0		T/2-2	ns	
8	SHD Delay Time (note 1)	SHD	10			ns	
11	SHR Aperture Delay	SHR		3.0		ns	
12	SHD Aperture Delay	SHD		2.5		ns	
11	Output Data Delay Time (time from ADCK edge)	DA4~DA0 DB4~DB0	1		9	ns	C=10pF
12	Pipe Line Delay	DA4~DA0 DB4~DB0		30		unit: # of ADCK cycles	3ch,6ch mode
				20			2ch,4ch mode
13	SHD = " H " inhibit period (time till the first ADCK to rise after SHD to fall)	SHD	3T+1			ns	6ch mode
			2T+1				4ch mode

(note 1)

Time from the ADCK edge where a falling edge of the internal A / D clock is generated.

In 2 channel, 4 channel modes, it is from ADCK to rise.

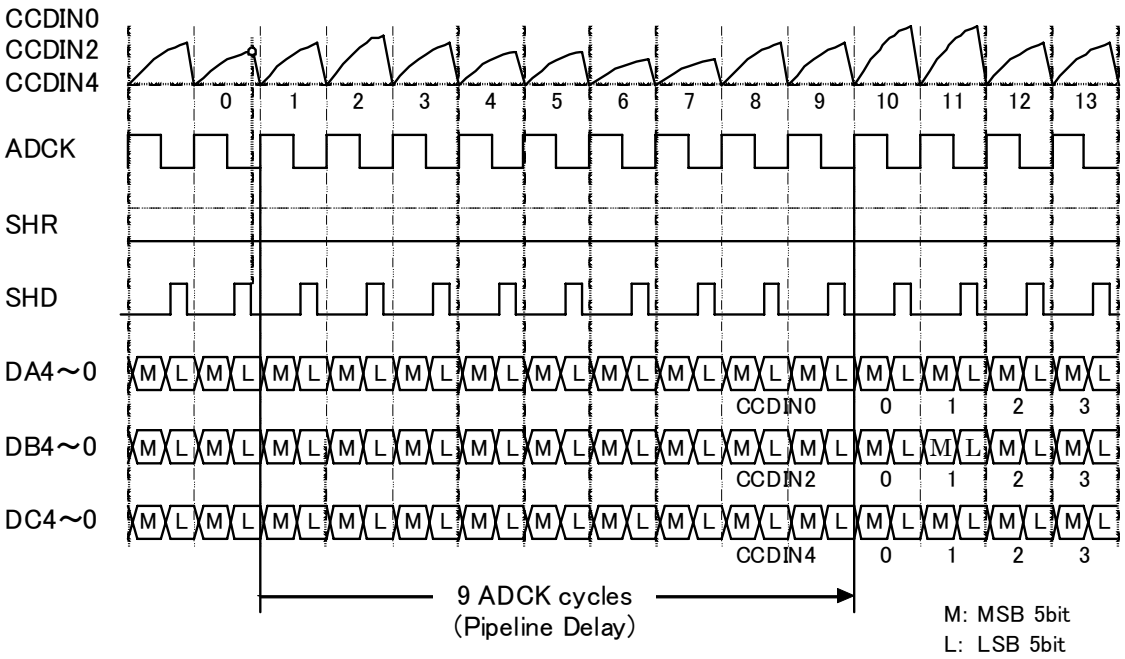
In 3 channel, 6 channel modes, it is from ADCK to fall.

Timings are specified at the points where specified levels by the DC Characteristics are intersected.

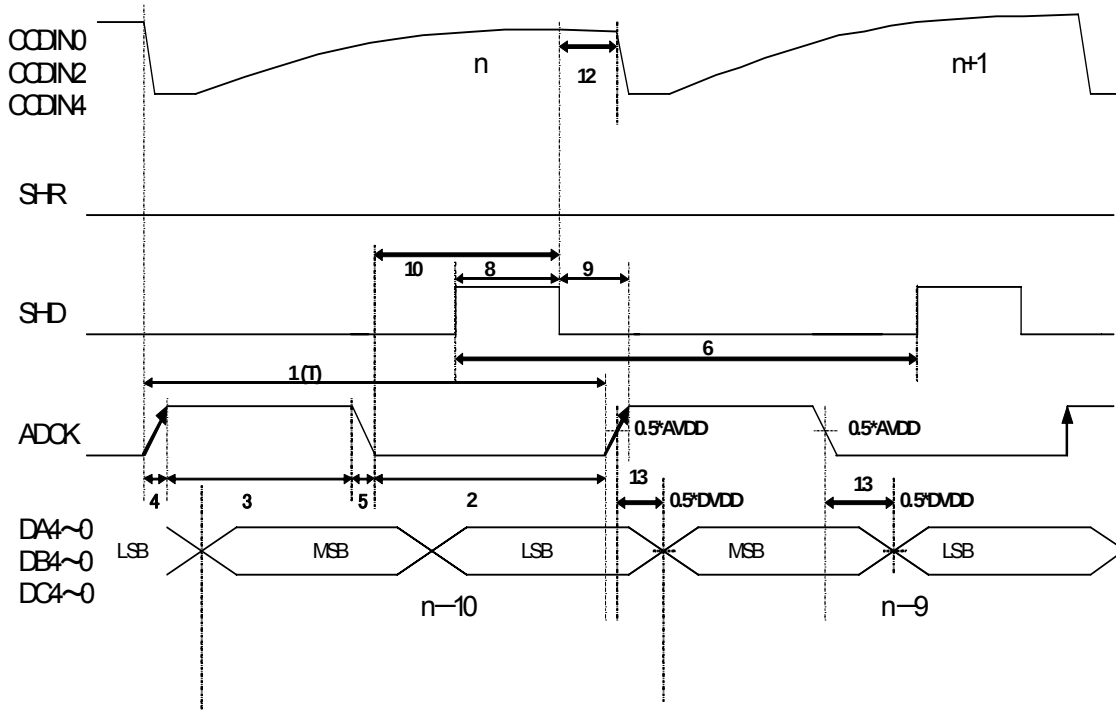
■ Timing Diagrams (1) : ADCK frequency = A/D conversion rate mode (5 Bit-wide output)

- 1 channel, 2 channel, 3 channel modes (DC direct-coupled, positive polarity)

Please refer to Switching Characteristics 1 table.



Timing Diagrams in 1 channel, 2 channel, 3 channel modes



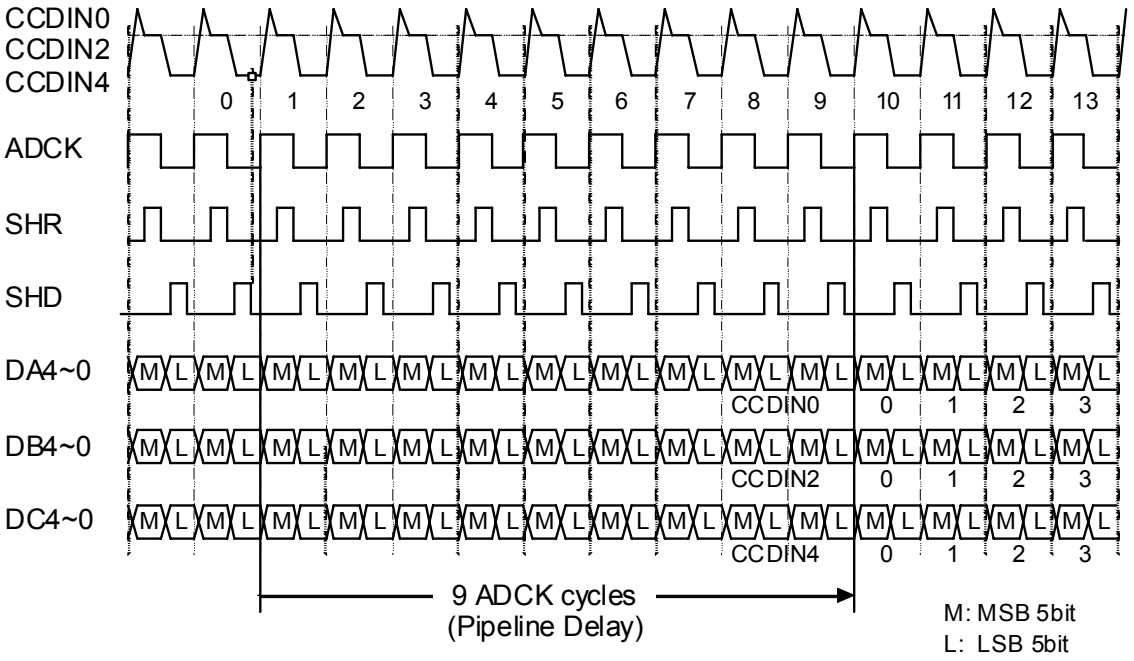
Detailed Timing Diagrams in 1 channel, 2 channel, 3 channel modes

■ Timing Diagrams (2) : ADCK frequency = A/D conversion rate mode (5 Bit-wide output)

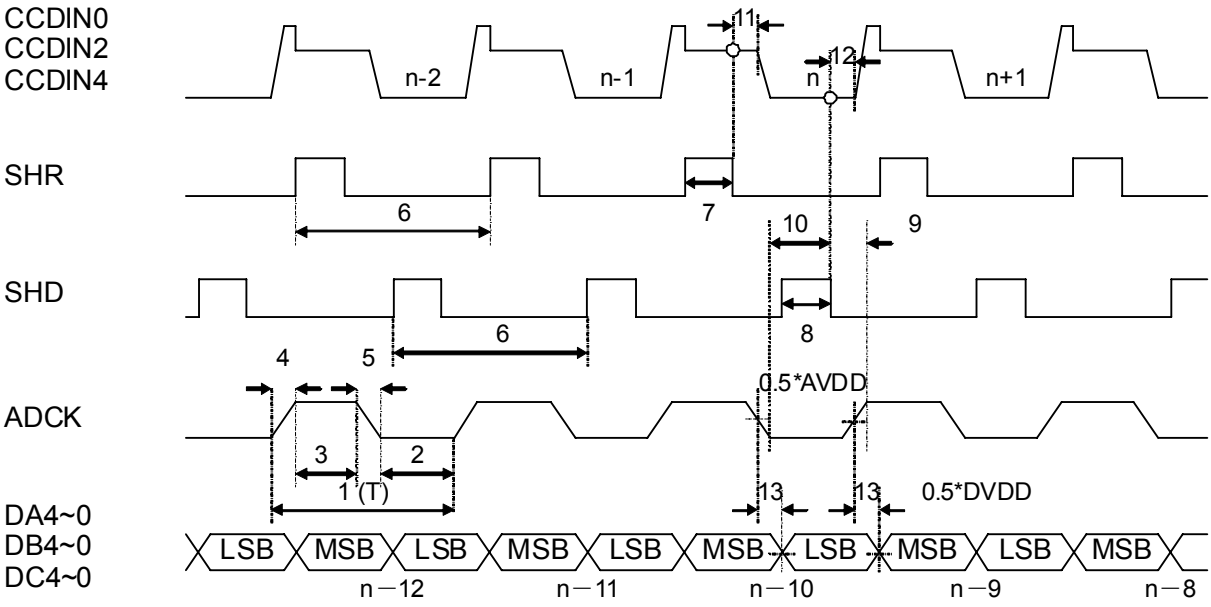
- 1 channel, 2 channel, 3 channel modes

(CDS mode & Clamp modes, negative polarity)

Please refer to Switching Characteristics 2 table.



Timing Diagrams in 1 channel, 2 channel, 3 channel modes

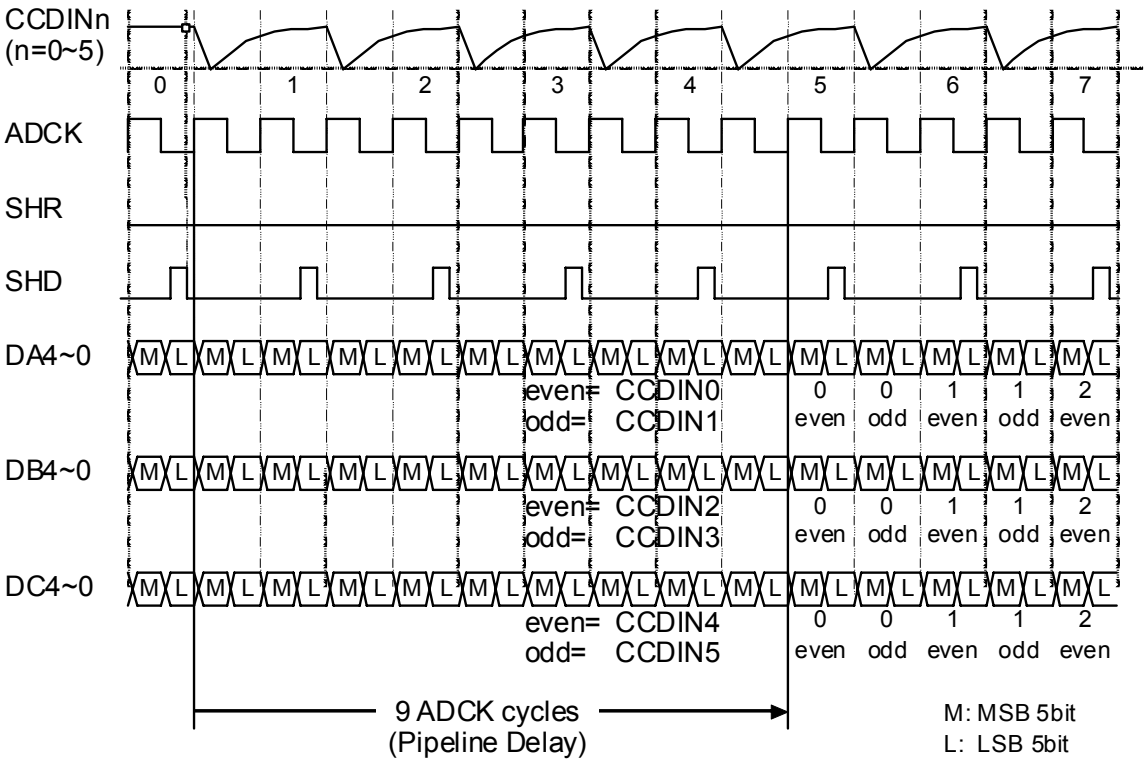


Detailed Timing Diagrams in 1 channel, 2 channel, 3 channel modes

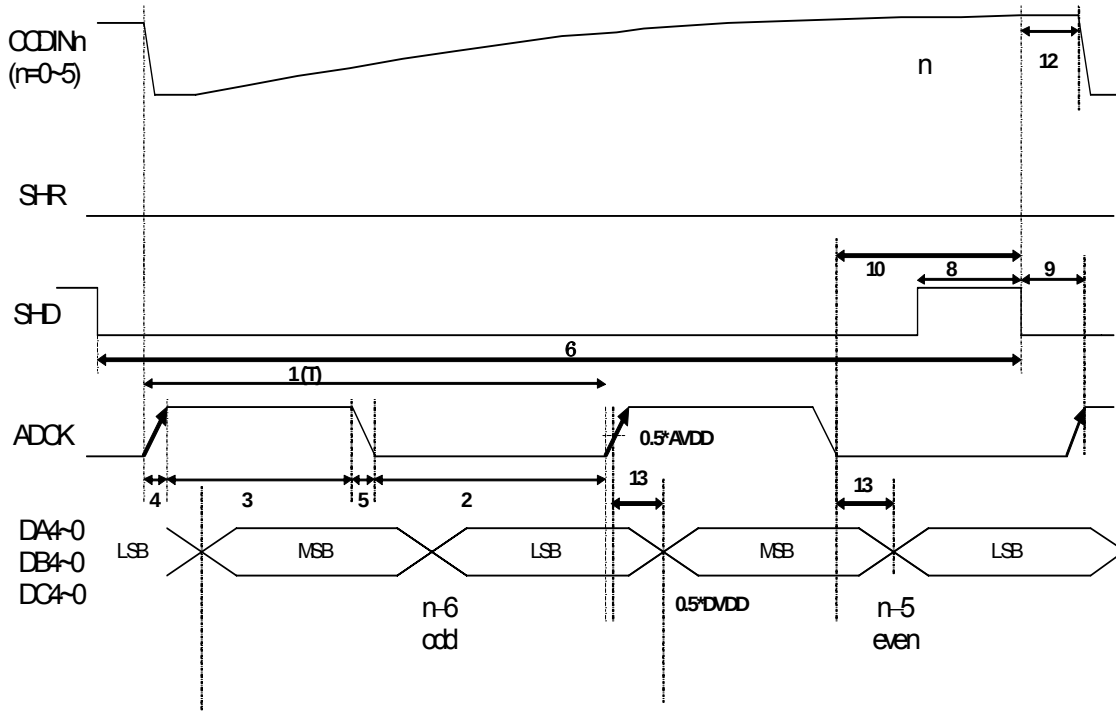
■ Timing Diagrams (3) : ADCK frequency = A/D conversion rate (5 Bit-wide output)

- 4 channel, 6 channel modes (DC direct-coupled mode, positive polarity)

Please refer to Switching Characteristics 1 table.



Timing Diagrams in 4 channel, 6 channel modes

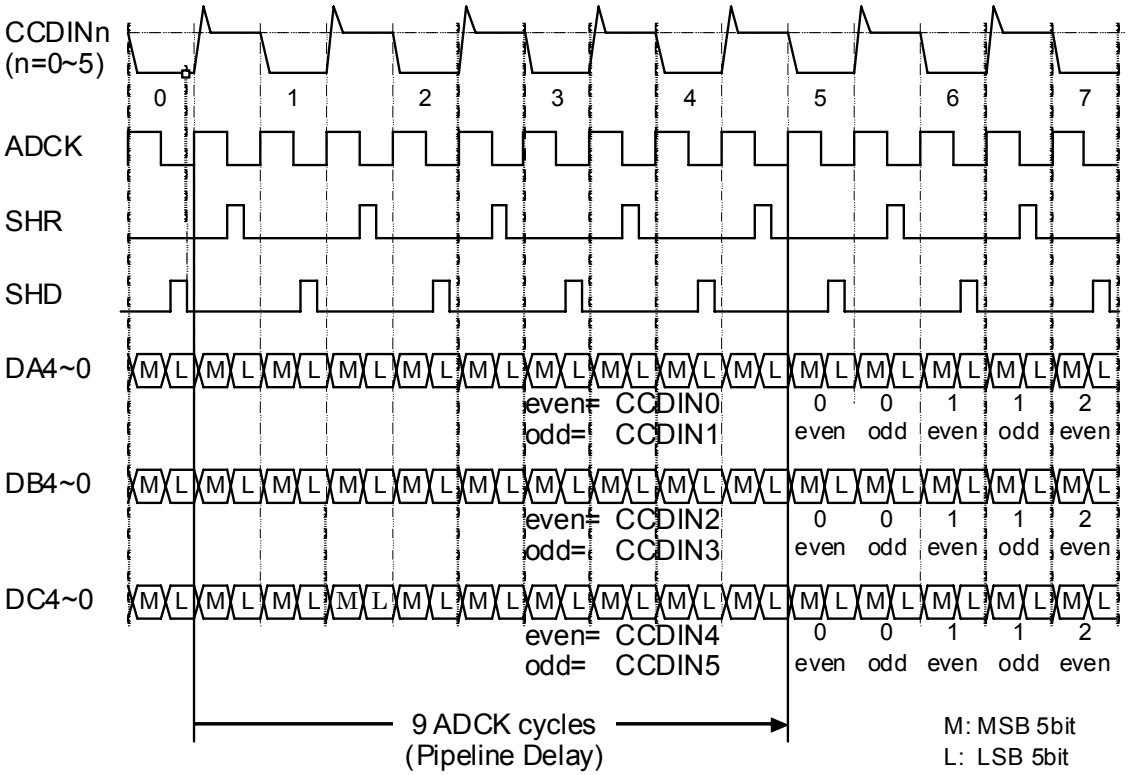


Detailed Timing Diagrams in 4 channel, 6 channel modes

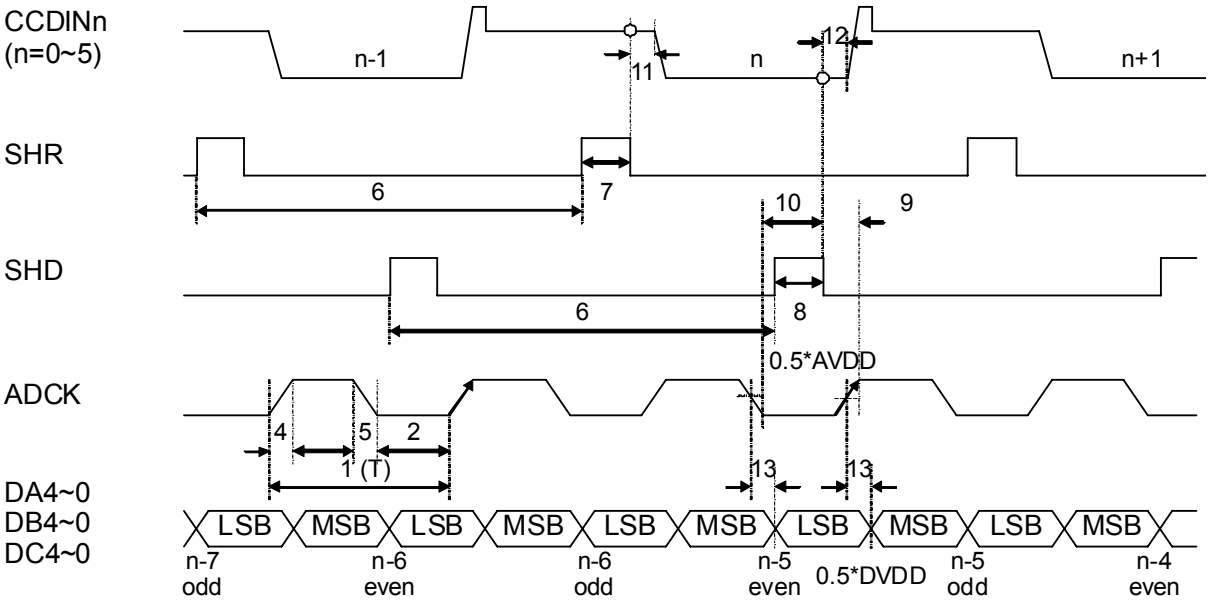
■ Timing Diagrams (4) : ADCK frequency = A/D conversion rate mode (5 Bit-wide output)

- 4 channel, 6 channel modes (CDS mode & Clamp mode, negative polarity)

Please refer to Switching Characteristics 2 table.



Timing Diagrams in 4 channel, 6 channel modes

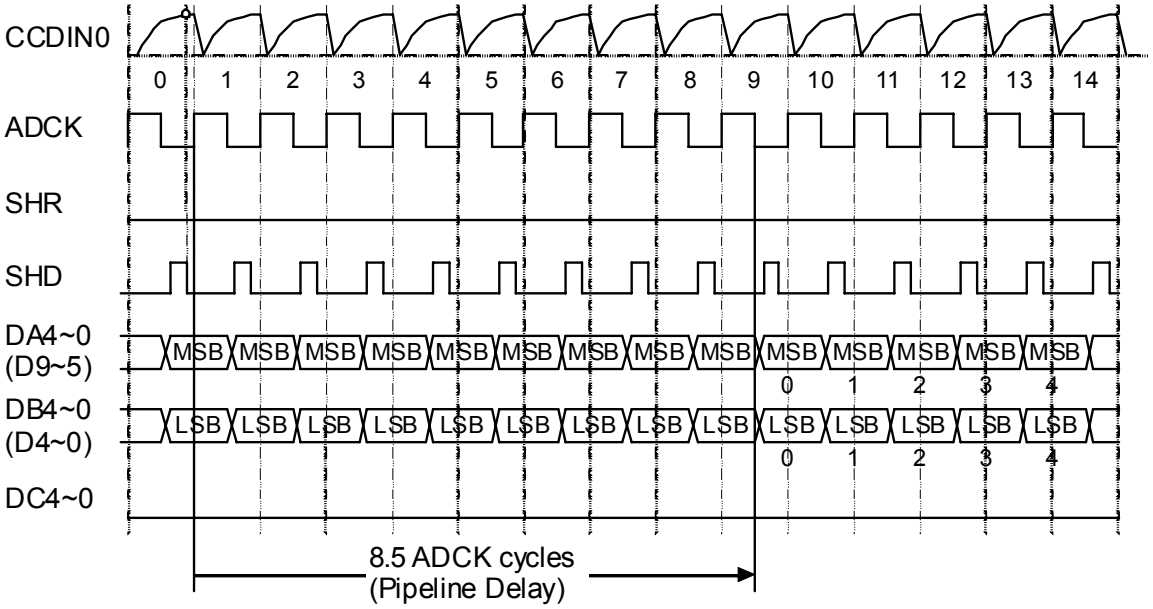


Detailed Timing Diagrams in 4 channel, 6 channel modes

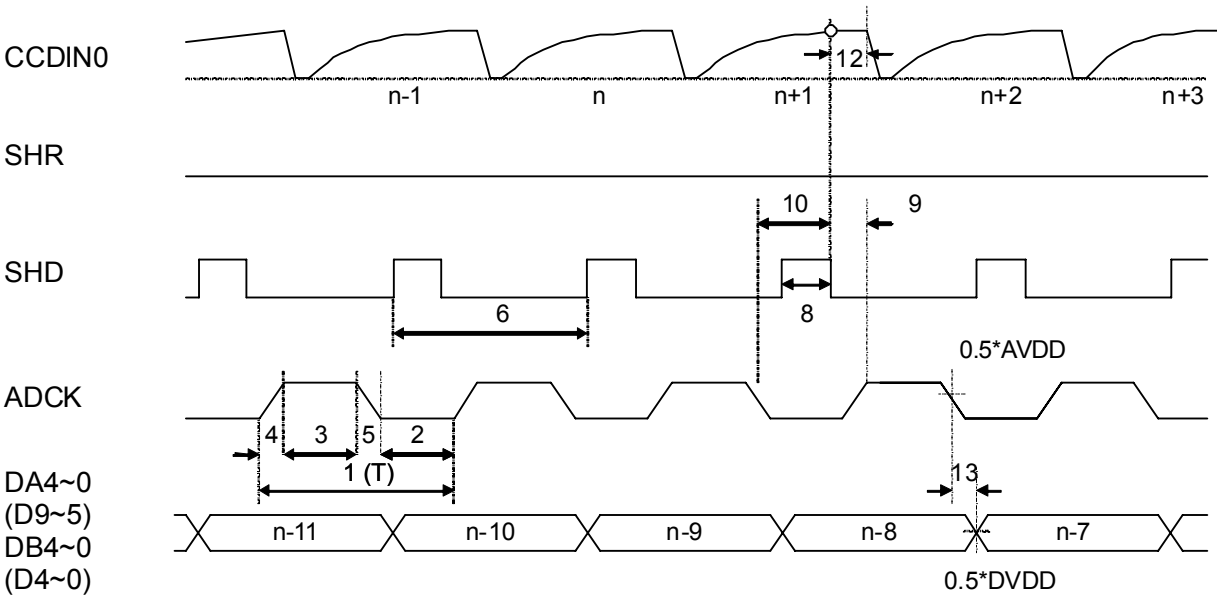
■ Timing Diagrams(5): ADCK frequency = A/D conversion rate mode (10 Bit-wide output)

- 1 channel mode (DC direct-coupled mode, positive polarity)

Please refer to Switching Characteristics 1 table.



Timing Diagrams in 1 channel mode

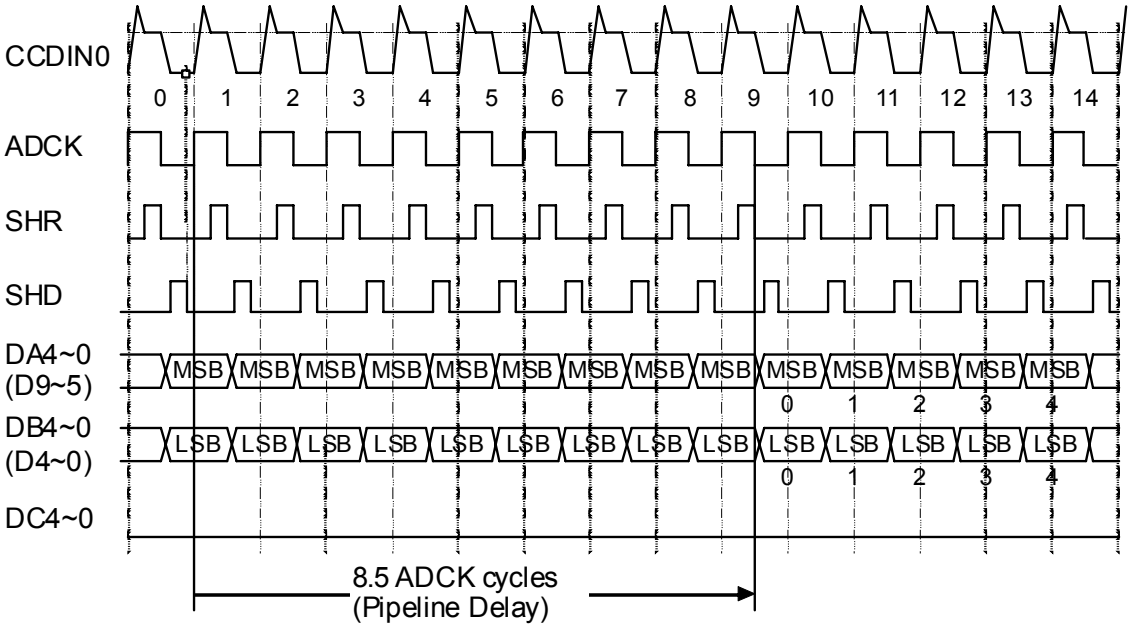


Detailed Timing Diagrams in 1 channel mode

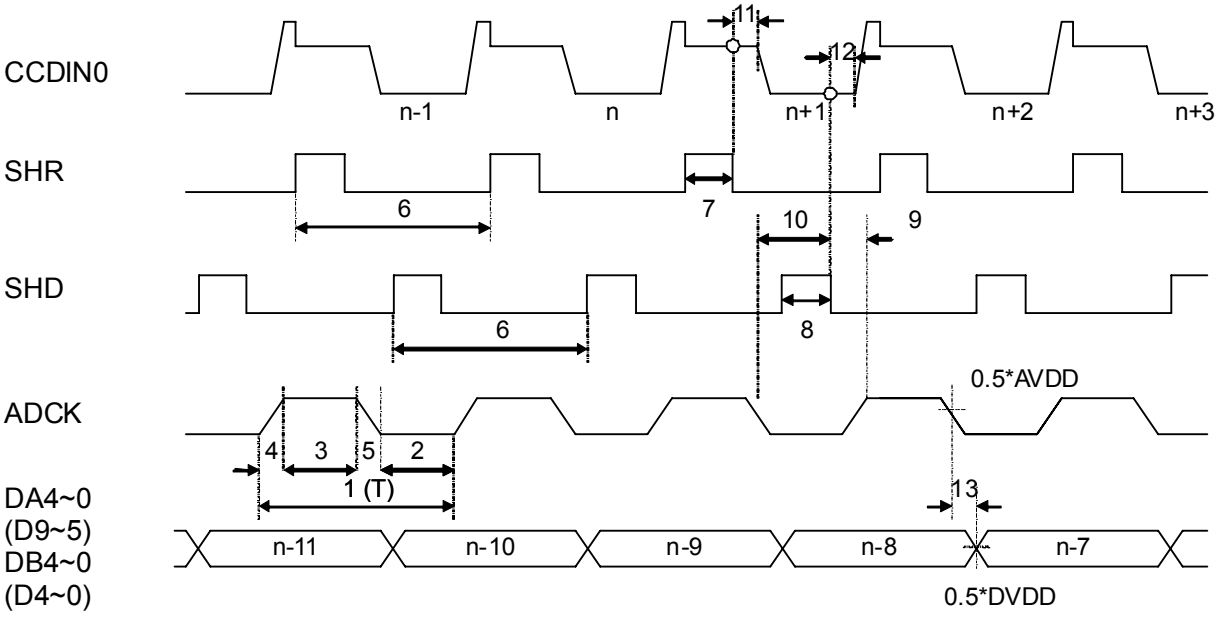
■ Timing Diagrams(6): ADCK frequency = A/D conversion rate mode (10 Bit-wide output)

- 1 channel mode (CDS mode & Clamp mode, negative polarity)

Please refer to Switching Characteristics 2 table.



Timing Diagrams in 1 channel mode

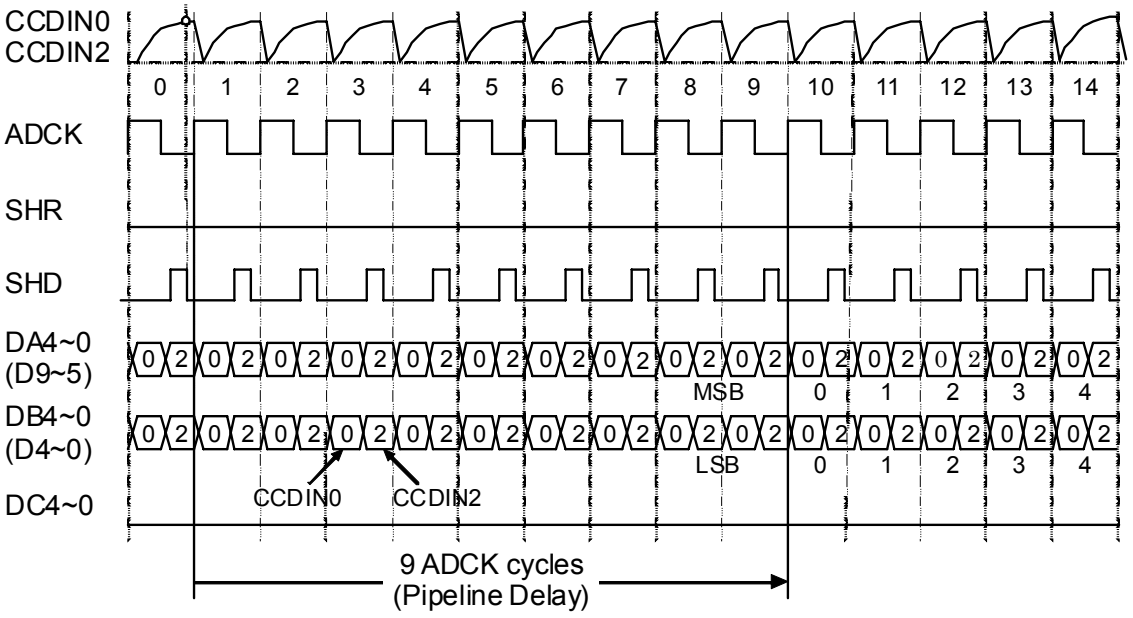


Detailed Timing Diagrams in 1 channel mode

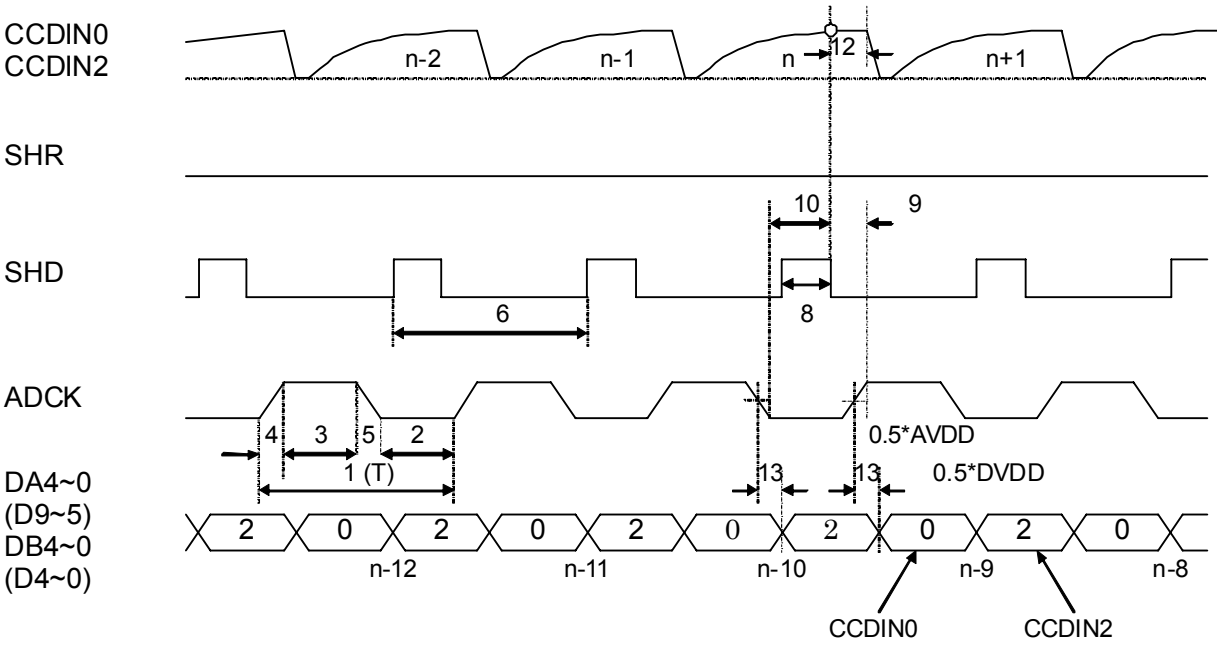
■ Timing Diagrams(7): ADCK frequency = A/D conversion rate mode (10 Bit-wide output)

- 2 channel mode (DC direct-coupled mode, positive polarity)

Please refer to Switching Characteristics 1 table.



Timing Diagrams in 2 channel mode

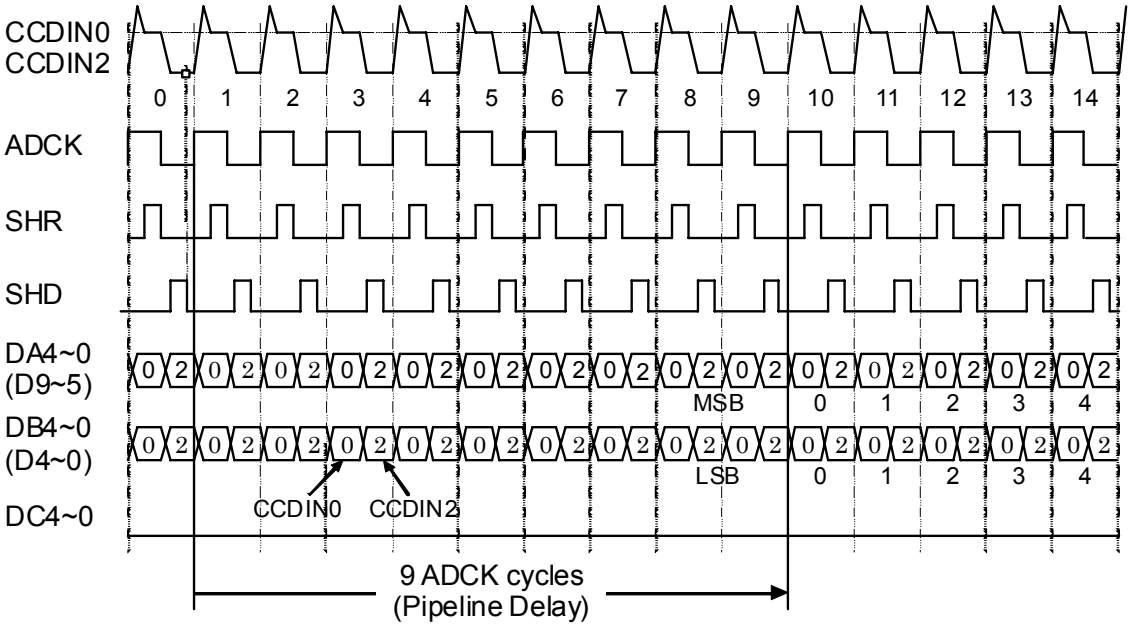


Detailed Timing Diagrams in 2 channel mode

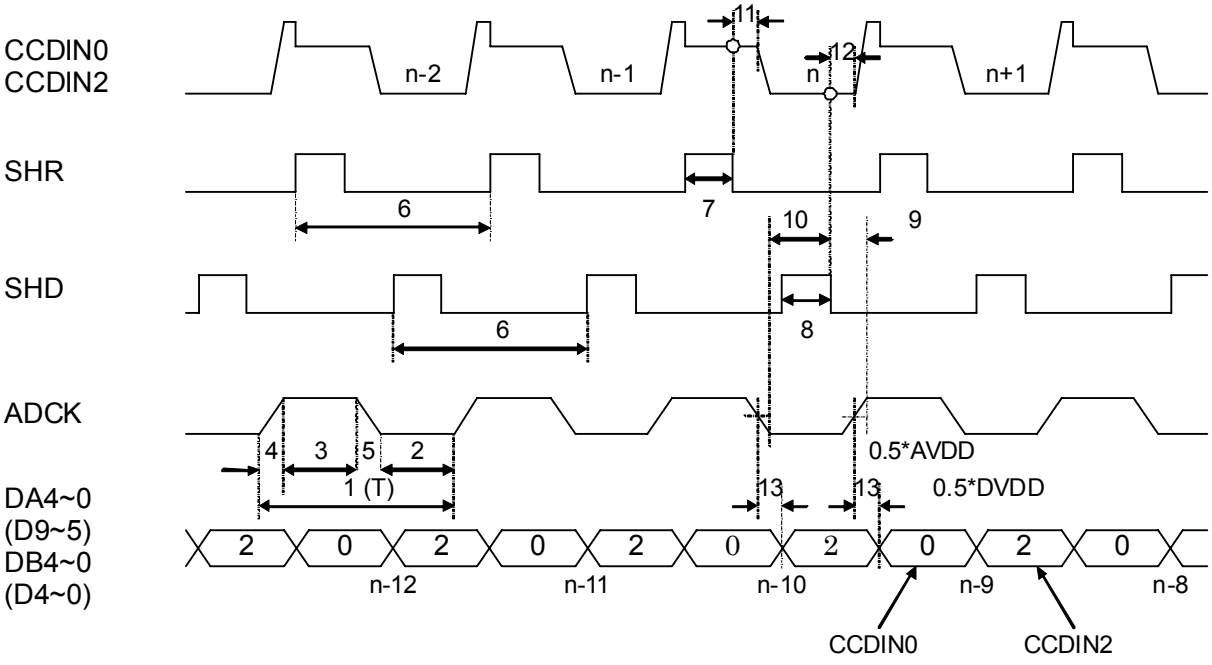
■ Timing Diagrams(8): ADCK frequency = A/D conversion rate mode (10 Bit-wide output)

- 2 channel mode (CDS mode & Clamp mode, negative polarity)

Please refer to Switching Characteristics 2 table.



Timing Diagrams in 2 channel mode

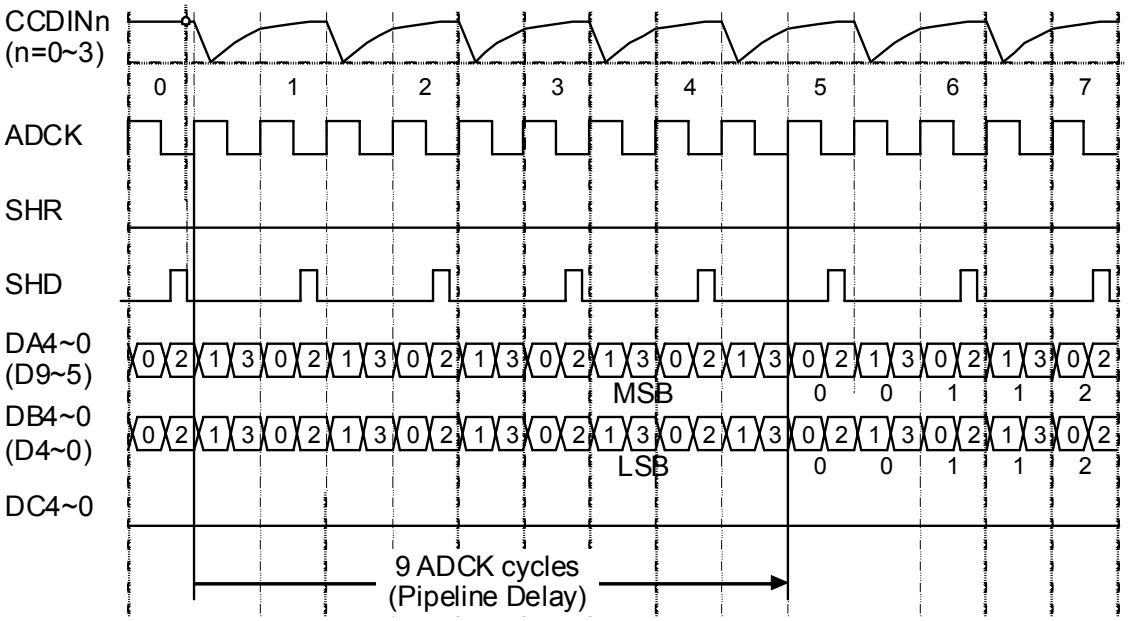


Detailed Timing Diagrams in 2 channel mode

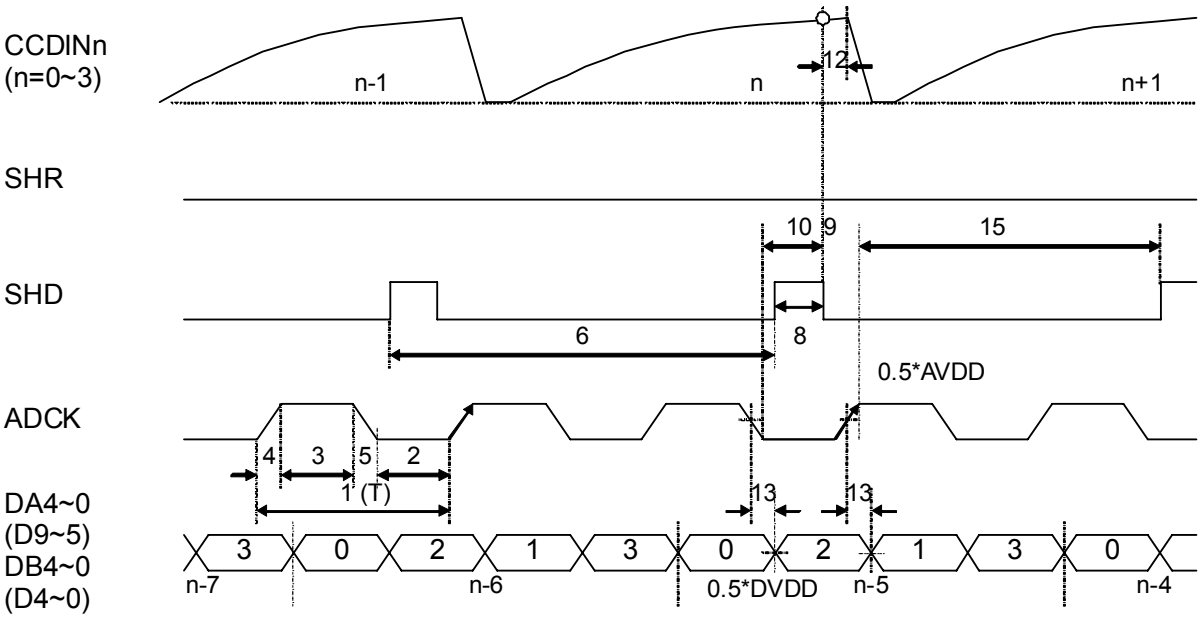
■ Timing Diagrams(9): ADCK frequency = A/D conversion rate mode (10 Bit-wide output)

- 4 channel mode (DC direct-coupled mode, positive polarity)

Please refer to Switching Characteristics 1 table.



Timing Diagrams in 4 channel mode

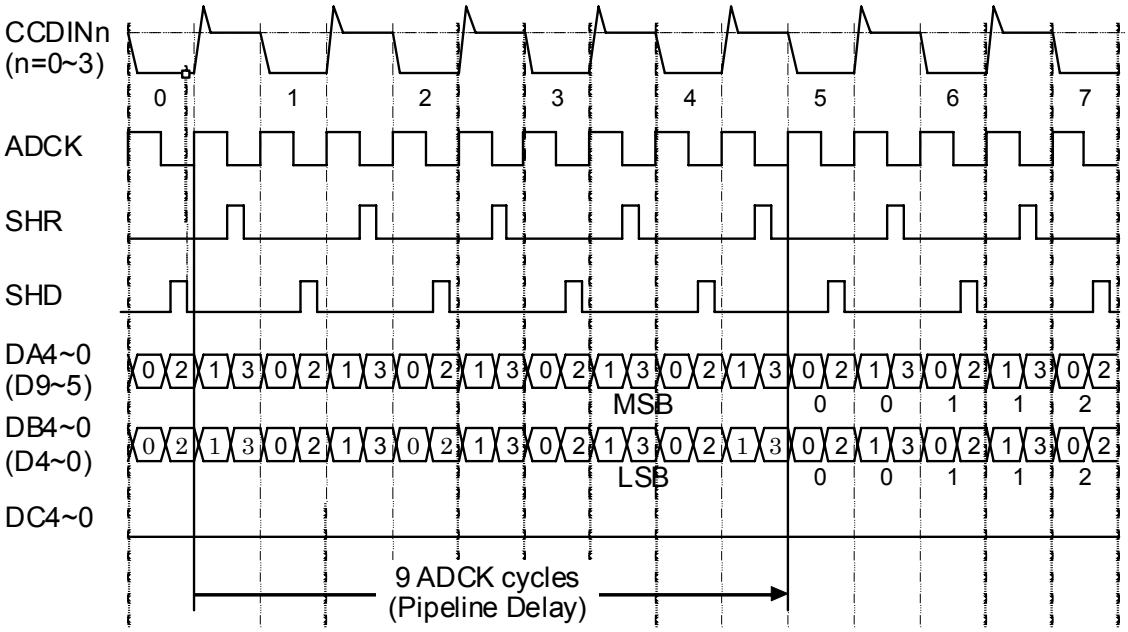


Detailed Timing Diagrams in 4 channel mode

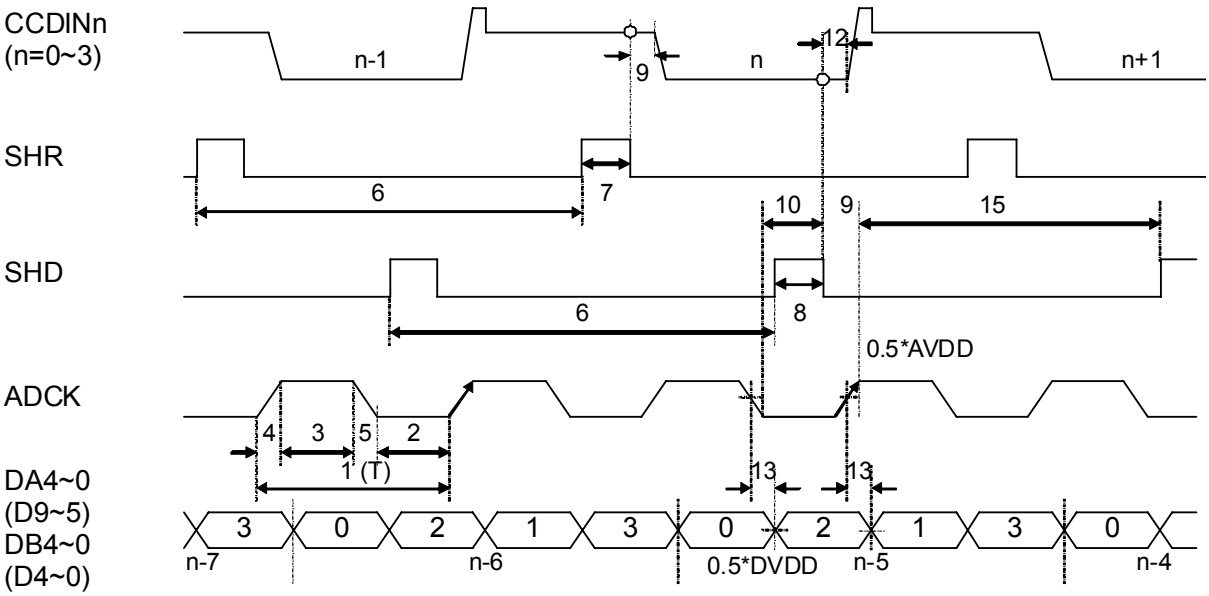
■ Timing Diagrams(10):ADCK frequency = A/D conversion rate mode (10Bit-wide output)

- 4 channel mode (CDS mode & Clamp mode, negative polarity)

Please refer to Switching Characteristics 2 table.



Timing Diagrams in 4 channel mode

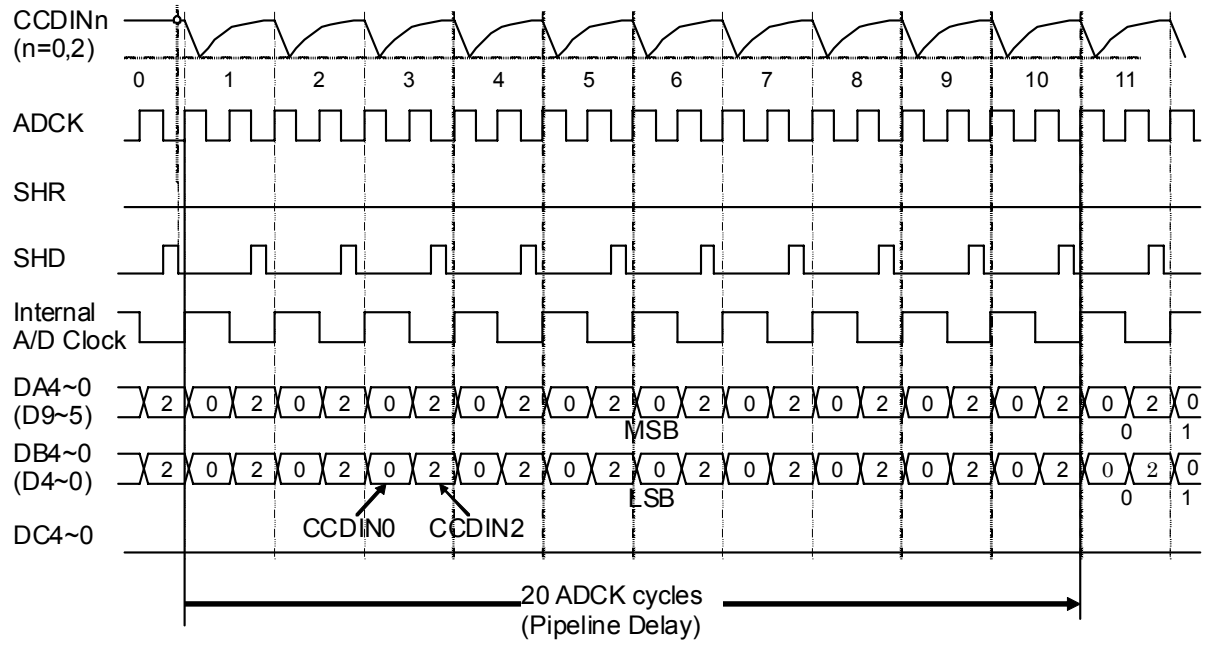


Detailed Timing Diagrams in 4 channel mode

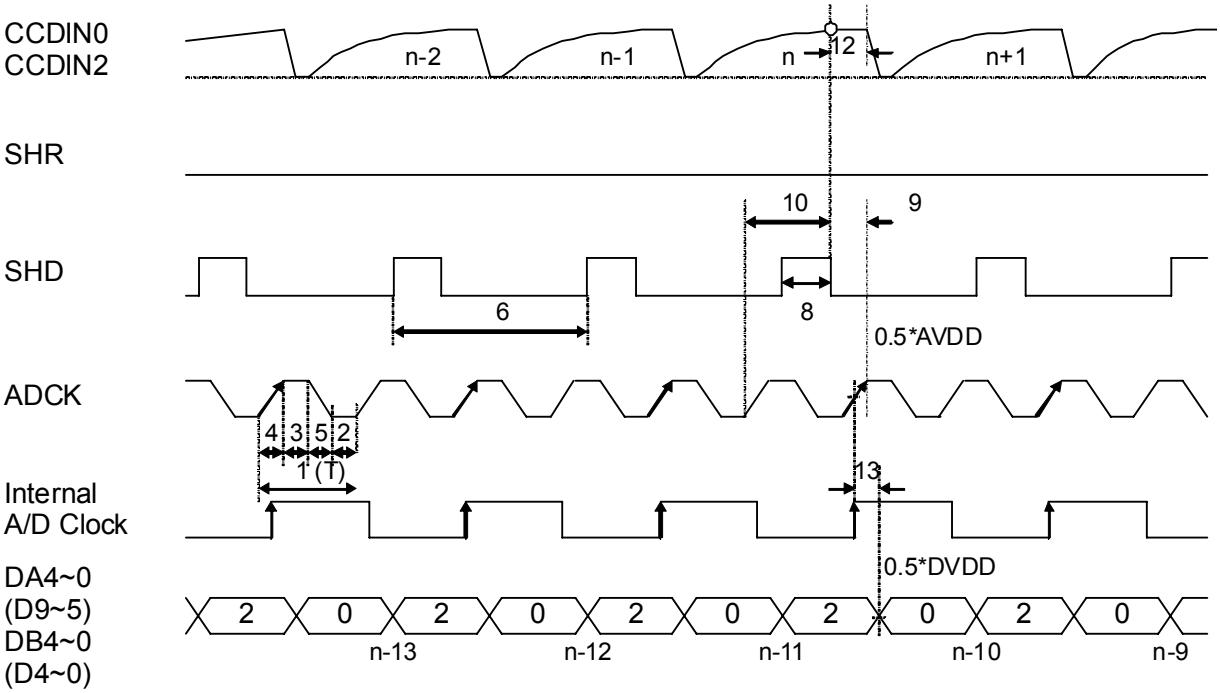
■ Timing Diagrams(11): ADCK frequency = total pixel rate mode (10 Bit-wide output)

- 2 channel mode (DC direct-coupled mode, positive polarity)

Please refer to Switching Characteristics 3 table.



Timing Diagrams in 2 channel mode

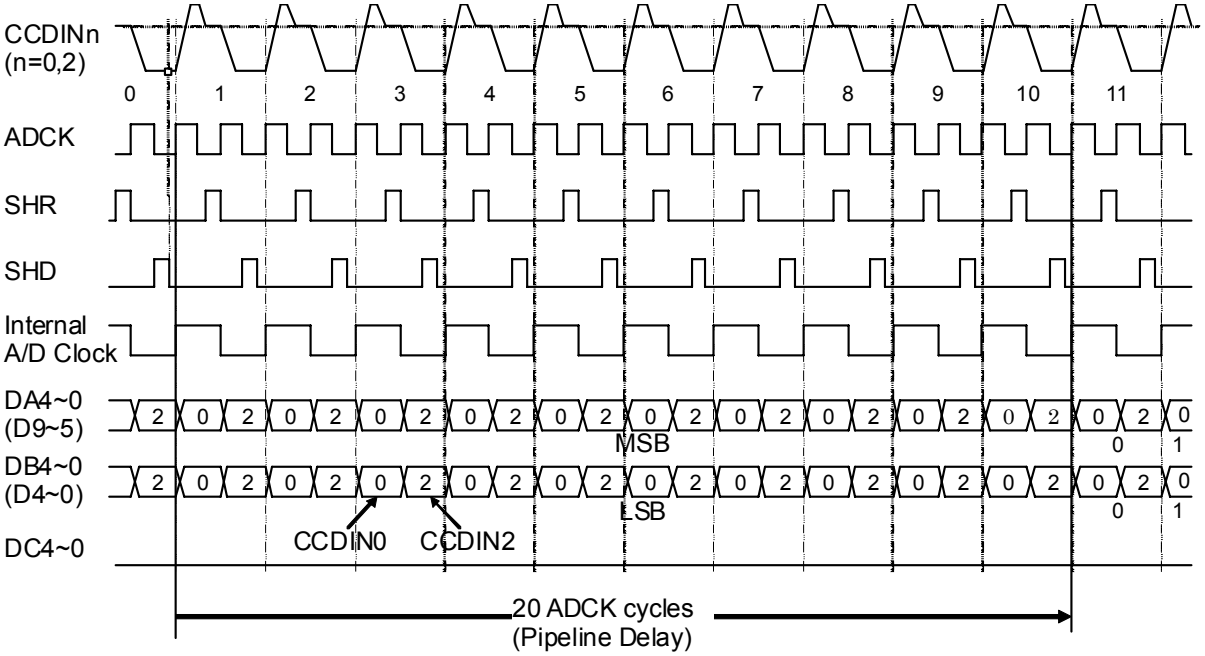


Detailed Timing Diagrams in 2 channel mode

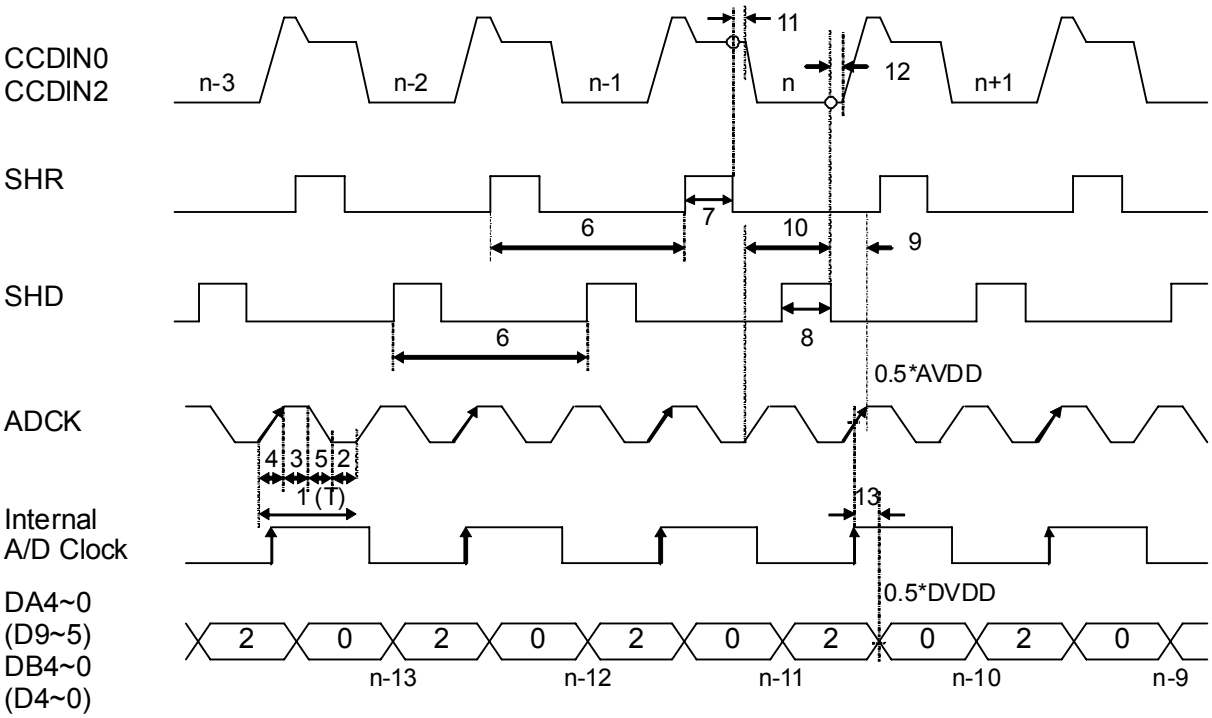
■ Timing Diagrams(12): ADCK frequency = total pixel rate mode (10 Bit-wide output)

- 2 channel mode (CDS mode & Clamp mode, negative polarity)

Please refer to Switching Characteristics 4 table.



Timing Diagrams in 2 channel mode

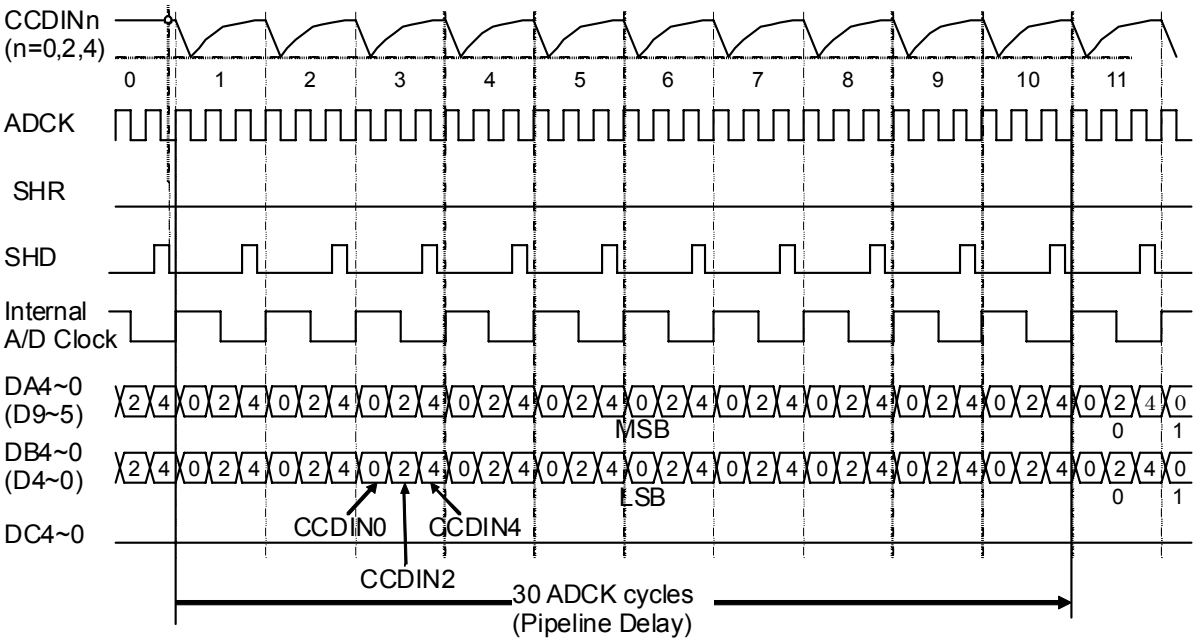


Detailed Timing Diagrams in 2 channel mode

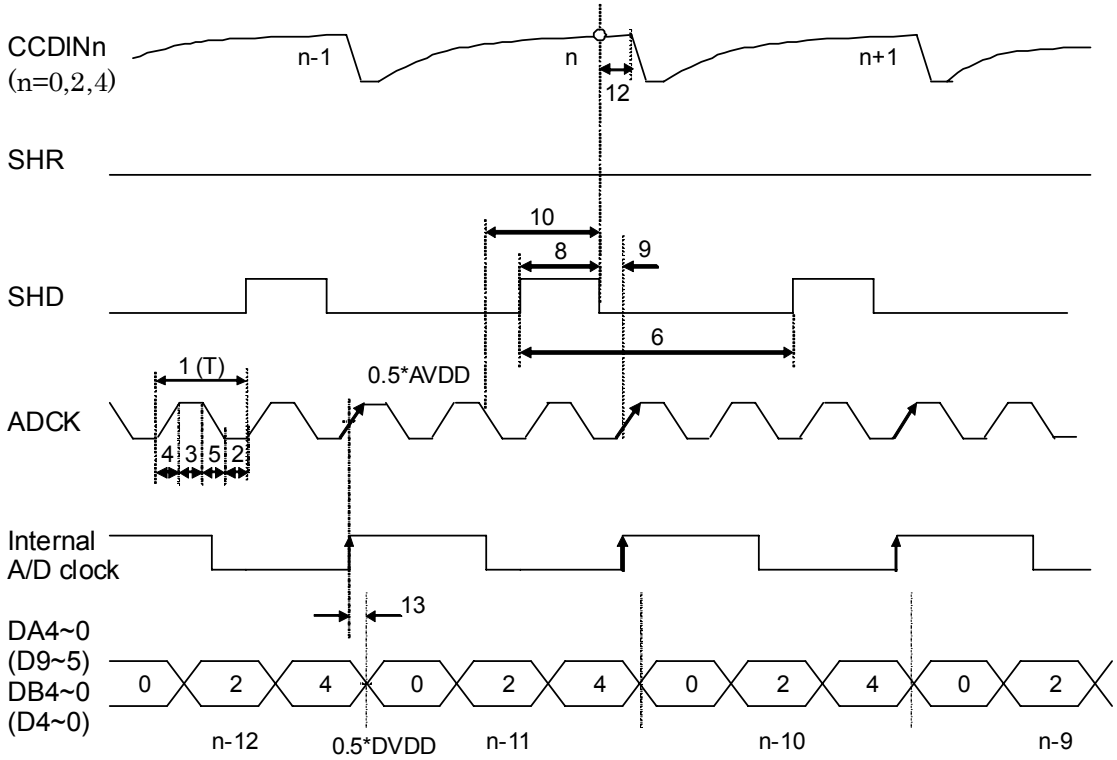
■ Timing Diagrams(13): ADCK frequency = total pixel rate mode (10 Bit-wide output)

- 3 channel mode (DC direct-coupled mode, positive polarity)

Please refer to Switching Characteristics 3 table.



Timing Diagrams in 3 channel mode

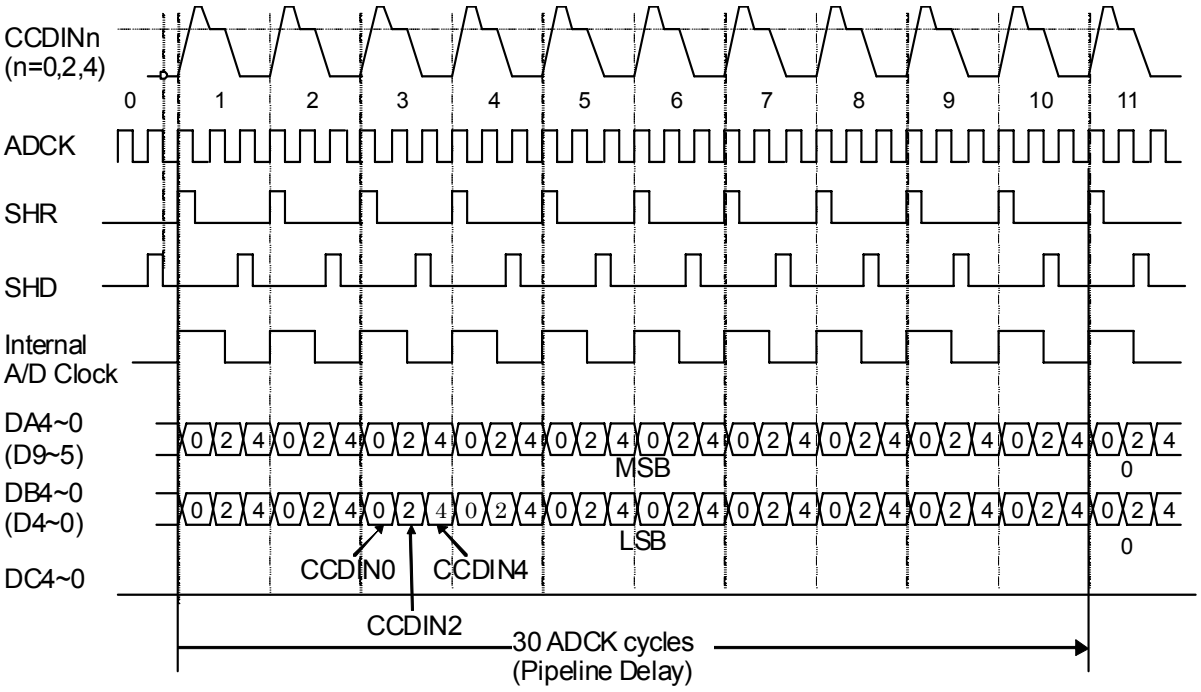


Detailed Timing Diagrams in 3 channel mode

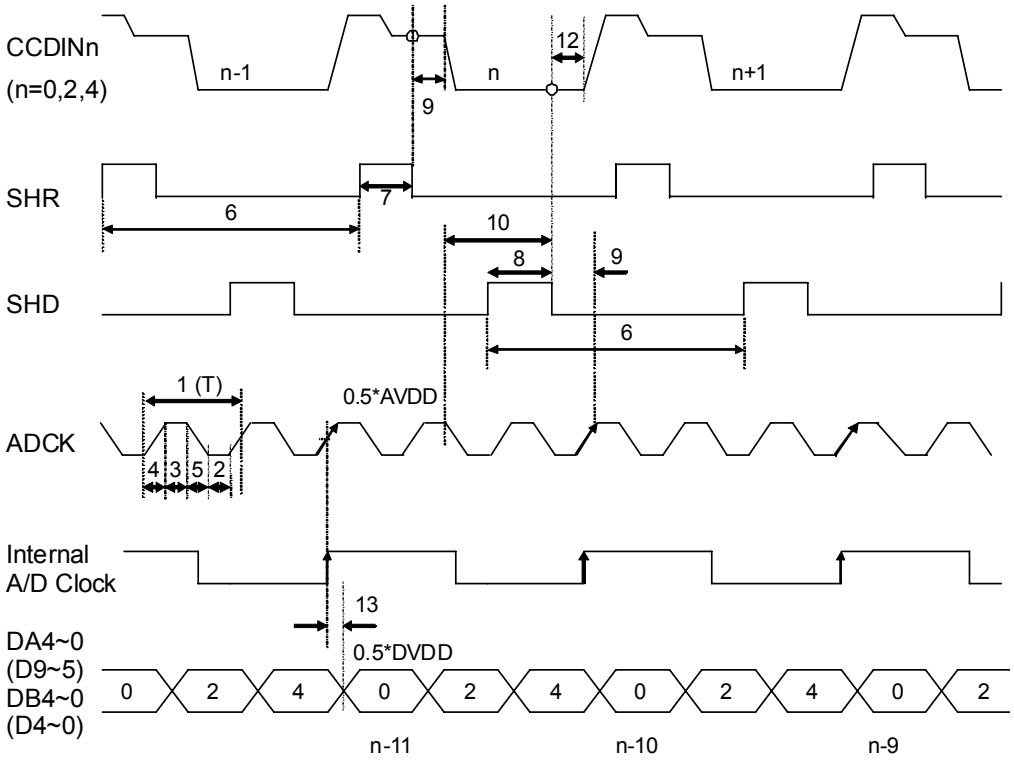
■ Timing Diagrams(14): ADCK frequency = total pixel rate mode (10 Bit-wide output)

- 3 channel mode (CDS mode & Clamp mode, negative polarity)

Please refer to Switching Characteristics 4 table.



Timing Diagrams in 3 channel mode

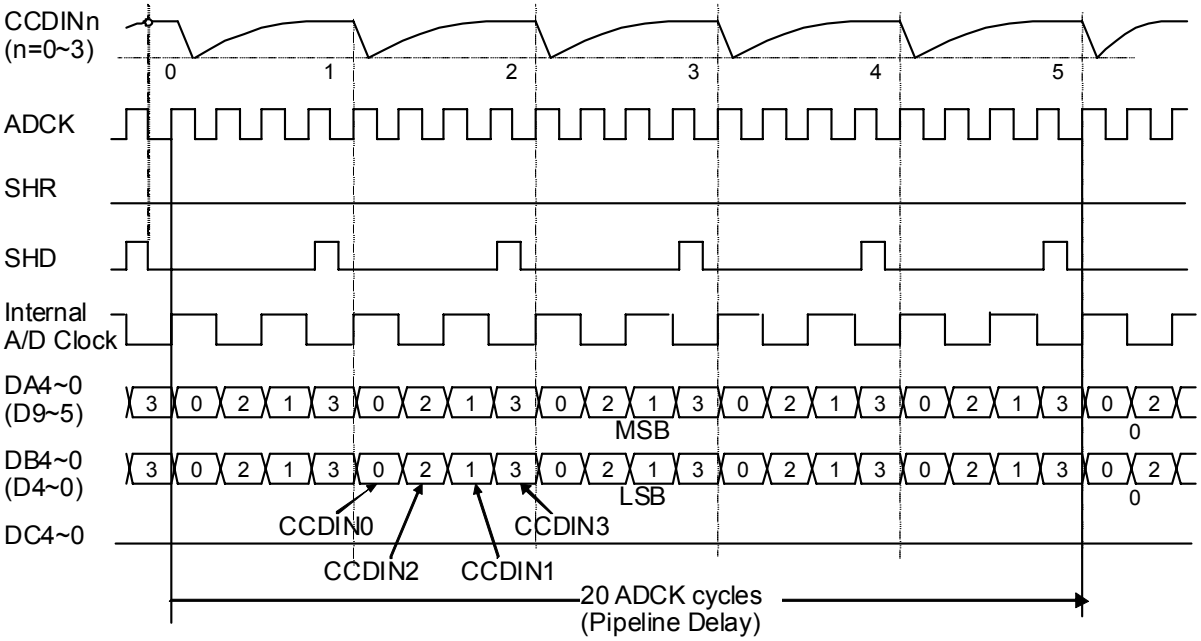


Detailed Timing Diagrams in 3 channel mode

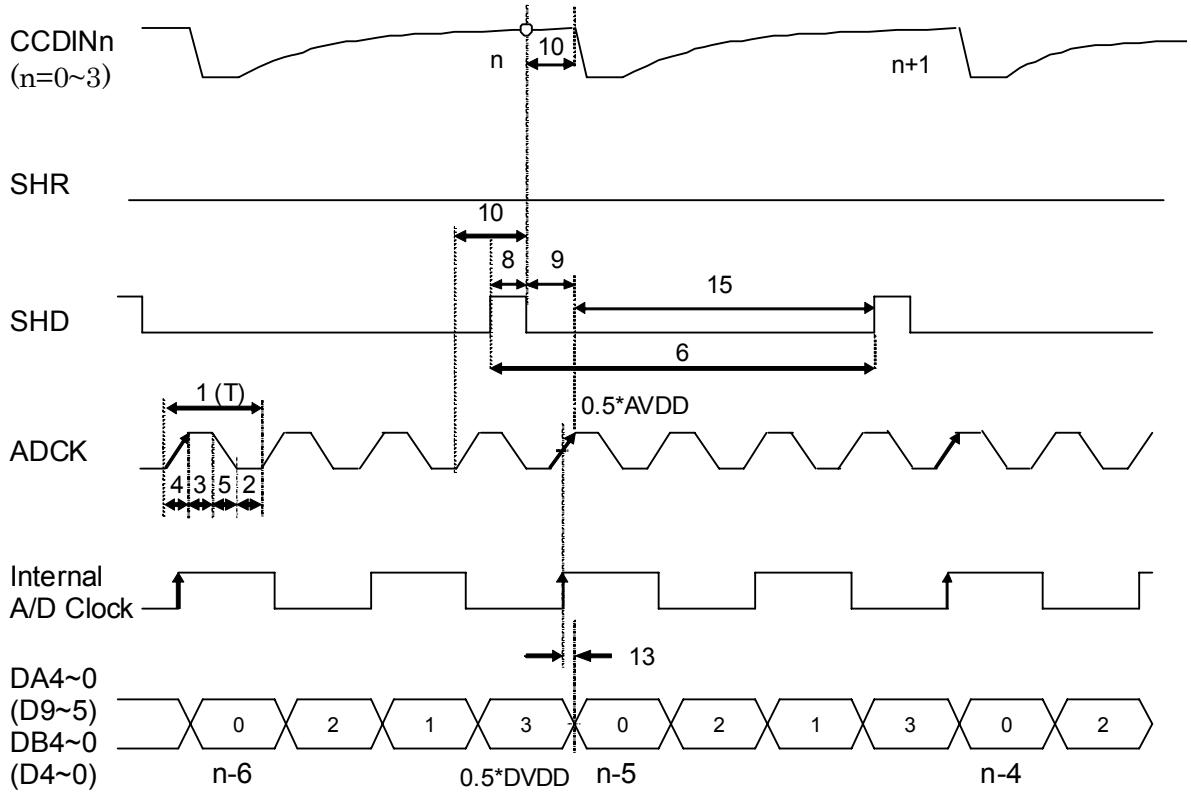
■ Timing Diagrams(15): ADCK frequency = total pixel rate mode (10 Bit-wide output)

- 4 channel mode (DC direct-coupled mode, positive polarity)

Please refer to Switching Characteristics 3 table.



Timing Diagrams in 4 channel mode

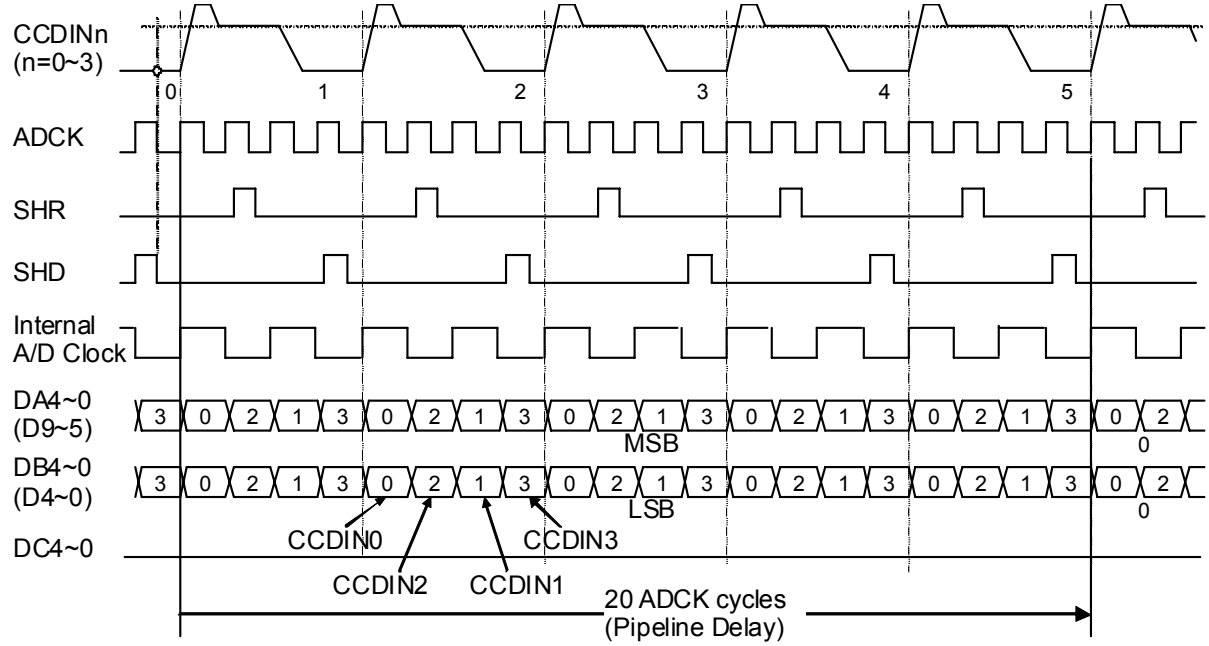


Detailed Timing Diagrams in 4 channel mode

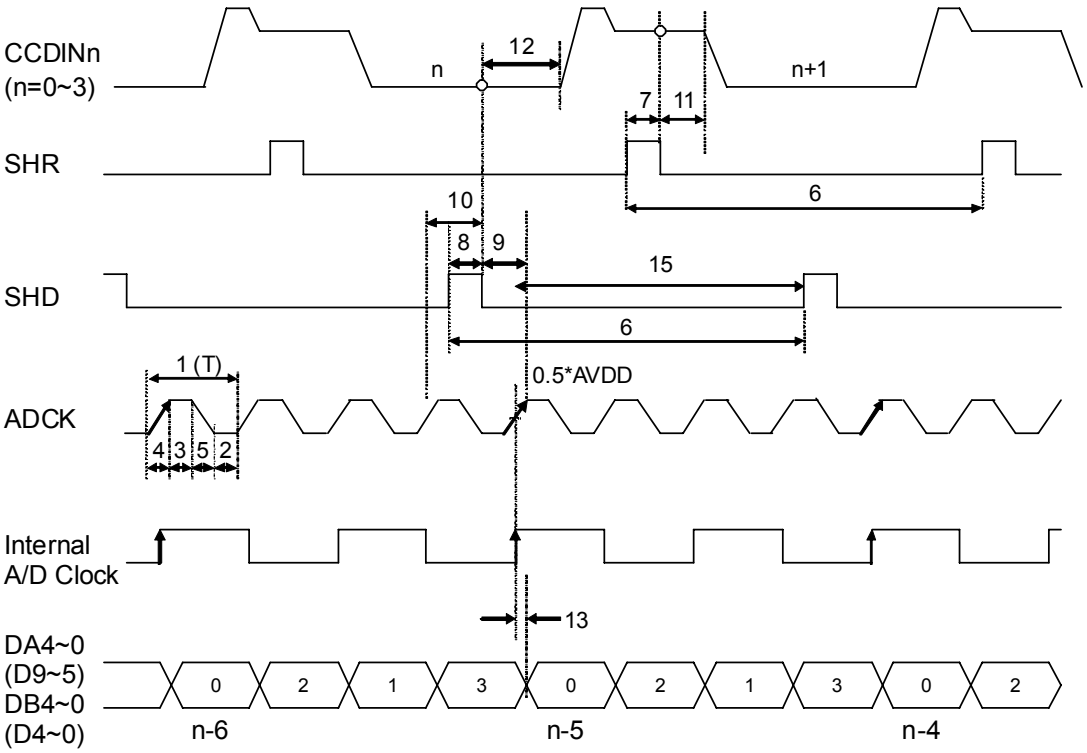
■ Timing Diagrams(16): ADCK frequency = total pixel rate mode (10 Bit-wide output)

- 4 channel mode (CDS mode & Clamp mode, negative polarity)

Please refer to Switching Characteristics 4 table.



Timing Diagrams in 4 channel mode

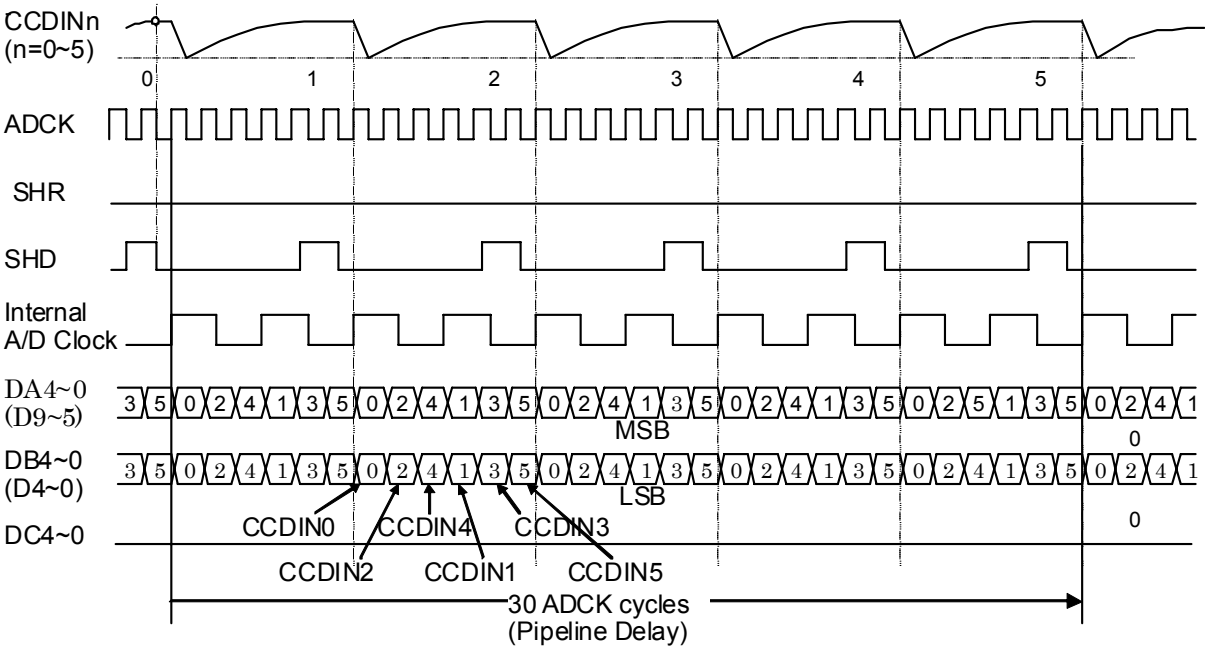


Detailed Timing Diagrams in 4 channel mode

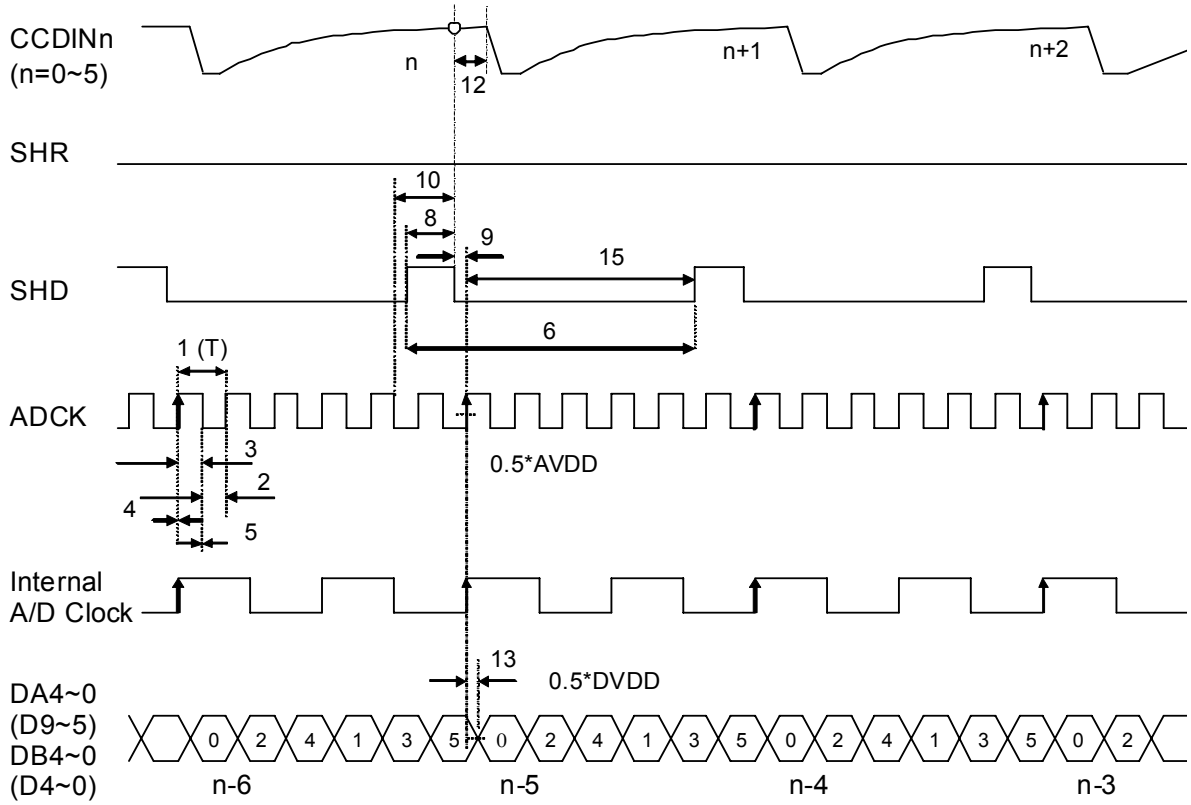
■ Timing Diagrams(17): ADCK frequency = total pixel rate mode (10 Bit-wide output)

- 6 channel mode (DC direct-coupled mode, positive polarity)

Please refer to Switching Characteristics 3 table.



Timing Diagrams in 6 channel mode

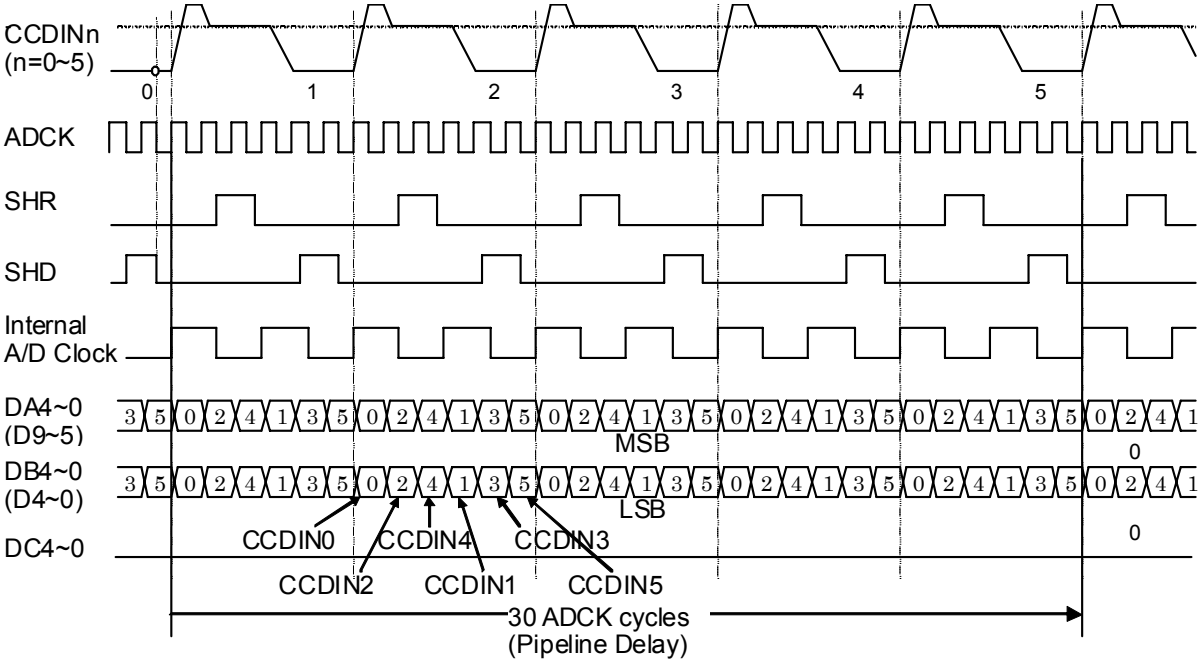


Detailed Timing Diagrams in 6 channel mode

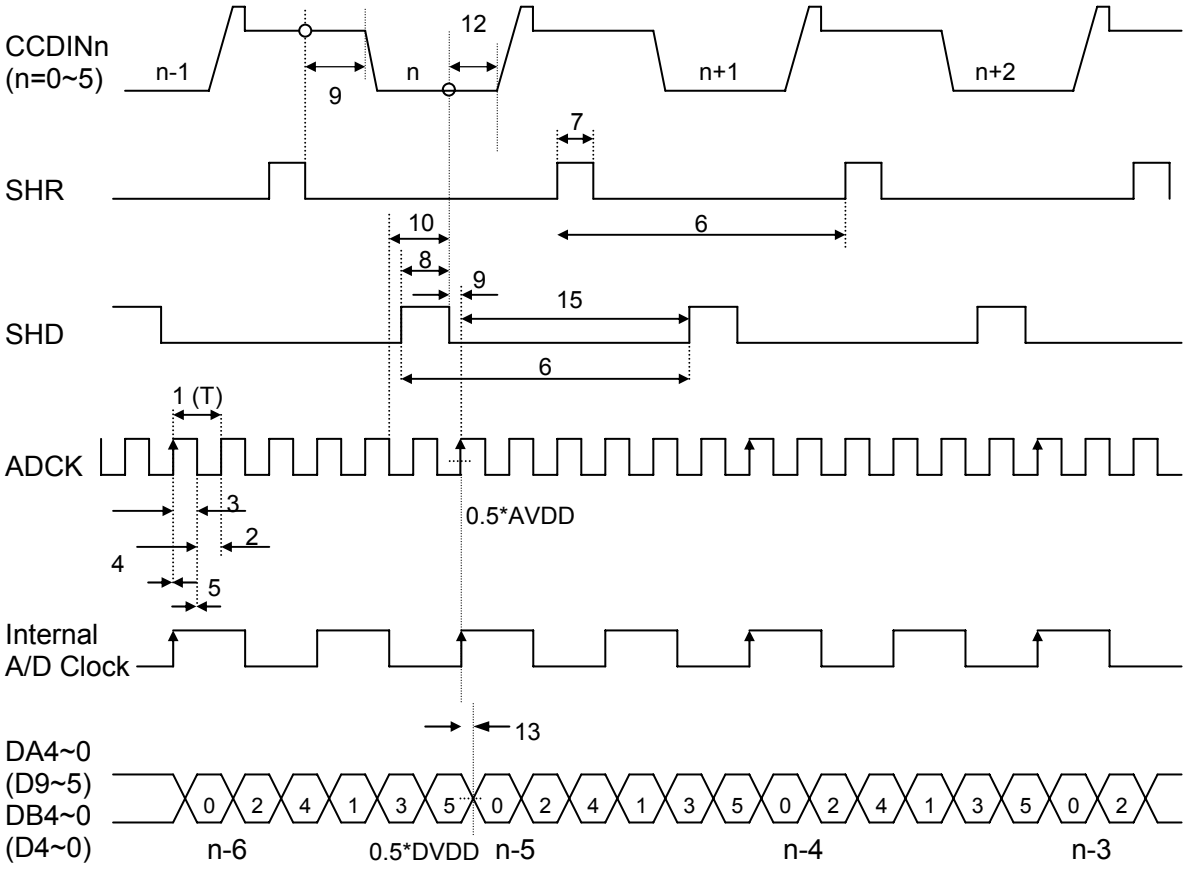
■ Timing Diagrams(18): ADCK frequency = total pixel rate mode (10 Bit-wide output)

- 6 channel mode (CDS mode & Clamp mode, negative polarity)

Please refer to Switching Characteristics 4 table.



Timing Diagrams in 6 channel mode



Detailed Timing Diagrams in 6 channel mode

■ Switching Characteristics : Serial I / F

(AVDD = 3.0 ~ 3.6 V, DVDD = 3.0 ~ 3.6 V, Ta = 0 ~ 70 °C)

Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit	Condition
Clock Cycle	Scyc	SDCLK			10	MHz	
Clock Pulse Width (" H " period)	Shi	SDCLK	40			ns	
Clock Pulse Width (" L " period)	Slo	SDCLK	40			ns	
Set-up Time (time to SDCLK)	Ssu	SDIN SDENB	20			ns	
Hold Time (time from SDCLK)	Sh	SDIN SDENB	20			ns	
Rise Time of SDCLK, SDENB	Sr	SDCLK SDENB			6	ns	0.3 AVDD →0.7 AVDD
Fall Time of SDCLK, SDENB	Sf	SDCLK SDENB			6	ns	0.3 AVDD →0.7 AVDD
SDENB High Level Pulse Width	Sdw	SDENB	40			ns	
Data delay time (time from SDCLK)	Sdly	SDOUT			30	ns	
Data Hold Time (time from SDENB)	Shld	SDOUT	0			ns	
Number of Serial Data	Snum	SDCLK		16			

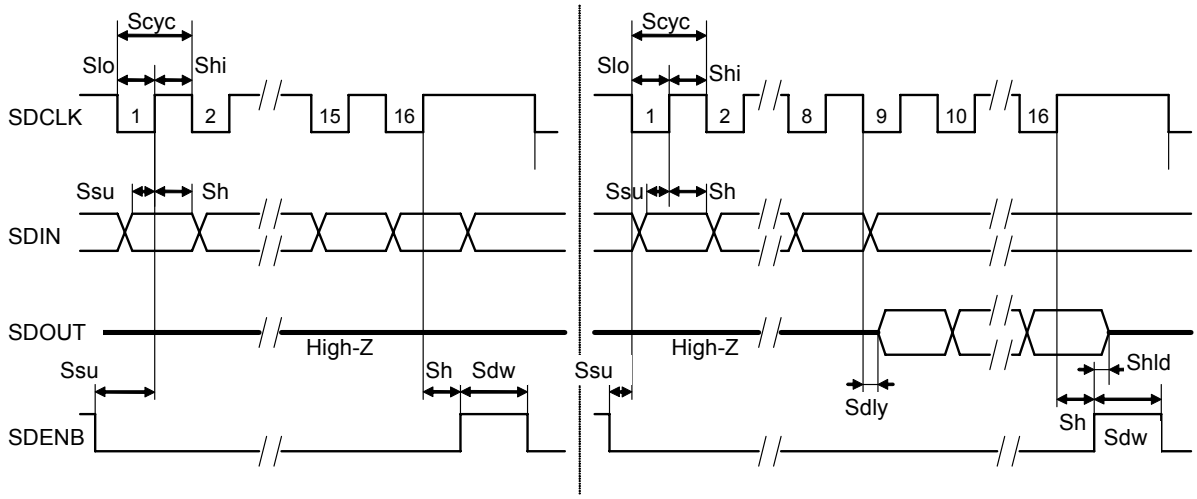


Figure 2

Write to AK8448 Read from AK8448

Control Registers

Address (Hex)	Data								
	Initial (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0	00	Sensor Mode	Interface	Signal Polarity	Channel Number			ADCK Freq.	Power Down
1	00	SHR SHD Polarity	Output as Power Down	Test pattern output	0	Output Data Width	Order of Channel 0 and 1	Order of Channel 2 and 3	Order of Channel 3 and 4
2	80	Offset Data for CCDIN0							
3	80	Offset Data for CCDIN1							
4	80	Offset Data for CCDIN2							
5	80	Offset Data for CCDIN3							
6	80	Offset Data for CCDIN4							
7	80	Offset Data for CCDIN5							
8	00	PGA Gain Data for CCDIN0							
9	00	PGA Gain Data for CCDIN1							
A	00	PGA Gain Data for CCDIN2							
B	00	PGA Gain Data for CCDIN3							
C	00	PGA Gain Data for CCDIN4							
D	00	PGA Gain Data for CCDIN5							
E	08	TEST							
F	00	TEST							

In this data sheet, R0 indicates a register at address 0, for example.
R0, D0 description means, D0 bit of register at address 0.
Each bit of registers to be described in the following is set to a condition as noted to be default after the reset.

☐ R0 Register

■ R0, D7-D6 Sensor I/F mode

D7	D6	Sensor Interface Mode
0	0	DC direct-coupled (default)
0	1	CDS
1	0	Clamp

■ R0, D5 Signal polarity

D5	Signal Polarity	Sensor Type
0	Negative	Signal swings to low voltage side from the reference level. CCD sensors etc. (default)
1	Positive	Signal swings to high voltage side from the reference level. CIS sensors etc.

■ R0, D4 ~ D2 Cannel Number

D4	D3	D2	Cannel Number	CCDIN					
				0	1	2	3	4	5
0	0	0	1(default)	○	-	-	-	-	-
0	0	1	2	○	-	○	-	-	-
0	1	0	3	○	-	○	-	○	-
0	1	1	4	○	○	○	○	-	-
1	0	0	6	○	○	○	○	○	○

○: denotes input channel(s) to be used in the selected # of channel mode.

Un-used functional blocks, CDS, DAC, PGA and ADC are automatically powered-down.

No capacitor connection is required on CCDINn & REFINn pins for the un-used channels. Those, un-used pins should be connected to AVSS.

■ R0, D1 ADCK Frequency

D1	ADCK Input Frequency	Note
0	A/D Conversion Rate (default)	Either 5 Bit-wide or 10 Bit-wide output data is output both at the rising edge and the falling edge of ADCLK.
1	Total Pixel Rate	10 Bit-wide output data is output at the rising edge of ADCK.

In the default mode, ADCK at the same frequency as ADC conversion rate should be input.

ADC data is output both at the rising edge and the falling edge of ADCK.

In total pixel rate mode, ADCK at the same frequency as a total sum of pixel rate of effective channels should be input. ADC data is output at the rising edge of ADCK.

■ R0, D0 Power-Down

D0	Operation
0	Normal Operation (default)
1	Power-Down

In Power-down mode, clock feed to the Digital part is stopped while Analog part is powered-down.

ADC data output conditions (DA0 ~ DA4, DB0 ~ DB4, DC0 ~ DC4) at power-down can be selected to be either fixed low or high-Z output by D6 bit of register R1.

☐ R1 Register

■ R1, D7 SHR, SHD Polarity Select

D7	Polarity
0	Active High (default)
1	Active Low

All diagrams shown in this data sheet are when SHR and SHD polarities are set at default conditions (active high).

■ R1, D6 Output Conditions at Power-Down

D6	Output conditions
0	Fixed to low (default)
1	High Z

R1, D5 Test pattern output

D5	Output
0	Normal (default)
1	Test pattern output

10-bit increment pattern is outputted at test pattern output.
（0,1,2,3,･･･,1022,1023,0,1,2,3,･･･）

■ R1, D3 Output Data width

D3	Output Data width
0	5 Bit (default)
1	10 Bit

When the setting of ADCK frequency is equal to total pixel rate mode (R0, D1 = 1), output data is output in 10 Bit-wide mode, regardless of output data width setting.

■ R1, D2-D0 Channel Processing Order

D2	Channels 0, 1 Processing Order
0	CCDIN0 → CCDIN1 → CCDIN0 → CCDIN1 (default)
1	CCDIN1 → CCDIN0 → CCDIN1 → CCDIN0 …

D1	Channels 2, 3 Processing Order
0	CCDIN2 → CCDIN3 → CCDIN2 → CCDIN3 (default)
1	CCDIN3 → CCDIN2 → CCDIN3 → CCDIN2 …

D0	Channels 4, 5 Processing Order
0	CCDIN4 → CCDIN5 → CCDIN4 → CCDIN5 (default)
1	CCDIN5 → CCDIN4 → CCDIN5 → CCDIN4 …

This is to select the processing order of corresponding input channel pair of the selected, single ADC. Processing order can be individually set at every pair.

This register is valid either in 4 channel mode / 5 Bit-wide output or 6 channel mode / 5 Bit-wide output.

All diagrams shown in this data sheet are when the channel processing order is set at default condition.

☐ R2~R7 Registers

■ D7-D0 Offset Data

D7-D0 (Straight Binary)	Offset Voltage	At Negative Mode	At Positive Mode
11111111	–298.7mV	Maximum Shift to White Level Side (ADC code large) ↑ Maximum Shift to Black Level Side (ADC code small)	Maximum Shift to Black level side (ADC code small) ↓ Maximum Shift to White Level Side (ADC code large)
11111110	-296.3mV		
:	:		
10000001	–2.4mV		
10000000 (default)	0mV		
01111111	2.4mV		
:	:		
00000001	298.7mV		
00000000(Inhibition)	(298.7mV)		

$$Offset(x) = \frac{298.7}{127} \times (128 - x) \quad mV \qquad 0 \leq x \leq 255$$

Default x=128

☐ R8~RD Registers

■ D7-D0 PGA Gain Data

Setting code and gain (ideal value) relation is expressed in the following equation.

$$Gain(x) = \frac{2 \times 208}{33.3 + 255 - x}$$ Where x is register set value (0 < = x < = 255)

At default x = 0

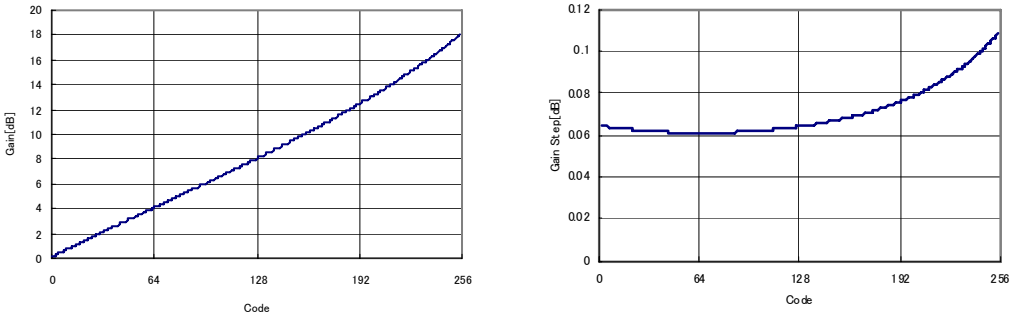


Figure 3 PGA Gain Curves (ideal values)

Operations

■ Sensor I/F Mode

AK8448 has three sensor interface modes: CDS, Clamp and DC connect. The sensor interface mode is selected by Sensor Interface Mode register R0, D7~D6.

- CDS mode

A mode to process the difference Vpix as its pixel level which is between the reference level Vprec of each pixel from the sensor output signal and its data level Vdata.
Reference level of the sensor signal is sampled at SHR and data level of the sensor signal is sampled at SHD respectively.
Sampling point is at the falling edge of SHR and SHD respectively.
When polarity of SHR and SHD is inverted by register (R1, D7 = 1), the sampling point becomes at the rising edge.

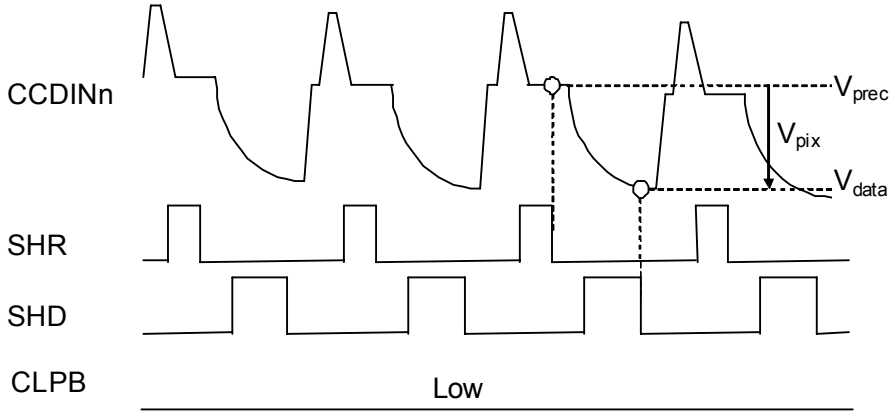


Figure 4 CDS Mode Timing Outline

- Clamp mode

A mode to process the difference Vpix as its pixel level which is between the internally generated Clamp level Vclamp and data level Vdata of the sensor output signal.
Data level of the sensor signal is sampled at SHD.

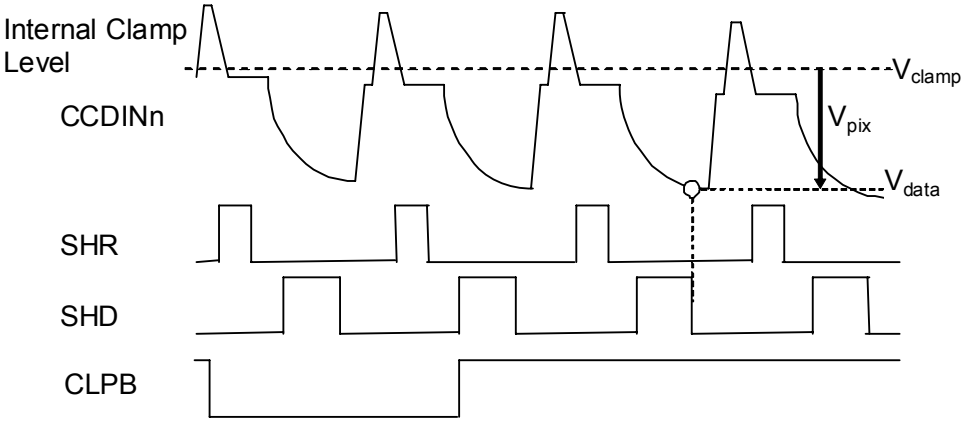


Figure 5 Clamp Mode Timing Outline

- DC direct-coupled mode

A mode to process a difference Vpix as its pixel level which is between a reference level fed on REFINn pin externally, and data level Vdata of the sensor output signal.
When no reference level exists in sensor output signal, this mode is used as an example. Data level of the sensor signal is sampled at SHD. Since SHR is not used, connect it to either Low or High.

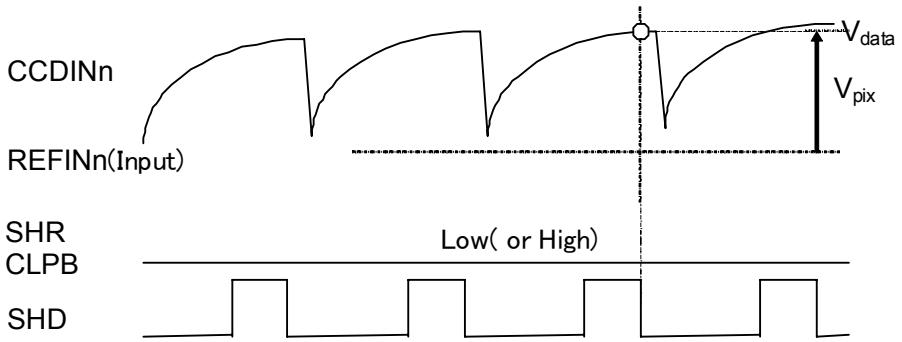


Figure 6 DC Direct-coupled Mode Timing Outline

■ Clamp Operation

In CDS mode and Clamp mode, Clamping is made in order to adjust the reference DC level of sensor signal to match the internal reference level of the AK8448.

Clamp operation is controlled by CLPB and SHR.

Clamp switch closes during CLPB = Low and SHR = High (" Low " when SHR, SHD polarities are inverted), and CCDINn (n = 0 ~ 5) pin signal is pulled toward the internal clamp level.

REFINn (n = 0 ~ 5) is also clamped in the same way.

In CDS mode, fix CLPB to low so that clamping is always enabled.

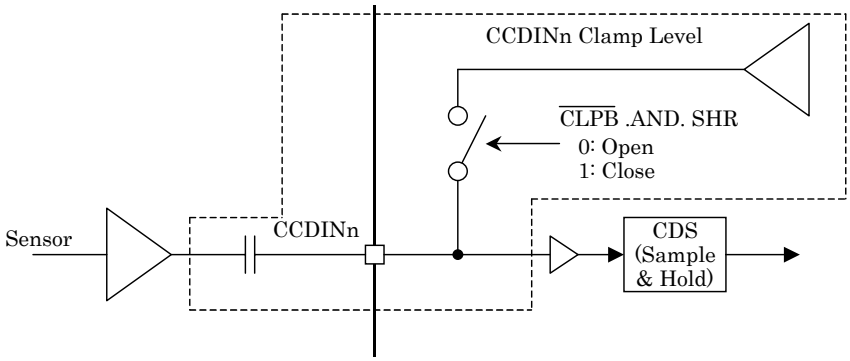


Figure 7 Clamp Circuit Outline

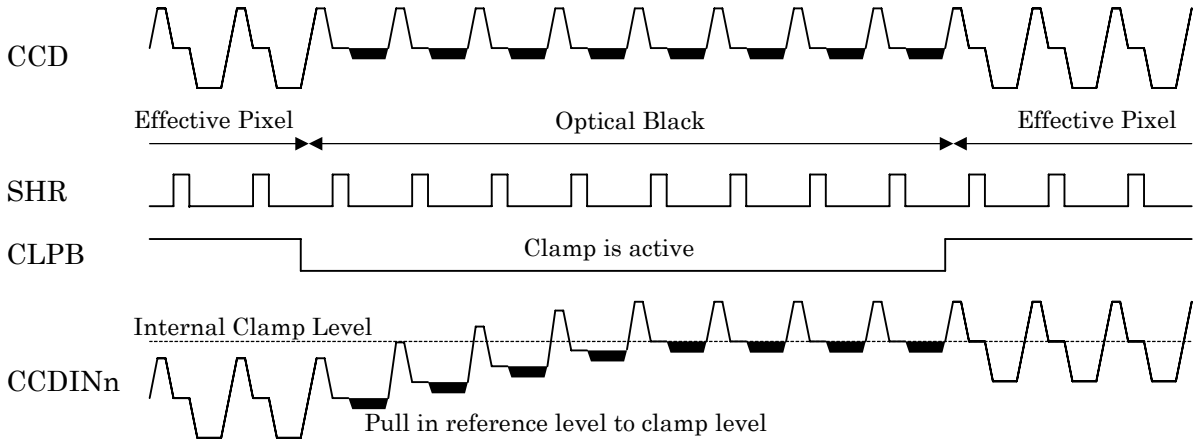


Figure 8 Clamp Operation Timing Outline

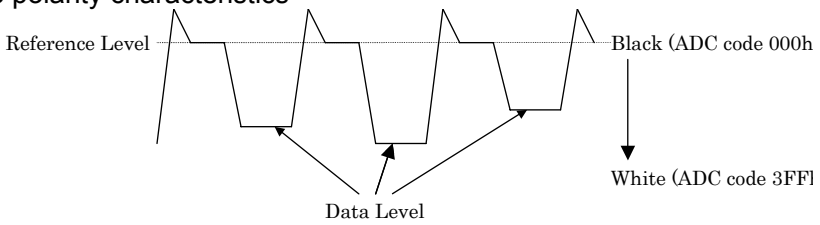
■ Signal Polarity

The AK8448 accepts both positive and negative input polarities.

Either signal polarity is selected by setting Signal Polarity register (R0,D5) to meet sensor types to be used.

In general, CCD exhibits negative polarity characteristics and CIS exhibits positive polarity characteristics. Either polarity can be selected, regardless of sensor I/F mode setting.

- Negative polarity characteristics



- Positive polarity characteristics

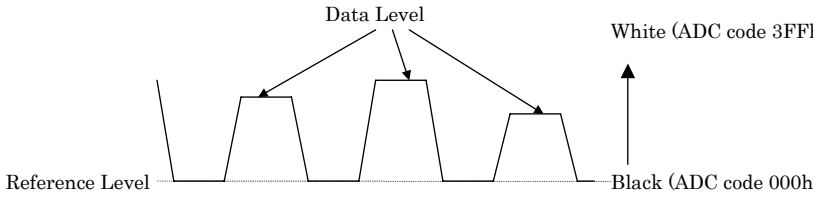


Figure 9 Signal Polarities

■ Output Data Control

ADC output data is output in either 5 Bit-wide or 10 Bit-wide by setting Data Width register (R1, D3).

When 5 Bit-wide data mode is selected, data is output on each of three 5 Bit buses – DA4 ~ DA0, DB4 ~ DB0 and DC4 ~ DC0 respectively which correspond to each ADC.

When 10 Bit-wide data mode is selected, data is output on 10 pins – DA4 (MSB) ~ DA0 and DB4 ~ DB0 (LSB).

In 5 Bit-wide data mode, the upper 5 Bit of data is output at the rising edge of ADCK, and the lower 5 Bit at the falling edge of ADCK.

In 10 Bit-wide data mode, two different channel data are output at the rising edge and at the falling edge of ADCK respectively.

It is also possible to output data at only the falling edge of ADCK in 10 Bit-wide data mode, by setting ADCK Frequency register (R0, D1).

In this operation, it is required to input ADCK at the frequency of a total sum of pixel rate of all channels (total pixel rate). Un-used buses DB4 ~ DB0 and DC4 ~ DC0 such as a case in 1 channel mode with 5 Bit-wide output, will output Low levels.

■ ADCK

A/D Conversion Rate mode and Total Pixel Rate mode

ADCK generates ADC conversion timing and ADC data output timing.

Whether to output data at both the rising edge and the falling edge of ADCK or to output data at only the rising edge can be selected by ADCK Frequency mode register.

A/D conversion rate mode is a mode where data is output at both the rising edge and the falling edge of ADCK.

In A/D conversion rate mode, input an ADCK clock of same frequency as ADC conversion rate.

Total pixel rate mode is a mode where data is output at only the ADCK rising edge. In this mode, input an ADCK clock of same frequency as a total sum of effective channels' pixel rates.

For example, when to process a 20 MHz / channel sensor signal in 3 channel mode, a 20 MHz ADCK is input in A/D conversion rate mode which is equal to ADC conversion rate.

Maximum Conversion Rate

Maximum operating speed of ADC data output buffers DA0 ~ DA4, DB0 ~ DB4, DC0 ~ DC4 is designed to be 80 Mbps.

When a total pixel rate mode is selected as ADCK frequency mode, maximum sampling rate per channel in 3 channel and 6 channel modes is limited by this output buffer speed.

For example, maximum conversion rate in 6 channel mode is 80 MSPS / 6 = 13.3 MSPS per channel, and not 20 MSPS.

Number of channels and its ADCK frequency, a possible data width combination and its maximum conversion rate per channel are listed in the following table.

[CDS, Clamp mode]

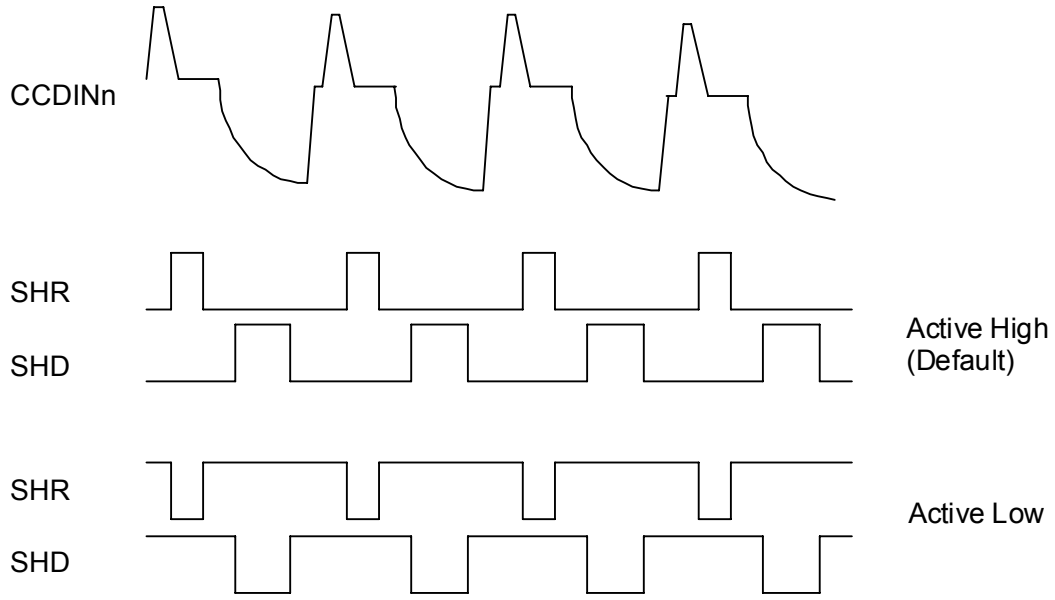
	A/D Conversion Rate Mode			Total Pixel Rate Mode		
# of Channels	5 bits Width	10 bits Width	Maximum Conversion Rate [SPS/CH]	5 bits Width	10 bits Width	Maximum Conversion Rate [SPS/CH]
1	○	○	40M	-	○Note1	40M
2	○	○	40M	-	○	40M
3	○	-	40M	-	○	26.6M
4	○	○	20M	-	○	20M
6	○	-	20M	-	○	13.3M

[DC Direct mode]

	A/D Conversion Rate Mode			Total Pixel Rate Mode		
# of Channels	5 bits Width	10 bits Width	Maximum Conversion Rate [SPS/CH]	5 bits Width	10 bits Width	Maximum Conversion Rate [SPS/CH]
1	○	○	15M	-	○Note1	15M
2	○	○	15M	-	○	15M
3	○	-	15M	-	○	15M
4	○	○	15M	-	○	15M
6	○	-	15M	-	○	13.3M

Note1: A/D conversion rate mode and total pixel rate mode have same timing waveforms in 1 channel / 10 Bit-wide output operation. Please use A/D conversion rate mode at the default state.

■ SHR/SHD Polarity



SHR/SHD polarity can be changed by register R1 Register.

Serial I / F

Write operation into and Read operation from Control registers are executed via a 4 – wire Serial Interface.

SDIN data while SDENB is at low is taken at the rising edge of SDCLK.

When the starting bit of SDIN data is " zero ", writing into register is made and when it is " one ", reading from register is made.

The second and the third bits (C1, C0) correspond to CE1 and CE0 pin data respectively and only when logical levels are at C1 = CE1 and C0 = CE0, either write in or read out operation is enabled.

The fourth bit must be zero.

Bits from the fifth to the eighth are for register address. MSB is the fifth bit and LSB is the eighth bit.

Bits from ninth to sixteenth are data for register. MSB (= D7) is the ninth bit and LSB (= D0) is the sixteenth bit.

■ Reset

Register values at the power-up are indeterminate including registers for test.

In order to avoid test registers from disturbing normal operation, a reset should be made right after the power-up.

When RESETB pin is set to low, each register is set to its default value while test registers are set to necessary values for normal operation.

Low duration time of RESETB should be 100 ns and longer.

Return RESETB pin to high after the reset, and necessary value should be written to each register. When reset is not made after power-up, write default values into test registers.

■ Power-Down

The AK8448 enters power-down mode when operation mode register R0,D1 is set at " 1 ". In power-down mode, supplying operation clock to Digital part is also stopped while current supply to Analog part is ceased.

When returning to normal operation from power-down mode (R0, D0 = 0), a wait time is required so that VCOM (reference voltage) is stabilized to its normal voltage since VCOM is made to 0 V at power-down.

Serial Interface

■ Writing into the AK8448

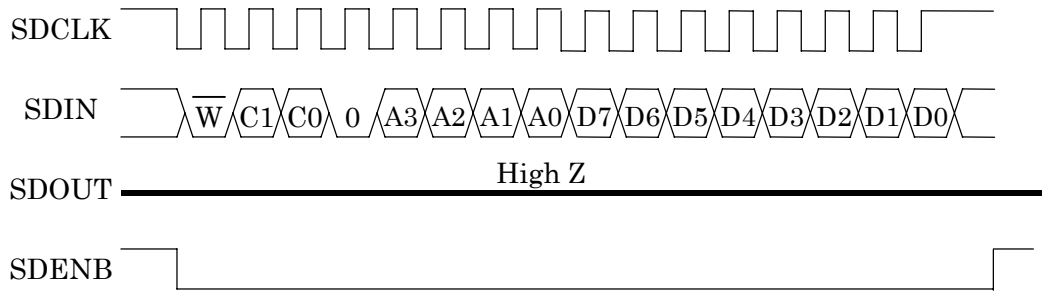


Figure 10 Write Into Register

■ Reading from the AK8448

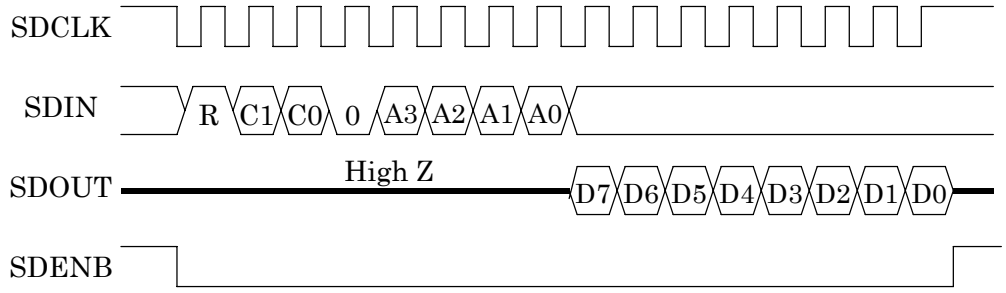
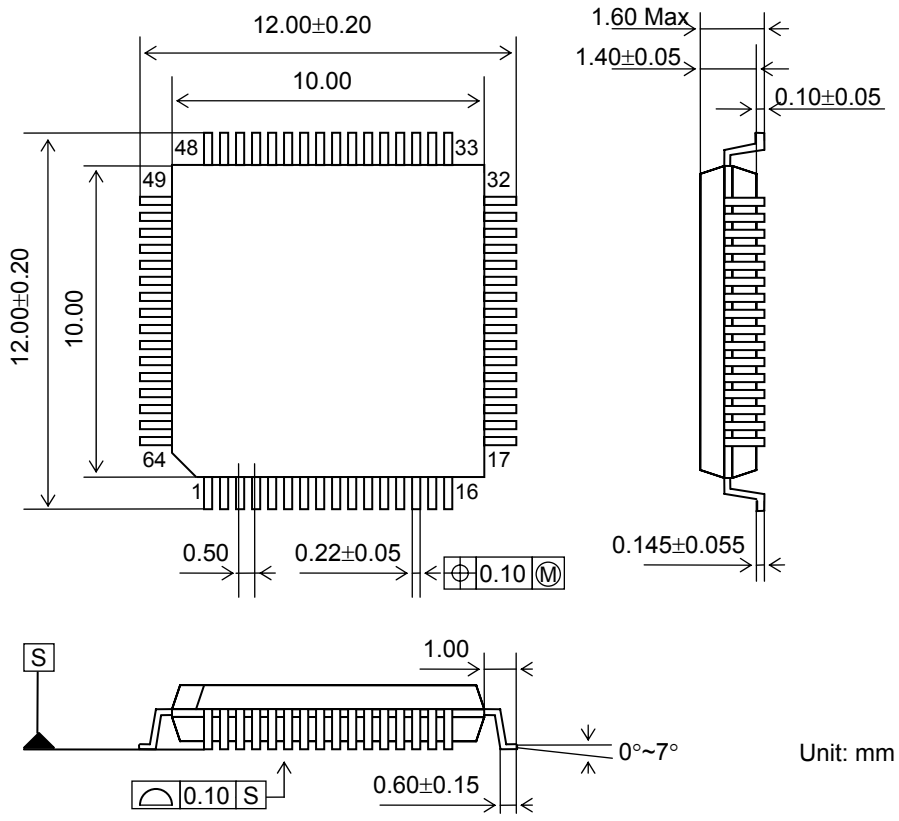


Figure 11 Read From Register

Package Outline Dimensions



Package Marking

(1) Pin # 1 identifier (The chamfered corner indicates pin number 1)

(2) Marketing code : AK8448VQ

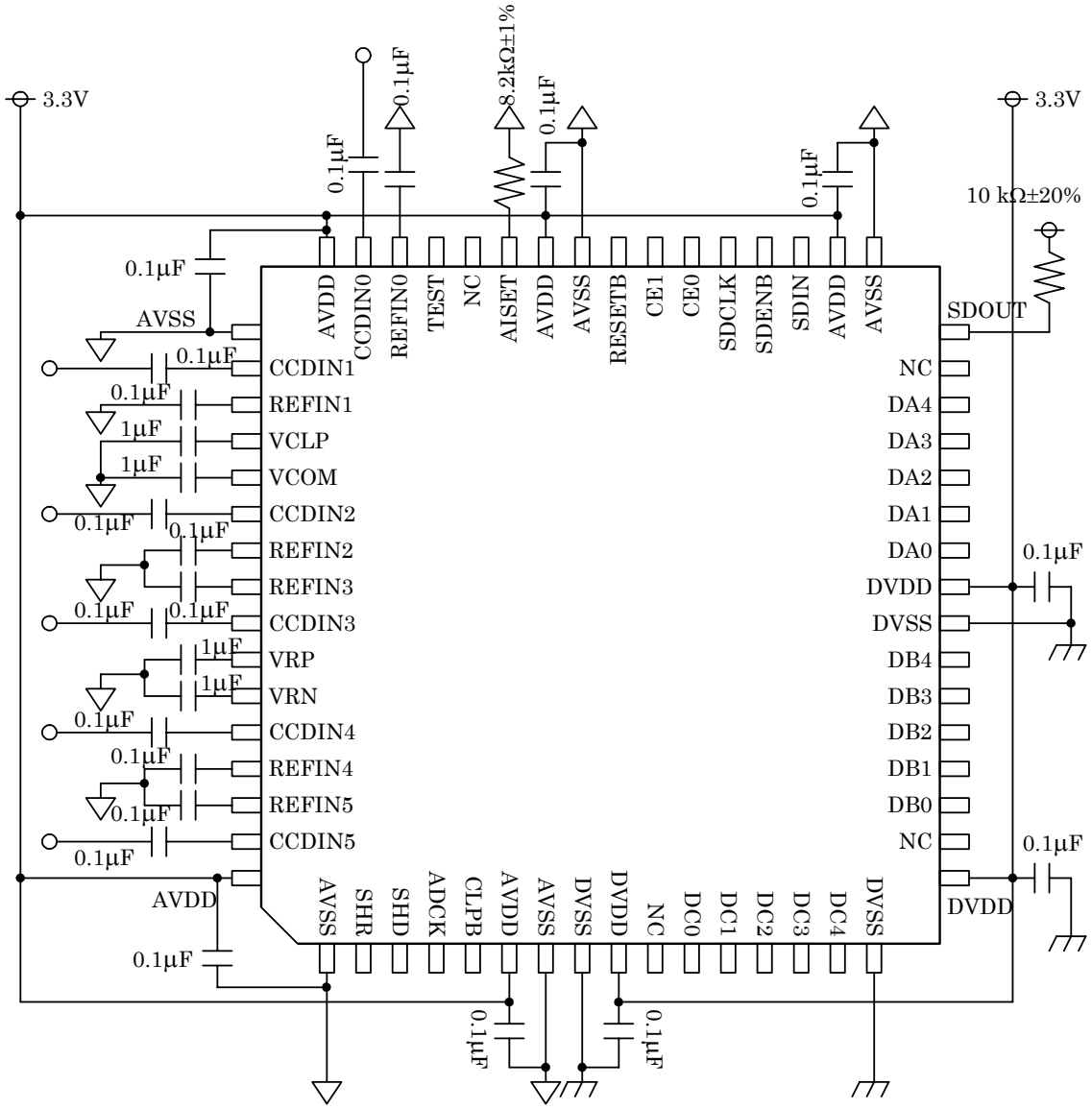
(3) Date code : xxxxxxx (7 digits)

Upper 4 digits : week code

Lower 3 bits : AKM's control code

External Circuit Examples

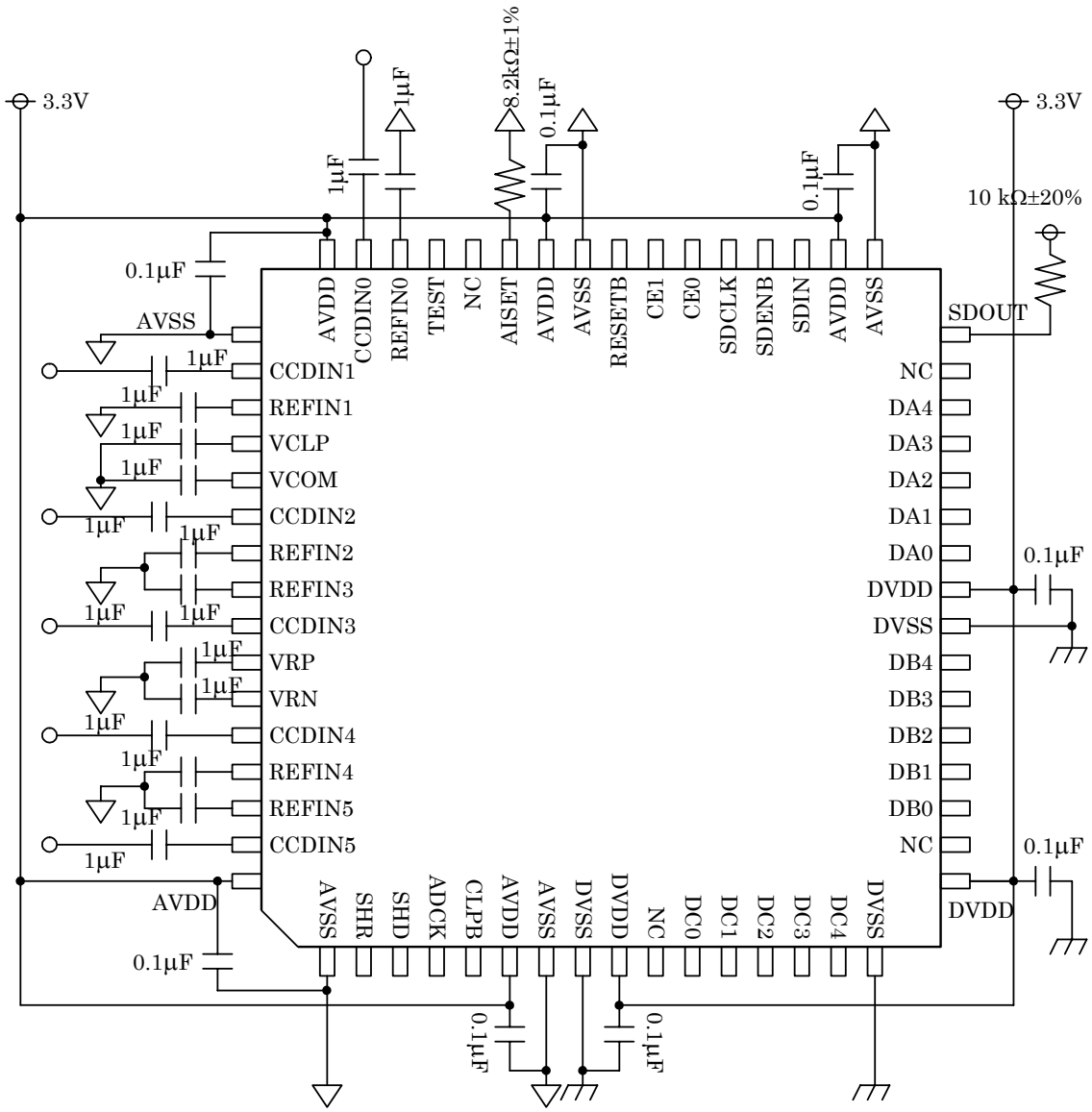
■ CDS Mode



Above example is for reference. Please select optimum capacitor values for a target system.

Figure 12 CDS Mode

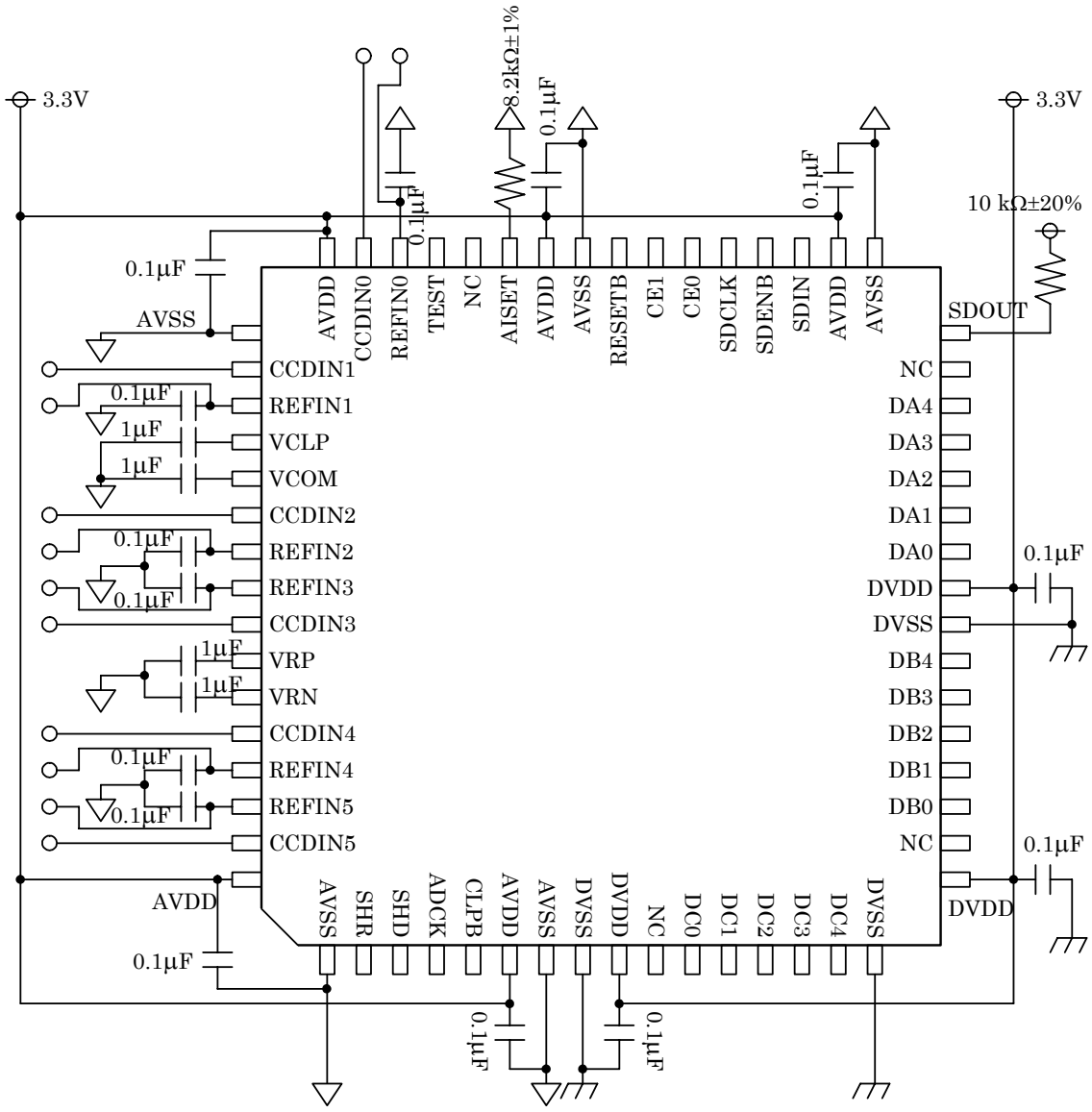
■ Clamp Mode



Above example is for reference. Please select optimum capacitor values for a target system.

Figure 13 Clamp Mode

■ DC Direct-coupled Mode



Above example is for reference. Please select optimum capacitor values for a target system.

Figure 14 DC Direct-Coupled Mode

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