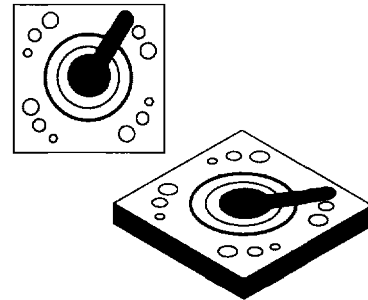
Alpha

Universal Chip Mixer and Detector Schottky Barrier Diodes

CDX76XX, CME7660

Features

- For Microwave MIC Assembly
- Mechanically Rugged Design Exceeds MIL 883 Wire Bond Specifications for Hybrid Assembly
- Optimized Barrier Heights for Mixer and Detector Applications
- Wide Range of Capacitances Available
- High Frequency Design
- Both "N" and "P" Type Silicon Semiconductor Material Available
- Ergonometric Design for Increased Production Line Throughput
- Large 4 Mil Diameter Bond Pad for Improved Bondability



Maximum Ratings

Tstg:	–65°/+175°C
Top:	–65°/+150°C
Pdiss CW:	100 mW
I max:	75 mA
PIV:	2.0 – 3.0 @ 10 μA

Description

The "Universal Chips" are designed for a high degree of device reliability in both commercial and industrial uses. The offset bond pad assures that no mechanical damage will occur at the junction during the wire bonding. Additionally the 4 mil bond pad eliminates performance variation due to bonding and is ideal for automated assembly, and improves efficiency during manual operations as well.

The choice on "N" and "P" type silicon allows for the designer to optimize the silicon material for the intended application.

- Doppler mixers, high sensitivity detectors will benefit from using the low noise characteristics of the "P" type silicon.
- Low conversion loss mixers and biased detectors can be designed using standard "N" type material.

Electrical Specifications

Zero Bias Detector (High Sensitivity Detector)

Outline Drawing: 526–006

Part Number	Band	Drive Level	VF (mV) 1mA	Cj (pF) 0V, 1 mHz	RT (Ω) 1.0 mA	VB (V) 1.0 mA	TSS[5] (dBm)	ZV[3] (k Ω)	γ[4][µV] [µW]
CDC7622	K	Zero Bias	180 300	0.1	30 – 80	2 0	–50	6 – 15	10000

"P" Type Mixer and Detector, Low Noise, Doppler

Outline Drawing: 526–006

Part Number	Band	Drive Level	VF (mV) 1mA	Cj (pF) 0V, 1 mHz	RT (Ω) 10 mA	VB (V) 10 µA	TSS (dBm)	ZV[1] (k Ω)	γ[2][µV] [µW]
CDB7619	K	Low	300 450	0.1	40	3.0	–48	2.8	5000
CDB7620	KU	Low	250 350	0.5 – 0.15	30	2.0	–46	2.8	8000

"N" Type Mixer and Detector

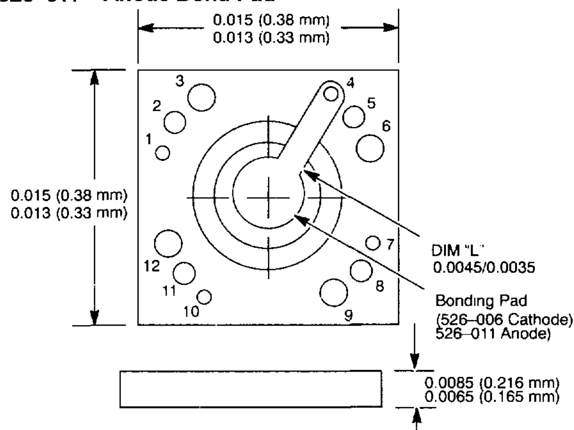
Outline Drawing: 526–011

Part Number	Band	Drive Level	VF (mV) 1mA	Cj (pF) 0V, 1 mHz	RT (Ω) 10 mA	VB (V) 10 mA
CDF7623	X	Low	240 300	0.15–0.30	10	2.0
CDF7621	K	Low	270 350	0.1	20	2.0
CME7660	KU	Med	350 450	0.05–0.15	10	3.0
CDE7618	K	Med	375 500	0.1	20	3.0
CDP7624	KU	Med/ High	450 575	0.05–0.15	15	3.0

1 Video impedance, 20 µA bias * bias dependent.
2. Voltage sensitivity, 20 µA bias, RL > 100 kΩ.
3. Video impedance at zero bias.
4. Voltage sensitivity at zero bias, RL = > 100 kΩ.
5. Video Bandwidth = 10 MHz.

Outline Drawing

526–006 = Cathode Bond Pad
526–011 = Anode Bond Pad



Assembly and Handling Procedure

Die Attach Methods

All universal chips are compatible with both eutectic and conductive epoxy die attach methods.

Eutectic composition preforms of Au/Sn or Au/Ge are useful when soldering devices in circuit. Gold/silicon eutectic die attach can be accomplished by scrubbing the chip directly to the gold plated bonding area.

Epoxy die attach with silver or gold filled conductive epoxies, can also be used where thermal heat sinking is not a requirement.

Wire Bonding

Two methods can be used to connect wire, ribbon, or wire mesh to the chips:

- Thermocompression
- Ballbonding

Alpha recommends use of pure gold wire (0.7 – 1.25 mil diameter).

Lead Plating	
Junction	DIM "L"
1, 4, 7, 10	0.005 (0.013 mm)
2, 5, 8, 11	0.008 (0.020 mm)
3, 6, 9, 12	0.0012 (0.030 mm)

NOTE: Lead Plating Tolerance = ±10%

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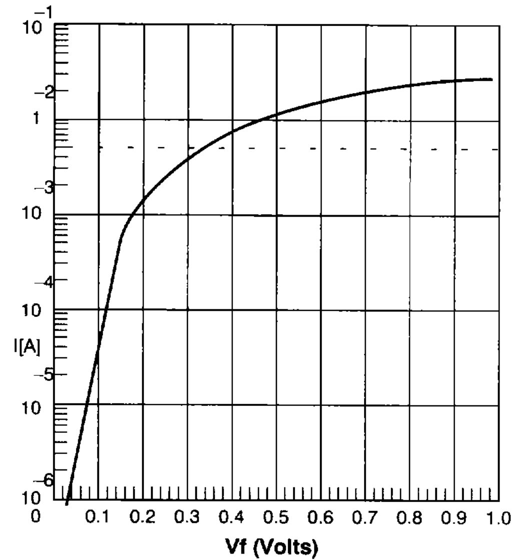
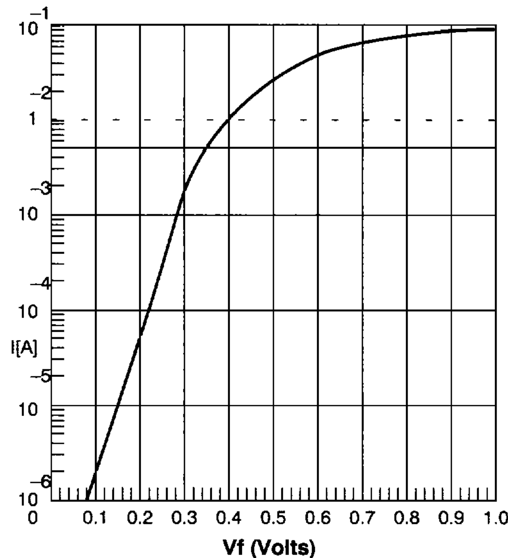
Spice Parameters Matrixes

Parameter	Unit	Part Number		
		CDF7621	CDC7622	CDB7619
I_S	A	8E–08	3E–06	3E–09
R_S	Ohm	6	26	26
n		1.04	1.04	1.04
T_D	s	1E–11	1E–11	1E–11
C_J0	pF	0.11	0.1	0.11
m		0.3	0.25	0.32
E_G	eV	0.69	0.69	0.69
V_J		0.51	0.34	0.54
X_{TI}		2	2	2
FC		0.5	0.5	0.5
B_V	V	2.5	2	3
IBV	A	1E–05	0.001	1E–05

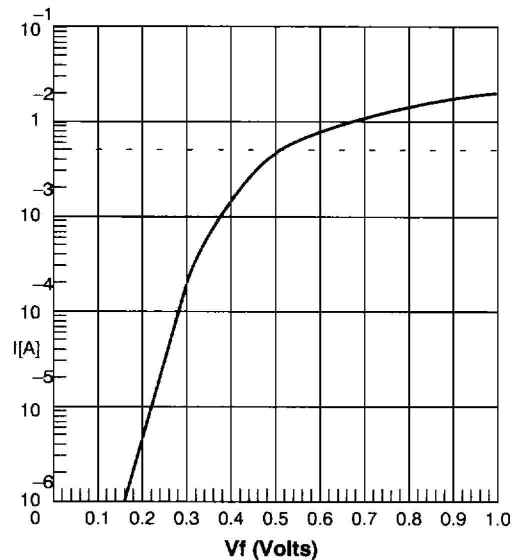


Part Number CDC7622

Performance Data



Part Number CDF7621



Part Number CDB7619

Shipping Information

Individual Chips

Standard packaging procedures at Alpha are for “wafflepack” delivery. Devices can also be package on “GelPack” carriers.

Wafer Shipment for Whole Wafer

Packaging options include delivery for devices on film frame where wafer is sawn on wafer gel pack for uncut, unsawn wafer.