N-Channel Enhancement MOSFET

GENERAL DESCRIPTION

The ME20N03 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦15mΩ@V_{GS}=10V
- $R_{DS(ON)}$ ≦20mΩ @V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

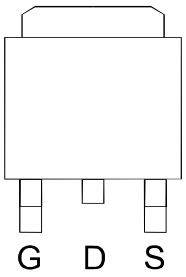
APPLICATIONS

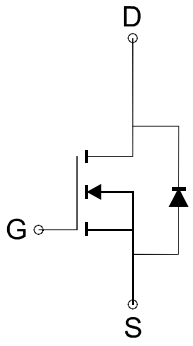
- Power Management in Desktop Computer
- Video Graphic Accelerate Card
- Battery Powered System
- DC/DC Converter

PIN CONFIGURATION

(TO-252)

Top View





N-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit		Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current	T_C=25℃	I_D	39(Note 1)		A
	T_C=100℃		25		
Pulsed Drain Current		I_{DM}	100		A
Maximum Power Dissipation	T_C=25℃	P_D	37		W
	T_C=70℃		24		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient(Note 2)		$R_{\theta JA}$	T≦10 sec	15	℃/W
			Steady State	45	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	3.3		℃/W

Note 1: Bonding wire current limit

Note 2: The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1	2	3	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		V_{DS}=30V, V_{GS}=0V T_J=55℃			5	
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D= 15A		11	15	mΩ
		V_{GS}=4.5V, I_D= 15A		16	20	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.75	1.1	V
DYNAMIC						
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f =1MHz		700	800	pF
Coss	Output Capacitance			120		
Crss	Reverse Transfer Capacitance			35		
Rg	Gate Resistance	V_{DS}=0, V_{GS}=0V, f =1MHz		0.9		Ω
Qg(4.5V)	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=10A		11	14	nC
Qg(10V)	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=10A		20	26	
Qgs	Gate-Source Charge			5		
Qgd	Gate-Drain Charge			4.9		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=15V, R_L =1.5Ω V_{GS}=1A, R_{GEN}=3Ω R_G=6Ω		14	17	ns
t_r	Turn-On Rise Time			12	15	
$t_{d(off)}$	Turn-Off Delay Time			43	55	
t_f	Turn-On Fall Time			4	6	

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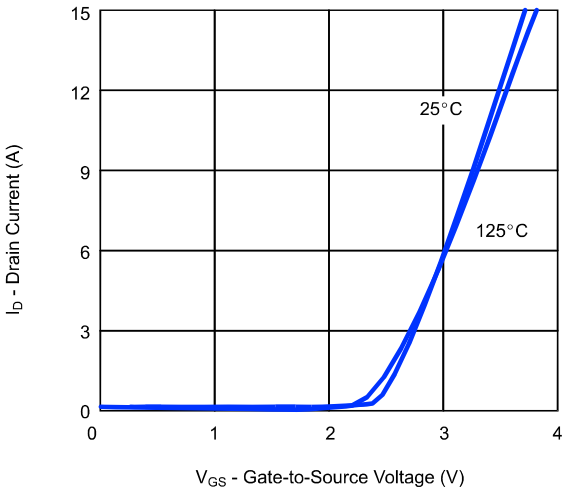
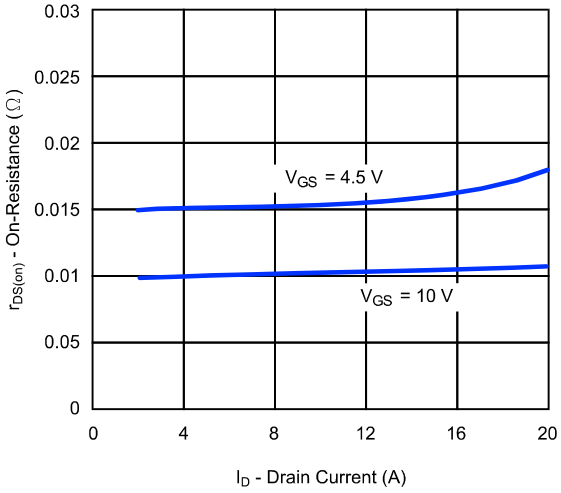
Typical Characteristics (T_J =25℃ Noted)

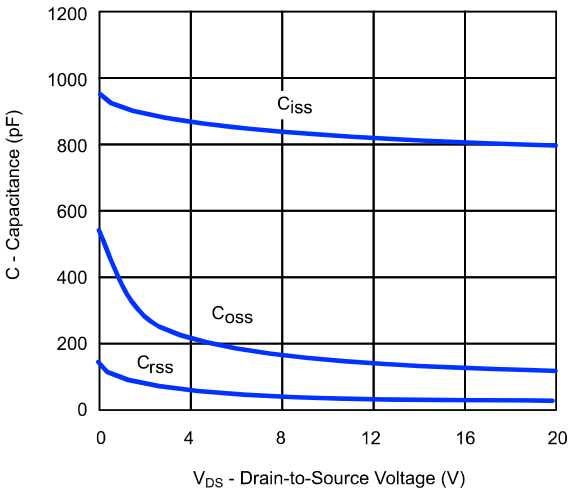
Transfer Characteristics



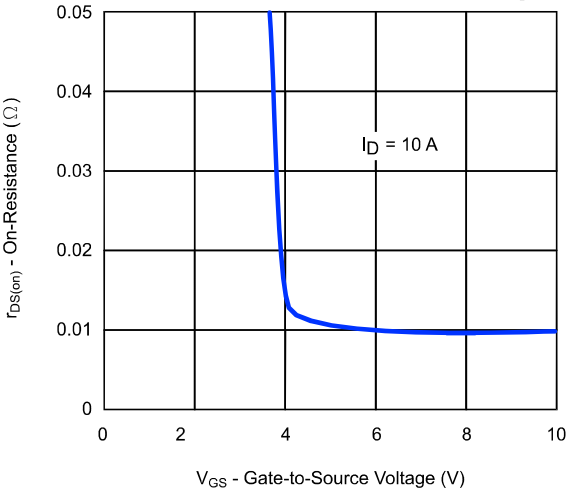
On-Resistance vs. Drain Current



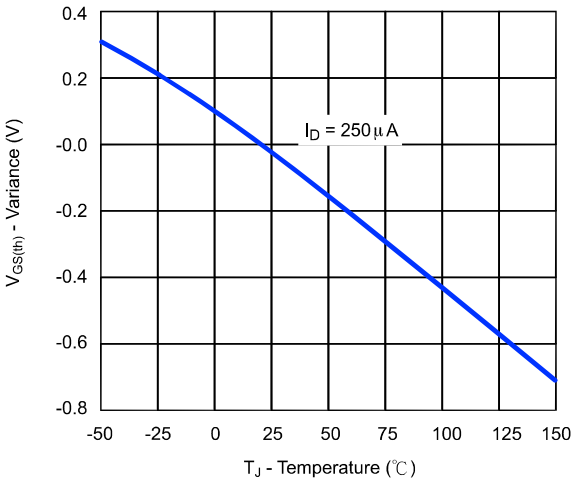
Capacitance



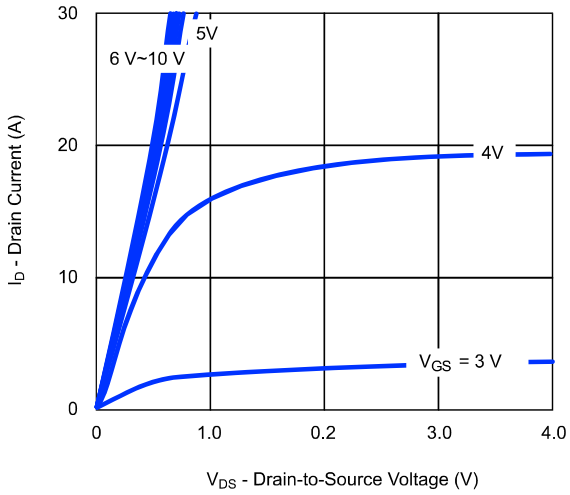
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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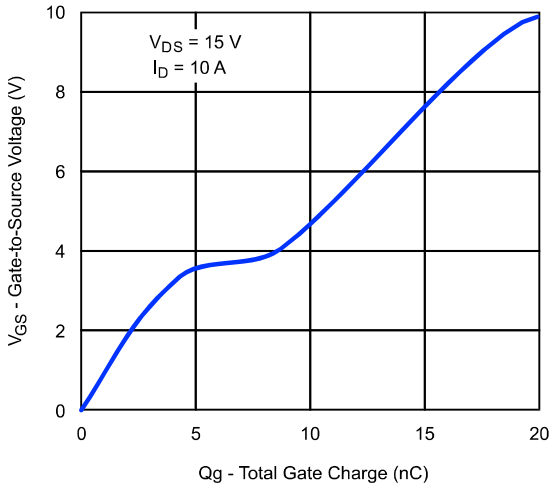
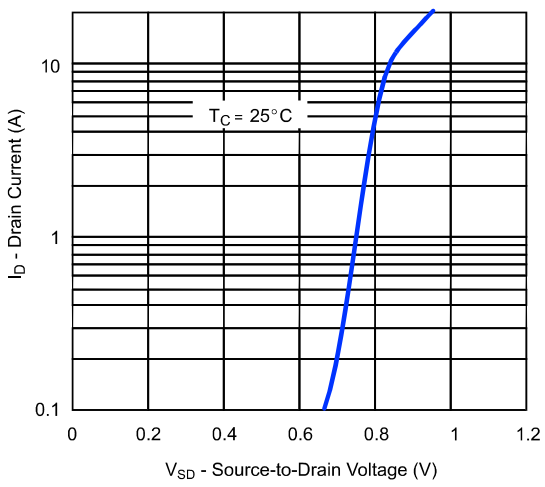
Typical Characteristics (T_J =25℃ Noted)

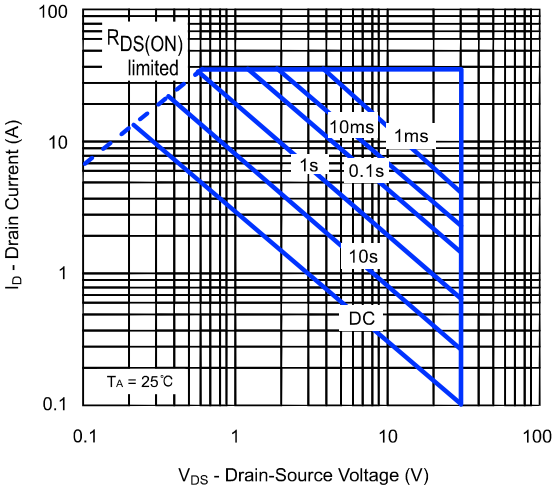
Gate Charge



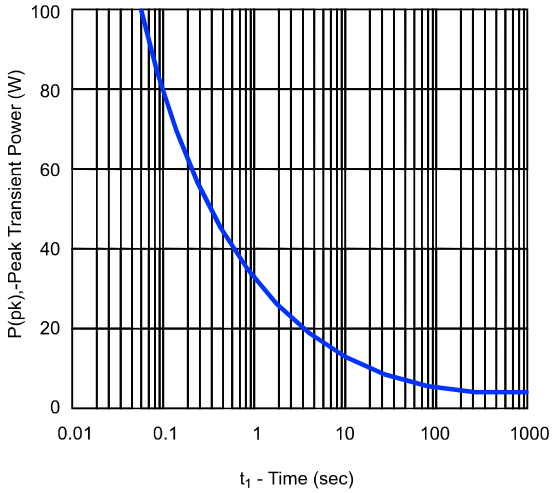
On-Resistance vs. Drain Current



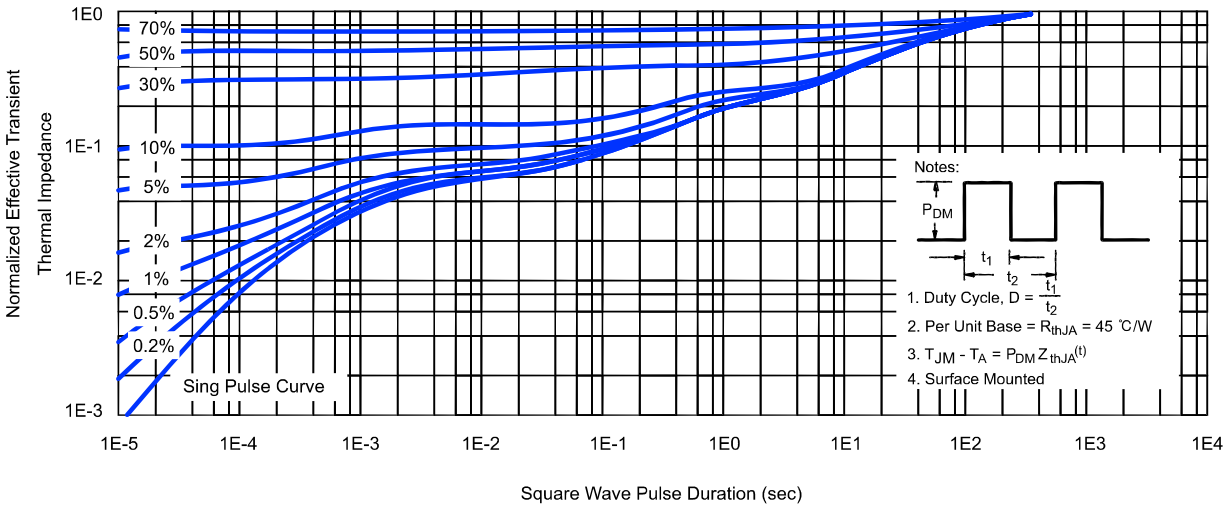
Maximum Forward Biased Safe Operating Area



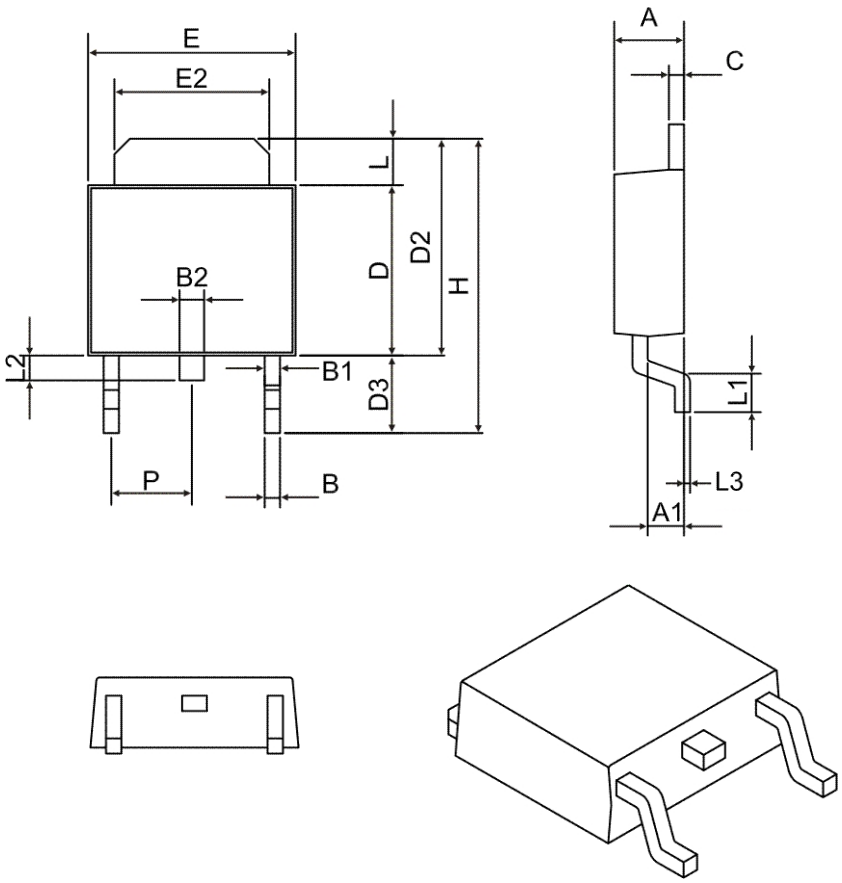
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



TO-252 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	2.00	2.50
A1	0.90	1.30
B	0.50	0.85
B1	0.50	0.80
B2	0.50	1.00
C	0.40	0.60
D	5.20	5.70
D2	6.50	7.30
D3	2.20	3.00
H	9.50	10.50
E	6.30	6.80
E2	4.50	5.50
L	1.30	1.70
L1	0.90	1.70
L2	0.50	1.10
L3	0	0.30
P	2.00	2.80