Data Sheet July 1999 File Number 2325.4

0.5A, 400V, 1.800 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17404.

Ordering Information

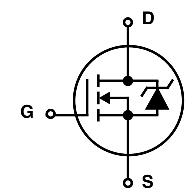
PART NUMBER	PACKAGE	BRAND
IRFD320	HEXDIP	IRFD320

NOTE: When ordering, use the entire part number.

Features

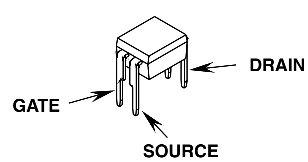
- 0.5A, 400V
- $r_{DS(ON)} = 1.800\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

HEXDIP



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

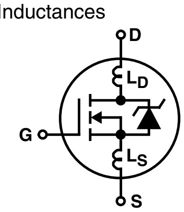
		IRFD320	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	400	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	400	V
Continuous Drain Current	I_D	0.5	A
Pulsed Drain Current (Note 3)	I_{DM}	2.0	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	1.0	W
Linear Derating Factor		0.008	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	100	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

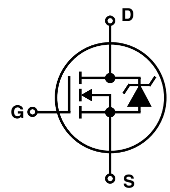
NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 9)	400	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V	0.5	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 0.25A, V_{GS} = 10V (Figures 7, 8)	-	1.5	1.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 10V, I_D = 2.0A (Figure 11)	1.7	2.0	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 0.5 x Rated BV_{DSS}, I_D ≈ 0.5A, R_G = 9.1Ω, V_{GS} = 10V, R_L = 398Ω for V_{DSS} = 200V MOSFET Switching Times are Essentially Independent of Operating Temperature	-	20	40	ns
Rise Time	t_r		-	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	25	50	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 0.5A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = 1.5μA (Figure 13), Gate Charge is Essentially Independent of Operating Temperature	-	12	15	nC
Gate to Source Charge	Q_{gs}		-	6.0	-	nC
Gate to Drain “Miller” Charge	Q_{gd}		-	6.0	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 10)	-	455	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF
Internal Drain Inductance	L_D	Measured From Drain Lead, 2.0mm (0.08in) from Package to Center of Die; Modified MOSFET Symbol Showing the Internal Device Inductances 	-	4.0	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 2.0mm (0.08in) from Package to Source Bonding Pad	-	6.0	-	nH
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	120	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier		-	-	0.5	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	2.0	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 2.0A$, $V_{GS} = 0V$ (Figure 12)		-	-	1.6	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, $I_{SD} = 2.0A$, $dI_{SD}/dt = 100A/\mu s$		-	450	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^oC$, $I_{SD} = 2.0A$, $dI_{SD}/dt = 100A/\mu s$		-	3.1	-	μC

NOTES:

2. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature.
4. $V_{DD} = 40V$, starting $T_J = 25^oC$, $L = 29.09mH$, $R_G = 50\Omega$, peak $I_{AS} = 2.5A$.

Typical Performance Curves Unless Otherwise Specified

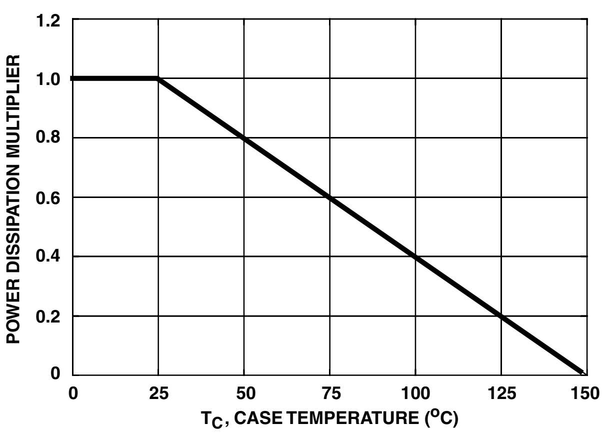


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

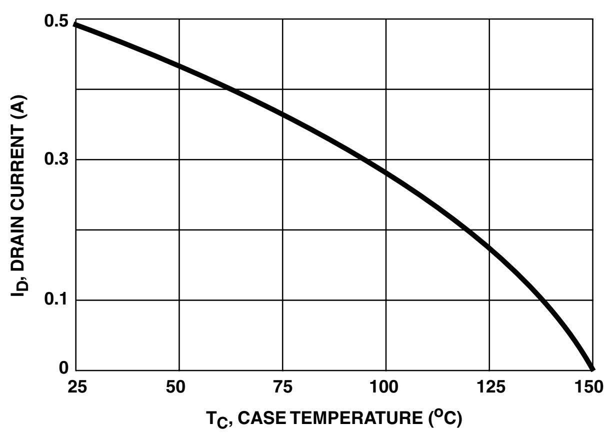


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

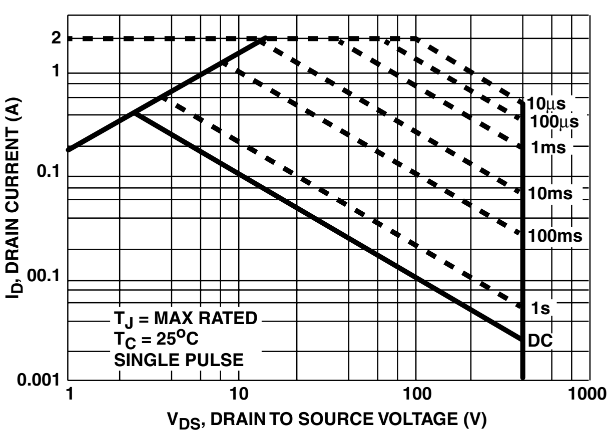


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

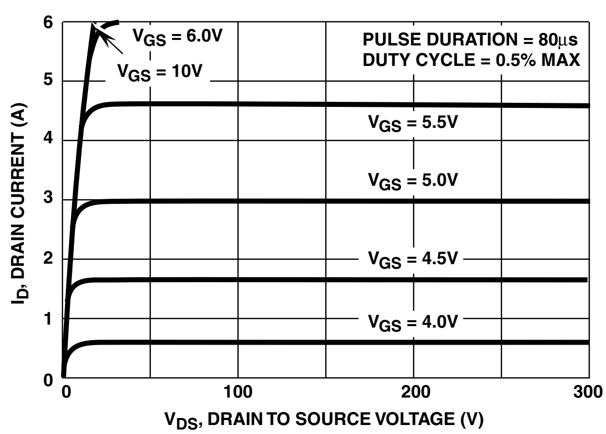


FIGURE 4. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified **(Continued)**

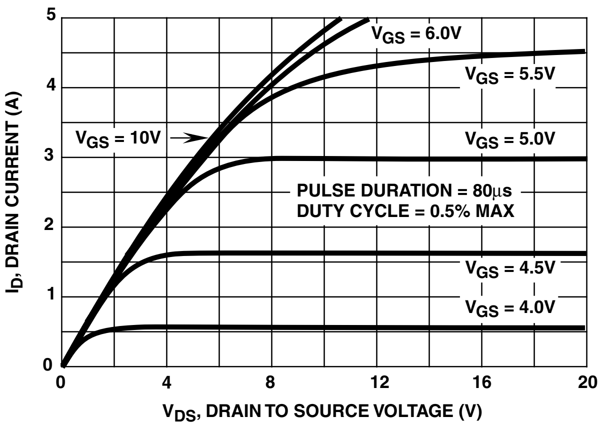


FIGURE 5. SATURATION CHARACTERISTICS

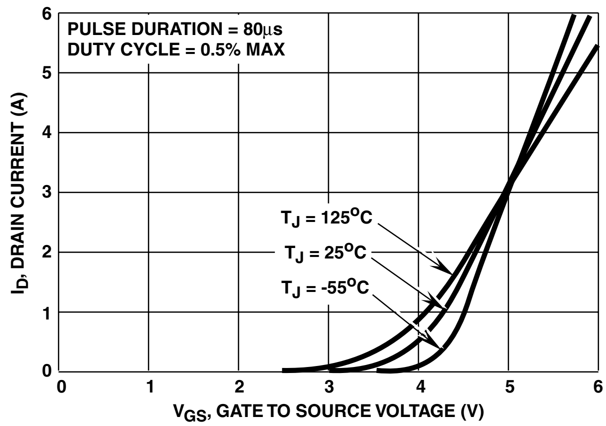
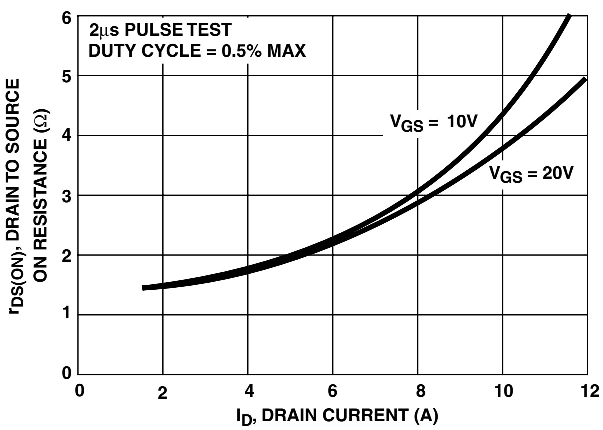


FIGURE 6. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2µs pulse is minimal.

FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

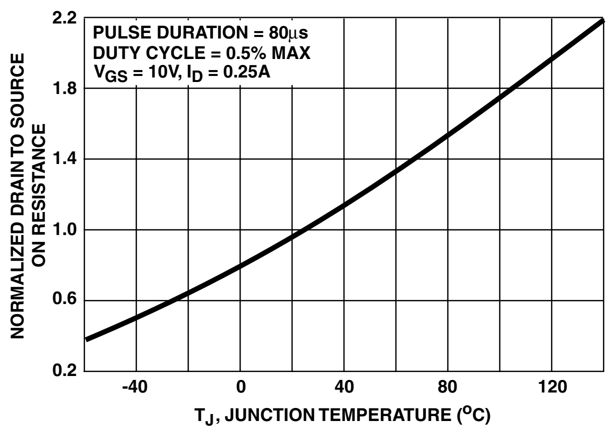


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

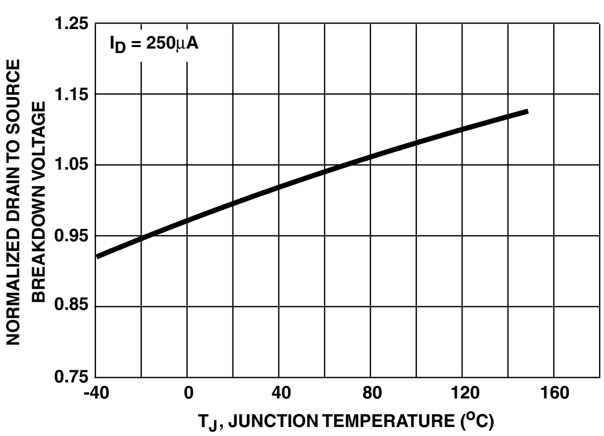


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

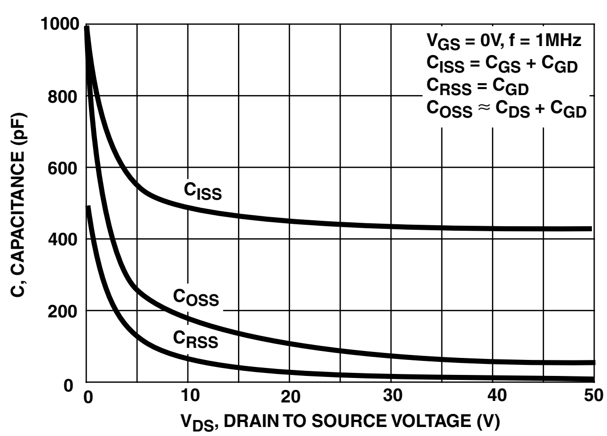


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

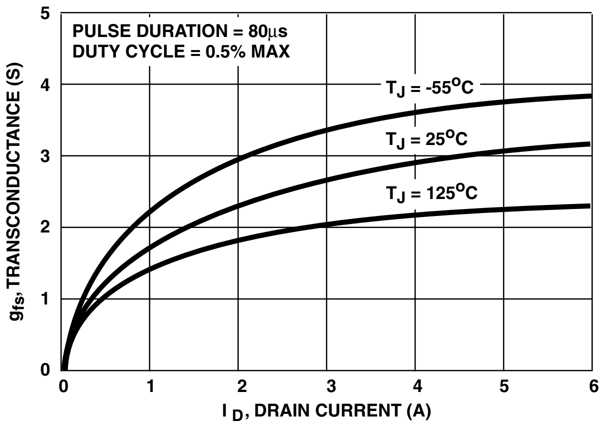


FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

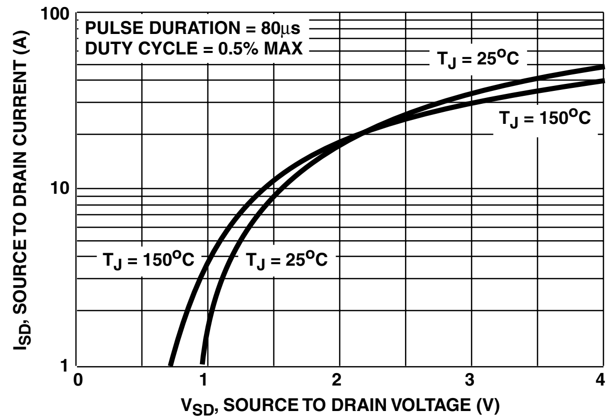


FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

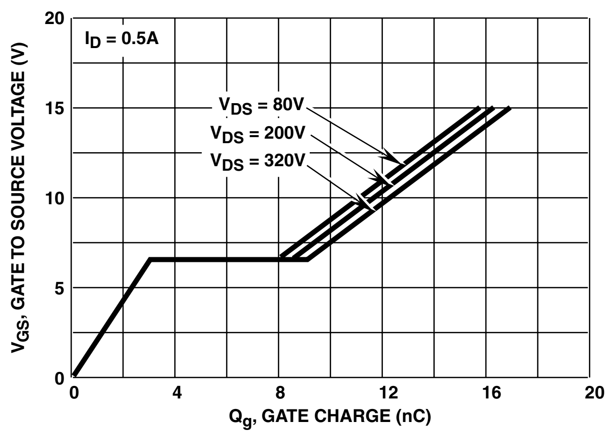


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

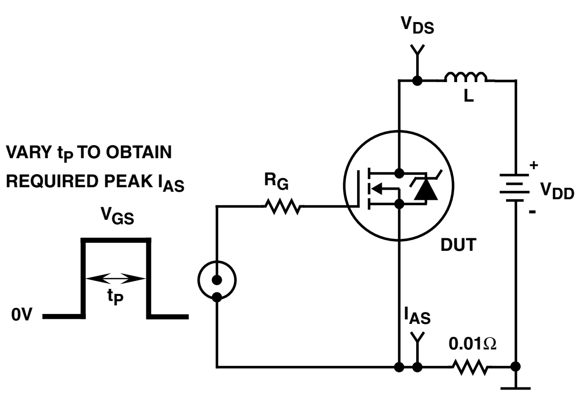


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

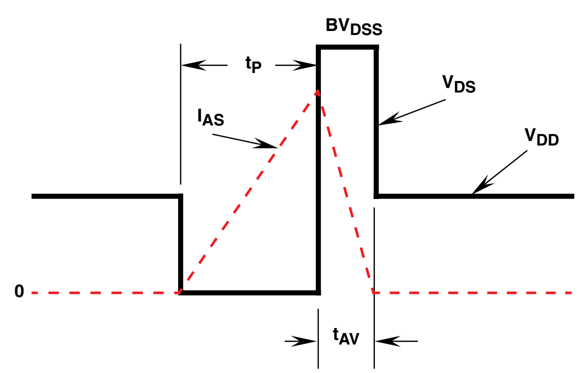


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

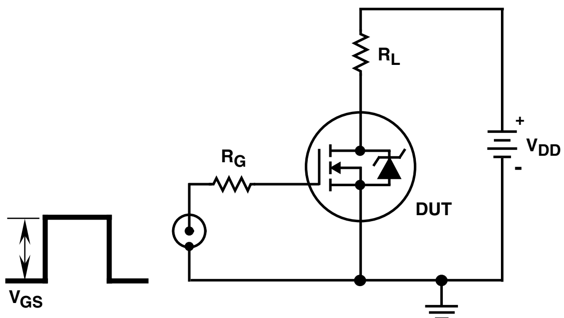


FIGURE 16. SWITCHING TIME TEST CIRCUIT

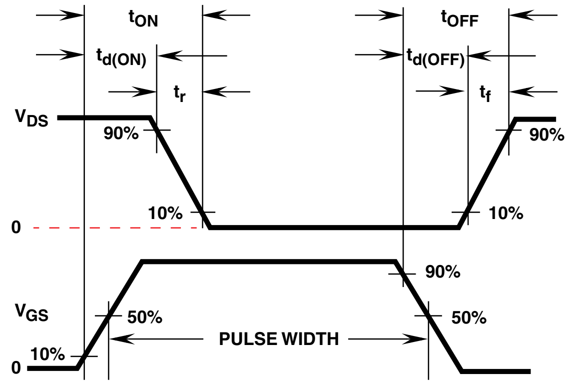


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

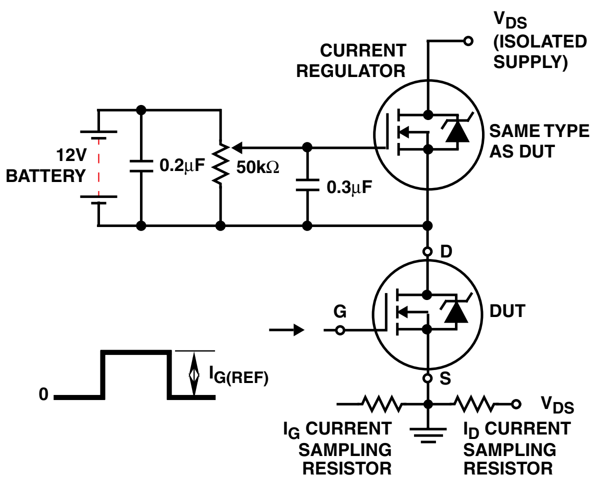


FIGURE 18. GATE CHARGE TEST CIRCUIT

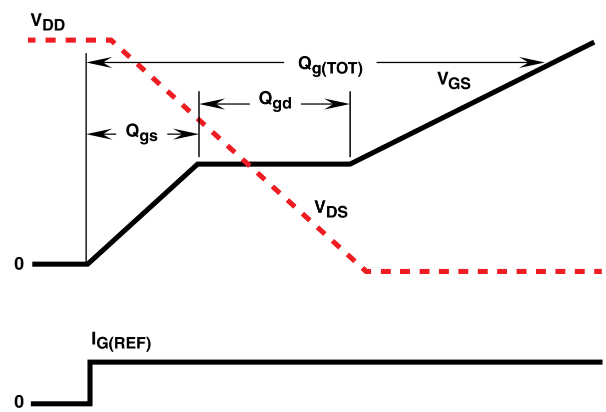


FIGURE 19. GATE CHARGE WAVEFORMS

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