

Faroudja Laboratories

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FLI 2200

Digital Component Video Deinterlacer/Line Doubler

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FLI 2200 Digital Component Video Deinterlacer/Line Doubler

Description

The FLI2200 is a single chip implementation of Faroudja Laboratories' award winning deinterlacing and postprocessing algorithms that produce the highest quality progressive video output from a variety of interlaced video inputs including 525/60 (NTSC) or 625/50 (PAL or SECAM). It uses patented and patent pending motion-adaptive deinterlacing that selects the optimal filtering on a per-pixel basis. This includes detection and proper interleaving of 3:2 and 2:2 pulldown for film-base sources, including continuous monitoring and compensation for bad edits that occur frequently in broadcast material due to poor scene cuts or insertion of commercials. Video material is processed by a set of content-sensitive spatio-temporal filters that adapt to the appropriate direction for smoothest interpolation using the patented Faroudja DCDi™ algorithm. The FLI2200 also includes motion-adaptive cross-color suppression that removes highly objectionable coloration artifacts produced by commonly used video decoders. Its internal processing uses 10 bits per channel to maintain the highest quality. Its inputs and outputs are 10 bits/channel for best quality but also supports 8 bits/channel for more cost-sensitive applications. The FLI2200 requires 4 MB of low cost SDRAM for best quality deinterlacing, but it can also be operated in an optimized intra-field mode without memory for more costsensitive applications. This makes possible the use of a single design for both high-end and low-end applications.

The FLI2200 integrates a number of functions to provide maximum flexibility in a low cost configuration. This includes an on-chip clock generator, SDRAM controller, display controller, input and output color-space converters. It uses a standard 2-wire serial control interface for easy control and access to the registers.

The FLI2200 can be connected without glue logic to the FLI2000 video decoder and FLI2220 Enhancer and OSD Generator to produce the highest quality video pipeline for premium applications. It is also fully compatible with other decoders having a ITU-R BT 656 output format.

Applications

Flat panel TV – LCD, PDP

Progressive scan TVs

Multimedia front/rear projectors

Home Theater

- Scan Converters
- Multimedia PCs/Workstations

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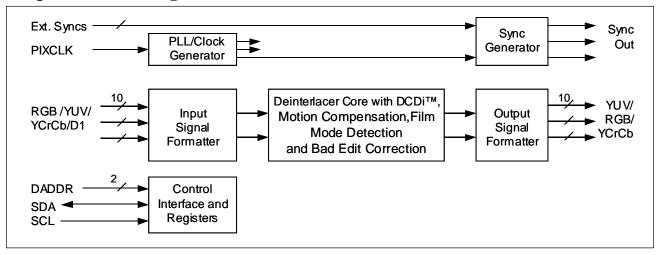
Features

- Motion-adaptive cross-color suppression removes artifacts produced by improper Y/C separation in lowcost video decoders
- Motion-adaptive video deinterlacing selects optimal filtering on a per-pixel basis
 - Film-mode for proper handling of 3:2 and 2:2 pulldown material
 - Bad-edit detection/correction compensates for poor scene cuts and insertions common in broadcast material
 - Motion-weighted interpolation for video sources produces maximum resolution without introducing motion artifacts
 - Directional Correlational Deinterlacing (DCDiTM) minimizes jaggies on angled lines
- ♦ 8/10-bit Y/Cb/Cr (D1) (ITU-R BT 656), 16/20-bit Y Cb/Cr (ITU-R BT 601), 24/30-bit RGB or YCbCr/YPbPr interlaced input options
 - Supports 525/60 (NTSC), 625/50 (PAL/SECAM)
 - Accepts up to 1100 pixels/line
- ◆ 8/10-bit, 16/20-bit YUV, 24/30-bit RGB or YCbCr/YPbPr progressive output options
- Supports 8- or 10-bit inputs and outputs
- 10-bit internal processing for highest quality
- Includes color-space converters at input and output for maximum flexibility
- Auto-detection of NTSC/PAL/SECAM inputs
- High-order filtering produces smooth chroma output in 4:2:2 to 4:4:4 or 4:4:4 to 4:2:2 conversions
- Resolution recovery maximizes output signal-to-noise ratio and dynamic range
- Can be operated without glue logic with FLI2000 Video Decoder and FLI2220 Enhancer and OSD Generator ICs to produce highest quality video pipeline
- Glue-less interface to most standard video decoders
- Built-in display timing generator
- On-chip clock generator eliminates external PLLs
- On-chip SDRAM controller
- Uses low cost SDRAM as field memory 4 MB
- Optimized intra-field operation allows memory-less configuration for lowest cost applications with same design and layout as for high-end applications
- 2-wire serial control interface for easy control

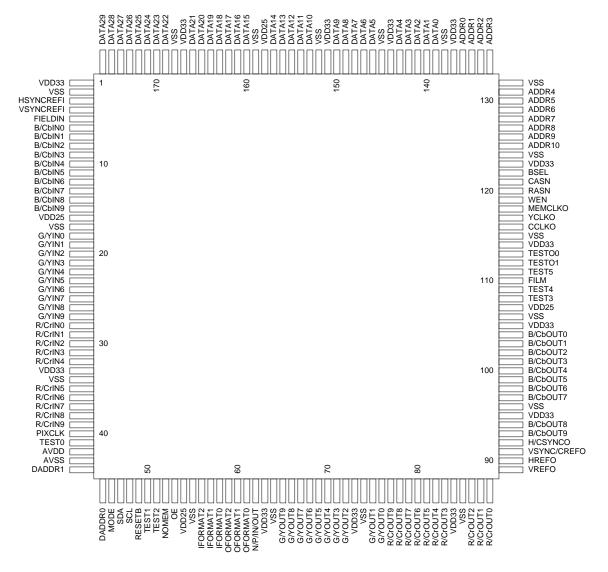
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• 176-pin TQFP package

Simplified Block Diagram



Packaging and Pinout Information



Package: 176-pin TQFP. $\theta_{ia} = xx \circ C/watt$

Pin Connections and Functions

Pin#	Name	Description
Power S	upply Connect	ions (not shown on Block diagram)
See list	V _{SS}	Ground connections. Connect to the digital ground plane. Pins: 2, 17, 34, 55, 64, 74, 85, 96, 106, 115, 124, 132, 138, 145, 152, 159, 168
See list	V _{DD33}	Pad Ring digital power connections. Connect to the digital 3.3 volt power supply and decouple to the digital ground plane. Pins: 1, 33, 63, 73, 84, 95, 105, 114, 123, 137, 144, 151, 167
See list	V _{DD25}	Core Logic digital power connections. Connect to the digital 2.5 volt power supply and decouple to the digital ground plane. Pins: 16, 54, 107, 158
43	AV _{SS}	Ground connection for the clock PLL circuits. Connect to the digital ground plane
42	AV _{DD}	Analog power connections for the clock PLL circuit. Connect to a separately decoupled 2.5 volt power supply and decouple directly to the AV_{SS} pin
Control	Signals	
49	RESETB	Reset. When this input is set low it will reset all the internal registers to the default states. Refer to the section on the control registers for details of these states. The device must be reset after it is powered-up.
53	OE	When this pin is set high the outputs of the FLI2200 will be enabled; when it is set low the outputs will be set into a high-impedance state.
56-58	IFORMAT ₂₋₀	Input signal format control. The settings of these pins set the format of the input signal. This can be overridden by the IFmtOvr bit, bit 3 in register $00_{\rm H}$, allowing this function to be set or changed via the I ² C bus. Please refer to the description of register $00_{\rm H}$ for details.
59-61	OFORMAT ₂₋₀	Output signal format control. The settings of these pins set the format of the output signal. This can be overridden by the OFmtOvr bit, bit 3 in register $07_{\rm H}$, allowing this function to be set or changed via the I ² C bus. Please refer to the description of register $07_{\rm H}$ for details.
44-45	DADDR ₁₋₀	The settings of DADDR ₁₋₀ allow the device address of the control bus to be programmed to prevent conflict with the other devices connected to the bus. DADDR ₁₋₀ allow the device address to be set to any of the following values: $C0/C1_H$, $C2/C3_H$, $E0/E1_H$, $E2/E3_H$. Please refer to the section "Control Bus Operation and Protocol" for further information.
46	MODE	When this pin is set low the control bus will operate in the slave mode; allowing the device to programmed from an external controller. When it is set high the FLI2200 will self-program from an external I^2C memory connected to the bus. Please refer to the "Control Bus Operation and Control Protocol" section for more details.
47	SDA	2-wire serial control bus data. Data can be written to the control registers via this pin when it is in the input mode and data can be read from the status registers when it is in the output mode. Refer to the section on the serial port for timing and format details and to the section on the registers for programming information.
48	SCL	2-wire serial control bus clock. When the control port operates in slave mode this pin will be an input and when it operates in the self programming mode it will be an output.
40	PIXCLK	Pixel clock input. This clock is used to drive all the circuits in the FLI2200. An internal PLL is used to upconvert this clock to provide the master clock signal and other clocks used internally. Note that when the FLI2200 is used in the D1 input mode the PIXCLK input should run at the rate of two cycles per pixel (one for luma and one for chroma).
62	N/P/IN/OUT	NTSC/PAL input or output. The default function of this pin is NTSC/PAL signal indicator output. When the input video signal is a 525 line signal this pin will be set high and when it is a 625 line signal the pin is set low. This function of this pin can be programmed to be an input according to the setting of this pin if the NPOp ₁₋₀ bits, bits 5-4 in register $03_{\rm H}$, are set to $00_{\rm H}$, overriding the internal line counter. i.e., it will treat the signal as a 525 line signal when it is set high and a 625 line signal when it is set low.

Pin #	Name	Description
Control	l Signals (contd.)	
52	NOMEM	No Memory Mode control input. This pin controls the operation of the FLI2200 as follows: When this pin is set low the device is used with external field memories and operates in the full set of deinterlacing modes, i.e., motion adaptive video deinterlacing and full frame film source deinterlacing using 3:2 pulldown detection (2:2 pulldown for 625/50 sources). When this pin is set high the FLI2200 is forced into the intra-field only deinterlacing mode, which requires no external memories, allowing the FLI2200 to be used in low-cost applications where the ultimate video quality is not a requirement. <i>To ensure proper startup of the SDRAMs this pin should be set high during the power-up sequence.</i> This can be overridden by the NMOvr bit, bit 1 in register $05_{\rm H}$, allowing this function to be set or changed via the I ² C bus. Please refer to the description of register $05_{\rm H}$ for details.
Input S	ignals	
27-18	G/YIN ₉₋₀	10-bit green or luminance signal input bus. The mode is set by the IFORMAT ₂₋₀ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_{H} , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00_{H} for details. This signal is sampled on the rising edge of PIXCLK.
15-6	B/CbIN ₉₋₀	10-bit blue or Cb chroma signal input bus. The mode is set by the IFORMAT ₂₋₀ pins. This can be overridden by the IFmtOvr bit, bit 3 in register $00_{\rm H}$, allowing this function to be set or changed via the I ² C bus. Please refer to the description of register $00_{\rm H}$ for details. Bits 6, 4 and 3 in register $08_{\rm H}$ specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr and Y Pb Pr modes the Cb or Pb signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
39-35 32-28	R/CrIN ₉₋₀	10-bit red or Cr chroma signal input bus. The mode is set by the IFORMAT ₂₋₀ pins. This can be overridden by the IFmtOvr bit, bit 3 in register $00_{\rm H}$, allowing this function to be set or changed via the I ² C bus. Please refer to the description of register $00_{\rm H}$ for details. Bits 6, 4 and 3 in register $08_{\rm H}$ specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr mode the Cr signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
3	HSYNCREFI	Horizontal sync or reference. The horizontal sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00_{H} . The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
4	VSYNCREFI	Vertical sync or reference. The vertical sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register $00_{\rm H}$. The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
5	FLDIN	Field identifier input. The field identifier output of the source signal should be connected to this pin. A low setting signifies an even field and a high level signifies an odd field. When bit 4 in register $00_{\rm H}$ is set low, the input timing is based on HREF and VREF and this signal is required. When this bit is set high the input timing is based on HSYNC and VSYNC and this signal is generated internally and is not required. When bit 5 in register 06 is set high this signal is also used as the frame boundary identifier for 30 Hz film sources.

Pin #	Name	Description
Output	Signals	
65-72 75-76	G/YOUT ₉₋₀	Green or luminance output bus. In the RGB mode this output is the Green signal and in the YCbCr mode it is the Y signal. The mode is set by the OFORMAT ₂₋₀ pins. This can be overridden by the OFmtOvr bit, bit 3 in register $07_{\rm H}$, allowing this function to be set or changed via the I ² C bus. Please refer to the description of register $07_{\rm H}$ for details. The signal is clocked out on the falling edge of YCLKO.
93-94 97-104	B/CbOUT ₉₋₀	Blue or Cb chrominance output bus. In the RGB mode this output is the Blue signal, in the Y Cb Cr mode it is the Cb signal. The mode is set by the OFORMAT ₂₋₀ pins. This can be overridden by the OFmtOvr bit, bit 3 in register $07_{\rm H}$, allowing this function to be set or changed via the I ² C bus. Please refer to the description of register $07_{\rm H}$ for details. The busses used in the multiplexed modes are set by means of bit 5 in register $08_{\rm H}$. The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
77-83 86-88	R/CrOUT ₉₋₀	Red or Cr chrominance output bus. In the RGB mode this output is the Red signal, in the YCbCr mode it is the Cr signal. The mode is set by the OFORMAT ₂₋₀ pins. This can be overridden by the OFmtOvr bit, bit 3 in register $07_{\rm H}$, allowing this function to be set or changed via the I ² C bus. Please refer to the description of register $07_{\rm H}$ for details. The busses used in the multiplexed modes are set by means of bit 5 in register $08_{\rm H}$. The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO in the RGB and YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
116	CCLKO	Chroma output sampling clock. This clock is derived from PIXCLK and will be at half the frequency of YCLKO. In 30-bit 4:2:2 output mode the chroma output signals will change on the falling edge of YCLKO prior to the next rising edge this clock.
117	YCLKO	Luma output sampling clock. This clock is derived from PIXCLK and is double the frequency of PIXCLK. In 30-bit and 20-bit output modes the output signals will change on the falling edge of this clock.
89	VREFO	Start of active field or frame indicator. This signal goes high to indicate the first active line in each field or frame and goes low during the vertical blanking interval. The polarity and timing of this signal are programmable.
90	HREFO	Start of active line indicator output. This signal goes high to indicate the first active pixel in each line and goes low during the horizontal blanking interval. The polarity and timing of this signal are programmable.
91	VSYNC/ CREFO	Vertical sync output. This signal provides the vertical sync function for the outputs. Its polarity is programmable to be active high or active low. It can also be programmed to be a composite reference for applications requiring this instead of sync.
92	H/CSYNCO	Horizontal or composite sync output. This signal provides the horizontal sync function for the outputs. Its polarity is programmable to be active high or active low. This signal can also be programmed to be the composite sync output, CSYNC.
110	FILM	Film mode detector output. This pin will be set high when the FLI2200 detects that the video input was converted from 24 fps film with a teleciné machine. If film mode is not detected this pin will be set low.

Pin #	Name	Description
SDRAM	Interface Signation	als
125-131 133-136	ADDR ₁₀₋₀	SDRAM Address bus. This signal bus is used to address the external SDRAM(s) used for field memories. It should be connected to the A_{10-0} bus of the memory chip(s). Please refer to the Applications section of this data sheet for further details.
176-169 166-160 157-153 150-146 143-139	DATA ₂₉₋₀	SDRAM Data bus. This signal bus is used to transfer the data to and from the external SDRAM(s) used for field memories. It should be connected to the DQ_{29-0} bus of the memory chip when using a 64 Mbit SDRAM. When using two 16 Mbit SDRAMs this 30-bit bus may be connected to the two 16-bit data busses of the memories in two ways: either connect 16 lines to one chip and 14 to the other, or connect 15 to both. In all cases the two unused data lines on the memory chip(s) should be connected to ground via 22 k Ω resistors. Please refer to the Applications section of this data sheet for further details.
118	MEMCLKO	SDRAM clock and 2x output sampling clock. This clock is derived from PIXCLK and will be at double the frequency of YCLKO. This active signal should be connected to the CLK pin(s) on the SDRAM(s). When the 10-bit output mode selected the output signals will also change at this clock rate and this should then be used as the output clock
119	WEN	SDRAM Write Enable. This active low signal should be connected to the WE pin(s) on the SDRAM(s).
120	RASN	SDRAM Row Address Select. This active low signal should be connected to the RAS pin(s) on the SDRAM(s).
121	CASN	SDRAM Column Address Select. This active low signal should be connected to the CAS pin(s) on the SDRAM(s).
122	BSEL	SDRAM Bank Select. When using two 16 Mbit SDRAMs this signal should be connected to the BA (also called BS or A_{11}) pin on both SDRAMs. When using a 64 Mbit SDRAM this signal should be connected to the BA0 (also called BS0 or A_{11}) pin on the SDRAM and BA1/BS1 (also called BA when BA0 is referred to as A_{11}) should be tied low.
Test Inp	uts	
41, 50, 51, 108, 109, 111	TEST ₅₋₀	These pins are used for test purposes only and should always be tied low for normal operation.
Test Out	puts	1
112, 113	TESTO ₁₋₀	These pins are test outputs and should be left unconnected in normal operation.

Description of Functional Blocks

Note on signal conventions used in this document:

The following conventions are used to denote the three component signal formats used in the FLI2200:

The name Cb is used to denote the B-Y component, regardless of the actual color space (Cb, Pb, etc.).

The name Cr is used to denote the R-Y component, regardless of the actual color space (Cr, Pr, etc.).

Y Cb Cr denotes a 3-bus signal, i.e., 3 x 10 bits, with the three components unmultiplexed. Signals in this format can have either 4:4:4 or 4:2:2 sampling structures. RGB signals will also be in this format, with a 4:4:4 sampling structure.

Y Cb/Cr denotes a 2-bus signal, i.e., 2 x 10 bits, with the Cb and Cr components multiplexed. Signals in this format will always have a 4:2:2 sampling structure.

Y/Cb/Cr denotes a 1-bus signal, i.e., 1 x 10 bits, with all three components multiplexed. Signals in this format will always have a 4:2:2 sampling structure. At the input this signal will be in parallel D1 format with either embedded timing codes or external horizontal and vertical timing references.

System Clock Generation Block

A number of system clocks are derived from the PIXCLK input using frequency multiplier circuits. This eliminates the need for an external high frequency clock driver and permits the device to be driven directly by the pixel clock of the input signal.

Control Interface and Register Block

The control interface and register block consists of a 2-wire serial bus controller and a number of control and status registers. When a write-byte command is received on the bus the controller writes bytes of data received from the bus into the control registers. When a read-byte command is received on the bus the decoder reads information bytes from the status registers and outputs them on the bus. The bus is generally I²C compatible.

Input Formatter Block

The input formatter block consists of two sections, the color space converter and the multiplexer/demultiplexer. The FLI2200 processes all signals in 4:2:2 Y Cb/Cr format. In order to allow the device to be operated with RGB inputs an optional color space conversion matrix is incorporated. After conversion the chroma components will be decimated to provide the 4:2:2 format.

The FLI2200 can also be used with component inputs. The signals can be in 3 x 10-bit Y Cb Cr format, 2 x 10-bit Y Cb/Cr format or 1 x 10-bit Y/Cb/Cr (D1) format. Regardless of which format is used the signals will all be converted into 2 x 10-bit Y Cb/Cr format in this block before further processing. Thus, if the input format selected is 3×10 -bit Y Cb Cr (or RGB) the chroma signals will be multiplexed, with an optional decimation stage for 4:4:4 inputs. Conversely, if the input mode selected is $1 \ge 10$ -bit Y/Cb/Cr at 27 MHz the luma and chroma signals will be demultiplexed. $2 \ge 10$ bit Y Cb/Cr signals will not require any processing in this block.

At the input, a programmable gain function can be used to maximize the signal range if the input signal has sync on Y or G. After the sync is stripped from the signal the gain function expands R G B or Y Cb Cr to the full 10-bit dynamic range to minimize quantization effects in the processing. The Y and Cb Cr signal gains can also be programmed independently. When the D1 mode is selected the embedded codes will be detected to generate all timing information, eliminating the need to use external syncs in this mode. The gains will be set automatically in this case.

Luma Processing Block

The luma processing block consists of a motion detector, film mode detector with bad-edit detector, the interpolator and luma line doubling FIFOs.

The motion detector is frame based and compares the luma value of the current pixel and the same pixel in the previous frame. This is done in both the odd and even fields to generate a motion vector which is then used to switch the signal processing between field interleave and spatial interpolation modes on a pixel by pixel basis. In this way, non-moving parts of the picture, where sharpness is readily detected by the viewer, will not be interpolated and will have maximum sharpness. Conversely, moving parts of the picture, where sharpness is not easily detected by the viewer, will be interpolated to avoid motion artifacts. The consequences of interleaving fields in areas of the picture containing motion are significantly worse than the loss of resolution caused by interpolation.

The film mode detector detects the 3:2 or 2:2 pulldown sequences from teleciné conversion. Converting 24 frame/sec. film to 60 field/sec. maps two film frames (1/12 sec.) into five video fields (also 1/12 sec.), alternating between three odd and two even fields and three even and two odd fields. This pattern repeats over ten video fields. For further information on film mode please refer to the Applications section of this data sheet. Converting 24 frame/sec. film to 50 field/sec. video is done by running the film at 25 frames/sec. This is the same procedure as converting 30 frame/sec. film to 60 field/sec. video and results in the much simpler pattern of one film frame being mapped into one odd and one even field of video. In all cases, the film mode detector detects these sequences in the signal and uses them to correctly pair odd and even fields originating from the same film frame. Once this is done, these field pairs can be interleaved without consideration of motion since there is, by definition, no motion between them. Film mode overrides video mode processing.

The bad edit detector continually monitors the sequences for breaks caused by video edits made after the teleciné transfer. There are 25 possible ways for the 3:2 pulldown sequence to be interrupted, and only two of these will not result in a break in the sequence. The bad edit detector looks for the break and forces the FLI2200 to switch out of film mode and into video mode before the bad edit is seen on the screen. The film mode detector will then reaquire the pulldown sequence, allowing the system to be switched back into film mode transparently.

Note that film mode detection is not done in the peripheral areas of the frame; this prevents the bad edit detector from causing the system to drop out of film mode in the presence of on-screen display (OSD) graphics, such as subtitles, added to the video in these regions by the source, e.g., a DVD player. However, any graphics added to the central zone can cause the system to drop out of film mode any time they change, since the changes will generally not be synchronized to the 3:2 pulldown sequence, in which case they will be indistinguishable from bad edits.

The intra-field interpolator is used to generate the missing pixels in the field when motion is detected in video mode and the pixels from the previous field cannot be interleaved. The FLI2200 uses a new diagonal interpolation algorithm, Directional Correlation DeinterlacingTM, (DCDiTM, patent pending) that computes and tracks the angles of edges and uses this information to optimally fill in the missing pixels. Conventional vertical interpolation algorithms work well on edges close to the horizontal and vertical directions but can completely break down as the angles of edges become more diagonal. Diagonal interpolation eliminates this problem. The operation of the FLI2200 can be forced into the intra-field diagonal interpolation mode at all times, allowing it to be used without external field memories in low-cost applications.

Finally, the results of the motion detector, film mode detector and bad edit detector are used to control the signal paths into the de-interleaving FIFOs, determining whether interpolated pixels or pixels from the previous field are used in the interleaving process.

Chroma Processing Block

The chroma processing block consists of a cross-color suppressor, chroma line-averager and the chroma line doubling FIFOs. Positioning the cross-color suppressor in the deinterlacer takes advantage of the frame buffers already required for temporal processing and eliminates the need to use a 3-D comb filter with duplicate frame buffers. The cross-color suppressor helps to eliminate residual cross-color after the decoder. With the exception of 3-D decoders, all decoders, such as the Faroudja FLI2000, use a 2-D comb filter and/or notch filter, which leave residual cross-color under certain circumstances, such as diagonal edges, and the frame-based cross-color suppressor eliminates this in most cases, leaving the residual cross-color at a very low level. Complete suppression is only possible in the absence of motion because some conditions (diagonal edges moving diagonally at rates with certain relationships to the field rate) result in signals which are completely impossible to fully separate because the luma and chroma spectra are completely superimposed. The chroma line averager is used to perform interpolation in the chroma path and passes the deinterlaced chroma

Field Memory Interface Block

signals into the line doubler memories.

The field memory interface block formats the data and generates all the addressing required to use standard SDRAM for the field memories. The FLI2200 requires memory in a 1 Mbit x 30 configuration. This can be achieved either by using two 16 Mbit (1 Mbit x 16) SDRAMs or one 64 Mbit (2 Mbit x 32) SDRAMs. The FLI2200 was designed to operate with the Micron MT48LC1M16A1 and MT48LC2M32B2; it is also compatible with the following devices:

Vendor	16 Mbit	64 Mbit
Fujitsu	MB81F161622C	MB81F643242B
Hyundai	HY57V161610	HY57V653220
Micron	MT48LC1M16A1	MT48LC2M32B2
Samsung	K4S161622D	K4S643232C

The FLI2200 is also compatible with 1M x 32 SGRAMs.

In all cases the speed grade required is application dependent, the SDRAM interface operates at twice the input pixel rate. For NTSC/PAL inputs (13.5 Mpix/sec.) the SDRAM clock speed requirement is 54 MHz, so that the lowest speed grade devices (10 nsec./100 MHz) will easily meet these requirements.

Output Formatter Block

The output formatter block consists of two sections, the multiplexer/demultiplexer and the color space converter. The multiplexer/demultiplexer allows the signal format to be converted from the 4:2:2 Y Cb/Cr format used internally to either Y Cb Cr or Y/Cb/Cr. An optional interpolation filter then allows the signals to be converted to 4:4:4 format when the Y Cb Cr mode is selected. The color space converter further allows the Y Cb Cr 4:4:4 signals to be converted into R G B 4:4:4 format. The 4:2:2 Y Cb Cr signal can also be converted into Y Pb Pr.

Memory Map

	101 9 1110	1								i
Regist Addr.	ter Name	7	6	5	Bits	3	2	1	0	Default Value
00 _H	INPUT	CClmpEn	YClmpEn	SOnYG	Sync/Ref	IFmtOvr		IFormat ₂₋₀)	D0 _H
01 _H	YCLAMP			I	YClamp ₇₋₀				<u> </u>	40 _H
02 _H	CCLAMP				CClamp ₇₋₀					00 _H
03 _H	NP	X	NPStat	NPOp ₁₋₀	- 7-0	CClamp ₉₋₈		YClamp ₉₋₈	2	18 _H
04 _H	DELAY		CDelay ₃₋₀			CSwapI		YDelay ₂₋₀		B4 _H
05 _H	MODE1	Fm2430	X	Test	Test	DCDiOn	FilmOn	NMOvr	NoMem	$0C_{\rm H}/8C_{\rm H}$
06 _H	MODE2	CSync	VITSEn	F30Hz	F30Inv	Force30	Motion ₁₋₀	I	PComp	05 _H
07 _H	OUTPUT	CSwapO	ChrPhs	CIntDis	OBlnkEn	OFmtOvr	10	OFormat ₂	-0	10 _H
)8 _H	IOSEL	D1Valid	CInSel	COutSel	D1InSel ₁₋₀	I		FSyncDel	-	52 _H
)9 _H	GAIN	X	X	X	X	X	X	YInGain	CInGain	03 _H
DA _H	FDELAY				BSStart ₇₋₀			1		4A _H
10 _H	HSSTN				HSStartN ₇					00 _H
11 _H	HSSPN				HSStopN ₇					00 _H
12 _H	HRSTN				HRStartN					00 _H
п 13 _н	HRSPN				HRStopN	-				00 _H
п 14 _н	VMSN	VSStartN ₅	. 1	VSStopN ₅		VRStartN	. 1	VRStopN	5 /	00 _H
15 _H	VSSSN	J	VSStartN ₃		J-4		VSStopN ₃		0-4	00 _H
п 16 _н	VRSSN		VRStartN	-			VRStopN			00 _H
п 17 _н	VBIMSN	X	VBStartN ₄	x	VBStopN ₄	VBIStartN		VBIStopN	J _{5 4}	00 _H
п 18 _Н	VBTN		VBStartN ₂		1 4		VBStopN ₃		5-4	00 _H
п 19 _Н	VBITN		VBIStartN	0			VBIStopN			00 _H
20 _H	HSSTP			3-0	HSStartP ₇ .	0		3-0		00 _H
21 _H	HSSPP				HSStopP ₇ -					00 _H
п 22 _н	HRSTP				HRStartP ₇					00 _H
и 23 _Н	HRSPP				HSRtopP ₇	-				н 00 _н
н 24 _н	HMSP	HSStartP ₉	0	HSStopP ₉		HRStartP ₉	0	HRStopP		н 00 _н
25 _H	VSSTP	9	-0	19	VSStartP ₇₋		-0	1,	7-0	00 _H
26 _H	VSSPP				VSStopP ₇ -	-				00 _H
27 _H	VRSTP				VRStartP ₇	-				01 _H
28 _H	VRSPP				VRStopP ₇ .	-				01 _H
29 _H	VBSTP				VBStartP ₇ .					01 _H
2A	VBSPP				VBStopP ₇					00 _H
2B	VBISTP				VBIStartP.	-				02 _H
	VBISPP				VBIStopP.					08 _H
2C				X	UseHSize			HSize ₁₀₋₈		03 _H
	VBTP	Test	X					10-8		I I H
2E _H	VBTP HSIZE	Test	X		HSize ₇₀					60 ₁₁
2C 2E _H 2F _H 30 _H	VBTP HSIZE INV1	Test ISyncInv	x ORefInv	OSyncInv	HSize ₇₋₀	HDatBlnk	Test	Test	CCSOn	60 _H 05 _H

Regis	ter				Bits					Default		
Addr.	Name	7	6	5	4	3	2	1	0	Value		
32 _H	EDBR				EdBlnkR7-	0				52 _H		
33 _H	EDBT				EdBlnkT ₇₋	0				42 _H		
34 _H	EDBBN				EdBlnkBN	I ₇₋₀				F4 _H		
35 _H	EDBBP		EdBlnkBP ₇₋₀									
36 _H	EDBMS								66 _H			
37 _H	FMBL				FmBlnkL ₇	-0				96 _H		
38 _H	FMBR				FmBlnkR ₇	-0				58 _H		
39 _H	FMBT				FmBlnkT ₇	-0				42 _H		
3A _H	FMBBN				FmBlnkBN	N ₇₋₀				F4 _H		
3B _H	FMBBP				FmBlnkBF) 7-0				58 _H		
3C _H	FMBMS	FmBlnkL ₈	FmBlnkR ₉	-8	FmBlnkT ₈	FmBlnkBl	N ₉₋₈	FmBlnkBl	P ₉₋₈	66 _H		
3D _H	TEST				Test ₇₋₀					14 _H		
3E _H	TEST				Test ₇₋₀					0E _H		
3F _H	TEST				Test ₇₋₀					60 _H		
40 _H	TEST				Test ₇₋₀					05 _H		
41 _H	TEST	x	x	x	X		Test ₃₋₀			0C _H		
42 _H	TEST				Test ₇₋₀	1				14 _H		
throug	gh	I	See regist	er descripti	ons for defa	ult values	of these reg	isters		I		
4C _H	TEST				Test ₇₋₀					38 _H		
4D _H	TEST						Test ₄₋₀			00 _H		
4E _H	PFILM						Test ₃₋₀			07 _H		
4F _H	PFTHR				Test ₇₋₀	1				04 _H		
50 _H	TEST					Test ₅₋₀				14 _H		
51 _H	TEST				Test ₇₋₀					18 _H		
52 _H	TEST				Test ₇₋₀					06 _H		
53 _H	TEST				Test ₇₋₀					30 _H		
54 _H	TEST				Test ₇₋₀					30 _H		
60 _H	PLL0				PLL MDiv	V ₇₋₀				18 _H		
61 _H	PLL1				PLL NDiv					30 _H		
62 _H	PLL2	Lock		Disable	РВур	PLLOvr		PDiv ₂₋₀		02 _H /82 _H		
63 _H	ODIS						ROutDis	GOutDis	BOutDis	00 _H		
64 _H	INV2		Test ₁₋₀	InvYClk			Test ₄₋₀			00 _H		
65 _H	TEST		- •	•	Test ₇₋₀					00 _H		
66 _H	SDEL						SDel ₄₋₀			00 _H		
67 _H	TEST			•	Test ₇₋₀		• •			08 _H		
71 _H	TEST				Test ₇₋₀					00 _H		
72 _H	TEST							Test ₂₋₀		00 _H		
7E _H	IDL				ChipID ₇₋₀			20		41 _H		
7F _H	IDH				ChipID ₁₅₋₈					4B _H		

Register Details

Address 00 _H : I	NPUT Control	Register . 1	Default valu	e D0 _H							
The eight bits in	the INPUT reg	gister contro	ol the front-e	end configura	tion, as show	n below:					
Bit	7	6	5	4	3	2	1	0			
Mnemonic	CCImpEn	YClmpEn	SOnYG	Sync/Ref	IFmtOvr	IFormat ₂	IFormat ₁	IFormat ₀			
Default value	1	1	0	1	0	0	0	0			
CCImpEn:	The CClmpE	n bit is used	l to enable th	e chroma clai	mp circuit, as	follows:					
			-	The input cla	-						
		Chroma clar a in register	-	The clamp le	vels will be s	et according to	the value of	the CClamp			
YCImpEn:	The YClmpE	n bit is used	l to enable th	e luma clamp	circuit, as fo	llows:					
		-		he input clam	-						
		luma clamp egister 01 _H .	enabled. Tl	he clamp leve	l will be set a	ccording to the	e value of the	YClamp			
SOnYG:	The SOnYG	bit is used a	according to	whether or n	ot there is syn	nc on the luma	/green input	, as follows:			
	$0^* = N$	No sync pul	ses on the lu	uma/green ch	annel input.						
	 0* = No sync pulses on the luma/green channel input. 1 = Luma/green channel input contains sync pulses. 										
	maximize the	e dynamic ra in register	ange of the p 09 _H . When	processing op this bit is set	erations, over	ded to full sca riding the sett can be set inc	ings of the Y	InGain and			
Sync/Ref:	The Sync/Re	f bit is used	to define th	e input timing	g signals, as f	ollows:					
	0 = T	The FLI220) is configur	red to use hori	zontal and ve	ertical reference	es as timing	signals.			
	1* = T	The FLI220	0 is configu	red to use hor	izontal and ve	ertical sync pu	lses as timin	g signals.			
IFmtOvr:	The IFmtOvr	bit is used	to control th	e input forma	t function, as	follows:					
	0* = The FLI2200 is configured to use the input format defined by the IFORMAT ₂₋₀ pins, pins 56-58. The formats defined will be same as those defined for the IFormat ₂₋₀ bits.										
				red to use the e pin settings		t defined by th	he IFormat ₂₋₀) bits in			
IFormat ₂₋₀ :	The IFormat ₂	₂₋₀ bits are u	sed to defin	e the format o	of the input si	gnals, as follo	ws:				
	IFormat ₂ 000	-0 -	signal forma v/Cr	t							
	001										
	010										
	011										
	10x										
	110			th embedded t	iming)						
	111			th external/se	-						
						sing the D1 in	put modes, 1	1x.			
	The busses us	sed for the r	nultiplexed	signals (Cb/C	r and Y/Cb/C	r) in modes 00	0 and 11x ar	e			
	determined b	y the setting	gs of the Cir	isei and DIIn	isel bits in re	gister 08 _H , as	snown on pag	ge 49.			

D'4	_	•		• .	shown below:		1	0
Bit	7	6	5	4	3	2	1	0
Mnemonic	YClamp ₇	YClamp ₆	YClamp ₅	YClamp ₄	YClamp ₃	YClamp ₂	YClamp ₁	YClamp
Default value	0	4	0	0	0	0	0	0
YClamp ₇₋₀		in conjunctio En bit is set h			$03_{\rm H}$, set the c	lamp level for	the luma sig	nal when
	000 _H * =	= Minimum cla	amp level 000	$O_{\rm H}(0).$				
	040 _H * =	= Default clam	np level 040 _H	(64).				
	3FF _H =	= Maximum cl	amp level, 3F	F _H (1023)				
Address $02_{\rm H}$: (The eight bits in					shown below:			
Bit	7	6	5	4	3	2	1	0
DI		CClaura	CClamp ₅	CClamp_4	CClamp ₃	CClamp ₂	CClamp ₁	CClamp
	CClamp ₇	CClamp ₆	13					
Mnemonic Default value	CClamp ₇ 0	0	0	0	0	0	0	0
Mnemonic	0 These bits,	0	0 on with bits 3	-2 in register	-	-	-	-
Mnemonic Default value	0 These bits, when the C	0 in conjunctio	0 on with bits 3 s set high, as	-2 in register follows:	-	-	-	-
Mnemonic Default value	0 These bits, when the C $000_{\rm H}^*$ =	0 in conjunctio CCImpEn bit i	0 on with bits 3 s set high, as amp level 000	-2 in register follows: 0 _H (0).	-	-	-	-

				1	ration and the	-		
is Read Only.: Bit	7	6	5	4	3	2	1	0
Mnemonic	/ X	NPStat	NPOp ₁	NPOp ₀	CClamp _o	CClamp ₈	YClamp _o	YClamp ₈
Default value	X	R/O	0	$100p_0$	1	0	0	0
Default value	л	NO	0	1	1	0	0	0
х:	This bit is	not used and	does not exi	st physically				
NPStat:	function. count, rega 0 =	This bit, as w rdless of the = 625 line sig	ell as the NI	P/IN/OUT pi ne NPOvr ₁₋₀	n when it is a	detector. It is an output, will gister, as follo	indicate the	
NPOp ₁₋₀ :	These bits	configure the	e operation o	f the FLI220	0 and the N/I	P/IN/OUT pin	, pin 62, as f	ollows:
- 1-0	NPOp ₁₋₀	Configuration	on			-	N/P/IN/OU7	Function
	00	= Set NTSC	PAL mode	according to	setting of N/	P/IN/OUT pir	n. Input	
	01*	= Auto dete	ct signal usin	ng internal N	TSC/PAL de	tector.	Output	
	10	= Force FLI	2200 to NTSC	Coperation.			Output	(high)
	11	= Force FLI	2200 to PAL o	operation.			Output	(low)
		,.		0	02 (1	1 1 10	.1 1	
	These are t These bits,	he most sign in conjuncti	ificant bits o on with bits	f the 10-bit v 7-0 in registe	value. See de er 01 _H , set the	elamp level for escription of re e clamp level	egister 02 _H fo for the luma	or details. signal.
CClamp ₉₋₈ : YClamp ₉₋₈ :	These are t These bits, These are t	he most sign in conjuncti he most sign	ificant bits o on with bits ificant bits o	f the 10-bit v 7-0 in registe f the 10-bit v	value. See de er 01 _H , set the	scription of re	egister 02 _H fo for the luma	or details. signal.
YClamp ₉₋₈ : Address 04 _H :	These are t These bits, These are t DELAY Con	he most sign in conjuncti he most sign trol Registe	ificant bits o on with bits ificant bits o r. Default v a	f the 10-bit v 7-0 in registe f the 10-bit v alue B4_H	value. See de er 01 _H , set the value. See de	escription of received and the scription of received as a scription of the scription	egister 02 _H fo for the luma egister 01 _H fo	or details. signal.
YClamp ₉₋₈ : Address 04 _H : The seven bits	These are t These bits, These are t DELAY Con	he most sign in conjuncti he most sign trol Register { register set	ificant bits o on with bits ificant bits o r. Default v a the luma and	f the 10-bit v 7-0 in registe f the 10-bit v alue B4_H d chroma del	value. See de er 01 _H , set the value. See de lay at the fror	e clamp level escription of re- escription of re- nt end, as show	egister 02 _H fo for the luma egister 01 _H fo	or details. signal. or details.
YClamp _{9.8} : Address 04 _H : The seven bits Bit	These are t These bits, These are t DELAY Con in the DELAY 7	he most sign in conjuncti he most sign trol Register 7 register set 6	ificant bits o on with bits ificant bits o r. Default v the luma and 5	f the 10-bit v 7-0 in registe f the 10-bit v alue B4 _H d chroma del 4	value. See de er $01_{\rm H}$, set the value. See de ay at the from 3	e clamp level escription of re- terescription of re- nt end, as show 2	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for wn below: 1	or details. signal. or details.
YClamp ₉₋₈ : Address 04 _H : The seven bits Bit Mnemonic	These are t These bits, These are t DELAY Con in the DELAY 7	he most sign in conjuncti he most sign trol Register 7 register set 6	ificant bits o on with bits ificant bits o r. Default v the luma and 5	f the 10-bit v 7-0 in registe f the 10-bit v alue B4 _H d chroma del 4	value. See de er $01_{\rm H}$, set the value. See de ay at the from 3	e clamp level escription of re- escription of re- nt end, as show	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for the luma and the luma egister $01_{\rm H}$ for the luma for the luma egister 1	or details. signal. or details.
YClamp _{9.8} : Address 04 _H : The seven bits Bit Mnemonic Default value	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1	he most sign in conjuncti he most sign trol Register trol Register set 6 CDelay ₂ 0	ificant bits o on with bits ificant bits o r. Default va the luma and 5 CDelay ₁ 1	f the 10-bit w 7-0 in register f the 10-bit w alue $B4_H$ d chroma del 4 CDelay ₀ 1	value. See de er 01 _H , set the value. See de lay at the from 3 CSwapI 0	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀
YClamp _{9.8} : Address 04 _H : The seven bits Bit Mnemonic Default value	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1 These bits	he most sign in conjuncti he most sign trol Register trol Register trol Register college 0 set the delay	ificant bits o on with bits ificant bits o r. Default v the luma and 5 CDelay ₁ 1 for the chron	f the 10-bit v 7-0 in registe f the 10-bit v alue B4 _H d chroma del 4 CDelay ₀ 1 na signals, a	value. See de er 01 _H , set the value. See de lay at the from 3 CSwapI 0	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀
YClamp _{9.8} : Address 04 _H : The seven bits Bit Mnemonic Default value	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1 These bits $0_{\rm H}$ =	he most sign in conjuncti he most sign trol Register trol Register trol Register trol Register trol Register trol	ificant bits o on with bits ificant bits o r. Default va the luma and 5 CDelay ₁ 1 for the chron chroma delay	f the 10-bit v 7-0 in registe f the 10-bit v alue $B4_H$ d chroma del 4 CDelay ₀ 1 ma signals, a , 0 pixels.	value. See de er 01 _H , set the value. See de lay at the from 3 CSwapI 0	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀
YClamp _{9.8} : Address 04 _H : The seven bits Bit Mnemonic Default value	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1 These bits $0_{\rm H} = B_{\rm H}^* =$	he most sign in conjuncti he most sign trol Register { register set 6 CDelay ₂ 0 set the delay = Minimum c	ificant bits o on with bits ificant bits o r. Default v the luma and 5 CDelay ₁ 1 for the chron	f the 10-bit v 7-0 in registe f the 10-bit v alue B4 _H d chroma del 4 CDelay ₀ 1 ma signals, a , 0 pixels.	value. See de er 01 _H , set the value. See de lay at the from 3 CSwapI 0	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀
YClamp _{9.8} : Address 04 _H : The seven bits Bit Mnemonic Default value CDelay ₃₋₀ :	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1 These bits $0_{\rm H} =$ $B_{\rm H}^* =$ $F_{\rm H} =$	he most sign in conjuncti he most sign trol Register (register set 6 CDelay ₂ 0 set the delay = Minimum c = Default chro	ificant bits o on with bits ificant bits o r. Default va the luma and 5 CDelay ₁ 1 for the chron chroma delay, 11 hroma delay, 7	f the 10-bit v 7-0 in register f the 10-bit v alue $B4_H$ d chroma del 4 CDelay ₀ 1 ma signals, a , 0 pixels. 15 pixels.	value. See de er 01 _H , set the value. See de ay at the from 3 CSwapI 0 s follows:	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂ 1	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀
YClamp _{9.8} : Address 04 _H : The seven bits Bit Mnemonic Default value CDelay ₃₋₀ :	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1 These bits $0_{H} =$ $B_{H}^{*} =$ $F_{H} =$ This bit sw	he most sign in conjuncti he most sign trol Register a register set 6 CDelay ₂ 0 set the delay = Minimum c = Default chro = Maximum c aps the Cb at	ificant bits o on with bits ificant bits o r. Default v the luma and 5 CDelay ₁ 1 for the chron chroma delay, ma delay, 11 hroma delay,	f the 10-bit v 7-0 in registe f the 10-bit v alue B4 _H d chroma del 4 CDelay ₀ 1 ma signals, a 5, 0 pixels. pixels. 15 pixels.	value. See de er 01 _H , set the value. See de ay at the from 3 CSwapI 0 s follows:	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂ 1	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀
YClamp _{9.8} : Address 04 _H : The seven bits Bit Mnemonic Default value CDelay ₃₋₀ :	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1 These bits $0_{\rm H} =$ $B_{\rm H}^* =$ $F_{\rm H} =$ This bit sw $0^* =$	he most sign in conjuncti he most sign trol Register trol Register cDelay ₂ 0 set the delay Minimum c Default chro aps the Cb an chroma cor	ificant bits o on with bits ificant bits o r. Default va the luma and 5 CDelay ₁ 1 for the chron chroma delay, 11 hroma delay, 7	f the 10-bit v 7-0 in register f the 10-bit v alue $B4_H$ d chroma del 4 CDelay ₀ 1 ma signals, a , 0 pixels. pixels. 15 pixels. nents at the i swapped (no	value. See de er 01 _H , set the value. See de ay at the fror 3 CSwapI 0 s follows:	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂ 1	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀
YClamp _{9.8} : Address 04 _H : The seven bits Bit Mnemonic Default value CDelay ₃₋₀ : CSwapI:	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1 These bits $0_{H} =$ $B_{H}^{*} =$ $F_{H} =$ This bit sw $0^{*} =$ 1 =	he most sign in conjuncti he most sign trol Register a register set 6 CDelay ₂ 0 set the delay = Minimum con = Default chros = Maximum con aps the Cb an = Chroma con	ificant bits o on with bits ificant bits o r. Default v the luma and 5 CDelay ₁ 1 for the chron chroma delay, 11 hroma delay, 11 hroma delay, 11 hroma delay, 13 hroma delay, 14	f the 10-bit v 7-0 in register f the 10-bit v alue $B4_H$ d chroma del 4 CDelay ₀ 1 ma signals, a , 0 pixels. pixels. 15 pixels. 15 pixels. nents at the i swapped (reverse	value. See de er 01 _H , set the value. See de ay at the from 3 CSwapI 0 s follows:	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂ 1	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀
YClamp _{9.8} : Address 04 _H : The seven bits Bit Mnemonic Default value CDelay ₃₋₀ : CSwapI:	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1 These bits $0_{\rm H} =$ $B_{\rm H}^* =$ $F_{\rm H} =$ This bit sw $0^* =$ 1 = These bits	he most sign in conjuncti he most sign trol Register (register set 6 CDelay ₂ 0 set the delay = Minimum c = Default chro = Maximum c aps the Cb an = Chroma cor = Chroma cor set the delay	ificant bits o on with bits ificant bits o r. Default va the luma and 5 CDelay ₁ 1 for the chron chroma delay, 11 hroma delay, 11 hroma delay, 11 hroma delay, 11 hroma delay, 3 md Cr compo nponents not nponents swa for the luma	f the 10-bit v 7-0 in register f the 10-bit v alue B4 _H d chroma del 4 CDelay ₀ 1 ma signals, a , 0 pixels. 15 pixels. 15 pixels. iswapped (no apped (revers signal, as fo	value. See de er 01 _H , set the value. See de ay at the from 3 CSwapI 0 s follows:	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂ 1	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀
	These are t These bits, These are t DELAY Con in the DELAY 7 CDelay ₃ 1 These bits $0_{\rm H} =$ $B_{\rm H}^* =$ $F_{\rm H} =$ This bit sw $0^* =$ 1 = These bits $0_{\rm H} =$	he most sign in conjuncti he most sign trol Register a register set a CDelay ₂ 0 set the delay a Minimum c Default chro a Default chro a chroma cor chroma cor set the delay a chroma cor set the delay	ificant bits o on with bits ificant bits o r. Default v the luma and 5 CDelay ₁ 1 for the chron chroma delay, 11 hroma delay, 11 hroma delay, 11 hroma delay, 13 hroma delay, 14	f the 10-bit v 7-0 in register f the 10-bit v alue B4 _H d chroma del 4 CDelay ₀ 1 ma signals, a 5, 0 pixels. 15 pixels. 15 pixels. 15 pixels. iswapped (no apped (revers signal, as fo pixels.	value. See de er 01 _H , set the value. See de ay at the from 3 CSwapI 0 s follows:	e clamp level escription of re- escription of re- nt end, as show 2 YDelay ₂ 1	egister $02_{\rm H}$ for the luma egister $01_{\rm H}$ for with below: 1 YDelay ₁	or details. signal. or details. 0 YDelay ₀

The six bits in the	he MODE1	register contro	ol various dein	terlacing fu	inctions, as sho	wn below:							
Bit	7	6	5	4	3	2	1	0					
Mnemonic	Fm2430	Х	Test	Test	DCDiOn	FilmOn	NMOvr	NoMen					
Default value	R/O	Х	0	0	1	1	0	0					
Fm2430:	This read	-only bit indic	ates the type of	of film mod	e detected, as f	ollows:							
	This read-only bit indicates the type of film mode detected, as follows: 0 = 2.2 pulldown detected. This is the normal mode when the video source is 625 line PAL. Note that 2:2 pulldown in NTSC indicates a 30 fps film source. This mode will only be active if the F30Hz bit in register 06_{H} is set high.												
	1	= 3:2 pulldov		his indicate	es 24 fps film in		s mode is not	active					
х:	This bits	is not used ar	nd does not ph	ysically ex	st.								
Test:	These bit	s turn on spec	cial test function	ons, as folle	ows:								
	0*	= Normal me	ode.										
	1	= Test mode,	, not for norm	al use.									
DCDiOn:	This bit c	controls the op	peration of the	interpolate	or, as follows:								
	0	= DCDi OFF	. Vertical inter	polation is	ised.								
	1*	= DCDi ON.	Diagonal Cor	relation inte	erpolation is use	ed.							
FilmOn:	This bit c	ontrols the op	eration of the	film mode o	letector, as foll	ows:							
	0	This bit controls the operation of the film mode detector, as follows: 0 = Film mode detector is disabled, all signals processed as video.											
	1*	= Film mode	detector is en	abled, film	and video sour	ced signals a	re processed s	separately.					
NMOvr:	This bit c	ontrols the op	eration of the l	FLI2200, as	follows:								
	0*	= Operating	mode is detern	nined by the	e setting of the	NOMEM pin	ı, pin 52.						
	1 of the NC	= Operating : MEM pin, pir		nined by th	e setting of the	NoMem bit,	overriding th	e setting					
NoMem:	This bit c	ontrols the op	eration of the l	FLI2200, as	follows:								
		cing modes, i.	e., motion ada	aptive video	eld memories a deinterlacing pulldown for	and full fran	ne film sourc						
	1 external	= The FLI22	00 is forced in owing the FLI	nto the intra	a-field only dea used in low-co	interlacing m	ode, which r	-					

Bit	7	6	5	4	3	shown below: 2	1	0
Mnemonic	CSync	VITSEn	F30Hz	F30Inv	Force30	Motion ₁	Motion ₀	PComp
Default value	0	0	0	0	0	1	0	1
CSync:	This bit co	ontrols the out	nut syncs as	follows as	follows			
0.5,110	0* :	= Horizontal s NC/CREFO o	sync appears			t and vertical	sync on the	
		= Composite : NC/CREFO or		on the H/CS	SYNCO outp	ut and compo	site reference	on the
VITSEn:	This bit co	ontrols the use	of the film	mode flag w	hich sometim	es appears or	n line 22, as fo	ollows:
	0* :	= Film mode	flag is ignor	ed and the ir	iternal film m	node detector	is operational	l .
	1 :	= Film mode	flag is used t	to control fil	m mode in th	e deinterlacer	:	
F30Hz:	This bit co as follows:	ontrols the filr	n mode dete	ctor when th	e signal come	es from a 525	line (NTSC)	source,
	,	= Disabled the This prevents film. Note th	the accident	al detection	of this mode	when the sou	rce is video, r	
		= Allow detec			-			
F30Inv:		ontrols the 30 = 1), as follow		ration when	the field flag	input is used	for frame det	ection
	0* :	= FLDIN $= 1$	identifies fir	st field in fra	ame.			
	1 :	= FLDIN $=$ 0	identifies fir	rst field in fra	ame.			
Force30:	This bit co	ontrols the 30	fps film ope	ration, as fol	lows:			
	0* :	= 30 fps film	mode operat	ion controlle	d by internal	film mode de	etector.	
	1 :	= 30 fps film	mode operat	ion controlle	d by FLDIN	signal.		
Motion ₁₋₀ :	These bits	set the motio	n processing	mode in the	e deinterlacer,	as follows:		
	Motio	n ₁₋₀ Mode						
	(0x Test n	node.					
		10* Norm	al operation					
		11 Test n	node.					
PComp:	This bit co	ontrols the ope	eration of the	e PAL line av	verager, as fol	llows:		
	0 =	= PAL line ave	erager will be	e operational	when 625 line	e (PAL) sourc	e signals are d	etected.
	signal	= PAL line ave s which have re line averagi	never been e	encoded into	composite PA			

The eight bits in		-		4				0
Bit	7 CSwar	6 ChrPhs	5 CIntDia	•	3 OEmatOr m	2 OFormat	1 OEorrmat	0 OEcomot
Mnemonic	CSwap		CIntDis	OBlnkEn	OFmtOvr	OFormat ₂	OFormat ₁	OFormat _o
Default value	0	0	0	1	0	0	0	0
CSwap:	This bit c follows:	controls the sec	quence of the	e chroma outp	outs prior to d	emultiplexing	g at the outpu	it, as
	0*	= Normal mo on the corres	-			Cb/Cr modes	and Cr and	Cb appear
	1	= Inverted co swapped in th			r signals will	be switched.	R and B wil	l also be
ChrPhs:	This bit	delays the chr	oma output i	n the Y/Cb/C	Cr mode, as fo	ollows:		
	0*	= Normal mo						
	1	= Chroma ou	tput is delay	ed by two lui	ma pixels/one	chroma pixe	1.	
CIntDis:	This bit c	controls the ch	roma interpo	olator, as follo	ows:			
	0*	= Chroma int	-			ed to generate	e 4:4:4 Y Cr (Cb outputs.
	1	= Chroma int						
		selected for a	ll 4:2:2 outp	ut formats.				
	Note: Sel	ecting the 4:4:	4 R G B outp	ut mode autor	matically enal	oles the chrom	a interpolato	r.
OBlnkEn:	This bit c	controls the ou	tput blanking	g, as follows:	:			
	0	= Output blan	-	-		be the same as	s the input in	the
		king regions.		1 (7)				
	1* regai	= Output blar dless of the in		1. The output	t signal will b	e blanked in t	he blanking r	regions
	8		-r 8					
OFmtOvr :	The OFm	ntOvr bit is use		-				
	0* pins	= The FLI220 59-61. The for						
	1	= The FLI220					2-0	
	-	this register,						_0 erre m
OFormat .	Those bit	s are used to d	lafing the for	mot of the or	tout signals	as follows:		
OFormat ₂₋₀ :			ut signal forn		itput signais,	as tonows.		
	010	2-0 -	B (4:4:4)	iat				
			rCb(4:2:2)					
				/Cr (double ra	ate D1, with ex	xternal/senara	te syncs)	
					te D1, with en			
			b Pr (4:2:2)	(0/	
		100 P						
			Cb Cr (4:4:4)	1				
			t mode					
	The busse	es used for the		signals (Cb/C	r and Y/Cb/C	r) in modes 0	1x and 101 ar	·e
		ed by the settir						

Address 08 _H : I	OSEL (IOSE	Lect) Contr	ol Register. D	efault value	52 _H			
The eight bits in						s, and set the	film sync del	ay in the
film mode detec	tor, as shown	below:					-	-
Bit	7	6	5	4	3	2	1	0
Mnemonic	D1Valid	CInSel	COutSel	D1InSel ₁	D1InSel ₀	FSyncDel ₂	FSyncDel ₁	FSyncDel ₀
Default value	R/O	1	0	1	0	0	1	0
D1Valid:	This bit inc is set as fol		llidity of the i	nput in Y/Cb	/Cr (D1) mod	le. It is a read	only function	n. This bit
	0 =	= The FLI22	00 has not bee	en able to loc	k onto the inp	out signal.		
	1 =	= The FLI22	00 has locked	onto the inpu	ıt signal.	_		
CInSel:	This bit sel mode, as fo		bus is used fo	or the multip	lexed chroma	input signal i	in the Y Cb/	Cr input
	0 =	= Multiplexe	d chroma sig	nal Cb/Cr is	input on the	B/CbIN bus.		
	1* =	= Multiplexe	d chroma sig	nal Cb/Cr is	input on the	R/CrIN bus.		
COutSel:	This bit sel mode, as fo		ous is used fo	r the multipl	exed chroma	output signal	in the Y Cb	/Cr output
	0* =	= Multiplexe	d chroma sigr	nal Cb/Cr is o	output on the l	B/CbOUT bus		
		Multiplexee	d pseudo-D1 s	signal Y/Cb/0	Cr is output of	n the R/CrOU'	T bus.	
	1 =	= Multiplexe	d chroma sigr	al Cb/Cr is o	utput on the I	R/CrOUT bus.		
		Multiplexee	d pseudo-D1 s	signal Y/Cb/0	Cr is output o	n the B/CbOU	T bus.	
D1InSel ₁₋₀ :	These bits	set the input	t bus used for	the D1 (Y/C	Cb/Cr) multip	lexed input si	gnal, as follo	ows:
	D1InSel ₁₋₀	D1 bus						
	00	G/Y						
	01	G/Y						
	10*	B/Cb						
	11	R/Cr						
FSyncDel ₃₋₀ :	These bits	set the delay	in the film n	node detector	r, as follows:			
	0 _H =	= Minimum	film sync dela	ay, zero field	s.			
		= Default filı	n sync delay,	2 fields.				
			ilm sync dela					
	11	= Not valid.	• •					
	11							

Address 09 _H : I The two bits in		gister set the	gain of the ir	nut signals a	fter sync rem	oval as show	n below [.]	
Bit	7	6	5	4	3	2	1	0
Mnemonic	X	x	x	x	x	z X	YInGain	CInGain
Default value	0	0	0	0	0	0	1	1
YInGain:	This bit set	ts the gain of	the luma in	put path, as fo	ollows:			
		= Gain = 1. nput signal h			when there is	no sync on the	he input sign	al and the
						e is sync on t e after sync re		al,
CInGain:		-	-	out path, as fo	-	-		
				nust be used v a full scale 1		no sync on th	he luma inpu	t signal
		-	•		•	e is sync on t	he luma inpu	t signal if
				atches that of		•	ne runiu inpu	it bighter if
Note that SOnY	G, bit 5 in reg	gister 00 _H , ov	errides these	bits when it i	s set low, forc	ing the gains	to 1.	
Address 0A _H : The eight bits in shown below:	G, bit 5 in reg BSStart (B land the BSStart (gister 00 _H , ov anking S amp register set th	errides these ling Start) C the start of the	bits when it i C ontrol Regi s sampling per	s set low, forcester. Default	ting the gains value 02_H prizontal blan	king level det	
Address 0A _H : The eight bits in shown below: Bit	G, bit 5 in reg BSStart (Bla n the BSStart 7	gister 00 _H , ov anking S amp register set th 6	errides these ling Start) C the start of the 5	bits when it i C ontrol Regis sampling per 4	s set low, ford ster. Default riod for the ho	ting the gains to value 02 _H prizontal bland 2	king level det 1	0
Address 0A _H : The eight bits in shown below:	G, bit 5 in reg BSStart (B land the BSStart (gister 00 _H , ov anking S amp register set th	errides these ling Start) C the start of the 5	bits when it i C ontrol Regi s sampling per	s set low, ford ster. Default riod for the ho	ting the gains value 02_H prizontal blan	king level det 1	0
Address 0A _H : The eight bits in shown below: Bit Mnemonic	G, bit 5 in reg BSStart (Bl a the BSStart 7 BSStart ₇ 0 These bits	gister 00 _H , ov anking S amp register set th 6 BSStart ₆ 1 set the start o	errides these ling Start) C the start of the 5 BSStart ₅ 0 f the 32-pixe	bits when it i Control Regis sampling per 4 BSStart ₄ 0 I sampling pe	s set low, ford ster. Default riod for the ho 3 BSStart ₃ 1 riod for the b	ting the gains to value 02 _H prizontal bland 2 BSStart ₂	king level det 1 BSStart ₁ 1 detector. The	0 BSStart ₀ 0
Address 0A _H : The eight bits in shown below: Bit Mnemonic Default value	TG, bit 5 in reg BSStart (Bla in the BSStart 7 BSStart ₇ 0 These bits adjustment follows:	gister $00_{\rm H}$, ov anking S amp register set th 6 BSStart ₆ 1 set the start o is in 1 pixel	errides these ling Start) C the start of the 5 BSStart ₅ 0 f the 32-pixe increments	bits when it i Control Regis sampling per 4 BSStart ₄ 0 I sampling pe	s set low, force ster. Default riod for the ho 3 BSStart ₃ 1 riod for the b e start of the	ting the gains z value 02_H prizontal bland 2 BSStart ₂ 0 lanking level	king level det 1 BSStart ₁ 1 detector. The	0 BSStart ₀ 0
Address 0A _H : The eight bits in shown below: Bit Mnemonic Default value	G, bit 5 in reg BSStart (Bla n the BSStart 7 BSStart ₇ 0 These bits adjustment follows: BSStar	gister 00 _H , ov anking S amp register set th BSStart ₆ 1 set the start o ∶ is in 1 pixel rtN ₇₋₀	errides these ling Start) C the start of the 5 BSStart ₅ 0 f the 32-pixe increments Timing re	bits when it i Control Regis sampling per 4 BSStart ₄ 0 l sampling per relative to the	s set low, force ster. Default riod for the ho 3 BSStart ₃ 1 riod for the b e start of the	ting the gains z value 02_H prizontal bland 2 BSStart ₂ 0 lanking level	king level det 1 BSStart ₁ 1 detector. The	0 BSStart ₀ 0
Address 0A _H : The eight bits in shown below: Bit Mnemonic Default value	G, bit 5 in reg BSStart (Bla n the BSStart 7 BSStart ₇ 0 These bits adjustment follows: BSStar	gister $00_{\rm H}$, ov anking Samp register set th BSStart ₆ 1 set the start o : is in 1 pixel rtN ₇₋₀ $00_{\rm H}$	errides these ling Start) C the start of the 5 BSStart ₅ 0 f the 32-pixe increments	bits when it i Control Regis sampling per 4 BSStart ₄ 0 l sampling per relative to the	s set low, force ster. Default riod for the ho 3 BSStart ₃ 1 riod for the b e start of the	ting the gains z value 02_H prizontal bland 2 BSStart ₂ 0 lanking level	king level det 1 BSStart ₁ 1 detector. The	0 BSStart ₀ 0
Address 0A _H : The eight bits in shown below: Bit Mnemonic Default value	G, bit 5 in reg BSStart (Bla n the BSStart 7 BSStart ₇ 0 These bits adjustment follows: BSStart (gister 00 _H , ov anking S amp register set th BSStart ₆ 1 set the start o ∶ is in 1 pixel rtN ₇₋₀	errides these ling Start) C the start of the 5 BSStart ₅ 0 f the 32-pixe increments Timing re 0 pixels	bits when it i Control Regis sampling per 4 BSStart ₄ 0 I sampling per relative to the elative to start	s set low, force ster. Default riod for the ho 3 BSStart ₃ 1 riod for the b e start of the	ting the gains z value 02_H prizontal bland 2 BSStart ₂ 0 lanking level	king level det 1 BSStart ₁ 1 detector. The	0 BSStart 0

Address 10 _H : I		•	1	1 •	. 1			
The eight bits in from a 525 line		-		e output horiz	zontal sync pi	lise when the	input signal	comes
Bit	7	6	5	4	3	2	1	0
Mnemonic	HSStartN ₇	HSStartN ₆	HSStartN ₅	HSStartN ₄	HSStartN ₃	HSStartN ₂	HSStartN ₁	HSStartN
Default value	0	0	0	0	0	0	0	0
HSStartN ₇₋₀ :	line (NTSC	C) source. The ments relative	he number is	a signed, tw	o's compleme	en the input si ent value. Th s signal as sho	e adjustmen	t is in 1
	HSSta	rtN ₇₋₀	Timing re	elative to defa	ault value			
	8	80 _H	–128 pixe	els				
	(00 _H *	Default ti	ming				
	T HSSPN (Hor	izontal S ync	+127 pixel StoP/NTSC)	ls Control Re				comes
The eight bits i	T HSSPN (Hor n the HSSPN	izontal S ync register set t	+127 pixel StoP/NTSC) the end of the	ls Control Re				l comes
The eight bits i from a 525 line	T HSSPN (Hor n the HSSPN	izontal S ync register set t	+127 pixel StoP/NTSC) the end of the	ls Control Re	zontal sync p			l comes 0
The eight bits i from a 525 line Bit	T HSSPN (Hor n the HSSPN (NTSC) sour 7	izontal S ync register set t rce, as shown 6	+127 pixel StoP/NTSC) the end of the below: 5	ls Control Re e output horiz 4	zontal sync pr 3	ulse when the	input signal	0
Address 11 _H : The eight bits i from a 525 line Bit Mnemonic Default value	T HSSPN (Hor n the HSSPN (NTSC) sour 7	izontal S ync register set t rce, as shown 6	+127 pixel StoP/NTSC) the end of the below: 5	ls Control Re e output horiz 4	zontal sync pr 3	ulse when the	input signal	0
The eight bits i from a 525 line Bit Mnemonic	HSSPN (Hor n the HSSPN (NTSC) sour 7 HSStopN ₇ 0 These bits line (NTSC	$F_{\rm H}$ izontal S ync register set t rce, as shown 6 HSStopN ₆ 0 set the end of C) source. The ments relativ	+127 pixel StoP/NTSC) the end of the below: 5 HSStopN ₅ 0 f the output h he number is	ls Control Re e output horiz 4 HSStopN ₄ 0 torizontal sym a signed, two	zontal sync pr 3 HSStopN ₃ 0 ac pulse when o's complement	ulse when the 2 HSStopN ₂	input signal 1 HSStopN ₁ 0 nal comes frue adjustmen	0 HSStopN ₀ 0 om a 525 t is in 1
The eight bits i from a 525 line Bit Mnemonic Default value	HSSPN (Hor n the HSSPN (NTSC) soun 7 HSStopN ₇ 0 These bits line (NTSC pixel incre	$F_{\rm H}$ izontal S ync register set t cce, as shown 6 HSStopN ₆ 0 set the end or C) source. The ments relativas as follows:	+127 pixel StoP/NTSC) the end of the a below: 5 HSStopN ₅ 0 f the output h he number is re to the defa	ls Control Re e output horiz 4 HSStopN ₄ 0 torizontal sym a signed, two	zontal sync pr 3 HSStopN ₃ 0 ac pulse when o's complement timing of this	ulse when the 2 HSStopN ₂ 0 the input sig ent value. Th	input signal 1 HSStopN ₁ 0 nal comes frue adjustmen	0 HSStopN ₀ 0 om a 525 t is in 1
The eight bits i from a 525 line Bit Mnemonic Default value	HSSPN (Hor n the HSSPN (NTSC) soun 7 HSStopN ₇ 0 These bits line (NTSC pixel incre diagrams, a HSSto	$F_{\rm H}$ izontal Sync register set t ce, as shown 6 HSStopN ₆ 0 set the end of C) source. The ments relative as follows: pN_{7-0} $30_{\rm H}$	+127 pixel S to P/NTSC) the end of the h below: 5 HSStopN ₅ 0 f the output h he number is re to the defa Timing re -128 pixe	ls Control Re e output horiz 4 HSStopN ₄ 0 orizontal sym- a signed, two ult standard to elative to defa- els	zontal sync pr 3 HSStopN ₃ 0 ac pulse when o's complement timing of this	ulse when the 2 HSStopN ₂ 0 the input sig ent value. Th	input signal 1 HSStopN ₁ 0 nal comes frue adjustmen	0 HSStopN ₀ 0 om a 525 t is in 1
The eight bits i from a 525 line Bit Mnemonic Default value	HSSPN (Hor n the HSSPN (NTSC) soun 7 HSStopN ₇ 0 These bits line (NTSC pixel incre diagrams, a HSSto	$F_{\rm H}$ izontal Sync register set t rce, as shown 6 HSStopN ₆ 0 set the end of C) source. The ments relatival as follows: pN ₇₋₀	+127 pixel StoP/NTSC) the end of the a below: 5 HSStopN ₅ 0 f the output h he number is re to the defa Timing re	ls Control Re e output horiz 4 HSStopN ₄ 0 orizontal sym- a signed, two ult standard to elative to defa- els	zontal sync pr 3 HSStopN ₃ 0 ac pulse when o's complement timing of this	ulse when the 2 HSStopN ₂ 0 the input sig ent value. Th	input signal 1 HSStopN ₁ 0 nal comes frue adjustmen	0 HSStopN ₀ 0 om a 525 t is in 1

Address 12 _H : H	IRSTN (Hori	zontal R efere	ence StarT/N	rsc) Control	Register. De	fault value 0	0,,	
The eight bits in comes from a 52	the HRSTN	register set t	he start of the	e output horiz				signal
Bit	7	6	5	4	3	2	1	0
Mnemonic	HRStartN ₇	HRStartN ₆	HRStartN ₅	$HRStartN_4$	HRStartN ₃	HRStartN ₂	HRStartN ₁	HRStartN ₀
Default value	0	0	0	0	0	0	0	0
HRStartN ₇₋₀ :	525 line (N	TSC) source ments relative	. The number	r is a signed, t	wo's complet	when the inp ment value. T ignal as show	The adjustme	nt is in 1
	HRSta	rtN ₇₋₀	Timing re	elative to defa	ault value			
	8	80 _H	–128 pixe	els				
	(00 _H *	Default ti	ming				
	7	7F _H	+127 pixel	ls				
Address 13_{H} : H The eight bits in from a 525 line (the HRSPN	register set tl	he end of the					gnal comes
Bit	7	6	5	4	3	2	1	0
Mnemonic	HRStopN ₇	HRStopN ₆	HRStopN5	$HRStopN_4$	HRStopN ₃	$HRStopN_2$	HRStopN ₁	$\mathrm{HRStopN}_{0}$
Default value	0	0	0	0	0	0	0	0
HRStopN ₇₋₀ :	525 line (N	TSC) source ments relative	. The number	r is a signed, t	wo's complet	when the inp ment value. T ignal as show	The adjustme	nt is in 1
			Timing ro	elative to defa	ault value			
	HRSto	pN ₇₋₀	rinning re					
		90 ₇₋₀ 80 _H	–128 pixe		un value			
	8	1.0	-	els				

the input signal Bit	7	6	5	4	3	2	1	0
Mnemonic			•	VSStopN	VRStartN ₅			
Default value	0	0	0	0	0	0	0	0
VSStartN ₅₋₄ :	when the in		mes from a 5	25 line (NTS	t 15 _H , set the s C) source. Thails.			
VSStopN ₅₋₄ :	when the i		omes from a	525 line (NT	15 _H , set the e SC) source. For details.			
VRStartN ₅₋₄ :	signal whe	n the input si	ignal comes	from a 525 li	er 16 _H , set the ne (NTSC) so 6 _H for details	ource. These		
VRStopN ₅₋₄ :	signal whe	en the input si	ignal comes	from a 525 li	r 16 _H , set the ne (NTSC) so 6 _H for details	ource. These		
The eight bits i	n the VSTN 1	register set th	e start and e	nd of the out			en the input	signal
The eight bits i comes from a 5 Bit	n the VSTN 1 25 line (NTS 7	register set th C) source, as 6	e start and e shown below 5	nd of the out w: 4	put vertical s	ync pulse wh	1	0
The eight bits i comes from a 5 Bit Mnemonic	n the VSTN 1 25 line (NTS 7	register set th C) source, as 6	e start and e shown below 5	nd of the out w: 4	put vertical s	ync pulse wh	1	0
Address 15 _H : The eight bits i comes from a 5 Bit Mnemonic Default value VSStartN ₃₋₀ :	n the VSTN n 25 line (NTS 7 VSStartN ₃ 0 These bits, pulse wher complement of this sign VSSta 2 (register set th C) source, as 6 VSStartN ₂ 0 , in conjuncti n the input sig nt value. The nal as shown	the start and expression is shown below 5 VSStartN ₁ 0 on with bits 2 gnal comes for adjustment in the timing	nd of the out v: 4 VSStartN ₀ 0 7-6 in registe rom a 525 lin is in 1 line i g diagrams, a lative to defa	put vertical s 3 VSStopN ₃ 0 or 14 _H , set the he (NTSC) so ncrements rel s follows:	ync pulse wh 2 VSStopN ₂ 0 start of the c urce. The nu	1 VSStopN ₁ 0 putput vertica umber is a sig	0 VSStopN 0 Il sync gned, two's
The eight bits i comes from a 5 Bit Mnemonic Default value	n the VSTN n 25 line (NTS 7 VSStartN ₃ 0 These bits, pulse when complement of this sign VSSta 2 (1 These bits, when the it complement of this sign	register set th C) source, as 6 VSStartN ₂ 0 , in conjuncti in the input sign nt value. The ral as shown rtN ₅₋₀ $20_{\rm H}$ $00_{\rm H}^*$ $1F_{\rm H}$ in conjunction nput signal control of the ral as shown	e start and ex shown below 5 VSStartN ₁ 0 on with bits 7 gnal comes fi e adjustment in the timing Timing re -32 lines Default tin +31 lines on with bits 5 omes from a e adjustment in the timing	nd of the out v: 4 VSStartN ₀ 0 7-6 in register rom a 525 lin is in 1 line i g diagrams, a lative to defa ming 5-4 in register 525 line (NT) is in 1 line i g diagrams, a	put vertical s 3 VSStopN ₃ 0 or 14 _H , set the le (NTSC) so ncrements rel s follows: ult value 14_{H} , set the of CSC) source. ncrements rel s follows:	ync pulse wh 2 VSStopN ₂ 0 start of the c urce. The nu ative to the c end of the out The number	1 VSStopN ₁ 0 putput vertica umber is a sig lefault standa	0 VSStopN 0 al sync gned, two's ard timing sync pulse two's
The eight bits i comes from a 5 Bit Mnemonic Default value VSStartN₃₋₀:	n the VSTN n 25 line (NTS 7 VSStartN ₃ 0 These bits, pulse wher complement of this sign VSSta 2 (1) These bits, when the in complement of this sign VSSto	register set th C) source, as 6 VSStartN ₂ 0 , in conjuncti in the input sign nt value. The hal as shown rtN ₅₋₀ $20_{\rm H}$ $20_{\rm H}$ $20_{\rm H}$ $10_{\rm H}^*$ $1F_{\rm H}$, in conjunction nput signal cont rt value. The hal as shown pN_{5-0}	e start and ex shown below 5 VSStartN ₁ 0 on with bits 7 gnal comes fi e adjustment in the timing Timing re -32 lines Default tin +31 lines on with bits 5 omes from a e adjustment in the timing Timing re	nd of the out w: 4 VSStartN ₀ 0 7-6 in register rom a 525 lin is in 1 line i g diagrams, a lative to defa ming 5-4 in register 525 line (NT) is in 1 line i	put vertical s 3 VSStopN ₃ 0 or 14 _H , set the le (NTSC) so ncrements rel s follows: ult value 14_{H} , set the of CSC) source. ncrements rel s follows:	ync pulse wh 2 VSStopN ₂ 0 start of the c urce. The nu ative to the c end of the out The number	1 VSStopN ₁ 0 putput vertica umber is a sig lefault standa	0 VSStopN 0 al sync gned, two's ard timing sync pulse two's
The eight bits i comes from a 5 Bit Mnemonic Default value VSStartN₃₋₀:	n the VSTN n 25 line (NTS 7 VSStartN ₃ 0 These bits, pulse wher complement of this sign VSSta 2 (1) These bits, when the in complement of this sign VSSto 2 2	register set th C) source, as 6 VSStartN ₂ 0 , in conjuncti in the input sign nt value. The ral as shown rtN ₅₋₀ $20_{\rm H}$ $00_{\rm H}^*$ $1F_{\rm H}$ in conjunction nput signal control of the ral as shown	e start and ex shown below 5 VSStartN ₁ 0 on with bits 7 gnal comes fi e adjustment in the timing Timing re -32 lines Default tin +31 lines on with bits 5 omes from a e adjustment in the timing	nd of the out w: 4 VSStartN ₀ 0 7-6 in register rom a 525 lin is in 1 line i g diagrams, a lative to defa ming 5-4 in register 525 line (NT is in 1 line i g diagrams, a lative to defa	put vertical s 3 VSStopN ₃ 0 or 14 _H , set the le (NTSC) so ncrements rel s follows: ult value 14_{H} , set the of CSC) source. ncrements rel s follows:	ync pulse wh 2 VSStopN ₂ 0 start of the c urce. The nu ative to the c end of the out The number	1 VSStopN ₁ 0 putput vertica umber is a sig lefault standa	0 VSStopN 0 al sync gned, two's ard timing sync pulse two's

comes from a 5.	n the VRTN re 25 line (NTSC			Ĩ		-		-
Bit	7	6	5	4	3	2	1	0
Mnemonic	VRStartN ₃	VRStartN ₂	VRStartN ₁	VRStartN ₀	VRStopN ₃	VRStopN ₂	VRStopN ₁	VRStopN ₀
Default value	0	0	0	0	0	0	0	0
VRStartN ₃₋₀ :	signal whe complemen of this sign VRSta	n the input sint value. The nal as shown	gnal comes e adjustment in the timing	from a 525 li		ource. The n	umber is a si	gned, two's
	0	00 _H *	Default ti	ming				
	3	8F _H	+31 lines					
VRStopN ₃₋₀ :	signal whe complement	n the input sint the input site of the second se	gnal comes e adjustment	from a 525 li	14 _H , set the end ne (NTSC) so ncrements rel s follows:	ource. The n	umber is a si	gned, two's
	VRSto	2 0	-	lative to defa	ult value			
		Ю _Н	-32 lines					
		00 _H *	Default ti	ming				
	3	8F _H	+31 lines					
Address 17 _H : N The six bits in t from a 525 line	he VBIMSN r	egister are th	e most signif				en the input s	ignal comes
Bit	7	6	5	4	3	2	1	0
Mnemonic	х	VBStartN ₄			VBIStartN ₅			
Default value	Х	0	х	0	0	0	0	0
VBStartN ₄ :	signal when	n the input sig	gnal comes fi		e _H , set the star (NTSC) source (atails.			
VBStopN ₄ :	when the ir		mes from a 5	25 line (NTS	θ _H , set the end C) source. Th			
	through sig	nal when the	input signal	comes from a	19 _H , set the s 525 line (NT register 19 _H	SC) source.		
VBIStartN ₅₋₄ :	significant							

Address 18 _H : V							han dha ina	(. . 1
The eight bits in comes from a 52				d of the outp	ut vertical bla	nking signal	when the inp	ut signal
Bit	7	6	5	4	3	2	1	0
Mnemonic	VBStartN ₃	VBStartN ₂	VBStartN ₁	VBStartN ₀	VBStopN ₃	VBStopN ₂	VBStopN ₁	VBStopN ₀
Default value	0	0	0	0	0	0	0	0
VBStartN ₃₋₀ :	when the in complement	put signal control to the second s	mes from a 5 e adjustment	25 line (NTS	_H , set the star C) source. Th ncrements rel s follows:	ne number is a	a signed, two	's
	VBSta	rtN ₄₋₀	Timing re	lative to defa	ault value			
	1	0 _H	-16 lines					
	0	00 _H *	Default ti	ning				
	0)F _H	+15 lines					
VBStopN ₃₋₀ :	when the in complement	put signal control to the second s	mes from a 5 e adjustment	25 line (NTS	_H , set the end C) source. Th ncrements rel s follows:	ne number is a	a signed, two	's
	VBSto	pN ₅₋₀	Timing re	lative to defa	ult value			
	1	0 _H	-16 lines					
	0	00 _H *	Default ti	ning				
	0)F _H	+15 lines					

Address 19 _H : V	VBITN (VBI d	lata T iming/N	NTSC) Contr	ol Register. I	Default value	28 _H		
The eight bits i signal comes fr	n the VBTN r	egister set the	e start and er	nd of the outp			signal when t	he input
Bit	7	6	5	4	3	2	1	0
Mnemonic	VBIStartN ₃	VBIStartN ₂	VBIStartN ₁	VBIStartN ₀	VBIStopN ₃	VBIStopN ₂	VBIStopN ₁	VBIStopN ₀
Default value	0	0	1	0	1	0	0	0
VBIStartN ₃₋₀ :	through sig contiguous lines. The relative to t VBISta 2 0	nal when the group of lin number is a s he default sta	input signal es during the igned, two's andard timing	comes from a VBI period complement g of this signa elative to defa	525 line (NT to be unblank value. The ad l as shown in	start of the ou 'SC) source. ' ted to pass the ljustment is in the timing di	This allows a rough the dat 1 line increr	a selected a on these ments
VBStopN ₃₋₀ :	through sig contiguous lines. The relative to t VBSto 2 0	nal when the group of lin number is a s he default sta	input signal es during the igned, two's andard timing	comes from a VBI period complement g of this signa elative to defa	to be unblank to be unblank value. The ad l as shown in	end of the out 'SC) source. ' ted to pass the ljustment is in the timing di	This allows a rough the dat 1 line increr	a selected a on these ments
Address 20_H: 1 The eight bits i a 625 line (PAL Bit	n the HSSTP i	register set th			ontal sync pu		input signal c 1	comes from 0
Mnemonic						HSStartP ₂		
Default value						0		
HSStartP ₇₋₀ :	pulse when complemen this signal a HSStar 2 0	the input signt value. The as shown in t	nal comes fro adjustment i he timing dia	om a 625 line s in 1 pixel in grams, as fol elative to defa ls ming	(PAL) source crements rela lows:	start of the ou e. The numbe tive to the def	r is a signed,	two's

The eight bits is 625 line (PAL)								
Bit			5	4	3	2	1	0
Mnemonic	HSStopP_	HSStopP.	HSStopP.	HSStopP.	HSStopP.	2 HSStopP ₂	HSStopP.	HSStopP
Default value	0	0	0	0	0	0	0	0
HSStopP ₇₋₀ :	pulse wher complemen this signal HSSto 2 (the input signt value. The as shown in t	adjustment i adjustment i he timing dia Timing re –512 pixe	om a 625 line s in 1 pixel in Igrams, as fol elative to defa ls ming	(PAL) source crements rela lows:	end of the out e. The numbe tive to the def	r is a signed,	two's
Address 22 _H : I The eight bits in from a 625 line	n the HRSTP	register set tl	ne start of the			-	-	gnal comes
Bit	7	6	5	4	3	2	1	0
Mnemonic	HRStartP ₇	HRStartP ₆	HRStartP ₅	$HRStartP_4$	HRStartP ₃	HRStartP	HRStartP.	HRStartP
	signal whe	n the input sig	gnal comes fi	0 3-2 in register rom a 625 line	0 • 24 _H , set the set (PAL) source	0 start of the ou e. The numb	0 tput horizont er is a signed	, two's
	These bits, signal whe complement this signal HRSta	in conjunction n the input signt value. The as shown in t	on with bits 3 gnal comes fr adjustment i he timing dia	0 3-2 in register rom a 625 line is in 1 pixel in agrams, as fol elative to defa ls ming	0 24 _H , set the set (PAL) source crements relations:	0 start of the ou	0 tput horizont er is a signed	al reference , two's
HRStartP ₇₋₀ : Address 23 _H : I The eight bits in from a 625 line	These bits, signal whe complement this signal HRSta (1 HRSPP (Horin the HRSPP)	in conjunction in the input signation to the input signation of the second se	on with bits 3 gnal comes fr adjustment i he timing dia Timing re -512 pixe Default ti +511 pixe	0 3-2 in register rom a 625 line is in 1 pixel in agrams, as fol elative to defa ls ming ls L) Control R	0 24 _H , set the set (PAL) source crements relations: ult value egister. Defa	0 start of the ou e. The numb tive to the def ult value 00 _H	0 tput horizont er is a signed. fault standard	al reference , two's timing of
HRStartP ₇₋₀ : Address 23 _H : I The eight bits it from a 625 line Bit	These bits, signal whe complement this signal HRSta (1 HRSPP (Horin the HRSPP (PAL) source, 7	in conjunction in the input signation that the input signation of the input signation of the input signature of	on with bits 3 gnal comes fi adjustment i he timing dia Timing re -512 pixe Default ti +511 pixe ence StoP/PA he end of the low: 5	0 3-2 in register rom a 625 line is in 1 pixel in agrams, as fol elative to defa ls ming ls L) Control R output horizo	0 24 _H , set the set (PAL) source crements relations: ult value egister. Defationtal reference	0 start of the ou e. The numb tive to the def ult value 00 _H e signal when 2	0 tput horizont er is a signed. fault standard the input sig 1	al reference , two's timing of
HRStartP ₇₋₀ : Address 23 _H : I The eight bits in from a 625 line Bit Mnemonic	These bits, signal whe complement this signal HRSta (1 HRSPP (Horin the HRSPP (PAL) source, 7	in conjunction in the input signation that the input signation of the input signation of the input signature of	on with bits 3 gnal comes fi adjustment i he timing dia Timing re -512 pixe Default ti +511 pixe ence StoP/PA he end of the low: 5	0 3-2 in register rom a 625 line is in 1 pixel in agrams, as fol elative to defa ls ming ls L) Control R output horizo	0 24 _H , set the set (PAL) source crements relations: ult value register. Defa ontal reference	0 start of the ou e. The numb tive to the def ult value 00 _H e signal when 2	0 tput horizont er is a signed. fault standard the input sig 1	al reference , two's timing of mal comes 0
HRStartP ₇₋₀ : Address 23 _H : I The eight bits it from a 625 line Bit Mnemonic Default value	These bits, signal whe complement this signal HRSta (1 HRSPP (Horition the HRSPP (PAL) source, 7 HRStopP ₇ 0 These bits, signal whe complement	in conjunction n the input signation to the input signation of the	on with bits 3 gnal comes fr adjustment i he timing dia Timing re -512 pixe Default ti +511 pixe ence StoP/PA he end of the low: 5 HRStopP ₅ 0 on with bits 1 gnal comes fr adjustment i he timing dia	0 3-2 in register rom a 625 line is in 1 pixel in agrams, as fol elative to defa ls ming ls L) Control R output horizod 4 HRStopP ₄ 0 1-0 in register rom a 625 line is in 1 pixel in agrams, as fol	0 $24_{\rm H}$, set the set (PAL) source acrements relations: ult value egister. Defator ontal reference 3 HRStopP ₃ 0 $24_{\rm H}$, set the set e (PAL) source crements relations: 0	0 start of the ou e. The numb tive to the def ult value 00 _H e signal when 2 HRStopP ₂	0 tput horizont er is a signed. fault standard the input sig 1 HRStopP ₁ 0 put horizonta er is a signed.	al reference , two's timing of times times
HRStartP ₇₋₀ : Address 23 _H : 1 The eight bits it from a 625 line Bit Mnemonic Default value	These bits, signal whe complement this signal HRSta () HRSPP (Horin the HRSPP (PAL) source, 7 HRStopP ₇ 0 These bits, signal whe complement this signal HRSto	in conjunction in the input signation that input signation that the input signation of the second	on with bits 3 gnal comes fr adjustment i he timing dia Timing re -512 pixe Default ti +511 pixe once StoP/PA he end of the low: 5 HRStopP ₅ 0 on with bits 1 gnal comes fr adjustment i he timing dia Timing re	0 3-2 in register rom a 625 line is in 1 pixel in agrams, as fol elative to defa ls ming ls L) Control R output horizo 4 HRStopP ₄ 0 1-0 in register rom a 625 line is in 1 pixel in agrams, as fol elative to defa	0 $24_{\rm H}$, set the set (PAL) source acrements relations: ult value egister. Defator ontal reference 3 HRStopP ₃ 0 $24_{\rm H}$, set the set e (PAL) source crements relations: 0	0 start of the ou e. The numb tive to the def ult value $00_{\rm H}$ e signal when 2 HRStopP ₂ 0 end of the out e. The numb	0 tput horizont er is a signed. fault standard the input sig 1 HRStopP ₁ 0 put horizonta er is a signed.	al reference , two's timing of times times
HRStartP ₇₋₀ : Address 23 _H : I The eight bits it from a 625 line Bit Mnemonic Default value	These bits, signal whe complement this signal HRSta (1) HRSPP (Hori: n the HRSPP (PAL) source, 7 HRStopP ₇ 0 These bits, signal whe complement this signal HRSto	in conjunction in the input signation to the input signation of th	on with bits $\frac{2}{3}$ gnal comes fr adjustment i he timing dia Timing re -512 pixe Default ti +511 pixe ence StoP/PA he end of the low: 5 HRStopP ₅ 0 on with bits I gnal comes fr adjustment i he timing dia Timing re -512 pixe	0 3-2 in register rom a 625 line is in 1 pixel in agrams, as folled elative to defails ming ls L) Control R output horizor 4 HRStopP ₄ 0 1-0 in register rom a 625 line is in 1 pixel in agrams, as folled elative to defails	0 $24_{\rm H}$, set the set (PAL) source acrements relations: ult value egister. Defator ontal reference 3 HRStopP ₃ 0 $24_{\rm H}$, set the set e (PAL) source crements relations: 0	0 start of the ou e. The numb tive to the def ult value $00_{\rm H}$ e signal when 2 HRStopP ₂ 0 end of the out e. The numb	0 tput horizont er is a signed. fault standard the input sig 1 HRStopP ₁ 0 put horizonta er is a signed.	al reference , two's timing of times times
Default value HRStartP ₇₋₀ : Address 23 _H : 1 The eight bits it from a 625 line Bit Mnemonic Default value HRStopP ₇₋₀ :	These bits, signal whe complement this signal HRSta () HRSPP (Hori- n the HRSPP (PAL) source, 7 HRStopP ₇ 0 These bits, signal whe complement this signal HRSto () 2 ()	in conjunction in the input signation that input signation that the input signation of the second	on with bits 3 gnal comes fr adjustment i he timing dia Timing re -512 pixe Default ti +511 pixe once StoP/PA he end of the low: 5 HRStopP ₅ 0 on with bits 1 gnal comes fr adjustment i he timing dia Timing re	0 3-2 in register rom a 625 line is in 1 pixel in agrams, as folled elative to defa ls L) Control R output horizod 4 HRStopP ₄ 0 1-0 in register rom a 625 line is in 1 pixel in agrams, as folled elative to defa ls ming	0 $24_{\rm H}$, set the set (PAL) source acrements relations: ult value egister. Defator ontal reference 3 HRStopP ₃ 0 $24_{\rm H}$, set the set e (PAL) source crements relations: 0	0 start of the ou e. The numb tive to the def ult value $00_{\rm H}$ e signal when 2 HRStopP ₂ 0 end of the out e. The numb	0 tput horizont er is a signed. fault standard the input sig 1 HRStopP ₁ 0 put horizonta er is a signed.	al reference , two's timing of times times

The eight ons h	n the HMSP re	egister are the	e most signifi	icant bits for	the vertical sy	nc and refere	nce timing si	ignals when
the input signal	comes from a	625 line (PA	L) source, as	shown below	v:			
Bit	7	6	5	4	3	2	1	0
Mnemonic	HSStartP ₉	HSStartP ₈	HSStopP99	HSStopP ₈	HRStartP ₉	HRStartP ₈	HRStopP9	HRStopP ₈
Default value	0	0	0	0	0	0	0	0
HSStartP ₉₋₈ :	when the ir	put signal co		525 line (PAL	r 20 _H , set the s b) source. The etails.			
HSStopP ₉₋₈ :	when the in	nput signal c		625 line (PA	r 21 _H , set the L) source. T details.			
HRStartP ₉₋₈ :	signal whe	n the input si	ignal comes f	from a 625 li	er 22 _H , set the ine (PAL) sou 22 _H for detai	rce. These a		
	bits of a 10		ee desemptio	in of register	н			
HRStopP ₉₋₈ :	These bits, signal whe	in conjuncti n the input si	on with bits a ignal comes f	7-0 in registe from a 625 li	$er 23_{\rm H}, \text{ set the}$ ine (PAL) sou $23_{\rm H}$ for detai	end of the ource. These a		
HRStopP ₉₋₈ : Address 25 _H : The eight bits it 625 line (PAL)	These bits, signal whe bits of a 10 VSSTP (V ert n the VSTP re	in conjuncti n the input si)-bit value. S ical Sync Sta egister set th	on with bits f ignal comes f Gee descriptio	7-0 in registe from a 625 li on of register ntrol Regist	er 23 _H , set the ine (PAL) sou 23 _H for detai er. Default v	end of the ource. These a ls.	re the most s	ignificant
Address 25 _H : The eight bits in 625 line (PAL)	These bits, signal whe bits of a 10 VSSTP (V ert n the VSTP re	in conjuncti n the input si)-bit value. S ical Sync Sta egister set th	on with bits f ignal comes f Gee descriptio	7-0 in registe from a 625 li on of register ntrol Regist e output vertic	er 23 _H , set the ne (PAL) sou 23 _H for detai er. Default v cal sync pulse	end of the ource. These a ls. ralue 00 _H when the inp	re the most s	ignificant
Address 25 _H : The eight bits it 625 line (PAL) Bit	These bits, signal when bits of a 10 VSSTP (Vert n the VSTP re source, as sho 7	in conjuncti n the input si o-bit value. S ical Sync Sta egister set the own below: 6	on with bits 7 ignal comes f Gee description ar T/PAL) Co e start of the 5	7-0 in registe from a 625 li on of register ntrol Regist e output vertic 4	er 23 _H , set the ne (PAL) sou 23 _H for detai er. Default v cal sync pulse 3	end of the ource. These a ls. alue 00 _H when the inp	re the most s put signal con 1	ignificant mes from a 0
Address 25 _H : The eight bits i 625 line (PAL) Bit Mnemonic	These bits, signal when bits of a 10 VSSTP (Vert n the VSTP re source, as sho 7	in conjuncti n the input si o-bit value. S ical Sync Sta egister set the own below: 6	on with bits 7 ignal comes f Gee description ar T/PAL) Co e start of the 5	7-0 in registe from a 625 li on of register ntrol Regist e output vertic 4	er 23 _H , set the ne (PAL) sou 23 _H for detai er. Default v cal sync pulse	end of the ource. These a ls. alue 00 _H when the inp	re the most s put signal con 1	ignificant mes from a 0
Address 25 _H : The eight bits in 625 line (PAL) Bit Mnemonic Default value	These bits, signal when bits of a 10 VSSTP (Vert n the VSTP re source, as sho 7 VSStartP ₇ 0 These bits line (PAL)	in conjuncti n the input si p-bit value. Si ical Sync Sta egister set the own below: 6 VSStartP ₆ 0 set the start of source. The	on with bits 7 ignal comes f Gee description ar T/PAL) Co e start of the 5 VSStartP ₅ 0 of the output number is a	7-0 in registe from a 625 li on of register ntrol Regist output vertic 4 VSStartP ₄ 0 vertical sync signed, two'	er $23_{\rm H}$, set the ine (PAL) sou $23_{\rm H}$ for detai er. Default v cal sync pulse 3 VSStartP ₃	end of the ource. These a ls. alue 00_{H} when the inp 2 VSStartP ₂ 0 the input signt value. The	the most solution signal control 1 VSStartP ₁ 0 al comes fro adjustment in	ignificant mes from a 0 VSStartP 0 m a 625 s in 1 line
Address 25 _H : The eight bits in 625 line (PAL) Bit Mnemonic Default value	These bits, signal whe bits of a 10 VSSTP (Vert n the VSTP re source, as sho 7 VSStartP ₇ 0 These bits line (PAL) increments as follows:	in conjuncti n the input si p-bit value. Si ical Sync Sta egister set the own below: 6 VSStartP ₆ 0 set the start of source. The relative to the	on with bits 7 ignal comes f See description ar T/PAL) Co e start of the 5 VSStartP ₅ 0 of the output i number is a he default sta	7-0 in registe from a 625 li on of register ntrol Regist output vertic 4 VSStartP ₄ 0 vertical sync signed, two'	er 23 _H , set the ne (PAL) sou 23 _H for detai er. Default v cal sync pulse 3 VSStartP ₃ 0 c pulse when t s complement g of this signal	end of the ource. These a ls. alue 00_{H} when the inp 2 VSStartP ₂ 0 the input signt value. The	the most solution signal control 1 VSStartP ₁ 0 al comes fro adjustment in	ignificant mes from a 0 VSStartP 0 m a 625 s in 1 line
Address 25 _H : The eight bits in 625 line (PAL) Bit Mnemonic Default value	These bits, signal when bits of a 10 VSSTP (Vert n the VSTP re source, as sho 7 VSStartP ₇ 0 These bits line (PAL) increments as follows: VSStar	in conjuncti n the input si p-bit value. So ical Sync Sta egister set the own below: 6 VSStartP ₆ 0 set the start of source. The relative to the rtP ₇₋₀	on with bits 7 ignal comes f See description ar T/PAL) Co e start of the 5 VSStartP ₅ 0 of the output i number is a he default sta	7-0 in registe from a 625 li on of register ntrol Regist output vertic 4 VSStartP ₄ 0 vertical sync signed, two' andard timing	er 23 _H , set the ne (PAL) sou 23 _H for detai er. Default v cal sync pulse 3 VSStartP ₃ 0 c pulse when t s complement g of this signal	end of the ource. These a ls. alue 00_{H} when the inp 2 VSStartP ₂ 0 the input signt value. The	the most solution signal control 1 VSStartP ₁ 0 al comes fro adjustment in	ignificant mes from a 0 VSStartP 0 m a 625 s in 1 line
Address 25 _H : The eight bits i	These bits, signal when bits of a 10 VSSTP (Vert n the VSTP re source, as shown 7 VSStartP ₇ 0 These bits line (PAL) increments as follows: VSStart 8	in conjuncti n the input si p-bit value. Si ical Sync Sta egister set the own below: 6 VSStartP ₆ 0 set the start of source. The relative to the	on with bits \hat{f}_{ignal} comes for \hat{f}_{ignal} comes for \hat{f}_{ignal} comes for \hat{f}_{ignal} (comes for \hat{f}_{ignal} comes for $\hat{f}_$	7-0 in register from a 625 li on of register ntrol Regist output vertic 4 VSStartP ₄ 0 vertical sync signed, two' andard timing	er 23 _H , set the ne (PAL) sou 23 _H for detai er. Default v cal sync pulse 3 VSStartP ₃ 0 c pulse when t s complement g of this signal	end of the ource. These a ls. alue 00_{H} when the inp 2 VSStartP ₂ 0 the input signt value. The	the most solution signal control 1 VSStartP ₁ 0 al comes fro adjustment in	ignificant mes from a 0 VSStartP 0 m a 625 s in 1 line

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625 line (PAL)			e end of the	output vertica	al sync pulse	when the inpu	it signal com	es from a
Bit	7	6	5	4	3	2	1	0
Mnemonic	VSStopP ₇	VSStopP _c		VSStopP ₄	VSStopP ₃		VSStopP ₁	VSStopP ₀
Default value	0	0	0	0	0	0	0	0
VSStopP ₇₋₀ :	(PAL) sour increments as follows:	rce. The num relative to the test of test	hber is a sign he default sta	ed, two's cor andard timing	pulse when the pulse when the pulse when the pulse when the pulse of this signates when the pulse when the puls	ue. The adju	stment is in	l line
	VSSto		-	elative to defa	ault value			
		80 _H	-128 line					
	C	00 _H *	Default ti	iming				
	7	'F _H	+127 line	es				
The eight bits i from a 625 line Bit	(PAL) source 7	e, as shown b 6	elow: 5	4	3	2	1	0
Mnemonic	VRStartP ₇	VRStartP ₆	VRStartP ₅	VRStartP ₄	VRStopP ₃	VRStopP ₂	VRStopP ₁	VRStopP
		0				2	-	
Default value VRStartP ₇₋₀ :			-		0 ence signal v two's comple	-	-	
	These bits 625 line (P line increm diagrams, a VRSta 8	set the start of AL) source. ants relative as follows:	of the output The number to the defau	vertical refer is a signed, it standard ti elative to defa s iming	rence signal w two's comple ming of this	when the inpu ment value.	t signal com The adjustme	es from a ent is in 1
VRStartP ₇₋₀ : Address 28 _H : The eight bits i	These bits 625 line (P line increm diagrams, a VRSta 8 () 7 VRSPP (V ert n the VRSPP	set the start of AL) source. nents relative as follows: rtP_{7-0} 30_{H} 20_{H}^{*} $20_$	of the output The number to the defau Timing re -129 line Default ti +126 line ce StoP/PAL the end of the	vertical refer is a signed, ilt standard ti elative to defa is iming es	rence signal w two's comple ming of this ault value egister. Defa	when the inpu ment value. signal as show ult value 01 _H	t signal com The adjustme wn in the tim	es from a ent is in 1 iing
VRStartP₇₋₀: Address 28 _H : The eight bits i from a 625 line Bit	These bits 625 line (P line increm diagrams, a VRSta 8 () 7 VRSPP (Vert n the VRSPP (PAL) source 7	set the start of AL) source. nents relative as follows: rtP_{7-0} 30_{H} 20_{H}^{*} $2F_{H}^{*}$ register set to a shown b 6	of the output The number to the defau Timing re -129 line Default ti +126 line ce StoP/PAL the end of the pelow: 5	vertical refer is a signed, i lt standard ti elative to defa is iming es .) Control Re e output verti	rence signal w two's comple ming of this ault value egister. Defa cal reference	when the inpu ment value. signal as show ult value 01 _H signal when 2	t signal com The adjustme wn in the tim the input sign 1	es from a ent is in 1 ling nal comes 0
VRStartP₇₋₀: Address 28 _H : The eight bits i from a 625 line Bit	These bits 625 line (P line increm diagrams, a VRSta 8 () 7 VRSPP (Vert n the VRSPP (PAL) source 7	set the start of AL) source. nents relative as follows: rtP_{7-0} 30_{H} 20_{H}^{*} $2F_{H}^{*}$ register set to a shown b 6	of the output The number to the defau Timing re -129 line Default ti +126 line ce StoP/PAL the end of the pelow: 5	vertical refer is a signed, i lt standard ti elative to defa is iming es .) Control Re e output verti	rence signal w two's comple ming of this ault value egister. Defa cal reference	when the inpu ment value. signal as show ult value 01 _H signal when 2	t signal com The adjustme wn in the tim the input sign 1	es from a ent is in 1 ling nal comes
VRStartP ₇₋₀ : Address 28 _H : The eight bits i from a 625 line Bit Mnemonic	These bits 625 line (P line increm diagrams, a VRSta 8 () 7 VRSPP (Vert n the VRSPP (PAL) source 7	set the start of AL) source. nents relative as follows: rtP_{7-0} 30_{H} 20_{H}^{*} $2F_{H}^{*}$ register set to a shown b 6	of the output The number to the defau Timing re -129 line Default ti +126 line ce StoP/PAL the end of the pelow: 5	vertical refer is a signed, i lt standard ti elative to defa is iming es .) Control Re e output verti	rence signal w two's comple ming of this ault value egister. Defa cal reference	when the inpu ment value. signal as show ult value 01 _H signal when 2	t signal com The adjustme wn in the tim the input sign 1	es from a ent is in 1 ling nal comes 0
VRStartP ₇₋₀ :	These bits 625 line (P line increm diagrams, a VRSta 8 0 7 VRSPP (Vert n the VRSPP (PAL) source 7 VRStopP ₇ 0 These bits 625 line (P line increm diagrams, a	set the start of AL) source. nents relative as follows: rtP_{7-0} 30_H 01_H * 2F_H fical R eference register set to e, as shown by 6 VRStopP ₆ 0 set the end of AL) source. nents relative as follows:	of the output The number to the defau Timing re -129 line Default ti +126 line ce StoP/PAL the end of the velow: 5 VRStopP ₅ 0 f the output The number to the defau	vertical refer is a signed, ilt standard ti elative to defa is iming es Control Re e output verti 4 VRStopP ₄ 0 vertical refere is a signed, ilt standard ti	rence signal w two's comple ming of this ault value egister. Defa cal reference 3 VRStopP ₃ 0 ence signal w two's comple ming of this	when the input ment value. signal as show ult value $01_{\rm H}$ signal when 2 VRStopP ₂ 0 hen the input ment value.	t signal come The adjustme wn in the tim the input sign the input sign VRStopP ₁ 0 signal come The adjustme	es from a ent is in 1 ling nal comes 0 VRStopP 1 s from a ent is in 1
VRStartP ₇₋₀ : Address 28 _H : The eight bits i from a 625 line Bit Mnemonic Default value	These bits 625 line (P line increm diagrams, a VRSta 8 (C 7 VRSPP (Vert n the VRSPP (PAL) source 7 VRStopP ₇ 0 These bits 625 line (P line increm	set the start of AL) source. nents relative as follows: rtP_{7-0} 30_H 01_H * 2F_H fical R eference register set to e, as shown by 6 VRStopP ₆ 0 set the end of AL) source. nents relative as follows:	of the output The number to the defau Timing re -129 line Default ti +126 line ce StoP/PAL the end of the velow: 5 VRStopP ₅ 0 f the output The number to the defau	vertical refer is a signed, i ilt standard ti elative to defa is iming es C) Control Re e output verti 4 VRStopP ₄ 0 vertical referen- is a signed, i	rence signal w two's comple ming of this ault value egister. Defa cal reference 3 VRStopP ₃ 0 ence signal w two's comple ming of this	when the input ment value. signal as show ult value $01_{\rm H}$ signal when 2 VRStopP ₂ 0 hen the input ment value.	t signal come The adjustme wn in the tim the input sign the input sign VRStopP ₁ 0 signal come The adjustme	es from a ent is in 1 ling nal comes 0 VRStopP 1 s from a ent is in 1
VRStartP ₇₋₀ : Address 28 _H : The eight bits i from a 625 line Bit Mnemonic Default value	These bits 625 line (P) line increm diagrams, a VRSta 8 (C) 7 VRSPP (Vert n the VRSPP (PAL) source 7 VRStopP ₇ 0 These bits 625 line (P) line increm diagrams, a VRSto	set the start of AL) source. nents relative as follows: rtP_{7-0} 30_H 01_H * 2F_H fical R eference register set to e, as shown by 6 VRStopP ₆ 0 set the end of AL) source. nents relative as follows:	of the output The number to the defau Timing re -129 line Default ti +126 line ce StoP/PAL the end of the velow: 5 VRStopP ₅ 0 f the output The number to the defau	vertical refer is a signed, i ilt standard ti elative to defa is iming es C) Control Re e output verti 4 VRStopP ₄ 0 vertical referen- is a signed, ilt standard ti elative to defa	rence signal w two's comple ming of this ault value egister. Defa cal reference 3 VRStopP ₃ 0 ence signal w two's comple ming of this	when the input ment value. signal as show ult value $01_{\rm H}$ signal when 2 VRStopP ₂ 0 hen the input ment value.	t signal come The adjustme wn in the tim the input sign the input sign VRStopP ₁ 0 signal come The adjustme	es from a ent is in 1 ling nal comes 0 VRStopP 1 s from a ent is in 1
VRStartP ₇₋₀ : Address 28 _H : The eight bits i from a 625 line Bit Mnemonic Default value	These bits 625 line (P line increm diagrams, a VRSta 8 (C 7 VRSPP (Vert n the VRSPP (PAL) source 7 VRStopP ₇ 0 These bits 625 line (P line increm diagrams, a VRSto 8	set the start of AL) source. nents relative as follows: rtP_{7-0} 30_{H} $2T_{H}$ ical R eference register set the end of AL) source. nents relative as follows: pP_{7-0}	of the output The number to the defau Timing re -129 line Default ti +126 line ce StoP/PAL the end of the below: 5 VRStopP ₅ 0 f the output The number to the defau Timing re	vertical refer is a signed, ilt standard ti elative to defa siming es () Control Ra e output verti 4 VRStopP ₄ 0 vertical refere is a signed, ilt standard ti elative to defa	rence signal w two's comple ming of this ault value egister. Defa cal reference 3 VRStopP ₃ 0 ence signal w two's comple ming of this	when the input ment value. signal as show ult value $01_{\rm H}$ signal when 2 VRStopP ₂ 0 hen the input ment value.	t signal come The adjustme wn in the tim the input sign the input sign VRStopP ₁ 0 signal come The adjustme	es from a ent is in 1 ling nal comes 0 VRStopP 1 s from a ent is in 1

				output vertic	al blanking si	ignal when th	e input signa	l comes
from a 625 line					2			0
Bit	7	6	5				1	0
Mnemonic						VBStartP ₂		
Default value	0	0	0	0	0	0	0	1
VBStartP ₇₋₀ :	line (PAL)	source. The	number is a si	igned, two's o	complement v	ten the input s value. The adj as shown in th	ustment is in	1 line
	VBSta	rtP ₇₋₀	Timing re	lative to defa	ult value			
	8	80 _н	-129 line	s				
	C)1 _H *	Default ti	ming				
Address 2A _H :	7 VBSPP (Ver	F _H tical B lankin	+126 line	s) Control Re				
Address 2A_H: The eight bits i from a 625 line	7 VBSPP (Ver n the VBSTP	F _H tical B lankin register set t	+126 line ag StoP/PAL) the end of the	s) Control Re				nal comes
The eight bits i from a 625 line	7 VBSPP (Ver n the VBSTP	F _H tical B lankin register set t	+126 line g StoP/PAL) the end of the pelow:	s) Control Re e output verti	ical blanking		he input sign	nal comes
The eight bits i	7 VBSPP (V er n the VBSTP (PAL) source 7	tical B lankin register set t e, as shown b 6	+126 line ag StoP/PAL) the end of the elow: 5	s Control Re e output verti 4	ical blanking 3	signal when the signal when th	he input sign	0
The eight bits i from a 625 line Bit	7 VBSPP (V er n the VBSTP (PAL) source 7	tical B lankin register set t e, as shown b 6	+126 line ag StoP/PAL) the end of the elow: 5	s Control Re e output verti 4	ical blanking 3	signal when	he input sign	0
The eight bits i from a 625 line Bit Mnemonic	7 VBSPP (Ver n the VBSTP (PAL) source 7 VBStopP ₇ 0 These bits 625 line (P	F_{H} tical B lankin register set t e, as shown b 6 VBStopP ₆ 0 set the end o AL) source. ients relative	+126 line g StoP/PAL) the end of the velow: 5 VBStopP ₅ 0 f the output v The number	s Control Re e output verti 4 VBStopP ₄ 0 vertical blank is a signed, t	acal blanking 3 VBStopP ₃ 0 king signal wl two's comple	signal when the signal when th	the input sign 1 VBStopP ₁ 0 signal come: The adjustme	0 VBStopP ₀ 0 s from a ent is in 1
The eight bits i from a 625 line Bit Mnemonic Default value	7 VBSPP (Ver n the VBSTP (PAL) source 7 VBStopP ₇ 0 These bits 625 line (P line increm	F_{H} tical B lankin register set t e, as shown b 6 VBStopP ₆ 0 set the end o AL) source. ients relative as follows:	+126 line g StoP/PAL) the end of the velow: 5 VBStopP ₅ 0 f the output v The number to the defau Timing re	s Control Re e output verti 4 VBStopP ₄ 0 vertical blank is a signed, to lt standard times elative to defa	3 VBStopP ₃ 0 king signal wl two's comple ming of this s	signal when the signal when t	the input sign 1 VBStopP ₁ 0 signal come: The adjustme	0 VBStopP ₀ 0 s from a ent is in 1
The eight bits i from a 625 line Bit Mnemonic Default value	7 VBSPP (Ver n the VBSTP (PAL) source 7 VBStopP ₇ 0 These bits 625 line (P line increm diagrams, a VBSto	F_{H} tical B lankin register set t e, as shown b 6 VBStopP ₆ 0 set the end o AL) source. tents relative as follows: pP ₇₋₀ 30_{H}	+126 line ag StoP/PAL) the end of the elow: 5 VBStopP ₅ 0 f the output v The number to the defau	s Control Re e output verti 4 VBStopP ₄ 0 vertical blank is a signed, to lt standard times elative to defa	3 VBStopP ₃ 0 king signal wl two's comple ming of this s	signal when the signal when t	the input sign 1 VBStopP ₁ 0 signal come: The adjustme	0 VBStopP ₀ 0 s from a ent is in 1
The eight bits i from a 625 line Bit Mnemonic Default value	7 VBSPP (Ver n the VBSTP (PAL) source 7 VBStopP ₇ 0 These bits 625 line (P line increm diagrams, a VBSto	F_{H} tical B lankin register set t e, as shown b 6 VBStopP ₆ 0 set the end o AL) source. tents relative as follows: pP ₇₋₀	+126 line g StoP/PAL) the end of the velow: 5 VBStopP ₅ 0 f the output v The number to the defau Timing re	s Control Re e output verti 4 VBStopP ₄ 0 vertical blank is a signed, the lt standard the elative to defa s	3 VBStopP ₃ 0 king signal wl two's comple ming of this s	signal when the signal when t	the input sign 1 VBStopP ₁ 0 signal come: The adjustme	0 VBStopP ₀ 0 s from a ent is in 1

comes from a 62	n the VBISTP 25 line (PAL)			e output v BI	uata pass-un	ough signal v	men me mp	it signai
Bit	7	6	5	4	3	2	1	0
Mnemonic	VBIStartP ₇	VBIStartP ₆	VBIStartP ₅	VBIStartP ₄	VBIStartP ₃	VBIStartP ₂	VBIStartP ₁	VBIStartP ₀
Default value	0	0	0	0	0	0	1	0
VBIStartP ₇₋₀ :	from a 625 to be unbla value. The	line (PAL) so nked to pass adjustment i	ource. This a through the	llows a select data on these crements relat	s-through sig ed contiguous lines. The nu tive to the def	s group of line 1mber is a sig	es during the ned, two's c	VBI period
	VBISta	artP ₇₋₀	Timing re	lative to defa	ult value			
	8	80 _H	-130 lines	1				
	C	2 _H *	Default tin	ning				
		Έ _H	+125 lines	1				
The eight bits in comes from a 6		U		4	3	2	1	
Rit		0	5	-	5	4	1	
		VRIStartP	VRIStartP	VBIStartP	VRIStonP	VRIStonP	VRIStonP	
Bit Mnemonic Default value		VBIStartP ₂ 0	VBIStartP ₁ 0	VBIStartP ₀ 0	VBIStopP ₃ 1	VBIStopP ₂ 0	VBIStopP ₁ 0	

	the HOVR reg	gister contro.	i the norizon	tai inne iengin,	as snown be	low.		
Bit	7	6	5	4	3	2	1	0
Mnemonic	Test	х	х	HSizeOvr	х	HSize ₁₀	HSize	HSize ₈
Default value	0	х	х	0	х	1	0	0 ँ
Test:	This bit is u	used to put th	ne device inte	o a special test	mode, as fo	llows:		
	0* =	Normal ope	rating mode.					
	1 =	Test mode,	not normally	used.				
x:	This bit is 1	not used and	does not ex	ist physically.				
HSizeOvr:	This bit con	ntrols the ho	rizontal line	length, as foll	ows:			
				natically set ac				
	-			signals and 8	-		-	
				y for fully ada		-		
		x · · · · ·	11 .1 1	\mathbf{N}				
		-		NMOvr bit is s	-			
	1 =	Line length	is set by the	number of clos	ck cycles in	each horizonta	al period, as o	determined
	1 = by the horiz	Line length zontal sync o	is set by the or reference in	number of cloo nput signal. In	ck cycles in this mode th	each horizonta ne HSize regis	al period, as o ter must be p	determined programmed
	1 = by the horiz to match th	Line length zontal sync o is number fo	is set by the r reference in r correct ope	number of cloo nput signal. In ration. This m	ck cycles in this mode th ode can only	each horizonta ne HSize regis y be used when	al period, as o ter must be p n the FLI220	determined programmed 0 is
	1 = by the horiz to match the configured	Line length zontal sync o is number fo in the stand-a	is set by the r reference in r correct ope alone mode v	number of cloo nput signal. In ration. This m vith no externa	ck cycles in this mode th ode can only l memory (ir	each horizonta ne HSize regis y be used when ntra-field deinn	al period, as o ter must be p n the FLI220 terlacing only	determined programmed 0 is y), i.e., the
	1 = by the horiz to match th configured NOMEM p	Line length zontal sync o is number fo in the stand- pin is tied hig	is set by the r reference in r correct ope alone mode w h or the NM	number of cloo nput signal. In ration. This m	ck cycles in this mode th ode can only l memory (in em bits are se	each horizonta ne HSize regis y be used when ntra-field deinn et high. When	al period, as o ter must be p n the FLI220 terlacing only	determined programmed 0 is y), i.e., the
HSize ₁₀₋₈ :	1 = by the horiz to match th configured NOMEM p external me	E Line length zontal sync o is number fo in the stand-t pin is tied hig emory for full	is set by the or reference in r correct ope alone mode v h or the NM ly adaptive do	number of cloo nput signal. In ration. This m vith no externa Ovr and NoMe einterlacing HS	ck cycles in o this mode th ode can only l memory (in em bits are so SizeOvr mus	each horizonta ne HSize regis y be used when ntra-field deim et high. When t be set low	al period, as o ter must be p n the FLI220 terlacing only n the device i	determined programmed 0 is y), i.e., the s used with
HSize ₁₀₋₈ :	1 = by the horiz to match the configured NOMEM p external me These bits,	Line length zontal sync o is number fo in the stand in is tied hig emory for full in conjuncti	is set by the or reference in r correct ope alone mode w h or the NM ly adaptive do on with bits	number of cloo nput signal. In ration. This m vith no externa Ovr and NoMe	ck cycles in this mode this mode the can only l memory (in the bits are selected by $2F_{\rm H}$, set the	each horizonta ne HSize regis y be used when ntra-field deim et high. When t be set low	al period, as o ter must be p n the FLI220 terlacing only n the device i	determined programmed 0 is y), i.e., the s used with
	1 = by the horiz to match th configured NOMEM p external me These bits, bit is set hi	Line length zontal sync o is number fo in the stand- in is tied hig emory for full in conjuncti gh . See des	is set by the or reference in r correct ope alone mode w h or the NM ly adaptive do on with bits scription of r	number of cloo nput signal. In ration. This m vith no externa Ovr and NoMe einterlacing HS 7-0 in register egister 2F _H for	ck cycles in this mode this mode the can only l memory (in the motion of the can bits are selected by $2F_{\rm H}$, set the details.	each horizonta ne HSize regis y be used when ntra-field deim et high. When t be set low e total line len	al period, as o ter must be p n the FLI220 terlacing only n the device i	determined programmed 0 is y), i.e., the s used with
HSize ₁₀₋₈ : Address 2F _H : The eight bits in	1 = by the horiz to match the configured NOMEM p external me These bits, bit is set hip HSIZE (Hori	Line length zontal sync o is number fo in the stand-a in is tied hig emory for full in conjuncti gh . See des izontal Size)	is set by the or reference in r correct ope alone mode w th or the NM ly adaptive do on with bits scription of r Control Re	number of cloo nput signal. In ration. This m vith no externa Ovr and NoMe einterlacing HS 7-0 in register egister 2F _H for egister. Defau	ck cycles in o this mode th ode can only l memory (in em bits are so SizeOvr mus 2 2F _H , set the c details.	each horizonta ne HSize regis y be used when ntra-field deint et high. When t be set low e total line len	al period, as o ter must be p n the FLI220 terlacing only n the device i	determined programmed 0 is y), i.e., the s used with
Address 2F _H :	1 = by the horiz to match the configured NOMEM p external me These bits, bit is set hip HSIZE (Hori	Line length zontal sync o is number fo in the stand-a in is tied hig emory for full in conjuncti gh . See des izontal Size)	is set by the or reference in r correct ope alone mode w th or the NM ly adaptive do on with bits scription of r Control Re	number of cloo nput signal. In ration. This m vith no externa Ovr and NoMe einterlacing HS 7-0 in register egister 2F _H for egister. Defau	ck cycles in o this mode th ode can only l memory (in em bits are so SizeOvr mus 2 2F _H , set the c details.	each horizonta ne HSize regis y be used when ntra-field deint et high. When t be set low e total line len	al period, as o ter must be p n the FLI220 terlacing only n the device i	determined programmed 0 is y), i.e., the s used with
Address 2F _H : The eight bits in	1 = by the horiz to match the configured NOMEM p external me These bits, bit is set hig HSIZE (Hori n the HSIZE re	Line length zontal sync o is number fo in the stand- in is tied hig emory for full in conjuncti gh . See des izontal Size) egister contro 6	is set by the r reference in r correct ope alone mode w h or the NMr ly adaptive de on with bits scription of r Control Re of the horizon 5	number of cloo nput signal. In ration. This m vith no externa Ovr and NoMe einterlacing HS 7-0 in register egister 2F _H for gister. Defau ntal line length 4	ck cycles in this mode this mode this mode the ode can only memory (in the bits are so the bi	each horizonta ne HSize regis y be used when htra-field deint et high. When t be set low e total line len H elow: 2	al period, as o ter must be p n the FLI220 terlacing only n the device i ngth when the	determined orogrammed 0 is y), i.e., the s used with e HSizeOvr
Address 2F _H : The eight bits in Bit	1 = by the horiz to match th configured NOMEM p external me These bits, bit is set hi HSIZE (Hori n the HSIZE re	Line length zontal sync o is number fo in the stand- in is tied hig emory for full in conjuncti gh . See des izontal Size) egister contro	is set by the or reference in r correct ope alone mode v h or the NM ly adaptive do on with bits scription of r Control Re ol the horizon	number of cloo nput signal. In ration. This m vith no externa Ovr and NoMe einterlacing HS 7-0 in register egister 2F _H for gister. Defau ntal line length 4	ck cycles in this mode this mode this mode the ode can only memory (in the bits are so the bi	each horizonta ne HSize regis y be used when htra-field deint et high. When t be set low e total line len H elow: 2	al period, as o ter must be p n the FLI220 terlacing only n the device i ngth when the	determined programmed 0 is y), i.e., the s used with e HSizeOvr
Address 2F _H : The eight bits in Bit Mnemonic	1 = by the horiz to match th configured NOMEM p external me These bits, bit is set hij HSIZE (Hori n the HSIZE re 7 HSize ₇ 0	Line length zontal sync o is number fo in the stand- in is tied hig emory for full in conjuncti gh . See des izontal Size) egister contro 6 HSize ₆ 1	is set by the r reference in r correct ope alone mode v h or the NM ly adaptive de on with bits scription of r Control Re ol the horizon 5 HSize ₅ 0	number of cloan nput signal. In ration. This m vith no externa Ovr and NoMe einterlacing HS 7-0 in register egister 2F _H for egister. Defaut ntal line length 4 HSize ₄	ck cycles in o this mode th ode can only l memory (in em bits are so SizeOvr mus $2F_{H}$, set the c details. It value $4C_{H}$, as shown b 3 HSize ₃ 1	each horizonta ne HSize regis y be used when ntra-field deint et high. When t be set low e total line len H elow: 2 HSize ₂ 1	al period, as o ter must be p n the FLI220 terlacing only n the device i ngth when the lthe Bisse 1 HSize 0	letermined orogrammed 0 is y), i.e., the s used with e HSizeOve 0 HSize ₀ 0

Bit	7	6	l the polarities 5	4	3	2	1	0
Mnemonic	ISyncInv	ORefInv	OSyncInv	DatBlnk	HDatBlnk	Test	IMode	CCSOn
Default value	0	0	0	0	0	1	0	1
ISyncInv:	This bit is	set according	g to the polari	ty of the syn	c inputs, as fol	lows:		
		-	nc inputs (activ	-				
	1 =	= Inverted sy	nc inputs (act	ive low).				
ORefInv:	This contro	ols the polari	ty of the H an	d V referenc	e outputs, as fo	ollows:		
	0* =	= Normal ref	erence outputs	s (active high	ı).			
	1 =	= Inverted re	ference output	ts (active lov	w).			
OSyncInv:	This contro	ols the polari	ty of the sync	outputs, as	follows:			
		•	nc outputs (act	0,				
	1 =	= Inverted sy	nc outputs (ad	ctive low).				
DatBlnk:	This contro	ols the passir	ng of ancillary	data, as foll	ows:			
	0* =	= Ancillary d	ata in the vert	ical blanking	g interval is not	passed.		
		P ₄₋₀ /HBStop			g interval is pas VBStopN/P ₅₋₀ b		-	-
HDatBlnk:	This contro	ols the passin	g of ancillary	data in the h	orizontal blank	ting interval	l, as follows:	
	0* =	= Ancillary d	ata in the hori	zontal blank	ting interval is i	not passed.		
		•			ting interval is period to the second s			
		-			rpolated lines,	•		(ieiii)
Test:	This contro	ols the opera	tion of the de	interlacer, as	s follows:			
	0 =	= Test mode.						
	1* =	= Normal op	erating mode.					
Test:	This contro	ols the opera	tion of the de	interlacer, a	s follows:			
	0* =	= Normal op	erating mode.					
	1 =	= Test mode.						
CCSOn:	This contro	ols the opera	tion of the Cr	oss Color Si	uppressor funct	tion, as follo	ows:	
					nis primarily a			
	1* =	= Cross Colo	r suppressor e	nabled. Thi	s is the normal	operating n	node.	

	the EDDI			er. Default va		ana of the i	maga usad in	the Ded
The eight bits in Edit Detector, a		-	i the position	i of the left ha	and side of the	e area of the f	mage used in	the Bad
Bit	7	6	5	4	3	2	1	0
Mnemonic	EdBlnkL ₇	EdBlnkL ₆	EdBlnkL5	EdBlnkL ₄	EdBlnkL3	EdBlnkL ₂	EdBlnkL ₁	EdBlnkL ₍
Default value	1	1	1	0	0	0	0	0
EdBlkL ₇₋₀ :					_H , set the pos alue is the nur			
Address 32 _H : H The eight bits in Edit Detector, a	n the EDBR re	egister contro				he area of the	image used	in the Bad
Bit	7	6	5	4	3	2	1	0
Mnemonic	EdBlnkR7	EdBlnkR ₆	EdBlnkR5	$EdBlnkR_{A}$	EdBlnkR ₃	EdBlnkR,	EdBlnkR ₁	EdBlnkR
Default value	0	1	0	1	0	0	1	0
Address 33 _H : H	of active vi	deo. Blank Top) Co	ontrol Registe	er. Default va				n the start
-	n the EDBT re	egister contro	n me position	f of the top of	the area of the	ie image used	in the Bad E	dit
Detector, as sho	own below:	-	-	-		C C		_
Detector, as sho Bit	own below: 7	6	5	4	3	2	1	0
The eight bits in Detector, as sho Bit Mnemonic Default value	own below: 7	6	5	4		2	1	0
Detector, as sho Bit Mnemonic	own below: 7 EdBlnkT ₇ 0 These bits,	6 EdBlnkT ₆ 1 in conjunction	5 EdBlnkT ₅ 0 on with bit 4	4 EdBlnkT ₄ 0 in register 3	3 EdBlnkT ₃	2 EdBlnkT ₂ 0 sition of the t	1 EdBlnkT ₁ 1 top of the are	0 EdBlnkT 0 ea of the
Detector, as sho Bit Mnemonic Default value EdBlkT ₇₋₀ : Address 34 _H : H The eight bits in Detector when	own below: 7 EdBlnkT ₇ 0 These bits, image used video. EDBBN (EDit n the EDBBN	6 EdBlnkT ₆ 1 in conjunction in the Bad I Blank Bottor register cont al comes fro	5 EdBlnkT ₅ 0 on with bit 4 Edit Detector n/NTSC) Con rol the position m a 525 line	4 EdBlnkT ₄ 0 in register 30 The value in the value in the value in	3 EdBlnkT ₃ 0 6 _H , set the po is the number r. Default val om of the area rce, as shown	2 EdBlnkT ₂ 0 sition of the too of pixels from ue F4_H a of the image below:	1 EdBlnkT ₁ 1 top of the are m the start o	0 EdBlnkT 0 ea of the f active Bad Edit
Detector, as sho Bit Mnemonic Default value EdBlkT ₇₋₀ : Address 34 _H : H The eight bits in Detector when Bit	own below: 7 EdBlnkT ₇ 0 These bits, image used video. EDBBN (EDit the EDBBN the input sign 7	6 EdBlnkT ₆ 1 in conjuncti- l in the Bad I Blank Bottor register cont al comes fro 6	5 EdBlnkT ₅ 0 on with bit 4 Edit Detector n/NTSC) Con rol the position m a 525 line 5	4 EdBInkT ₄ 0 in register 3 The value in ntrol Register on of the bott (NTSC) sour 4	3 EdBlnkT ₃ 0 $6_{\rm H}$, set the po is the number r. Default val om of the area rce, as shown 3	2 EdBlnkT ₂ 0 sition of the tool of pixels from the image below: 2	$\frac{1}{\text{EdBInkT}_{1}}$ top of the are m the start o e used in the 1 1	0 EdBlnkT 0 ea of the f active Bad Edit 0
Detector, as sho Bit Mnemonic Default value EdBlkT ₇₋₀ : Address 34 _H : F The eight bits in Detector when Bit Mnemonic	own below: 7 EdBlnkT ₇ 0 These bits, image used video. EDBBN (EDit the EDBBN the input sign 7	6 EdBlnkT ₆ 1 in conjunction in the Bad I Blank Bottor register cont al comes fro 6 EdBlnkT ₆	5 EdBlnkT ₅ 0 on with bit 4 Edit Detector n/NTSC) Con rol the position m a 525 line 5	4 EdBlnk T_4 0 in register 30 The value in introl Register on of the bott (NTSC) source 4 EdBlnk T_4	3 EdBlnkT ₃ 0 $6_{\rm H}$, set the pois is the number r. Default val om of the area rec, as shown 3 EdBlnkT ₃	2 EdBlnkT ₂ 0 sition of the too f pixels from ue F4_H a of the image below: 2 EdBlnkT ₂	$\frac{1}{\text{EdBlnkT}_{1}}$ top of the are m the start of e used in the 1 1 EdBlnkT_{1}	0 EdBlnkT 0 ea of the f active Bad Edit 0 EdBlnkT
Detector, as sho Bit Mnemonic Default value	own below: 7 EdBlnkT ₇ 0 These bits, image used video. EDBBN (EDit the EDBBN the input sign 7	6 EdBlnkT ₆ 1 in conjuncti- l in the Bad I Blank Bottor register cont al comes fro 6	5 EdBlnkT ₅ 0 on with bit 4 Edit Detector n/NTSC) Con rol the position m a 525 line 5	4 EdBInkT ₄ 0 in register 3 The value in ntrol Register on of the bott (NTSC) sour 4	3 EdBlnkT ₃ 0 $6_{\rm H}$, set the po is the number r. Default val om of the area rce, as shown 3	2 EdBlnkT ₂ 0 sition of the tool of pixels from the image below: 2	$\frac{1}{\text{EdBInkT}_{1}}$ top of the are m the start o e used in the 1 1	0 EdBlnkT 0 ea of the f active Bad Edit

					om of the area		used in the E	Bad Edit
Detector when t	he input signa				as shown belo			
Bit	7	6	5	4	3	2	1	0
Mnemonic	EdBlnkT ₇	EdBlnkT ₆	5	EdBlnkT ₄	EdBlnkT ₃	EdBlnkT ₂	EdBlnkT ₁	EdBlnkT ₍
Default value	0	1	0	1	1	0	0	0
EdBlkBN ₇₋₀ :	of the imag		Bad Edit Det	ector when the	ister 36 _H , set ne input signa active video.			
Address 36 _H : H The eight bits ir shown below:								ctor, as
Bit	7	6	5	4	3	2	1	0
Mnemonic	EdBlnkL ₈	EdBlnkR ₉	EdBlnkR ₈	EdBlnkT ₈	EdBlnkBN ₉	EdBlnkBN ₈	EdBlnkBP ₉	EdBlnkBP,
Default value	0	1	1	0	0	1	1	0
EdBlkL ₈ :	This bit, in area of the	conjunction image used i	with bits 7-0 n the Bad Eo) in register 3 lit Detector.	31 _H , sets the p See descripti	oosition of the on of register	e left hand sid 31 _H for deta	le of the ils.
EdBlkR ₉₋₈ :					er 32 _H , set the tor. See descr			
EdBlkT ₈ :					33 _H , sets the potion of regist			rea of the
EdBlkBN ₉₋₈ :	the image u		ad Edit Dete	ctor when th	· 34 _H , set the p e input signal s.			
EdBlkBP ₉₋₈ :	the image u		ad Edit Dete	ctor when th	· 35 _H , set the _I e input signal s.			
	MBL (FilM I	Blank Left) C	-		11	e area of the i	mage used in	the Film
Address 37 _H : F The eight bits ir Mode Detector,		0	of the position					
The eight bits ir Mode Detector,		0	5	4	3	2	1	0
The eight bits ir Mode Detector, Bit	as shown bel	ow:	5	4	3 FmBlnkL ₃		1 FmBlnkL ₁	0 FmBlnkL
The eight bits ir	as shown bel 7	ow: 6	5	4				

	n the FMBR r	egister contro	ol the position	n of the right	hand side of t	he area of the	image used	in the Filn
Mode Detector,	as shown bel	ow:	-	-			-	
Bit	7	6	5	4	3	2	1	0
Mnemonic	FmBlnkR ₇	FmBlnkR ₆	$FmBlnkR_5$	$FmBlnkR_4$	FmBlnkR ₃	$FmBlnkR_2$	FmBlnkR ₁	FmBlnkR
Default value	0	1	0	1	1	0	0	0
FmBlkR ₇₋₀ :		the image us			ister 3C _H , set etor. The valu			
Address 39 _H : F The eight bits in Detector, as sho	n the FMBT re					he image used	l in the Film	Mode
Bit	7	6	5	4	3	2	1	0
Mnemonic	FmBlnkT ₇	FmBlnkT ₆	FmBlnkT ₅	$FmBlnkT_4$	$FmBlnkT_3$	FmBlnkT ₂	FmBlnkT ₁	FmBlnkT
Default value	0	1	0	0	0	0	1	0
The eight bits in	n the FMBBN	register con	trol the positi	on of the bott	tom of the are	a of the image		Film
The eight bits in Mode Detector	F MBBN (Fil N in the FMBBN when the inp	register con ut signal con	trol the positi nes from a 52	on of the both 25 line (NTS)	tom of the are C) source, as	a of the imageshown below	:	
The eight bits in Mode Detector Bit	F MBBN (FilM the FMBBN when the inp 7	register con ut signal con 6	trol the positi nes from a 52 5	on of the both 25 line (NTSO 4	tom of the are C) source, as 3	a of the imag shown below 2	: 1	0
The eight bits in Mode Detector Bit Mnemonic	F MBBN (FilM the FMBBN when the inp 7 FmBlnkT ₇	register cont ut signal con 6 FmBlnkT ₆	trol the positi nes from a 52 5 FmBlnkT ₅	on of the both 25 line (NTS) 4 FmBlnkT ₄	tom of the are C) source, as 3 FmBlnkT ₃	a of the images shown below 2 FmBlnkT ₂	: 1 FmBlnkT ₁	0 FmBlnkT
Mnemonic	F MBBN (FilM the FMBBN when the inp 7	register con ut signal con 6	trol the positi nes from a 52 5	on of the both 25 line (NTSO 4	tom of the are C) source, as 3	a of the imag shown below 2	: 1	0
The eight bits in Mode Detector Bit	F MBBN (FilM the FMBBN when the inp 7 FmBlnkT ₇ 1 These bits, the image u	register cont ut signal con 6 FmBlnkT ₆ 1 in conjunctions in the Fil	trol the positi nes from a 52 5 FmBlnkT ₅ 1 on with bits 3 Im Mode Det	on of the both 25 line (NTS) 4 FmBlnkT ₄ 1 3 and 2 in reg ector when the	tom of the are C) source, as 3 FmBlnkT ₃	a of the images shown below 2 FmBlnkT ₂ 1 the position of comes from a	: fmBlnkT ₁ 0 of the top of	0 FmBlnkT 0 the area of
The eight bits in Mode Detector Bit Mnemonic Default value FmBlkBN ₇₋₀ : Address 3B _H : 1 The eight bits in	FMBBN (FilM the FMBBN when the inp 7 FmBlnkT ₇ 1 These bits, the image u source. Th FMBBP (FilM the FMBBP	register cont ut signal con 6 FmBlnkT ₆ 1 in conjunctionsed in the Fill e value is the 1 B lank B otto register cont	trol the positi nes from a 52 5 FmBlnkT ₅ 1 on with bits 3 Im Mode Dete e number of li om/PAL) Con rol the positio	on of the both 25 line (NTS) 4 FmBlnkT ₄ 1 B and 2 in reg ector when the ines from the htrol Register on of the both	tom of the are C) source, as 3 FmBlnkT ₃ 0 ister 3C _H , set is input signal start of active : Default vale om of the area	a of the images shown below 2 FmBlnkT ₂ 1 the position of comes from a e video. ue 58_H a of the image	: FmBlnkT ₁ 0 of the top of a 525 line (N	0 FmBlnkT 0 the area of TSC)
The eight bits in Mode Detector Bit Mnemonic Default value FmBlkBN₇₋₀: Address 3B _H : 1 The eight bits in Detector when the	FMBBN (FilM the FMBBN when the inp 7 FmBlnkT ₇ 1 These bits, the image u source. Th FMBBP (FilM the FMBBP	register cont ut signal con 6 FmBlnkT ₆ 1 in conjunctionsed in the Fill e value is the 1 B lank B otto register cont	trol the positi nes from a 52 5 FmBlnkT ₅ 1 on with bits 3 Im Mode Dete e number of li om/PAL) Con rol the positio	on of the both 25 line (NTS) 4 FmBlnkT ₄ 1 B and 2 in reg ector when the ines from the htrol Register on of the both	tom of the are C) source, as 3 FmBlnkT ₃ 0 ister 3C _H , set is input signal start of active : Default vale om of the area	a of the images shown below 2 FmBlnkT ₂ 1 the position of comes from a sevideo. Ine 58_H a of the image ow: 2	: FmBlnkT ₁ 0 of the top of a 525 line (N	0 FmBlnkT 0 the area of TSC)
The eight bits in Mode Detector Bit Mnemonic Default value FmBlkBN ₇₋₀ : Address 3B _H : 1 The eight bits in Detector when the Bit	FMBBN (FilM the FMBBN when the inp 7 FmBlnkT ₇ 1 These bits, the image u source. Th FMBBP (FilM the FMBBP	register cont ut signal con 6 FmBlnkT ₆ 1 in conjunctionsed in the Fill e value is the I B lank B ottor register cont al comes from	trol the positi nes from a 52 5 FmBlnkT ₅ 1 on with bits 3 Im Mode Dete e number of li om/PAL) Con rol the position n a 625 line (li 5	on of the both 25 line (NTS) 4 FmBlnkT ₄ 1 B and 2 in reg ector when the ines from the htrol Register on of the both PAL) source, 4	tom of the are C) source, as 3 FmBlnkT ₃ 0 ister 3C _H , set is input signal start of active : Default vale om of the area	a of the images shown below 2 FmBlnkT ₂ 1 the position of comes from a comes from a comes from a comes from a come structure of the image of t	: 1 FmBlnkT ₁ 0 of the top of a 525 line (N e used in the	0 FmBlnkT 0 the area of TSC) Film Mod 0
The eight bits in Mode Detector Bit Mnemonic Default value	FMBBN (FilM the FMBBN when the inp 7 FmBlnkT ₇ 1 These bits, the image u source. Th FMBBP (FilM the FMBBP the input signa 7	register cont ut signal con 6 FmBlnkT ₆ 1 in conjunction sed in the Fill e value is the register cont al comes from 6	trol the positi nes from a 52 5 FmBlnkT ₅ 1 on with bits 3 Im Mode Dete e number of li om/PAL) Con rol the position n a 625 line (li 5	on of the both 25 line (NTS) 4 FmBlnkT ₄ 1 B and 2 in reg ector when the ines from the htrol Register on of the both PAL) source, 4	tom of the are C) source, as 3 FmBlnkT ₃ 0 ister 3C _H , set is input signal start of active : Default valu om of the area as shown below 3	a of the images shown below 2 FmBlnkT ₂ 1 the position of comes from a sevideo. Ine 58_H a of the image ow: 2	: FmBlnkT ₁ 0 of the top of a 525 line (N e used in the 1	0 FmBlnkT 0 the area of TSC) Film Mod 0

Address 3C _H : FMBMS (Film Blank Most Significant bits) Control Register. Default value 66 _H									
The eight bits in shown below:	n the FMBMS	S register con	trol the positi	ion of the are	a of the image	used in the F	Film Mode D	etector, as	
Bit	7 6 5 4 3 2 1 0								
Mnemonic	$FmBlnkL_8$ $FmBlnkR_9$ $FmBlnkR_8$ $FmBlnkT_8$ $FmBlnkBN_9$ $FmBlnkBN_8$ $FmBlnkBP_9$ $FmBln$								
Default value	0	1	1	0	0	1	1	0	
EdBlkL ₈ :					1 _H , sets the po description o			of the area	
EdBlkR ₉₋₈ :					r 32 _H , set the p or. See descrip				
EdBlkT ₈ :					33 _H , sets the p cription of reg			rea of the	
EdBlkBN ₉₋₈ :	image used		Aode Detecto	or when the ir	r 34 _H , set the p nput signal cor				
EdBlkBP ₉₋₈ :	image used		Aode Detecto	or when the ir	r 35 _H , set the p nput signal cor				
			D • 4						

Address $3D_H$ through Address 54_H : Test Registers

These 24 registers are used purely for test purposes and should not be changed at any time for normal operation. The default values are listed below for reference only.

Address Def	fault value	Address Def	fault value
$3D_{H}$	14 _H	49_{H}	37 _H
3E _H	$0E_{H}$	$4A_{H}$	1C _H
$3F_{H}$	$60_{ m H}$	$4B_{H}$	58 _H
$40_{\rm H}$	05_{H}	$4C_{H}$	38 _H
$41_{\rm H}$	$0C_{H}$	$4D_{H}$	$00_{\rm H}$
42 _H	14 _H	$4E_{H}$	07 _H
43 _H	D5 _H	$4F_{H}$	04 _H
44 _H	28 _H	50 _H	$14_{\rm H}$
45_{H}	64 _H	51 _H	18 _H
46 _H	08 _H	52 _H	06 _H
$47_{ m H}$	70 _H	53 _H	30 _H
48_{H}	CO _H	54 _H	30 _H

Bit	7	6	5	4	3	2	1	0
Mnemonic	MDiv ₇	MDiv ₆	MDiv ₅	$MDiv_4$	MDiv ₃	MDiv ₂	MDiv ₁	MDiv ₀
Default value	0	0	0	1	1	0	0	0
MDiv ₇₋₀ :	used to set 1 MHz \leq f _c f _{CLKIN} 8 to 16 MH 16 to 32 M 32 to 54 M	the M pre-di $CLKIN/M \le 2 P$ MDiv Hz 08_{H} Hz 10_{H} Hz 20_{H}	vider factor f MHz. PDiv s NDiv 1 08 _H 2 10 _H 2 20 _H	in the PLL ac hould then be PDiv 3 _H 2 _H 1 _H grammed aut	eccording to the set so that 2	The requirement the input pixel $2^{(6-PDiv)} = MD^2$ the PLLOvr b	clock freque iv. The value	ncy, so tha es will be:
					., as shown be	elow:		
The eight bits in				N in the PLI	2, as shown be 3	elow: 2	1	0
The eight bits in Bit	n the PLL1 reg 7	gister set the c 6	livider factor 5	N in the PLI	3			0 NDiv ₀
Address 61 _H : 1 The eight bits in Bit Mnemonic Default value	n the PLL1 reg 7	gister set the c 6	livider factor 5 NDiv ₅	N in the PLI	3	2		

Bit	below:												
	7	6	5	4	3	2	1	0					
Mnemonic	Lock	Х	Disable	РВур	PLLOvr	PDiv ₂	PDiv ₁	PDiv ₀					
Default value	R/O	Х	0	0	0	0	1	0					
Lock			ock status of th	e PLL, as sł	nown below. I	t is a read-onl	y (R/O) func	tion.					
		= PLL not lo											
	1	= PLL locked	1.										
х:	This bit is	not used an	d does not exis	t physically	·.								
Disable:	This bit al	lows the PL	L to be disable	d for test pu	rposes, as foll	ows:							
	0*												
	1	= PLL is dis	abled for test p	urposes.									
PByp:	This bit al	lows the PL	L to be bypasse	ed for test p	urposes, as fol	lows:							
	0*	= PLL is not	bypassed. The	is is the nor	mal mode of o	peration.							
	1	= PLL is by	passed.										
PLLOvr:	This bit controls the programming of the PLL, as follows:												
			will be program		-	-	-						
		NDiv = 30 _H case it will l	, MDiv = $0C_{H}$) unless the l for a 27 M	D1 (Y/Cb/Cr) Hz clock (PD	input format iv = 2, NDiv	is selected, i = 30 _H , MDiv	n which					
		NDiv = 30 _H case it will l	, MDiv = $0C_{\rm H}$) unless the l for a 27 M	D1 (Y/Cb/Cr) Hz clock (PD	input format iv = 2, NDiv	is selected, i = 30 _H , MDiv	n which					
PDiv ₂₋₀ :	1 These bits	NDiv = 30 _H case it will I = PLL regis set the post	, MDiv = $0C_{H^{2}}$ be programmed ters at addresse -divider factor) unless the l for a 27 M es 60 _H - 62 _F P in the PL	D1 (Y/Cb/Cr) Hz clock (PD must be prog L, determinin	input format iv = 2, NDiv grammed man g the clock fr	is selected, i = 30 _H , MDiv ually. equency. PD	n which $f = 18_{\rm H}$).					
PDiv ₂₋₀ :	1 These bits be set as s	NDiv = 30 _H case it will I = PLL regis set the post hown in the	, $MDiv = 0C_H \lambda$ be programmed ters at addresse) unless the l for a 27 M es 60 _H - 62 _F P in the PL the PLL1 r	D1 (Y/Cb/Cr) [Hz clock (PD ₁ must be prog L, determinin egister above,	input format iv = 2, NDiv grammed man g the clock fr such that $2^{(6-1)}$	is selected, i = $30_{\rm H}$, MDiv ually. equency. PD PDiv) = MDiv	n which $f = 18_{\rm H}$).					
	1 These bits be set as s double the	NDiv = 30 _H case it will I = PLL regis set the post hown in the clock, as re	, MDiv = $0C_H$ be programmed ters at addresse -divider factor description of equired. See de) unless the l for a 27 M es 60 _H - 62 _F P in the PL the PLL1 r escription o	D1 (Y/Cb/Cr) [Hz clock (PD ₁ must be prog L, determinin egister above,	input format iv = 2, NDiv grammed man g the clock fr such that $2^{(6-1)}$	is selected, i = $30_{\rm H}$, MDiv ually. equency. PD PDiv) = MDiv	n which $f = 18_{\rm H}$).					
PDiv ₂₋₀ : Address 63 _H : 6 The OUTPUT	1 These bits be set as s double the OUTPUT Co	NDiv = 30 _H case it will I = PLL regis set the post hown in the clock, as re ntrol Regist	, MDiv = $0C_H$ be programmed ters at addresse -divider factor description of equired. See de er 2. Default v) unless the 1 for a 27 M es $60_{\rm H}$ - $62_{\rm F}$ P in the PL the PLL1 r escription o alue $00_{\rm H}$	D1 (Y/Cb/Cr) Hz clock (PD _I must be prog L, determinin egister above, f register 60 _H	input format iv = 2, NDiv grammed man g the clock fr such that $2^{(6-1)}$	is selected, i = $30_{\rm H}$, MDiv ually. equency. PD PDiv) = MDiv	n which $f = 18_{\rm H}$).					
Address 63 _H : 0	1 These bits be set as s double the OUTPUT Co	NDiv = 30 _H case it will I = PLL regis set the post hown in the clock, as re ntrol Regist	, MDiv = $0C_H$ be programmed ters at addresse -divider factor description of equired. See de er 2. Default v) unless the 1 for a 27 M es $60_{\rm H}$ - $62_{\rm F}$ P in the PL the PLL1 r escription o alue $00_{\rm H}$	D1 (Y/Cb/Cr) Hz clock (PD _I must be prog L, determinin egister above, f register 60 _H	input format iv = 2, NDiv grammed man g the clock fr such that $2^{(6-1)}$	is selected, i = $30_{\rm H}$, MDiv ually. equency. PD PDiv) = MDiv	n which $f = 18_{\rm H}$).					
Address 63 _H : 0 The OUTPUT Bit Mnemonic	1 These bits be set as s double the OUTPUT Co control regist	NDiv = 30 _H case it will I = PLL regis set the post hown in the clock, as re ntrol Regist er controls s	, MDiv = $0C_H$ be programmed ters at addresse -divider factor description of equired. See de er 2. Default v ome of the out) unless the 1 for a 27 M es $60_{\rm H}$ - $62_{\rm F}$ P in the PL the PLL1 r escription o alue $00_{\rm H}$ put function	D1 (Y/Cb/Cr) (Hz clock (PD) $_{\rm H}$ must be prog L, determinin egister above, f register $60_{\rm H}$	input format iv = 2, NDiv grammed man g the clock fr such that $2^{(6-1)}$ for more deta	is selected, i = $30_{\rm H}$, MDiv ually. equency. PD $^{\rm PDiv}$ = MDiv ils.	n which r = 18 _H). Piv should . This wil					
The OUTPUT Bit	1 These bits be set as s double the OUTPUT Co control regist 7	NDiv = 30 _H case it will I = PLL regis set the post hown in the clock, as re ntrol Regist er controls s 6	, MDiv = $0C_H$ be programmed ters at addresse -divider factor description of equired. See de er 2. Default v ome of the out) unless the 1 for a 27 M es $60_{\rm H}$ - $62_{\rm F}$ P in the PL the PLL1 r escription o alue $00_{\rm H}$ put function 4	D1 (Y/Cb/Cr) Hz clock (PD IHz clock (PD L, determinin egister above, f register $60_{\rm H}$ s, as follows: 3	input format iv = 2, NDiv grammed man g the clock fr such that 2 ⁽⁶⁻ for more deta	is selected, i = 30_{H} , MDiv ually. equency. PD $^{PDiv)} = MDiv$ ils.	n which = 18 _H). Piv should . This will					
Address 63 _H : 0 The OUTPUT Bit Mnemonic	1 These bits be set as s double the OUTPUT Co control regist 7 x x x	NDiv = 30 _H case it will I = PLL regis set the post hown in the clock, as re ntrol Regist er controls s 6 x x x	, MDiv = $0C_H$ be programmed ters at addresse -divider factor description of equired. See de er 2. Default v ome of the outp 5 x) unless the l for a 27 M es 60 _H - 62 _F P in the PL the PLL1 r escription o alue 00 _H put function 4 x x x	D1 (Y/Cb/Cr) Hz clock (PD Hz clock (PD L, determinin egister above, f register 60_H s, as follows: 3 x x x	input format iv = 2, NDiv grammed man g the clock fr such that 2 ⁽⁶⁻ for more deta	is selected, i = $30_{\rm H}$, MDiv ually. equency. PD PDiv) = MDiv ils. 1 GOutDis	n which = 18 _H). Piv should . This wil					
Address 63 _H : 6 The OUTPUT Bit Mnemonic Default value	1 These bits be set as s double the OUTPUT Co control regist 7 x x x These bits	NDiv = 30 _H case it will 1 = PLL regis set the post hown in the clock, as re ntrol Regist er controls s 6 x x x are not use	, MDiv = $0C_H$ be programmed ters at addresse -divider factor description of equired. See de er 2. Default v ome of the out 5 x x x) unless the 1 for a 27 M es $60_H - 62_F$ P in the PL the PLL1 r escription o alue 00_H put function 4 x x x x	D1 (Y/Cb/Cr) Hz clock (PD IHz clock (PD L, determinin egister above, f register 60_H s, as follows: 3 x x x x	input format iv = 2, NDiv grammed man g the clock fr such that 2 ⁽⁶⁻ for more deta 2 ROutDis 0	is selected, i = $30_{\rm H}$, MDiv ually. equency. PE PDiv) = MDiv ils. 1 GOutDis 0	n which = 18 _H). Piv should . This wil					

PLL, as shown belo Bit Mnemonic Default value	7			lie FLL2 leg	ister control t	he operation of	of the clock g	eneration
Mnemonic Default value		6	5	4	3	2	1	0
	Test	Test	InvYClk	Test	Test	Test	Test	Test
	0	0	0	0	0	0	0	0
	These bits a operation.	ll put the F	LI2200 into sp	ecial test mo	des and shou	ld always be s	et low for no	rmal
	This bit con follows:	trols the ph	ase of the inter	nal 27 MHz	sampling clo	ck used in the	IFormat = 11	x modes, a
	0* =	Sampling c	lock has same	phase as PIX	CLK, sample	es on falling ed	lgesof PIXCI	LK
	1 =	Sampling c	lock is inverted	d relative to I	PIXCLK, sam	ples on rising	edges of PIX	CLK
	It is rec	commended	that this settin	g be used in	the IFormat	= 11x modes		
Address 65 _H : Test	-			1 . 1 1	1	C	1	TD1 1 C 1
This register is use value is $00_{\rm H}$ (for re			oses and should	l not be char	nged at any ti	me for norma	l operation.	The defaul
H (<i>JT</i> ²						
Address 66 _H : Inp	ut HSvnc D	elav Contr	ol Register. De	efault value	00			
						C. 11		
The Input HSync I	Delay control	ol register c	ontrols the inp	ut horizonta	l sync timing.	, as follows:		
The Input HSync I Bit	Delay contro 7	ol register c 6	ontrols the inp 5	ut horizonta 4	l sync timing. 3	, as follows: 2	1	0
Bit	-	-	5	4	3		-	0
The Input HSync I Bit Mnemonic Default value	7	6	5	4	3	2	-	Ũ
Bit Mnemonic Default value	7 x x	6 x x	5 x x	4 IHSyncDel ₄ 0	3 IHSyncDel ₃ 0	2 IHSyncDel ₂	IHSyncDel ₁	IHSyncDe
Bit Mnemonic Default value x:	7 x x These bits a	6 x x are not used	5 x x and do not ex	4 IHSyncDel ₄ 0 ist physicall	3 IHSyncDel ₃ 0 y.	2 IHSyncDel ₂ 0	IHSyncDel ₁ 0	IHSyncDe 0
Bit Mnemonic Default value x: IHSyncDel ₄₋₀ :	7 x x These bits a These bits s The adjustn	6 x x are not used tet the input nent is in 1	5 x x and do not ex horizontal syn pixel increme	4 IHSyncDel ₄ 0 ist physicall ac timing. The nts relative	3 IHSyncDel ₃ 0 y. he number is	2 IHSyncDel ₂ 0 a signed, two	IHSyncDel ₁ 0	IHSyncDe 0 nt value.
Bit Mnemonic Default value x: IHSyncDel ₄₋₀ :	7 x x These bits a These bits s The adjustm shown in th	6 x x are not used set the input nent is in 1 ne timing di	5 x x and do not ex horizontal syn pixel increme agrams, as fol	4 IHSyncDel ₄ 0 ist physicall ac timing. The nts relative to lows:	3 IHSyncDel ₃ 0 y. he number is to the default	2 IHSyncDel ₂ 0 a signed, two	IHSyncDel ₁ 0	IHSyncDe 0 nt value.
Bit Mnemonic Default value x: IHSyncDel ₄₋₀ :	7 x x These bits a These bits s The adjustn shown in th ISyncD	6 x x are not used set the input nent is in 1 ne timing di Del ₄₋₀	5 x x and do not ex horizontal syn pixel increme agrams, as fol Timing rel	4 IHSyncDel ₄ 0 ist physicall ac timing. The nts relative to lows: lative to defa	3 IHSyncDel ₃ 0 y. he number is to the default	2 IHSyncDel ₂ 0 a signed, two	IHSyncDel ₁ 0	IHSyncDe 0 nt value.
Bit Mnemonic Default value x: IHSyncDel ₄₋₀ :	7 x x These bits a These bits s The adjustm shown in th ISyncD	6 x x are not used set the input nent is in 1 ne timing di	5 x x and do not ex horizontal syn pixel increme agrams, as fol	4 IHSyncDel ₄ 0 ist physicall ic timing. The nts relative lows: lative to defa	3 IHSyncDel ₃ 0 y. he number is to the default	2 IHSyncDel ₂ 0 a signed, two	IHSyncDel ₁ 0	IHSyncDe 0 nt value.

Address 7E and Address 7F_H: Chip Identification Registers. Default values: $7E_H = 41_H$, $7F_H = 4B_H$ (Read Only) The eight bits in the IDL and IDH registers contain the 16-bit chip identification information. Register $7E_H$ contains the lower byte and register $7F_H$ contains the upper byte, so that the chip identification number is $4B41_H$.

Control Bus Operation and Control Protocol

When the MODE pin (pin 46) is set low the FLI2200 operates as a slave device, responding to commands from a master controlling the bus. The protocol is generally I²C compatible. Between operations the master sets the bus into the idle state, during which the master releases both the clock (SCL) and data (SDA) lines so that they both go high. All operations commence with a START (S) command from the master; this is indicated by the master setting the SDA line low while the clock is in the high state, as shown in Fig. 1. The clock then goes low and an operation begins. All write operations consist of 8-bit (byte) transfers either from or to the master, after which the receiving slave responds with an Acknowledge (A) by setting the SDA line low for one clock cycle. In the read operation process is similar but the receiver (the master in this case) omits the acknowledge after the data byte is read from the FLI2200. During the course of all operations the SDA line will only change while the SCL line is low, and should remain stable while SCL is high. The master indicates the end of an operation or set of operations with a STOP (P) command, indicated a rising edge on SDA while SCL is high. Sets of multiple operations can be executed by means of further START commands at the end of each operation with or without a STOP.

In all cases, the first byte is always the Slave Address byte, sent from the master to select the desired device. The settings of the $ADDR_{1-0}$ pins allow the device address of the FLI2200 to be programmed to prevent conflict with the other devices connected to the bus. The slave address can be set to any of the following values, as follows:

ADDR ₁₋₀	Device Address
00	C0/C1 _H
01	C2/C3 _H
10	E0/E1 _H
11	E2/E3 _H

The seven MSBs of the Slave Address byte are the Slave Address itself and the LSB is the Read/Write bit. When the R/W bit is set low (write mode) it indicates that the master is going to transfer more bytes, as shown in Fig. 2. The minimum write operation consists of two more bytes, the Register Address (which selects the register to be written) followed by the Data Byte for that address. The FLI2200 will respond with an Acknowledge after each byte. The master follows these with a STOP command, terminating the operation. Multiple registers can also be written sequentially using the Auto Increment capability of the FLI2200. By sending further bytes of data before the STOP command, as shown in Fig. 3, the address is automatically incremented as each sequential byte is written. This is followed by a STOP bit, as before, to terminate the operation.

When the R/W bit is set high (read mode) it indicates that the master intends the Slave to respond with a data byte from the specified register address. The register address must first be set by writing a Register Address byte to the FLI2200 (with R/W set high) without an accompanying Data Byte. The FLI2200 then responds by sending the contents of that register, as shown in Fig. 4. The master should terminate the operation at this point by **Not** (**N**) issuing an Acknowledge, followed by a STO**P** command. The FLI2200 only has one register containing a read-only bit, the PAL status bit, bit 7 in register 07_H. Consequently, multiple byte read with auto increment is not supported in the FLI2200.

In addition, although it is technically legal under I^2C protocol to abort a sequence after issuing a **S**TART followed by a device address, the FLI2200 will not release the bus unless it receives a **S**TOP before another **S**TART is issued once it is addressed in this way.

When the MODE pin is set high the FLI2200 will self program from an I²C compatible serial memory by reading 128 bytes of data after it is reset. The memory must first be pre-programmed with the necessary programming information.

Control Bus Timing

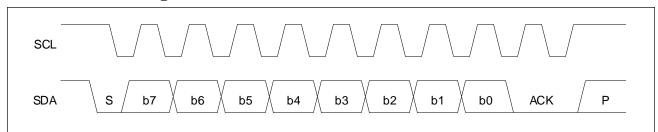
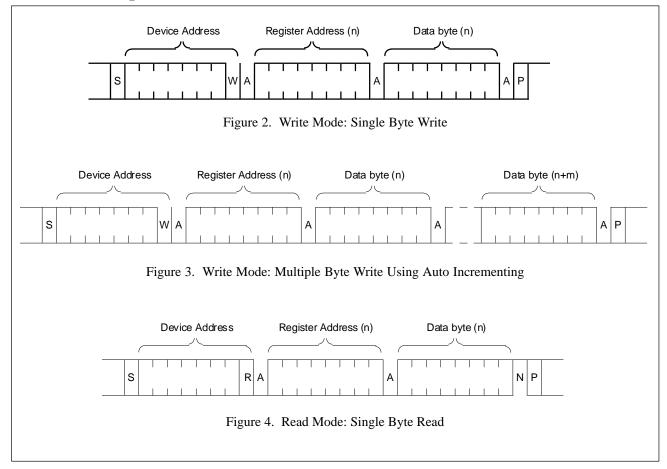


Figure 1. Control Interface Timing

Control Bus Operation and Control Protocol



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	-40 to $+85^{\circ}$ C
Storage temperature (T _{ST})	-65 to $+150^{\circ}$ C
Voltage on V _{DD33} pins with respect to ground (V _{SS})	-0.5 to $+V$
Voltage on V_{DD25} pins with respect to ground (V_{SS})	-0.5 to $+V$
Voltage on any pin with respect to ground (V _{SS})	-0.3 to $+3.6$ V
Input current on any pin during overload condition	-10 to $+10$ mA
Absolute sum of all input currents during overload condition	100 mA
Power dissipation	1.75 W

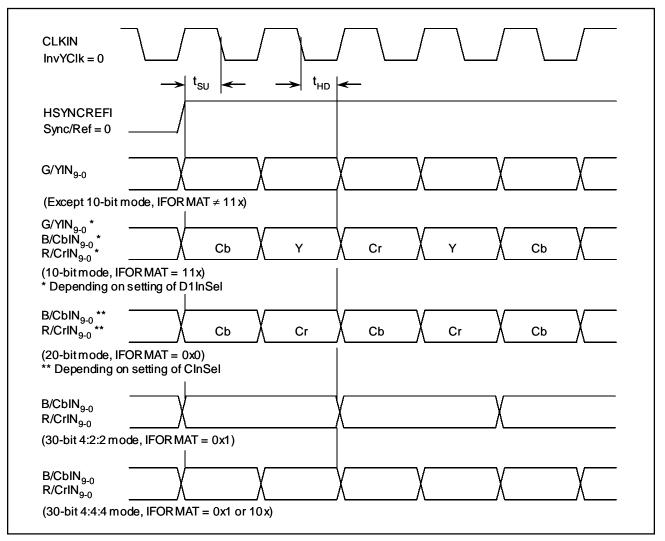
Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions $(V_{IN} > V_{DD} \text{ or } V_{IN} < V_{SS})$ the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

D.C. Characteristics

Unless otherwise noted, limits printed in **bold** characters are electrical testing limits at $V_{DD33} = 3.3$ volts, $V_{DD25} = 2.5$ volts and $T_A = 25^{\circ}$ C. All other limits are design goals for $V_{DD33} = 3.3$ volts $\pm 5\%$, $V_{DD25} = 2.5$ volts $\pm 5\%$ and $T_A = 0^{\circ}$ to 70° C. This data sheet is preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact Faroudja Laboratories for the most current product information.

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input low voltage	V _{IL}	-0.3		0.8	Volts	
Input high voltage	V _{IH}	2.0		V _{DD33} +0.3	Volts	
Output low voltage	V _{OL}			0.4	Volts	See note
Output high voltage	V _{OH}	$0.85 \cdot V_{DD33}$		V _{DD33}	Volts	See note
Input leakage current	IL			± 10	μA	$0 < V_{IN} < V_{DD}$
Pullup resistor value	R _{PU}	50		250	kΩ	TEST ₂₋₀ only
Digital input pin capacitance	CI			4	pF	$f_{\text{TEST}} = 1 \text{ MHz}$
Digital output pin capacitance	Co			8	pF	$f_{\text{TEST}} = 1 \text{ MHz}$
Bidirectional pin capacitance	C _B			2	pF	$f_{\text{TEST}} = 1 \text{ MHz}$
Power supply current	I _{DD33}		45		mA	$V_{DD33} = 3.3$ volts
			50		mA	V _{DD33} =3.6 volts
						$f_{CLKIN} = 13.5 \text{ MHz},$
						$RESET = V_{SS}$
	I _{DD25}		350		mA	V _{DD25} =2.5 volts
			375		mA	V _{DD25} =2.65 volts
						$f_{CLKIN} = 13.5 \text{ MHz},$
						$RESET = V_{SS}$

Input Signal Timing



Input Signal Timing

Symbol	Description	Min.	Max.	Units	Conditions
f _{PIXCLK}	Input clock frequency		13.5	MHz	IFormat $\neq 11x$, NOMEM = 0 or NMOvr = 1 NoMem = 0
			27	MHz	IFormat = $11x$, NOMEM = 0 or NMOvr = 1 NoMem = 0
			37.5	MHz	IFormat $\neq 11x$, NOMEM = 1 or NMOvr = 1 NoMem = 1
			75	MHz	IFormat = 11x, NOMEM = 1 or NMOvr = 1 NoMem = 1
t _{SU}	Input to clock setup	0		nsec.	
t _{HD}	Input to clock hold	0		nsec.	

Output Signal Timing

усько
ссіко
G/YOUT ₉₋₀
(10-bitmode, OFOR MAT = 11x)
G/YOUT ₉₋₀
(Except 10-bit mode, OFOR MAT \neq 11 x)
B/CbOUT ₉₋₀ * Cb Cr Cb Cr Cb Cr Cb
(20-bit mode, OFOR MAT = 0x0) * Depending on setting of COutSel
R/CrOUT ₉₋₀ B/CbOUT ₉₋₀
(30-bit 4:2:2 mode, OFOR MAT = 0x1)
R/CrOUT ₉₋₀ B/CbOUT ₉₋₀
(30-bit 4:4:4 mode, OFOR MAT = 0x1 or 10x)

Output Signal Timing

Symbol	Description	Min.	Nom.	Max.	Units	Conditions
f _{YCLKOUT}	Output luma clock frequency Clock to output delay	_3		75 +3	MHz nsec.	
^t PDO	clock to output delay	-3			nsee.	

Applications Information

Deinterlacing video signals: Optimal solutions for optimal images under different conditions

There are several different conditions that exist in video signals that require different approaches to deinterlacing. The first and most obvious is a moving image (or portion of an image) versus a still image (or portion of an image). It is fairly obvious that still images can be deinterlaced simply by interleaving the odd and even fields, i.e., forming a full frame of 525 (in the case of NTSC) lines by taking the 262.5 lines from the odd field 1, 3, 5, etc. and interleaving them with the 262.5 lines from the even field (2, 4, 6, etc.) to form a complete frame of 525 lines (1, 2, 3, 4, etc.) and displaying it at the field rate, i.e., 59.94 Hz. However, if anything in the image moves between the odd and even fields the results will be disastrous! An example is shown in Fig. A1, below, where the car is moving from left to right. If the car is moving at 60 mph it will have moved 1.5 feet between the frames.

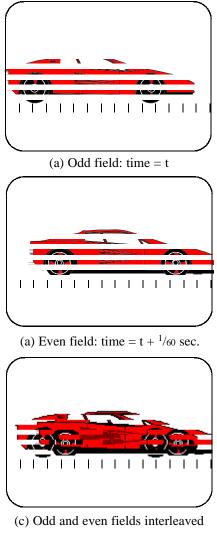


Fig. A1. The result of interleaving fields containing motion.

The way to deal with a moving image is to deal with the fields independently and generate the missing lines in each field by interpolation. There are several way in which this can be done, the easiest being to assume that the image is always going to be in motion, and interpolate all the time. This, of course, results in an image which appears to very soft when (and where) there is no motion as a result of the fact that the true vertical resolution has been reduced, relative to the original image.

The second method is to use a motion detector of some kind to detect whether anything has moved from frame to frame and to use this to control the system: interpolate when motion is detected, interleave when no motion is detected. Although it is possible to implement a motion detector simply by computing a metric for each field and comparing it with that for the same field from the previous frame, this only allows the choice of interleave versus interpolate to be made on a field by field basis. In addition, unless a field memory (delay) is used, the metric for the current field cannot be computed until the field has already been displayed. This is an extremely undesirable condition since the motion/no motion condition on a per field basis changes continuously. Even when the field delay is used, this method is far from optimum because any motion anywhere in the image will cause the system to switch into interpolate mode, resulting in soft images in areas of the picture containing no motion, a very common condition.

A much better way is to compute a motion metric on a pixel by pixel basis, and this is the method used in the FLI2200. The motion detector is frame based and compares the luma value of the current pixel and the same pixel in the previous frame. This is done in both the odd and even fields to generate a motion vector which is then used to switch the signal processing between field interleave and interpolation modes on a pixel by pixel basis. In this way, non-moving parts of the picture, where sharpness is readily detected by the viewer, will not be interpolated and will have maximum sharpness. Conversely, moving parts of the picture, where sharpness is not easily detected by the viewer, will be interpolated to avoid motion artifacts.

The most common method of implementing the interpolation function is to use a 2-line memory and generate the interpolated pixels from the pixel above (previous line) and the pixel below (next line). This implementation can be improved by using more "previous" and "next" lines to implement a higher order interpolating filter, giving slightly sharper images. However, no matter how complex the interpolating filter is, it always operates on the basis that the current pixel is

related to the pixels above and below it, which is completely untrue of diagonal edges. Whenever an edge is not vertical, the current pixel is related to those diagonally above and below it in a relationship which depends on the angle of the edge, e.g., if the angle is 45°, the relationship is "one up and one across" and "one down and one across". With other angles becomes more complex and will involve non-integer relationships. Consequently, it is extremely difficult to implement such a "diagonal interpolation" algorithm, but this has been achieved in the FLI2200. This new algorithm (patent pending) computes and tracks the angles of edges and uses this information to optimally fill in the missing pixels. It greatly improves the quality of moving images, particularly those in fairly slow motion, such as the waving flag shown in Fig. A2 below, by eliminating the "jaggies" conventionally generated by interpolation.

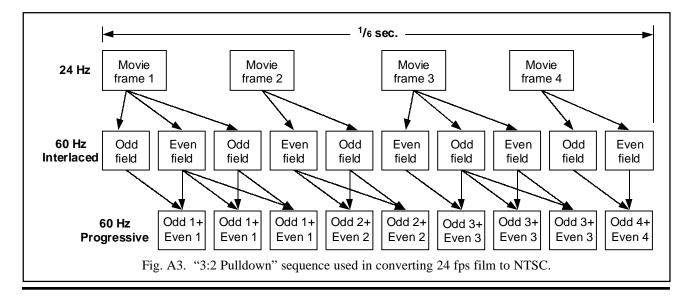


Fig. A2. Conventional vertical interpolation on diagonal edges (L) versus diagonal interpolation (R)

Deinterlacing images which originated from progressive scan sources, including film

Whenever an interlaced image is generated from a progressively scanned image (where the original frame rate equals the field rate after interlacing) the resulting odd and even field pairs will originate from the same frame and, by definition, there will be no motion between them since the images occurred at the same point in time. A special instance of this is the conversion of film to video in a teleciné machine. There are two types of teleciné machines. The first is the one used to convert 24 fps film to 60 field/sec. (30 fps) video, i.e., NTSC. Since it is not practical to run a 24 fps film at 30 fps the technique used is called "3:2 pulldown", in which each film frame is alternately mapped into three video fields and two video fields. The resulting ratio of two film frames to five video fields matches the rate of the film precisely to the 59.94 fields/sec. rate of the video when the film is run at 23.976 fps. The mapping sequence is shown in Fig. A3, below. Note that there are alternating consecutive pairs of odd fields and even fields originating from the same film frame. This makes it possible for a frame based motion detector to synchronize a state machine to this sequence (US patent 4,982,280) and match the odd and even fields originating from the same frame. In this way the video can be deinterlaced by interleaving these fields at all times, regardless of motion, resulting in the ultimate image quality.

The second type of teleciné is the "one film frame to one pair of video fields" type (sometimes referred to as "2:2 pulldown"). This type is primarily used to convert conventional 24 frame/sec. (fps) film to 50 field/sec. video, i.e., PAL. In this case the film is actually run at 25 fps. The 4% speed increase is not noticeable in the video, but those with the sense of "perfect pitch" can detect the raised pitch of the sound track. This type of teleciné is also used to convert 30 fps film to NTSC video. Although there are no pairs of the same field (odd or even) originating form the same film frame in the resulting video it is still possible to detect the sequence by using a field based motion detector and use this to match pairs of fields originating from the same film frame, allowing them to be interleaved, again resulting in the ultimate image quality.



The video resulting from both types of teleciné machines has one problem: if the video is edited, it is possible for the sequence to be broken. In the 2:2 pulldown case there are four possibilities:

- 1. Good cut (at video frame start)
- 2. Bad cut (mid frame, between odd and even fields)
- 3. Good restart (at frame start)
- 4. Bad restart (mid frame)

Both the good cut/good restart and bad cut/bad restart combinations will result in the preservation of the sequence, although the bad cut/bad restart combination will result in a single bad frame (odd and even fields did not originate from the same film frame). Both the good cut/bad restart and bad cut/good restart combinations will break the sequence and result in bad video until the "film mode detect" state machine is resequenced, which typically takes up to 12 frames. Note that if the editor is frame based, only the good cut/good restart combination will occur. The situation with 3:2 pulldown derived video is significantly worse. Even with a frame based editor there are 25 possible cases since the transfer sequence repeats over a period of five video frames, resulting in five possible cut points and five possible restart points. Only two of these will result in good edits, the other 23 resulting in the "film mode detect" state machine going out of sync and having to be resequenced. Thus it is virtually guaranteed that a video edit in NTSC will cause the system to lose sync, resulting in very bad deinterlacing artifacts until it is resequenced.

To minimize the consequences of bad edits, the FLI2200 incorporates a bad edit detector. This will detect even the single bad frame resulting from the bad/bad combination in PAL and, since it operates in a "look forward" mode, will cause the system to switch out of film mode before even a single bad field is displayed. The resulting lower quality video mode is preferable to the alternative, given the pixel by pixel motion handling and the high quality of the diagonal interpolation, even in the single bad frame case.

Interfacing the FLI2200 to video and MPEG decoders with ITU-R BT656 outputs

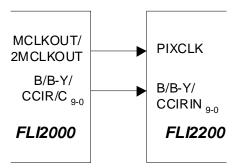


Fig. A4. Interfacing the FLI2200 to the FLI2000 NTSC/PAL decoder using the ITU-R BT656 (D1) format.

Interfacing the FLI2200 to an 8- or 10-bit parallel ITU-R BT656 (D1) signal source, suchas the FLI2000, is very simple since the FLI2200 can decode these signals. Since these signals include timing information in the horizontal and vertical banking intervals, no other syncs are required, so that the only interconnections required are the 10-bit data and the clock, as shown in Fig. A4. The input signal format can be controlled by means of the IFORMAT₂₋₀

pins (pins 56-58). The correct setting for the ITU-R BT656 input mode is 110. This setting can be overridden by the IFmtOvr bit, bit 3 in register 00_{H} , allowing this function to be set or changed via the control bus if preferred. Please refer to the description of register 00_{H} for details. It is recommended that the interconnections be kept short since the operating speed in this mode is 27 MHz.

Input modes and busses

The FLI2200 has very flexible input and output controls that make it very easy to use in all applpications. The input formats and modes are summarized in the table below. For reference, the signals are as follows:
$$\begin{split} & \text{IFORMAT}_{2\text{-}0} \text{ pins are pins 56-58} \\ & \text{IFormat}_{2\text{-}0} \text{ are bits 2-}0 \text{ in register } 00_{\text{H}} \\ & \text{IFmtOvr is bit 3 in register } 00_{\text{H}} \\ & \text{CInSel is bit 6 in register } 08_{\text{H}} \\ & \text{D1InSel}_{1\text{-}0} \text{ are bits 4-3 in register } 08_{\text{H}} \end{split}$$

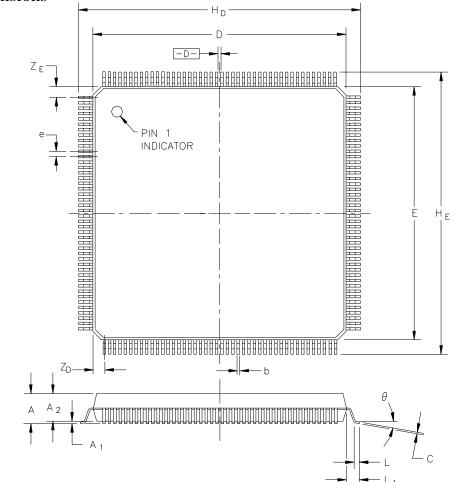
					Input	signals on	busses	
IFORMAT ₂₋₀	IFmtOvr	IFormat ₂₋₀	CInSel	D1InSel ₁₋₀	G/YIN	B/CbIN	R/CrIN	Clock rate/mode
000	0	x	0	х	Y	Cb/Cr	х	(13.5 MHz, 4:2:2)
000	0	x	1	х	Y	х	Cb/Cr	(13.5 MHz, 4:2:2)
001	0	x	х	х	Y	Cb	Cr	(13.5/6.75 MHz, 4:2:2)
010	0	x	0	х	Y	Pb/Pr	х	(13.5 MHz, 4:2:2)
010	0	x	1	х	Y	х	Pb/Pr	(13.5 MHz, 4:2:2)
011	0	x	х	х	Y	Pb	Pr	(13.5/6.75 MHz, 4:2:2)
100	0	x	Х	х	G	В	R	(13.5 MHz, 4:4:4)
101	0	x	Х	х	G	В	R	(13.5 MHz, 4:4:4)
110	0	x	х	00	Y/Cb/Cr	х	х	(27 MHz, embedded timing)
110	0	x	х	01	Y/Cb/Cr	х	х	(27 MHz, embedded timing)
110	0	x	х	10	х	Y/Cb/Cr		(27 MHz, embedded timing)
110	0	x	х	11	х	х	Y/Cb/Cr	(27 MHz, embedded timing)
111	0	x	х	00	Y/Cb/Cr	х	х	(27 MHz, separate timing/syncs)
111	0	x	х	01	Y/Cb/Cr	х	х	(27 MHz, separate timing/syncs)
111	0	x	х	10	х	Y/Cb/Cr	х	(27 MHz, separate timing/syncs)
111	0	x	х	11	х	х	Y/Cb/Cr	(27 MHz, separate timing/syncs)
x	1	000	0	х	Y	Cb/Cr	х	(13.5 MHz, 4:2:2)
x	1	000	1	х	Y	х	Cb/Cr	(13.5 MHz, 4:2:2)
x	1	001	х	х	Y	Cb	Cr	(13.5/6.75 MHz, 4:2:2)
x	1	001	0	х	Y	Pb/Pr	х	(13.5 MHz, 4:2:2)
x	1	010	1	х	Y	х	Pb/Pr	(13.5 MHz, 4:2:2)
x	1	011	х	х	Y	Pb	Pr	(13.5/6.75 MHz, 4:2:2)
x	1	100	х	х	G	В	R	(13.5 MHz, 4:4:4)
x	1	101	х	х	G	В	R	(13.5 MHz, 4:4:4)
x	1	110	х	00	Y/Cb/Cr	х	х	(27 MHz, embedded timing)
x	1	110	х	01	Y/Cb/Cr	х	х	(27 MHz, embedded timing)
x	1	110	х	10	х	Y/Cb/Cr		(27 MHz, embedded timing)
x	1	110	Х	11	х	х	Y/Cb/Cr	(27 MHz, embedded timing)
x	1	111	Х	00	Y/Cb/Cr	х	x	(27 MHz, separate timing/syncs)
x	1	111	х	01	Y/Cb/Cr	х	х	(27 MHz, separate timing/syncs)
x	1	111	Х	10	х	Y/Cb/Cr	x	(27 MHz, separate timing/syncs)
x	0	111	х	11	х	х	Y/Cb/Cr	(27 MHz, separate timing/syncs)

Output modes and busses

The FLI2200 has very flexible input and output controls that make it very easy to use in all applications. The output formats and modes are summarized in the table below. For reference, the signals are as follows: $\begin{array}{l} \text{OFORMAT}_{2\text{-}0} \text{ pins are pins 59-61} \\ \text{OFormat}_{2\text{-}0} \text{ are bits 2-}0 \text{ in register 07}_{\text{H}} \\ \text{OFmtOvr is bit 3 in register 07}_{\text{H}} \\ \text{COutSel is bit 5 in register 08}_{\text{H}} \end{array}$

				Input signals on busses				
OFORMAT ₂₋₀	OFmtOvr	OFormat ₂₋₀	COutSel	G/YOUT	B/CbOUT	R/CrOUT	Clock rate/mode	
000	0	Х	х	G	В	R	(27 MHz, 4:4:4)	
001	0	х	х	Y	Cb	Cr	(27/13.5 MHz, 4:2:2)	
010	0	х	0	Y	Cb/Cr	Y/Cb/Cr	(27/54 MHz, 4:2:2, separate timing/syncs)	
010	0	х	1	Y	Y/Cb/Cr	Cb/Cr	(27/54 MHz, 4:2:2, separate timing/syncs)	
011	0	х	0	Y	Cb/Cr	Y/Cb/Cr	(27/54 MHz, 4:2:2, embedded timing)	
011	0	х	1	Y	Y/Cb/Cr	Cb/Cr	(27/54 MHz, 4:2:2, embedded timing)	
100	0	х	х	Y	Pb	Pr	(27/13.5 MHz, 4:2:2)	
101	0	х	0	Y	Pb/Pr	х	(27 MHz, 4:2:2)	
101	0	х	1	Y	х	Pb/Pr	(27 MHz, 4:2:2)	
110	0	х	х	Y	Cb	Cr	(27 MHz, 4:4:4)	
111	0	х	х	х	х	х	Test mode only	
Х	1	000	х	G	В	R	(27 MHz, 4:4:4)	
Х	1	001	х	Y	Cb	Cr	(27/13.5 MHz, 4:2:2)	
Х	1	010	0	Y	Cb/Cr	Y/Cb/Cr	(27/54 MHz, 4:2:2, separate timing/syncs)	
Х	1	010	1	Y	Y/Cb/Cr	Cb/Cr	(27/54 MHz, 4:2:2, separate timing/syncs)	
Х	1	011	0	Y	Cb/Cr	Y/Cb/Cr	(27/54 MHz, 4:2:2, embedded timing)	
х	1	011	1	Y	Y/Cb/Cr	Cb/Cr	(27/54 MHz, 4:2:2, embedded timing)	
х	1	100	х	Y	Pb	Pr	(27/13.5 MHz, 4:2:2)	
х	1	101	0	Y	Pb/Pr	х	(27 MHz, 4:2:2)	
х	1	101	1	Y	х	Pb/Pr	(27 MHz, 4:2:2)	
х	1	110	х	Y	Cb	Cr	(27 MHz, 4:4:4)	
х	1	111	Х	х	Х	х	Test mode only	

Package Dimensions



	-	Millimeters		Inches			
Ref.	Min.	Тур.	Max.	Min.	Тур.	Max.	
A	1.40		1.60	0.055		0.063	
A1	0.05		0.15	0.002		0.006	
A2	1.35		1.45	0.053		0.057	
b	0.17		0.27	0.007		0.011	
C	0.09		0.20	0.003		0.008	
D		24.0			0.945		
E		24.0			0.945		
e		0.50			0.020		
H _D		26.0			1.024		
H _E		26.0			1.024		
L	0.45	0.60	0.75	0.018	0.024	0.029	
L1		1.00			0.039		
Z _D		1.25			0.05		
Z _E		1.25			0.05		
θ	0°		7°	0°		7 °	

Note: Inch dimensions are derived from the original metric dimensions and may be approximate.

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