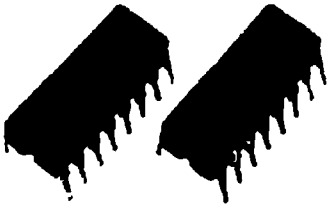
BURR-BROWN®



MPC4D
MPC8S

CMOS ANALOG MULTIPLEXERS

FEATURES

- LOW POWER CONSUMPTION
  CMOS analog switches
  15mW at 100kHz
- PROTECTS SIGNAL SOURCES
  Break-before-make switching
- HIGH THROUGHPUT RATE
- RELIABLE MONOLITHIC CONSTRUCTION

DESCRIPTION

The MPC8S is a single-ended monolithic 8-channel analog multiplexer and the MPC4D is a monolithic 4-channel differential input/output multiplexer. The digital and analog inputs are protected from overvoltage inputs that exceed either power supply. These CMOS devices feature self-contained binary channel address decoding and are compatible with DTL, TTL, or CMOS input levels. Channel interaction is eliminated during overvoltage conditions and also in the event of a power loss. They are packaged in a 16-pin DIP and dissipate typically 7.5mW.

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PDS-356C

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DESCRIPTION

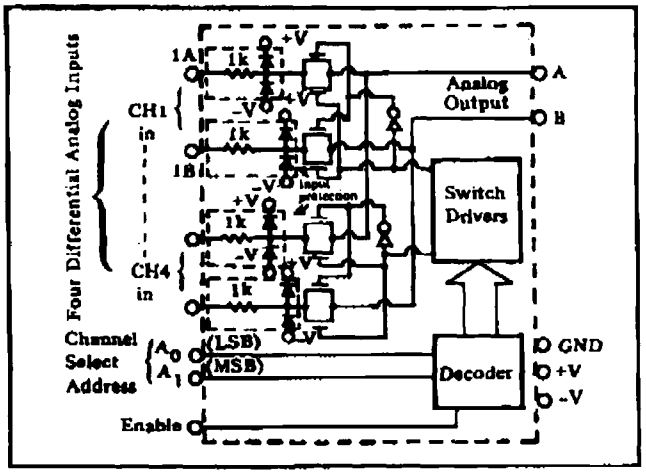
The MPC8S is a single-ended monolithic 8-channel analog multiplexer and the MPC4D is a monolithic differential input/output channel analog multiplexer constructed with failure-protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200kHz from signal sources of up to ±10 volts amplitude.

These DTL/TTL/CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable an 8-channel group (MPC8S) or a 4-channel group (MPC4D) facilitating channel expansion in either single-mode or multitiered matrix configurations.

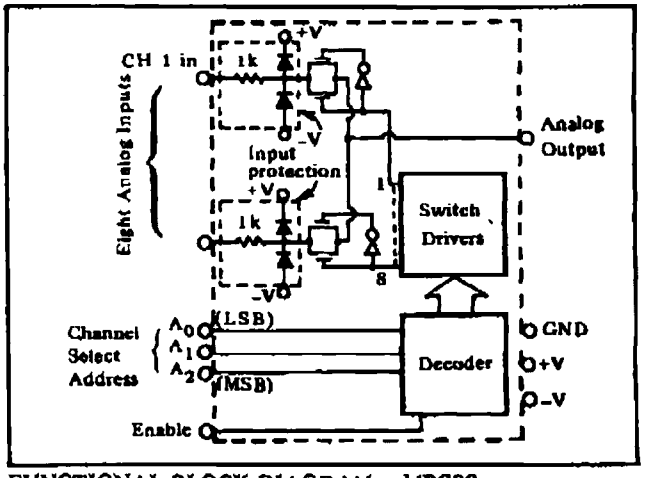
Digital and analog inputs are failure protected from either overvoltages that exceed the power supplies or from the loss of power.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

These devices are housed in compact 16-pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are pin and package compatible with the 508/509 series.



FUNCTIONAL BLOCK DIAGRAM – MPC4D



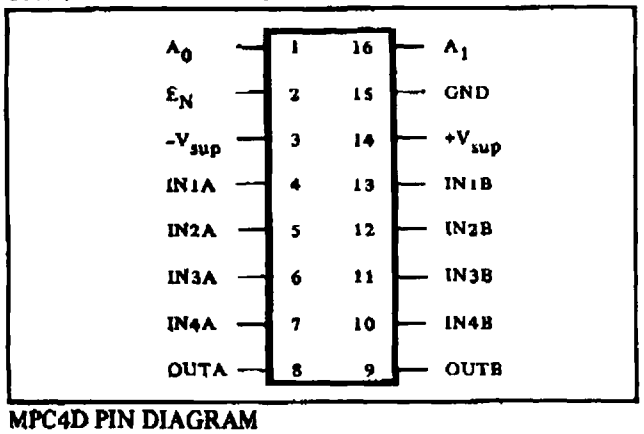
FUNCTIONAL BLOCK DIAGRAM – MPC8S

A_1	A_0	E_N	"On" Switch Pair
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

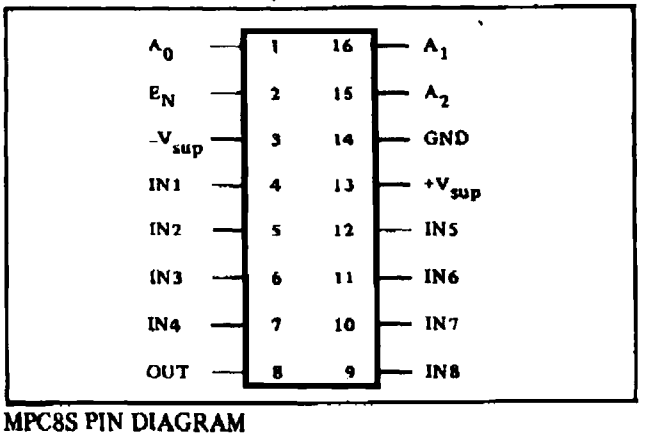
TRUTH TABLE –MPC4D

A_2	A_1	A_0	E_N	On Switch
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE – MPC8S



MPC4D PIN DIAGRAM



MPC8S PIN DIAGRAM

SPECIFICATIONS

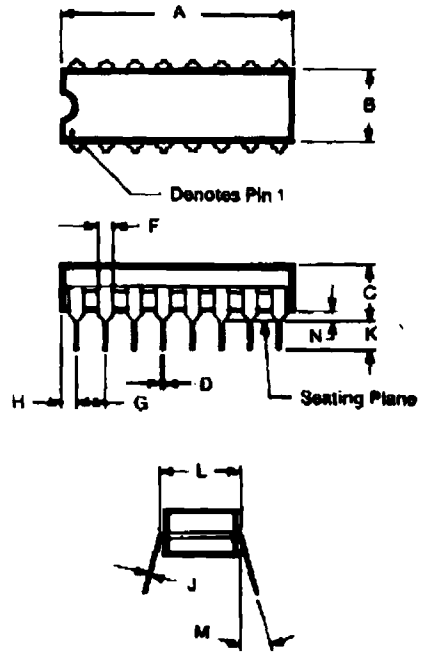
Typical for following conditions: V + = +15V, V - = -15V, $R_{source} \leq 1000\ \Omega$, T_A = 25°C unless otherwise noted.

ELECTRICAL

MODELS	MPC8S	MPC4D	Units
INPUT			
ANALOG INPUT			
Voltage Range	±15		V
Maximum Overvoltage	+V supply +20		V
	-V supply -20		V
Current at Maximum Overvoltage per channel[1]	±18		mA
Number of Input Channels			
Single-ended	8		
Differential		4	
ON Characteristics			
ON Resistance (R_{ON})			
Typical	1.5		kΩ
Maximum	1.8		kΩ
R_{ON} Drift vs. Temperature (0°C to +75°C)	0.25		%/°C
R_{ON} Mismatch			
Channel-to-channel	50	50	Ω
Differential	N/A	50	Ω
Input Leakage (I_L)	0.1		nA
Input Leakage Drift	See Figure 9		
OFF Characteristics			
OFF Resistance	10^{11}		Ω
Output Leakage			
(All channels disabled)	0.2		nA
Input Leakage[6]	0.02		nA
Leakage Drift	See Figure 9		
Output Leakage with Input Overvoltage			
of +35V	1		nA
of -35V	1		μA
DIGITAL INPUTS			
Logic "0" (V_L)[1,2,3]	-V supply ≤ V_L < 0.8 at 1 nA		V
Logic "1" (V_H)[1,2,3]	+4V ≤ V_H ≤ + V supply at 1 nA		V
Channel Select	3 bit binary code - one of eight	2 bit binary code - one of four	
Enable	Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel.		
POWER REQUIREMENTS			
Rated Power Supply Voltages	±15		V
Supply Range			
+Supply	+10 to +20		V
-Supply	-10 to -20		V
Supply Drain			
At 1 MHz Switching Speed	+4, -2		mA
AT 100 kHz Switching Speed	±0.5		mA
Typical Power Consumption			
DC to 10 kHz	7.5		mW
DYNAMIC CHARACTERISTICS			
Gain Error (20 MΩ load) maximum	0.01		%
Crosstalk[4]	0.005		% of OFF channel signal
Settling Time[4]			
To ±2mV ±(0.01%)	5		μs
To ±20mV ±(0.10%)	2		μs
Common-mode Rejection (minimum)	N/A	120	dB
Switching Time			
Turn ON	0.5		μs
Turn OFF	0.3		μs
Recovery Time from Input Overvoltage Pulse of 35V for 100 μsec			
To 0.01%	150		μs
To 0.10%	15		μs
OUTPUT			
Voltage Range	±15		V
Capacitance to Ground	25	12[5]	pF
Capacitance Mismatch	N/A	±10	%
TEMPERATURE			
Specification	0 to +75		°C
Storage	-65 to +150		°C

MPC4D AND MPC8S

Ceramic DIP Package



NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.780	.885	19.30	22.48
B	.220	.280	5.59	7.11
C	—	.200	—	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.300 BASIC		7.62 BASIC	
M	—	15°	—	15°
N	.020	.050	0.51	1.27

NOTES

1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to 0.75W for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Maximum overvoltage is $\pm V_{SUPPLY}$ ±4V at ±15mA.
3. 20V peak-to-peak 1000Hz sinewave; R_{SOURCE} = 1000Ω. same signal on all unused channels.
4. For 20V between switched channels, R_{SOURCE} = 1000Ω. See Figure 5 for settling time versus source impedance (R_S).
5. From each side of MPC4D to ground.
6. Leakage measurement made with all OFF channel inputs fed in parallel to +20V.

DISCUSSION OF PERFORMANCE

Static Transfer Accuracy

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

SINGLE-ENDED MULTIPLEXER STATIC ACCURACY

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of 10^8 ohms or greater will keep resistive loading errors to 0.002% or less for 1000 ohm source impedances. A 10^6 ohm load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000 ohm source resistance will present less than 0.001% loading error and 10,000 ohm source resistance will increase source loading error to 0.01% with a 10^8 ohm load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\epsilon_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

INPUT OFFSET VOLTAGE

Bias current generates an input OFFSET voltage as result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10 nanoamperes will generate an offset voltage of 20μV if a 1000 ohm source is used, and 200μV if a 10,000 ohm source is used. In general, for the MPC8S, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_S)$$

where I_b = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{SOURCE} = Source resistance

DIFFERENTIAL MULTIPLEXER STATIC ACCURACY

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10 to 100 millivolts.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications. Refer to Figure 2.

LOAD (OUTPUT DEVICE) CHARACTERISTICS

- Use devices with very low bias current. Generaly, FET input amplifiers should be used for low level signals less than 50mV RSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be 10^{10} ohms or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC4D is used for multiplexing high-level signals of ±1 volt to ±10 volts full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

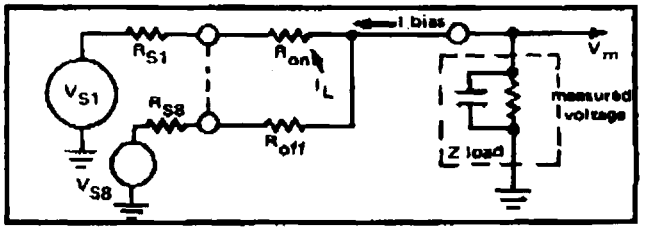


FIGURE 1: MPC8S Static Accuracy Equivalent Circuit.

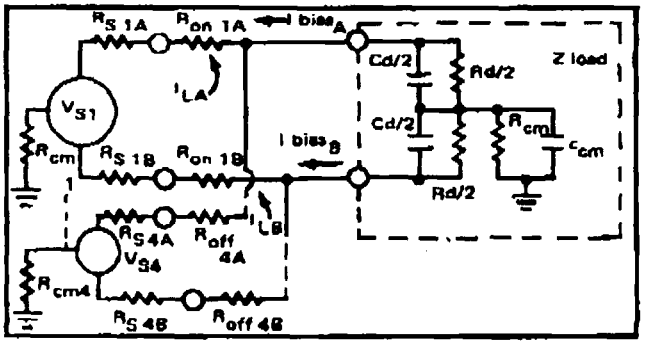


FIGURE 2: MPC4D Static Accuracy Equivalent Circuit.

SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\frac{dV}{dt}$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figure 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. If effect, the amplitude of the transients seen at the source and load are:

$$dV_{load} = \frac{i}{C}\,dt$$

where $i = C\frac{dV}{dt}$ of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Settling Time Curve. This graph shows the settling time for a 20 volt step change on the input. The settling time for smaller step changes on the input will be less than that shown.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10 volt signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the three (MPC4D) or seven (MPC8S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the R_{ON} and R_{SOURCE} impedances of the ON channel. Crosstalk is measured with a 20 volt pk-pk 1000 Hertz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (MPC4D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC4D, protection is provided for common-mode signals of ±20 volts above the power supply voltages with no damage to the analog switches.

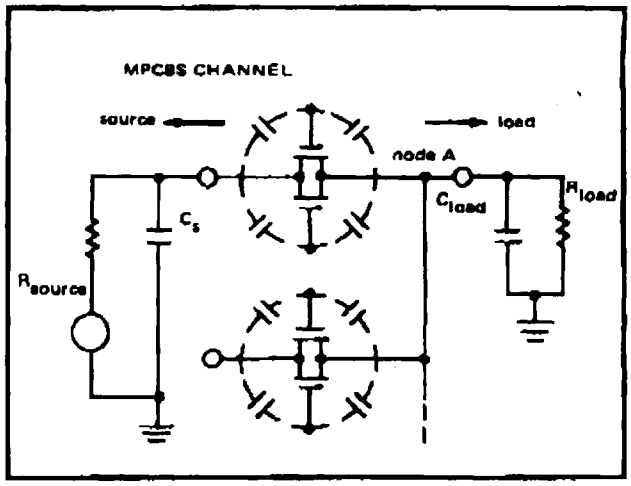


FIGURE 3: Settling Time Effects – MPC8S

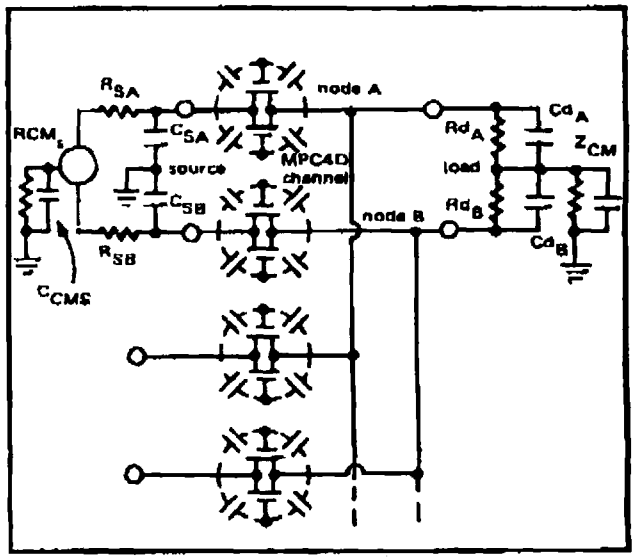


FIGURE 4: Settling & Common-Mode Effects – MPC4D.

The CMR of the MPC4D and Burr-Brown's INA110 Instrumentation Amplifier (G = 100) is 110dB at DC to 10Hz with a 6dB/octave rolloff to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown INA110 Instrumentation Amplifier connected for gains of 500, 100, and 10.

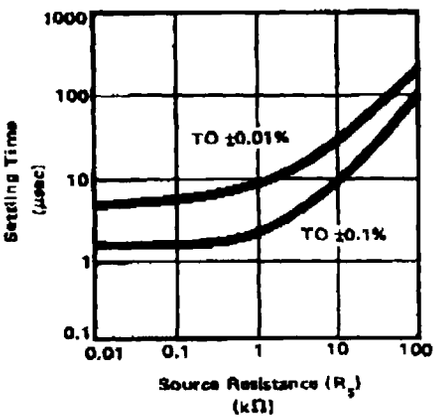
Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

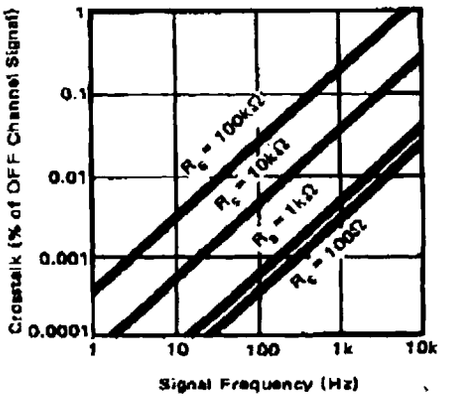
AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

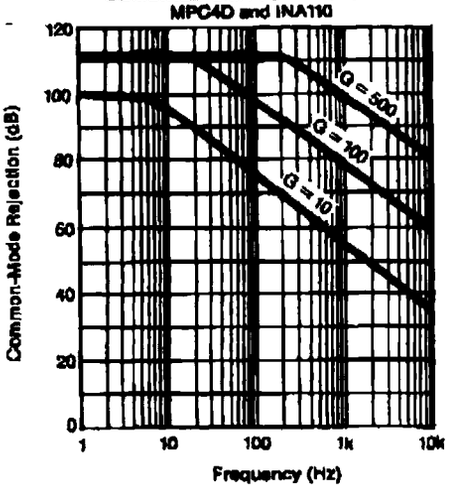
SETTLING TIME VS SOURCE RESISTANCE FOR 20V STEP CHANGE



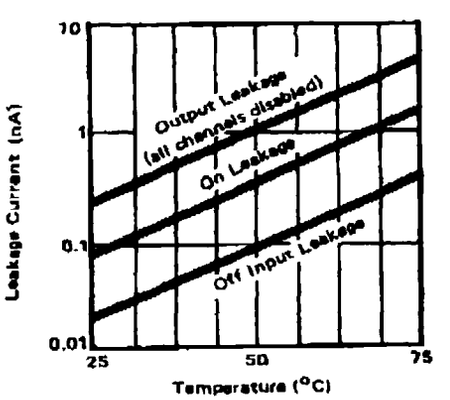
CROSSTALK VS SIGNAL FREQUENCY



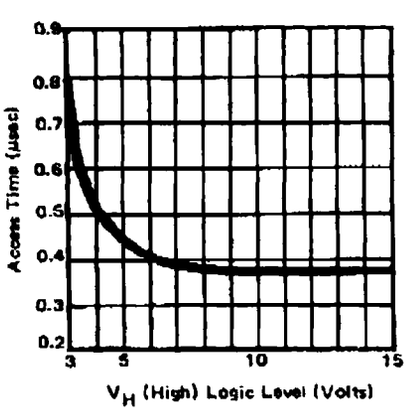
COMBINED CMR VS FREQUENCY MPC4D and INA110



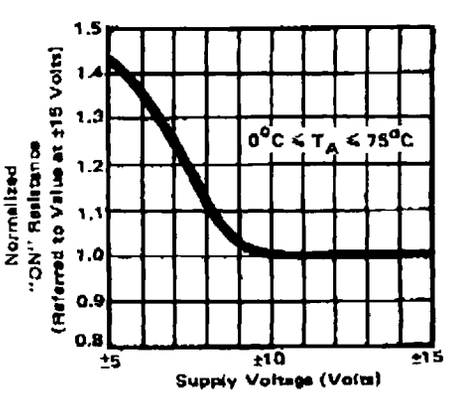
LEAKAGE CURRENT VS TEMPERATURE



ACCESS TIME VS LOGIC LEVEL (HIGH)



NORMALIZED "ON" RESISTANCE VS SUPPLY VOLTAGE



OPERATION & INSTALLATION INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 2-bit (MPC4D) or 3-bit (MPC8S) Channel Select Address (shown in the Truth Tables on Page 2). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15 volt and/or -15 volt supply voltage is absent or shorted to ground, the MPC4D and MPC8S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Footnote 1, Page 3).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended. See Typical Performance Curves (Access Time).

To preserve common-mode rejection of the MPC4D, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

SINGLE-ENDED MULTIPLEXER (MPC8S)

Up to 32 channels (4 multiplexers) can be connected to a single node, or up to 64 channels using 9 MPC8S multiplexers on a two-tiered structure as shown in Figures 5 and 6.

DIFFERENTIAL MULTIPLEXER (MPC4D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 x 1 or 16 channels using a 4 x 4 configuration.

SINGLE NODE EXPANSION

The 32 x 1 configuration is simply eight MPC4D units tied to a single node. Programming is accomplished with a 5 bit counter, using the 2 LSB's of the counter to control Channel Address inputs A_0 and A_1 and the 3 MSB's of the counter to drive a 1 of 8 decoder. The 1 of 8 decoder then is used to drive the ENABLE inputs (pin 2) of the MPC4D multiplexers.

TWO TIER EXPANSION

Using a 4 x 4 2-tier structure for expansion to 16 channels, the programming is simplified A 4-bit counter output does not require a 1 of 8 decoder. The 2 LSB's of the counter drive the A_0 and A_1 inputs of the four first tier multiplexers and the 2 MSB's of the counter are applied to the A_0 and A_1 inputs of the second tier multiplexer.

Single vs. Multi-Tiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single node configuration, data cannot be taken from any channel, where as only one channel group is failed (4 or 8) in the multi-tiered configuration.

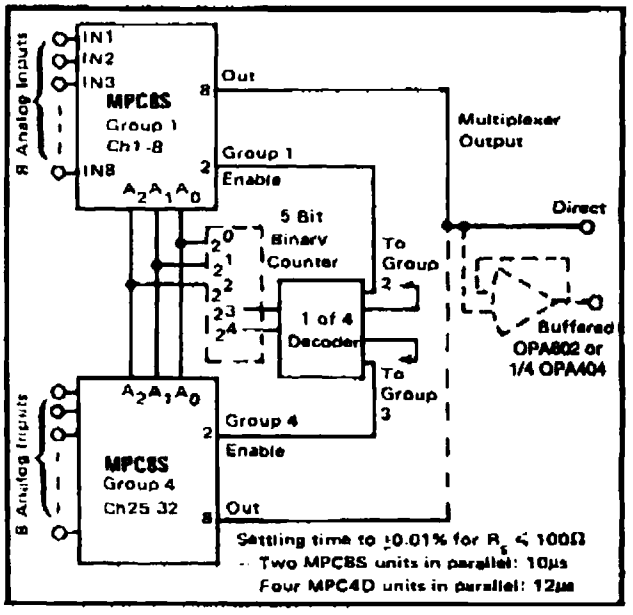


FIGURE 5. 32-Channel, Single-Tier Expansion.

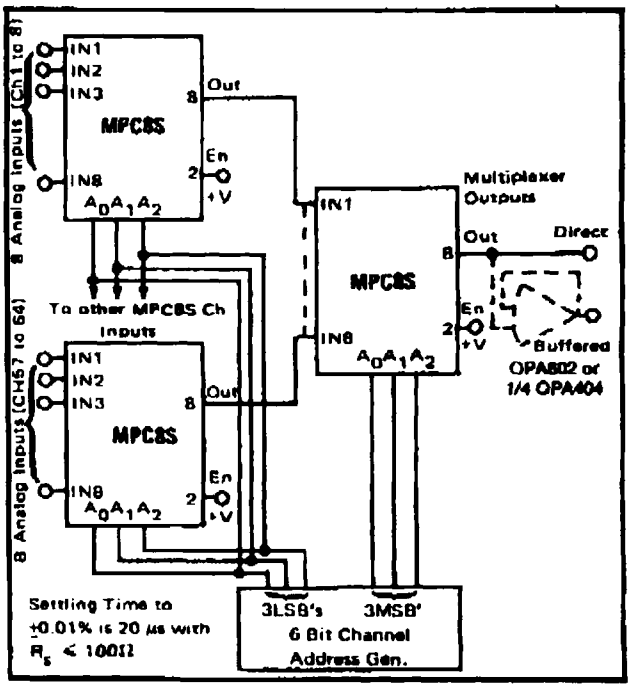


FIGURE 6. Channel Expansion Up to 64 Channels Using 8 × 8 Two-Tiered Expansion.