HEWLETT® PACKARD

Fiber Optic Data Links

Technical Data

DLT1040-STX Transmitter
DLR1040-STX Receiver

Features

- **FDDI PMD/ATM UNI or Fiber Channel FC-O Versions Available**
- **Single +5 V Power Supply**
- **Compact 16-pin DIP Package with Metal or Plastic ST® Connector Receptacle**
- **Pin Compatible with ODL125®, ODL156® or ODL200®**

Applications

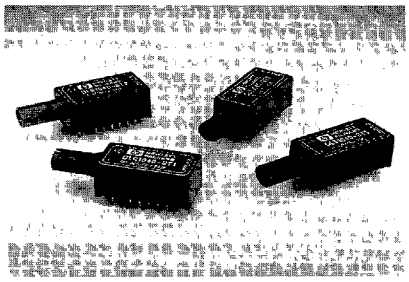
- **FDDI Concentrators, Bridges, Routers and Gateways**
- **ATM Switches, Hubs and NICs**
- **Fiber Channel Mainframes, Controllers, Switches and Peripherals**
- **Local Area Networks**
- **Point-to-Point Data Communications**

Description

The DLT/R1040-STX series data links are high performance cost efficient modules for serial optical data communications applications specified at 125 Mbd for FDDI PMD applications and 156 Mbd for ATM UNI applications or 266 Mbd for Fiber Channel FC-0 applications.

These modules are designed for 50 or 62.5 µm core multimode communications fiber and operate at a nominal wavelength of 1310 nm. They incorporate our high performance, reliable, long wavelength optical devices and proven circuit technology to give long life and consistent service.

The transmitter uses an advanced edge-emitting (ELED) source which provides exceptional performance on both 62.5 and 50 µm core fibers.



The receiver uses an MOVPE grown planar PIN Photodetector for low dark current and excellent responsivity.

Modules are available with either metal or plastic ST® connector receptacles.

A pseudo-ECL logic interface simplifies interface to FDDI physical layer chip sets.

General Description

The DLT/R1040-STX data link modules are designed to provide a simple interface between Pseudo-ECL (PECL)[1] logic and multi-mode optical fiber. The devices are pin compatible with AT&T's ODL125®, ODL156®, or ODL 200® line of data link components.

The modules are asynchronous having no internal clock recovery or regeneration. This allows operation in pulse-time modulated analog transmission systems (PFM & PPM) as well as in digital applications.

The PECL interface is used to simplify connection to a number of commercially available products such as Motorola's MC68836 FCG chip or AMD's TAXI® and SuperNet® chipsets. The module can be used over a range of signal rates, but are guaranteed to meet FDDI PMD, ATM UNI or Fiber Channel FC-0 specifications when used within the operating conditions specified in this document[2,3,4].

GND: Ground connections
These pins are to be connected to the system digital ground (usually 0 V).

V_{CC}: Positive power supply pins
These pins are to be connected to the nominal +5 V power supply.

DATA, $\overline{\text{DATA}}$: Serial data inputs
These pins are PECL differential inputs. When DATA is HIGH relative to /DATA, the optical source is turned on. For single-ended data sources, either input can be connected to V_{BB}.

V_{BB}: PECL input bias source
This pin provides a mid-swing reference voltage. It can be used to bias one transmitter input if a single-ended data source is to be used. V_{BB} is nominally 1.29 volts below V_{CC}.

GND: Ground connections
These pins are to be connected to the system digital ground (usually 0 V). The pins are not all internally connected to each other, but should be connected together on the system board.

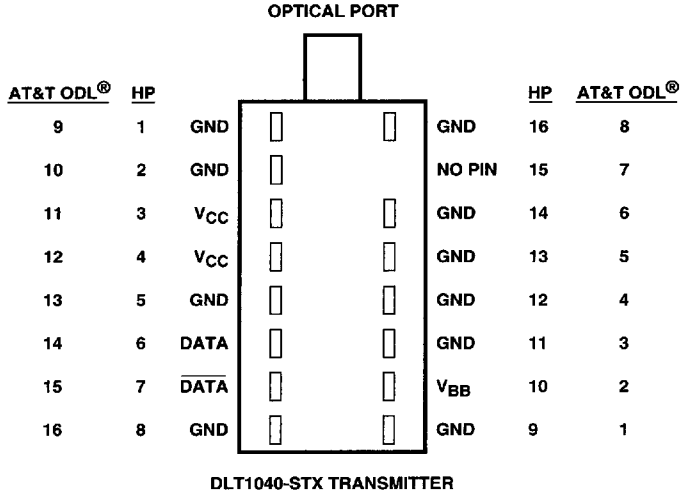
SD, $\overline{\text{SD}}$: Signal Detect Outputs
These pins are PECL outputs. SD is HIGH when sufficient optical power is present at the input port. This function is defined in PMD section 9.1.1.

V_{CC}: Positive power supply pins
These pins are to be connected to the nominal +5 V power supply.

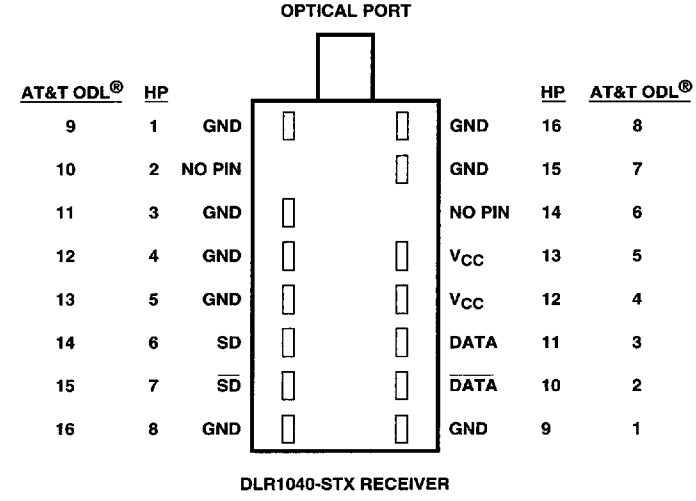
DATA, $\overline{\text{DATA}}$: Serial data outputs
These pins are PECL outputs. DATA is HIGH during an optical pulse at the receiver input.

Connection Diagrams - Top View

Important Note: HP pin numbering and AT&T ODL® pin numbering conventions differ. Both are shown below as a cross reference.



DLT1040-STX TRANSMITTER



DLR1040-STX RECEIVER

1. Pseudo-ECL Logic is ECL Logic operated from +5 V power supplies.
2. FDDI PMD is American National Standard x3. 166-1990.
3. ATM UNI is the ATM Forum Draft User Network Interface Standard, Revision 3.0.
4. Fiber Channel FC-0 is a draft American National Standard.

Functional Description: Transmitter

Design

The transmitter uses a highly reliable ELED as its optical source. The ELED has the advantage of a narrow numerical aperature. Thus it can couple almost as much light into a 50 µm core fiber as it can into 62.5 µm core fiber. The optical output is obtained by modulating the current in the ELED with a hybrid differential bipolar drive circuit. This circuit includes current pulse shaping and temperature compensation circuitry which optimizes the output pulse shape. Figure 1 shows a block diagram of the transmitter circuits.

The transmitter is DC coupled throughout and thus it can be used with any data pattern or data rate from DC to the specified maximum signal rate.

Thermal Performance

The output power of the transmitter varies with temperature with a temperature coefficient $< 1\%/°C$. This variation is caused by thermal changes in the conversion efficiency of the ELED. Internal temperature compensation of the ELED drive current tends to stabilize the output power, but design tradeoffs require that some residual fluctuation remains.

Single-Ended Operation

The transmitter provides a V_{BB} output which is familiar to users of ECL logic. V_{BB} is a reference voltage of 1.29 V below V_{CC} (nominally 3.71 V above ground). This voltage is half-way between a PECL HIGH and a PECL LOW. It can thus be used to bias one of the differential Data inputs if the signal source available is single-ended. It is important to note that PECL logic is referenced to the positive power supply (V_{CC}) and has no rejection of noise on that node. Thus if a single-ended, ground-referenced signal source is used, power supply noise coupled to V_{BB} may exceed the allowable ECL logic noise margin.

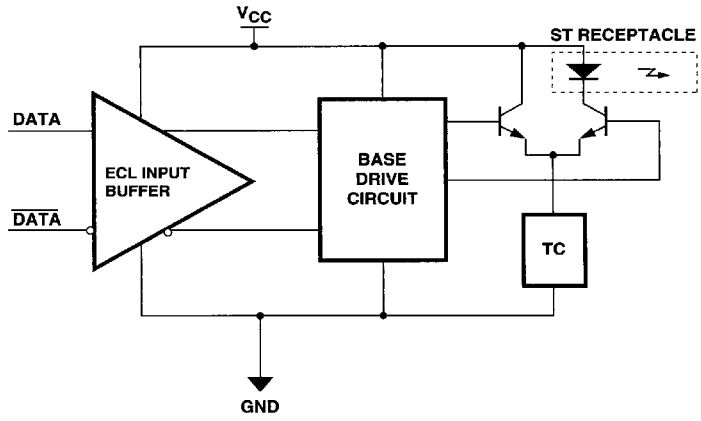


Figure 1. Simplified Transmitter Schematic.

Product Safety Notes

Optical Hazards - The transmitter optical output cannot present an eye hazard. Good safety practices suggest, however, that personnel should not look directly into an optical port during testing or servicing. This avoids hazards resulting from misidentifying a high power optical port.

Functional Description: Receiver

Design

The receivers contain InGaAs/InP photo detectors, silicon bipolar IC preamplifiers and hybrid postamp/decision circuits. The preamp and photodetector are mounted in a hybrid sub-assembly to minimize stray capacitance and to provide shielding. This technique yields a highly reliable, but also high performance, receiver module.

The postamplifier is AC- coupled to the preamplifier as illustrated in Figure 2. The coupling capacitor of the receiver is large enough to pass 4B5B FDDI coded data at 125 Mbd without significant distortion or performance penalty. If a lower signal rate, or a code which has significantly more low frequency content is used, sensitivity, jitter and pulse distortion can be degraded.

Figure 2 also shows a filter network which limits the bandwidth of the preamp output signal. The filter is designed to band limit the preamp output noise and thus improve the receiver sensitivity. These components will also reduce the sensitivity of the receiver as the signal bit rate is increased above the specified signal rate.

Noise Immunity

The receiver includes internal circuit components to filter power supply noise. Testing has shown excellent rejection of power supply noise in the frequency range of 0 to 100 kHz (the range where filter circuit elements become physically large). In addition, rejection of EMI has been tested from 10 kHz to 1 GHz at a field strength of 3 V/m with negligible performance degradation.

Under some conditions of EMI and power supply noise, power supply filtering may be necessary. If receiver sensitivity is found to be degraded by power supply noise, the filter network illustrated in Figure 3 may be used to improve performance. The values of the filter components are recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.

Terminating the Outputs

The PECL Data outputs of the receiver may be terminated with the standard Thevenin-equivalent 50 Ω to V_{CC} - 2 V terminations shown in Figure 4. Other standard ECL terminating techniques may be used. The two outputs of the receiver should be terminated with identical load circuits to avoid unnecessarily large AC current in V_{CC}. If the outputs are loaded identically, the AC current is largely nulled.

The SD outputs of the receiver are PECL logic and must be loaded if they are to be used. Either or both of the outputs may be used. The signal detect circuit is much slower than the data path, so the AC noise generated by an asymmetrical load is negligible. Power consumption may be reduced by using a higher than normal load impedance for the SD outputs. Transmission line effects are not generally a problem as the switching rate is slow.

The Signal Detect Circuit

The signal detect circuit works by sensing the peak level of the received signal and comparing this level to a reference. The signal detect switching levels comply with the FDDI PMD specification over the specified operating temperature and signal pattern.

Soldering

The transmitter and receiver modules are designed to be wave soldered onto a printed wiring board. It is, however, important to keep fluids and dirt out of the optical port during these and subsequent operations. HP supplies a process cap with each part to be used in aqueous or solvent based flux removal systems. Subsequently, the process caps may also serve as dust caps.

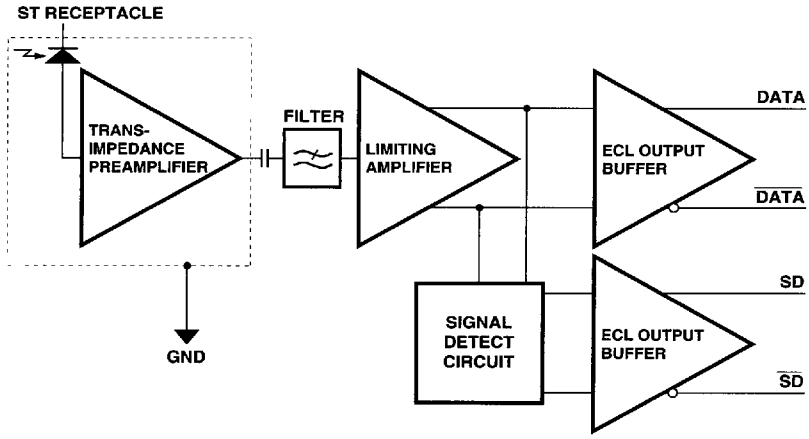


Figure 2. Receiver Block Diagram.

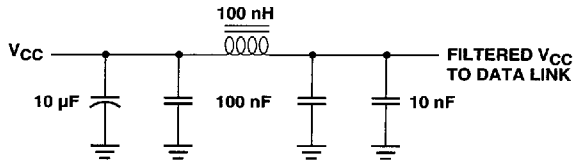
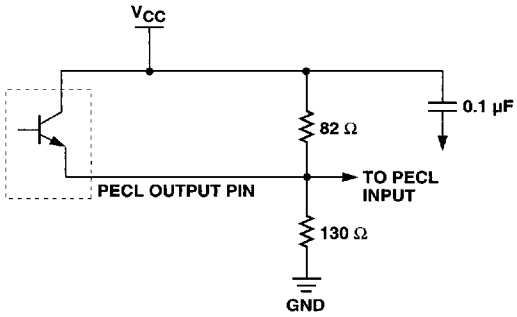
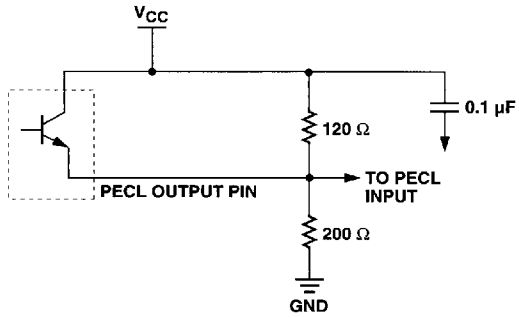


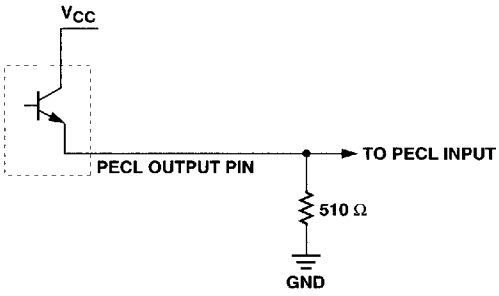
Figure 3. π Filter Network for Noise Filtering.



50 Ω Transmission Line Termination



75 Ω Transmission Line Termination

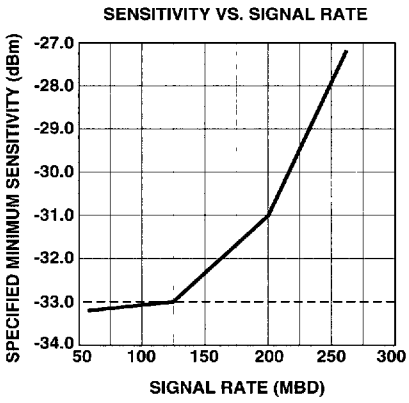


Simplified Termination for Signal Detect Outputs

Figure 4. PECL Output Terminations.

The figures above give recommended PECL output terminations. The simplified termination consumes about half the power of the other two techniques. Its impedance is too high to match a practical microstrip transmission line and thus it should only be used in situations where the line length is short relative to the signal propagation velocity. For standard FR-4 epoxy-glass board this length is about 5 cm.

DLR1040-ST/1 Performance over Range of Signal Rates



Specifications - Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Storage Temperature	T_S	-40	+85	°C
Lead Soldering Temperature/Time			240/10	°C/s
Relative Humidity	RH		non-condensing	% RH
V_{BB} Output Current		-1	+1	mA
Output Current (other outputs)	I_{OUT}	0	30	mA
Input Voltage		0	V_{CC}	V
Power Supply Voltage	V_{CC}	0	6	V

Operating Environment

Parameter	Symbol	Minimum	Maximum	Units
Power Supply Voltage	V_{CC}	+4.5	+5.5	V
Data Rate: DLT1040-ST/1		DC	156	Mbd
DLR1040-ST/1		1	156	Mbd
DLT1040-ST2		DC	266	Mbd
DLR1040-ST2		1	266	Mbd
Ambient Operating Temperature	T_{OP}	0	70	°C

Performance Specifications – Transmitter

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Center Wavelength	λc	1270	1300	1380	nm
Output Spectral Width (FWHM)	Δλ		80	120	nm
Operating Optical Output Power Range[1]	P_{OUT}	-19.0	-15.5	-14.0	dBm
Optical Rise and Fall Time[2]					
DLT1040-ST/1	Tr/Tf			3.5	ns
DLT1040-ST2				2.5	ns
Duty Cycle Distortion	DCD			0.6	ns
Extinguished Optical Power[3]	P_{OFF}	0		30	nW
Differential Input Voltage[4]	ΔVin	100		300	mV
Input Current (High)[5]	I_{IN}		50		μA
V_{BB} Output Voltage[6]			-1.3		V
Power Supply Current[7]	I_{CC}		125	160	mA
Extinction Ratio		0		10	%

Physical Properties

Lead Finish	Pb/Sn Solder Coat
Weight	10g nominal
Vibration (non op)	MIL-STD-883C, Method 2007A; 4 cycles per axis @ 20 G
Shock (non op)	MIL-STD-883C, Method 2002B; 500 G, 5 cycles per orientation
ESD	Class 2 per MIL-STD-883, Method 3015

Performance Specifications – Receiver

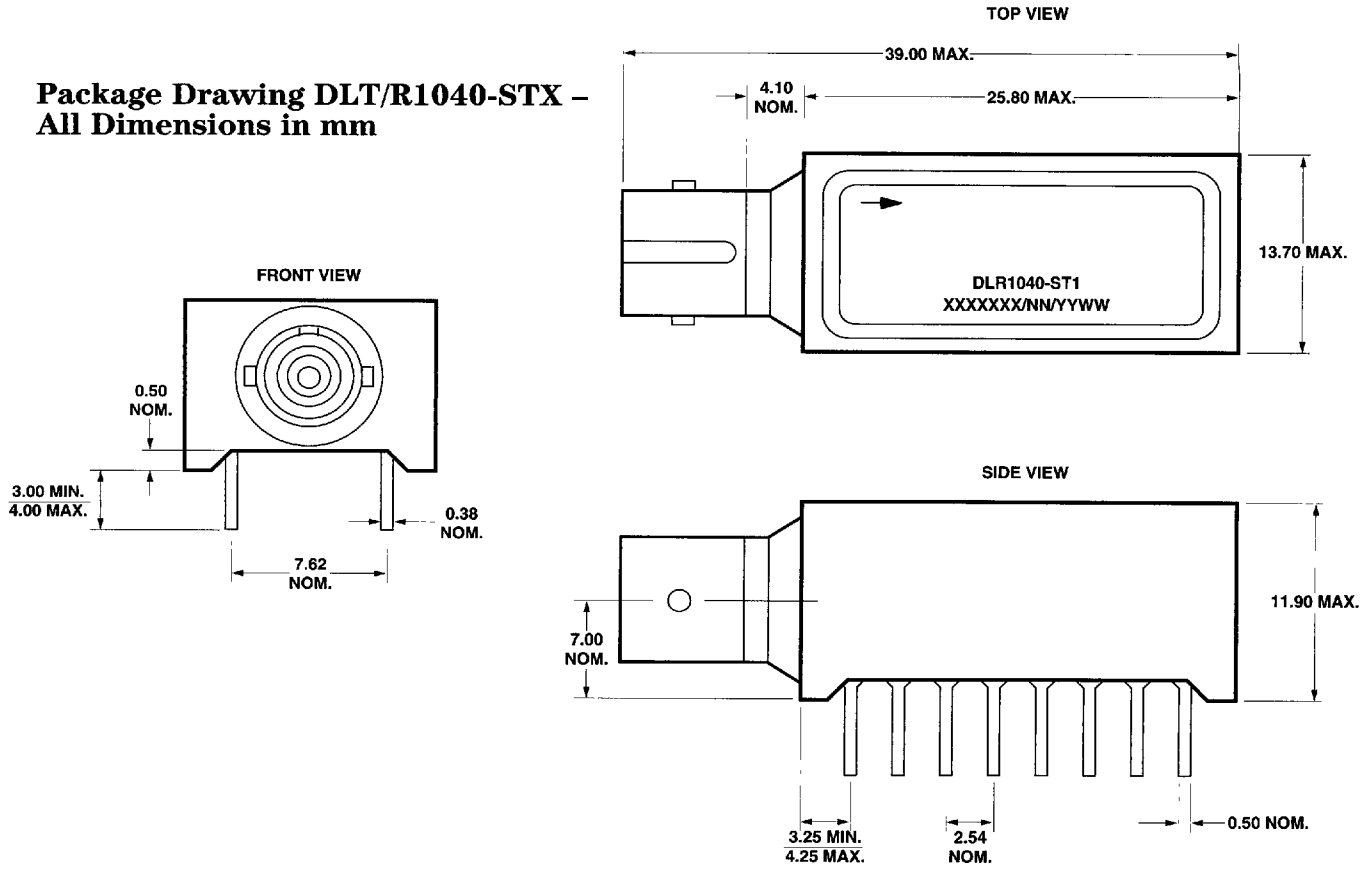
Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Center Wavelength	λ_C	1270	1300	1380	nm
Operating Optical Input Power Range[8,9]					
DLR1040-ST/1	P	-33.0		-14.0	dBm
DLR1040-ST2	P	-29.0		-14.0	dBm
Input Pulse Width	τ	5		1000	ns
Input Duty Cycle[10]		40	50	60	%
Pulse Width Distortion	PWD			0.7	ns_{p-p}
Power to Assert SD[11]					
DLR1040-ST/1	P_{SDA}			-31	dBm
DLR1040-ST2	P_{SDA}			-26	dBm
Error Rate for SD Deassert[12]	BER			0.01	Errors/Bit
SD Output Hysteresis		1.5			dB
SD Output Assertion Time	t_{SDA}			100	µs
SD Output Deassertion Time	t_{SDD}			350	µs
Output High Voltage[13]	V_{OH}	-1.0		-0.7	V
Output Low Voltage[13]	V_{OL}	-2.0		-1.6	V
Output Rise/Fall Time	t_R, t_F	0.5	1	1.5	ns
Power Supply Current[14]	I_{CC}	80	100	120	mA

Notes:

1. Output power temperature sensitivity is typically <1% per °C. Maximum and minimum values include this variation. Output power specified with 50% duty cycle data, 62.5 µm core, 0.275 NA fiber.
2. Optical rise and fall times are measured 10 to 90% on a 12.5 MHz square wave signal.
3. Extinguished optical power is measured with /$\overline{\text{DATA}}$ HIGH and DATA LOW.
4. Voltage difference at the inputs required to switch the optical output state.
5. HIGH input state is defined as the input pin having voltage at least 300 mV more positive than its complement.
6. Specified with no load current. Measured w.r.t. V_{CC}.
7. The power supply current varies with temperature. Maximum current is specified at V_{CC} = +5.5 V @ 70°C.
8. For the DLR1040-ST and DLR1040-ST1 sensitivity are measured with the 125 Mbd FDDI Appendix B test pattern. Both DATA and /$\overline{\text{DATA}}$ are PECL terminated. At 156 Mbd, with a balanced 2^{23}-1 PRBS input signal, the specified sensitivity for the DLR1040-ST and DLR1040-ST1 is -31.0 dBm.
9. For the DLR1040-ST2, the sensitivity is specified as -26.0 dBm under 266 Mbd Fiber Channel FC-0 test conditions.
10. Specifications assume a long-term 50% duty cycle.
11. This is the maximum power below which SD may be deasserted.
12. This is the maximum error rate at which SD may remain asserted.
13. These voltages are measured w.r.t. V_{CC}.
14. The current excludes the output load current.

HEWLETT® PACKARD

Package Drawing DLT/R1040-STX – All Dimensions in mm



Ordering Information

When ordering, please specify the part number as indicated below:

DL*1040 - ST X

- Option Suffix
  - blank = 125 Mbd FDDI; 156 Mbd ATM; metal receptacle
  - 1 = 125 Mbd FDDI; 156 Mbd ATM; plastic receptacle
  - 2 = 266 Mbd Fiber Channel; plastic receptacle
- Connector Suffix
  - ST = ST® Receptacle
- Model name
  - DLT1040 = Transmitter
  - DLR1040 = Receiver

Allowable part number table:

DLT1040-ST	DLT1040-ST2
DLR1040-ST	DLR1040-ST2
DLT1040-ST1	
DLR1040-ST1	

Handling Precautions

The DLT/R1040-STX can be damaged by current surges or overvoltage. Power supply transient precautions should be taken. Normal handling precautions for electrostatic sensitive devices should be taken.

For more information:

United States*

Europe*

Far East/Australasia: (65) 290-6305

Canada: (416) 206-4725

Japan: (81) 3 3331-6111

*Call your local HP sales office listed in your telephone directory. Ask for a Components representative.

Obsoletes 5962-0048E (8/94)

Printed in U.S.A. 5963-5342E (1/95)