

STRUCTURE : Silicon Monolithic Integrated Circuit  
 PRODUCT NAME : Synchronous rectification with built-in FET type DC/DC converter IC  
 MODEL NAME : **BD8645EFV**

- FEATURES :
- Synchronous rectification with built-in FET type DC/DC converter
  - Reference voltage accuracy FB 0.8V±1%
  - Switching frequency 250kHz~2.3MHz (Synchronizable with external clock.)
  - Over current protection circuit
  - Thermal shutdown
  - Output voltage watch (VDET) function
  - Input low voltage detection (UVLO) function
  - Soft start / Start delay circuit

◎ABSOLUTE MAXIMUM RATING (Ta=25°C)

| Parameter               | Symbol                         | Limits            | Unit |
|-------------------------|--------------------------------|-------------------|------|
| Input supply voltage    | V <sub>IN</sub>                | 7                 | V    |
| Input terminal voltage  | V <sub>INP</sub> <sup>*1</sup> | V <sub>IN</sub>   | V    |
| Output terminal voltage | V <sub>OUT</sub> <sup>*2</sup> | V <sub>IN</sub>   | V    |
| Output current          | I <sub>OUT</sub>               | 5                 | A    |
| Power dissipation       | Pd                             | 3.2 <sup>*3</sup> | W    |
| Operating temperature   | Topr                           | -40 ~ 85          | °C   |
| Storage temperature     | Tstg                           | -55 ~ 150         | °C   |

\*1 V<sub>INP</sub> Application terminal : SYNCLK, EN, SS/DELAY, FB

\*2 V<sub>OUT</sub> Application terminal : SW, VDET, FC, RT

\*3 (70mm×70mm, thickness 1.6mm, and four layer glass epoxy substrates)When mounting substrate and the package back exposure part are connected with solder.

Operating at higher than Ta=25°C, 25.6mW shall be reduced per 1

◎Operation condition

| Parameter            | Symbol           | MIN | TYP | MAX | Unit |
|----------------------|------------------|-----|-----|-----|------|
| Input supply voltage | V <sub>IN</sub>  | 4   | -   | 5.5 | V    |
| Output current       | I <sub>OUT</sub> | -   | -   | 4   | A    |

This product is not designed for protection against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

Be careful to handle because the content of the description of this material might correspond to the labor (technology in the design, manufacturing, and use) in foreign country exchange and Foreign Trade Control Law.

◎Electrical characteristic

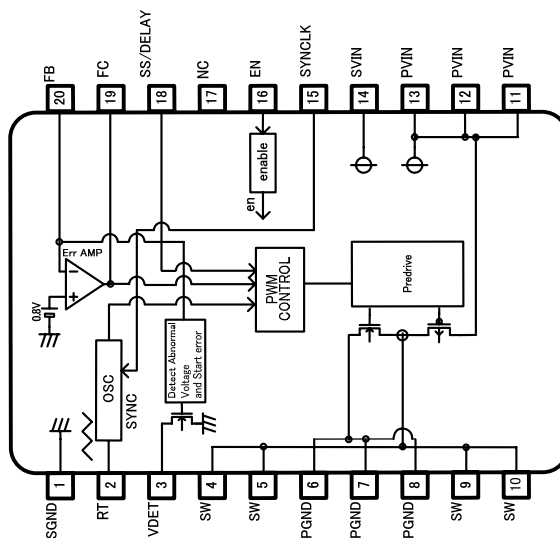
(Unless otherwise noted Ta=25°C, V<sub>IN</sub>=5.0V)

| Parameter                         | Symbol                | Specification value |      |       | UNIT | Condition                                     |
|-----------------------------------|-----------------------|---------------------|------|-------|------|---|
|                                   |                       | MIN                 | TYP  | MAX   |      |   |
| VIN supply current (operating)    | I <sub>Q active</sub> | -                   | 500  | 700   | μA   | V <sub>FB</sub> = 0.83V, V <sub>FC</sub> = 1V |
| VIN supply current (standby)      | I <sub>Q stby</sub>   | -                   | 0    | 10    | μA   | V <sub>EN</sub> = 0V                          |
| Reference voltage (VREF)          | V <sub>REF</sub>      | 0.792               | 0.8  | 0.808 | V    |   |
| Output rise detection voltage     | V <sub>OVP</sub>      | 30                  | 60   | 90    | mV   | Monitoring FB terminal                        |
| Output decrease detection voltage | V <sub>LVP</sub>      | -90                 | -60  | -30   | mV   | Monitoring FB terminal                        |
| Terminal VDET output current      | I <sub>VDET</sub>     | 0.4                 | -    | -     | mA   | V <sub>VDET</sub> < 0.3V                      |
| Oscillation frequency             | f <sub>OSC</sub>      | 2.0                 | 2.3  | 2.6   | MHz  | R <sub>RT</sub> = 43kΩ                        |
| Pch FET ON resistance             | R <sub>PFET</sub>     | -                   | 70   | 105   | mΩ   | I <sub>SW</sub> = 1A                          |
| Nch FET ON resistance             | R <sub>NFET</sub>     | -                   | 50   | 85    | mΩ   | I <sub>SW</sub> = -1A                         |
| UVLO voltage                      | V <sub>UVLO</sub>     | 2.35                | 2.50 | 2.65  | V    |   |
| SW leak current                   | I <sub>LSW</sub>      | -                   | 0    | 10    | μA   | V <sub>EN</sub> = 0V, V <sub>IN</sub> = 5.5V  |
| EN terminal H threshold voltage   | V <sub>ENH</sub>      | 1.1                 | -    | -     | V    |   |
| EN terminal L threshold voltage   | V <sub>ENL</sub>      | -                   | -    | 0.4   | V    |   |
| FC sink current                   | I <sub>FCSI</sub>     | 5                   | 10   | -     | μA   |   |
| FC source current                 | I <sub>FCSO</sub>     | -                   | -10  | -5    | μA   |   |
| SS/DELAY terminal source current  | I <sub>SSSO</sub>     | 2                   | 4    | 6     | μA   |   |

●V<sub>FB</sub>:FB terminal voltage、V<sub>EN</sub>:EN terminal voltage、V<sub>FC</sub>:FC terminal voltage、V<sub>VDET</sub>: VDET < 0.3V

●Current capability should not exceed Pd.

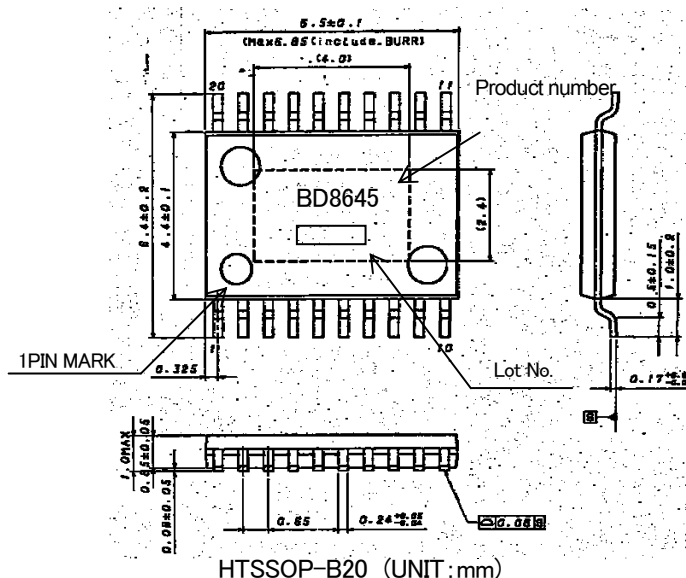
◎BLOCK DIAGRAM



◎PIN ASSIGNMENT

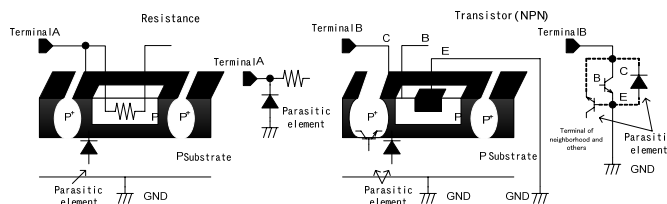
| No. | Symbol | Description   | No. | Symbol   | Description  |
|-----|--------|---|-----|----------|--|
| 1   | SGND   | Signal GND terminal                                 | 11  | PVIN     | Power supply input terminal                        |
| 2   | RT     | Frequency adjustment resistance connection terminal | 12  | PVIN     | Power supply input terminal                        |
| 3   | VDET   | Output abnormality detection terminal               | 13  | PVIN     | Power supply input terminal                        |
| 4   | SW     | Switching output terminal                           | 14  | SVIN     | Signal system power supply input terminal          |
| 5   | SW     | Switching output terminal                           | 15  | SYNCLK   | Input terminal for external clock synchronization  |
| 6   | PGND   | Power GND terminal                                  | 16  | EN       | Enable input terminal                              |
| 7   | PGND   | Power GND terminal                                  | 17  | NC       | -  |
| 8   | PGND   | Power GND terminal                                  | 18  | SS/DELAY | Soft start adjustment capacity connection terminal |
| 9   | SW     | Switching output terminal                           | 19  | FC       | Phase amends terminal                              |
| 10  | SW     | Switching output terminal                           | 20  | FB       | Feedback terminal                                  |

◎PACKAGE OUTLINE



## ◎NOTE ON USE

1. About the absolute maximum rating  
Attention is brushed off enough to the quality control, it is likely to destroy when the absolute maximum rating such as impressed voltages (VCC\_IN,DCIN) and ranges (Topr) of the operating temperature as it is exceeded, the mode of breakings of the short or the opening, etc. cannot be specified, and examine it in this IC to give physical measures for safety such as fuses when a special mode that exceeds the absolute maximum rating is assumed.
2. About the reverse-connection of the power supply connector  
IC might destroy it by reversely connecting the power supply connector. Give measures such as putting the diode between power supply terminals of power supply and IC outside for the reverse-touching destruction protection.
3. Power supply line  
Please do measures such as putting the bypass capacitor in power supply-GND nearest pin of this IC as the route of the resurrection current to cause the return of the current in which it resurrected it by the counter electromotive force of the coil.  
Please confirm the characteristic of the electrolytic capacitor enough as the capacity omission etc. at the low temperature never happen, and decide it.
4. About grand potential  
Any state of operation must become the lowest potential about the potential of the terminal GND. Moreover, confirm whether there is terminal that is actually the voltage of GND or less including transients.
5. About the heat design  
Think about permissible loss (Pd) in an actual state of use, and do the heat design with the margin enough.
6. About the short and the miss-installation between terminals  
Note the direction and the miss-registration of IC enough when you install it in the set substrate. IC might destroy it as well as reversely connecting the power supply connector when installing it by mistake. Moreover, there is fear of destruction when the foreign body enters between terminals, the terminal, the power supply, and grandeur and it is short-circuited.
7. About operation in strong electromagnetic field  
In use in strong electromagnetic field, note that there is a possibility of malfunctioning.
8. About the capacitor during output-GND  
The current charged the capacitor with when VCC is 0V or is GND and is short-circuited when a big capacitor is connected between GND output by some factors flows into the output and it is likely to destroy it. Give the capacitor between GND output to 0.1μF or less.
9. About the inspection by the set substrate  
It is likely to suffer stress to IC and discharge electricity every one process when you connect the capacitor with the pin with low impedance when inspecting it in the set substrate. Moreover, detach it after connecting after the power supply is turned off without fail when detaching it to G in the inspection process, inspecting, and turning off the power supply. n addition, be give the earth to the assembly process as a static electricity measures, and careful enough when it transports and you preserve it.
10. About each input terminal  
This IC is a monolithic IC which has a P<sup>+</sup> isolations and P substrate to isolate elements each other.  
This P layer and an N layer in each element form a PN junction to construct various parasitic elements.  
For instance, the potential difference operates in resistance as shown in the figure below when resistance and the transistor connect it with the terminal and the playground (GND) >(terminal B) joint of PN operates as a parasitic diode in playground (GND) >(terminal A) transistor (NPN). In addition, the NPN transistor of parasitism works with N layer of the element of the above-mentioned parasitic diode and the neighborhood and others in transistor (NPN). A parasitic element in IC composition is inevitably formed because of the potential relation.  
A parasitic element can operate, the interference with the circuit operation be caused, it malfunction, and, consequently, it cause destruction. Therefore, do not do the usage that a parasitic element operates as a voltage that is lower than the playground (GND;P substrate) is impressed to the input terminal enough. Moreover, do not impress the voltage to the input terminal when you do not impress the power-supply voltage to IC. Give each input terminal to me the voltage below the power-supply voltage or in the guarantee value of an electric characteristic when you similarly impress the power-supply voltage.



Example of IC of simple structure

11. Earth wiring pattern  
If small signal GND and large current GND exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GND, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.
12. Thermal Shut-Down  
When a thermal shutdown operates, the DC/DC converter controller of all Ch is turned off. When a thermal shutdown is released, the DC/DC converter controller of all Ch becomes an operation beginning from turning off.

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