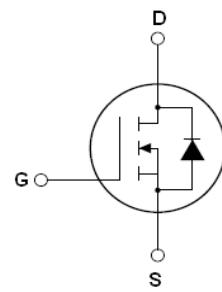


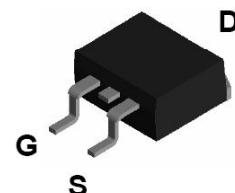
Features:

- Advanced trench process technology
- avalanche energy, 100% test
- Fully characterized avalanche voltage and current

ID =60A
BV=100V
R_{dson}=16mΩ (Max.)


Description:

The SSF1016D is a new generation of high voltage and low current N-Channel enhancement mode trench power MOSFET. This new technology increases the device reliability and electrical parameter repeatability. SSF1016D is assembled in high reliability and qualified assembly house.


Application:

- Power switching application

SSF1016D TOP View (DPAK)
Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @T _c =25°C	Continuous drain current,V _{GS} @10V	60	A
I _D @T _c =100°C	Continuous drain current,V _{GS} @10V	50	
I _{DM}	Pulsed drain current ①	240	
P _D @T _C =25°C	Power dissipation	144	W
	Linear derating factor	1.5	W/°C
V _{GS}	Gate-to-Source voltage	±20	V
E _{AS}	Single pulse avalanche energy ②	380	mJ
dv/dt	Peak diode recovery voltage	31	v/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-case	—	0.52	—	C/W
R _{θJA}	Junction-to-ambient	—	—	62	

Electrical Characteristics @T_J=25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source breakdown voltage	100	—	—	V	V _{GS} =0V,I _D =250μA
R _{DS(on)}	Static Drain-to-Source on-resistance	—	11	16	mΩ	V _{GS} =10V,I _D =30A
V _{GS(th)}	Gate threshold voltage	2.0	—	4.0	V	V _{DS} =V _{GS} ,I _D =250μA
I _{DSS}	Drain-to-Source leakage current	—	—	2	μA	V _{DS} =100V,V _{GS} =0V
		—	—	10		V _{DS} =100V, V _{GS} =0V,T _J =150°C
I _{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source reverse leakage	—	—	-100		V _{GS} =-20V
Q _g	Total gate charge	—	90		nC	

Q_{gs}	Gate-to-Source charge	—	20	—	nS	$I_D=30A, V_{GS}=10V$ $V_{DD}=30V$
Q_{gd}	Gate-to-Drain("Miller") charge	—	31	—		
$t_{d(on)}$	Turn-on delay time	—	18.2	—		$V_{DD}=30V$
t_r	Rise time	—	15.6	—		$I_D=2A, R_L=15\Omega$
$t_{d(off)}$	Turn-Off delay time	—	70.5	—	pF	$R_G=2.5\Omega$
t_f	Fall time	—	13.8	—		$V_{GS}=10V$
C_{iss}	Input capacitance	—	3150	—		$V_{GS}=0V$
C_{oss}	Output capacitance	—	350	—	pF	$V_{DS}=25V$
C_{rss}	Reverse transfer capacitance	—	240	—		$f=1.0MHz$

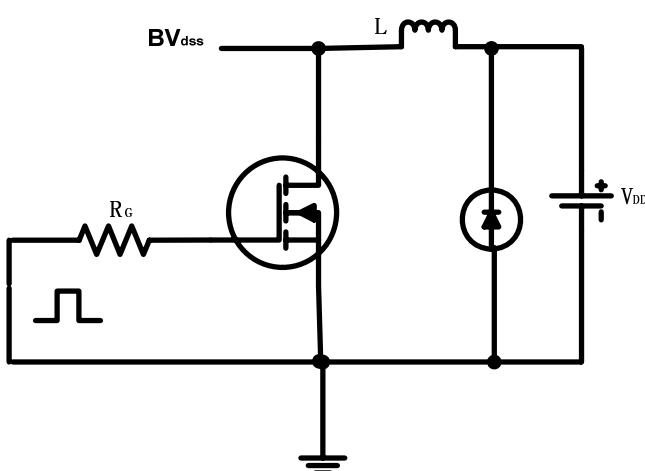
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	300		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J=25^\circ C, I_S=60A, V_{GS}=0V$ ③
t_{rr}	Reverse Recovery Time	—	57	—	nS	$T_J=25^\circ C, I_F=75A$ $dI/dt=100A/\mu s$ ③
Q_{rr}	Reverse Recovery Charge	—	107	—	μC	
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_s + LD$)				

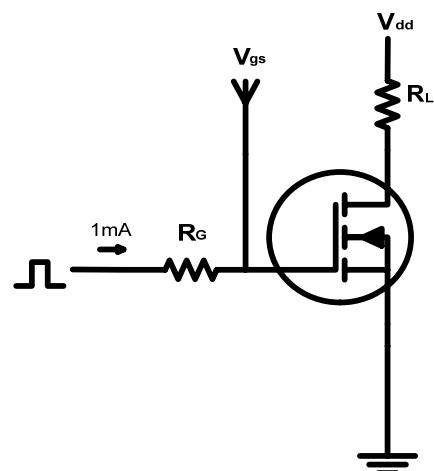
Notes:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Test condition: $L = 0.3mH$, $V_{DD} = 50V$, $I_D = 37A$
- ③ Pulse width $\leq 300\mu s$, duty cycle $\leq 1.5\%$; $R_G = 25\Omega$ Starting $T_J = 25^\circ C$

EAS Test Circuit:

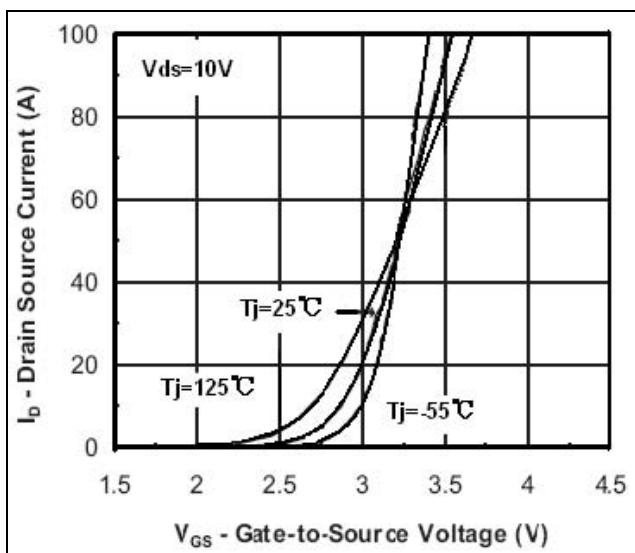
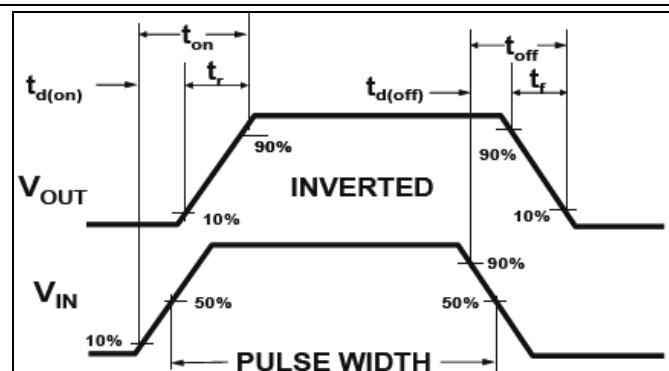
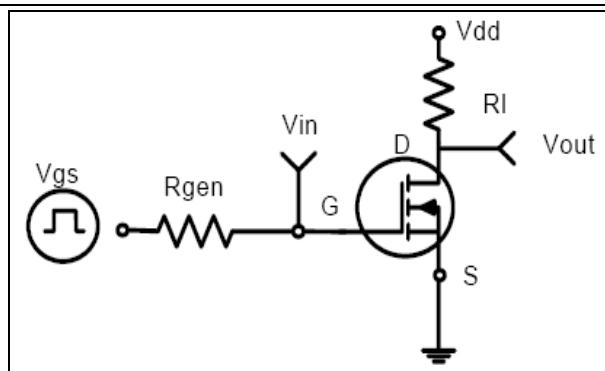
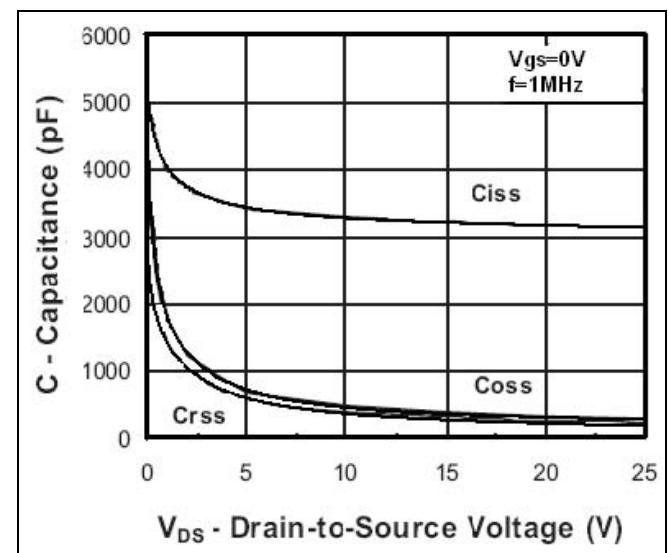
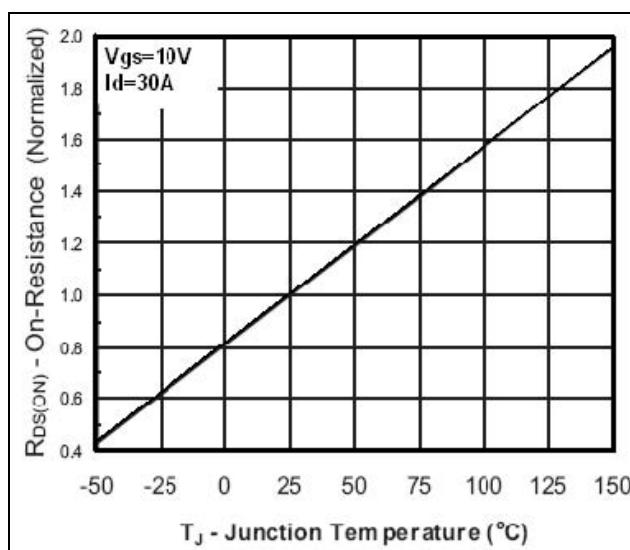
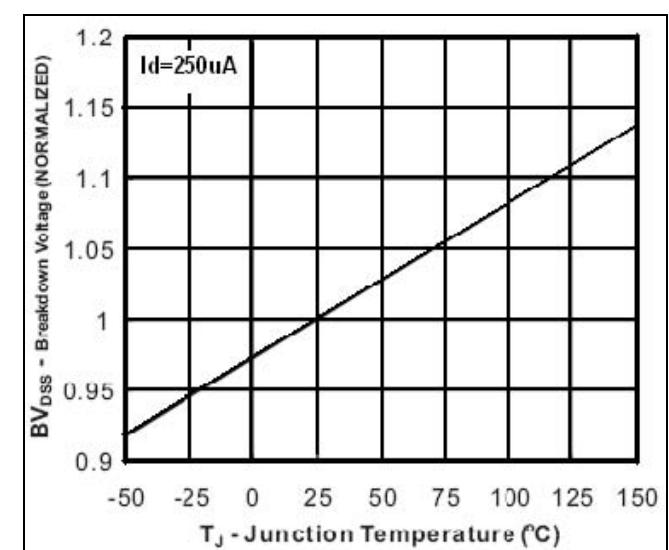


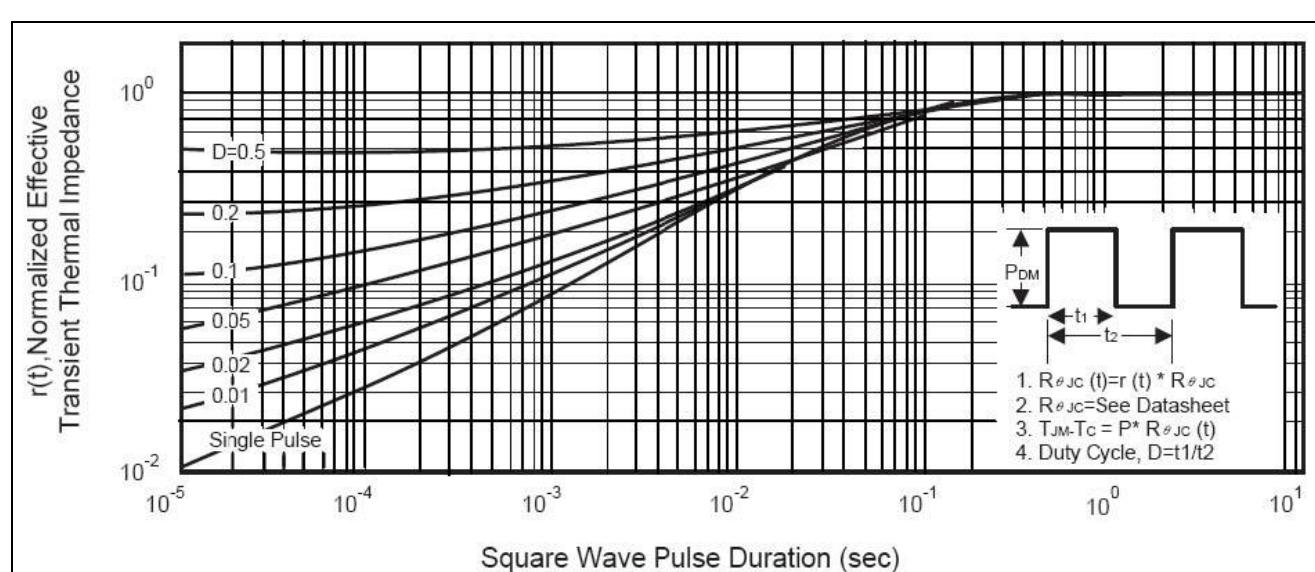
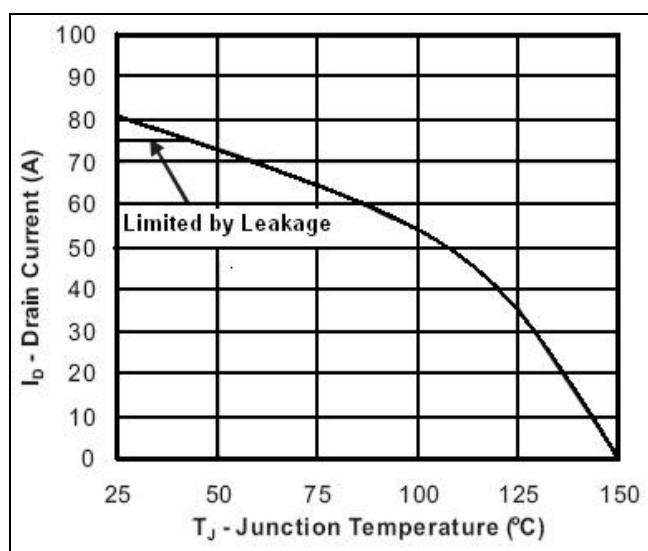
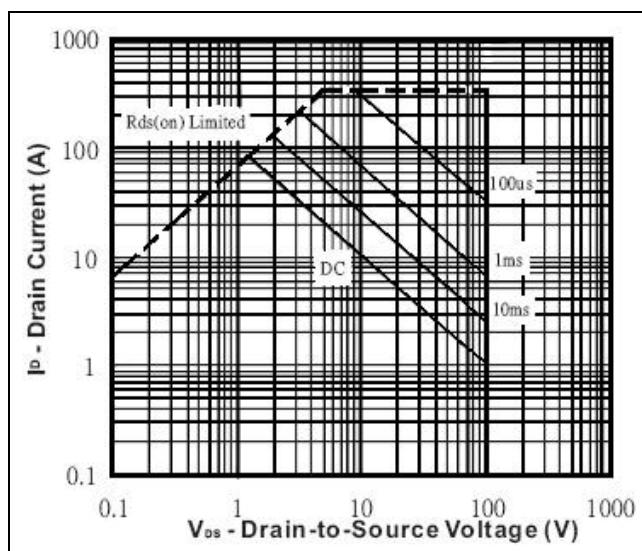
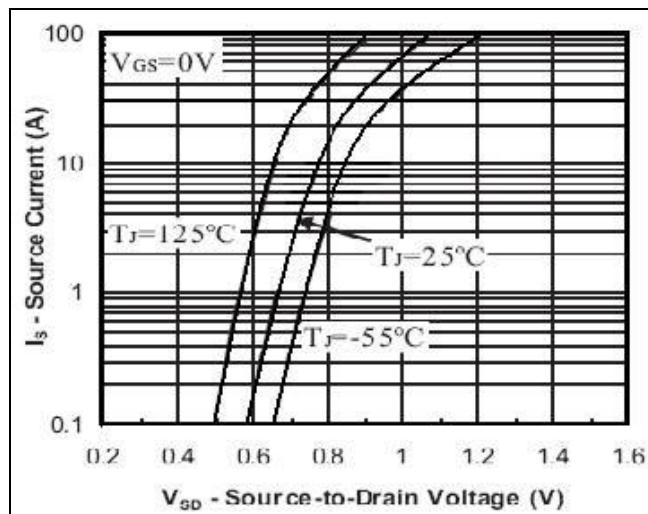
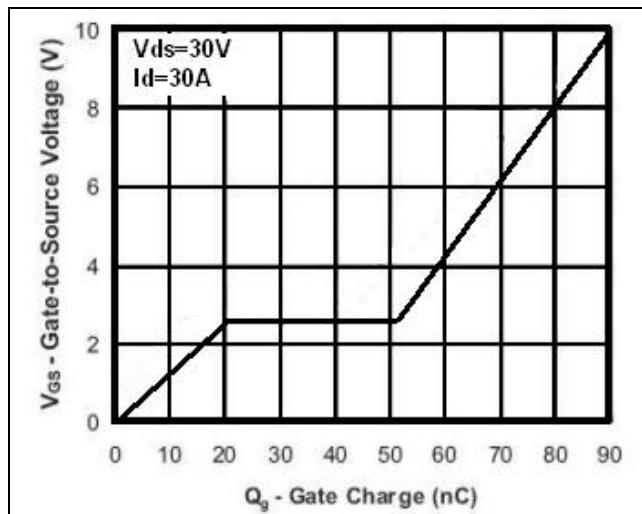
Gate Charge Test Circuit:

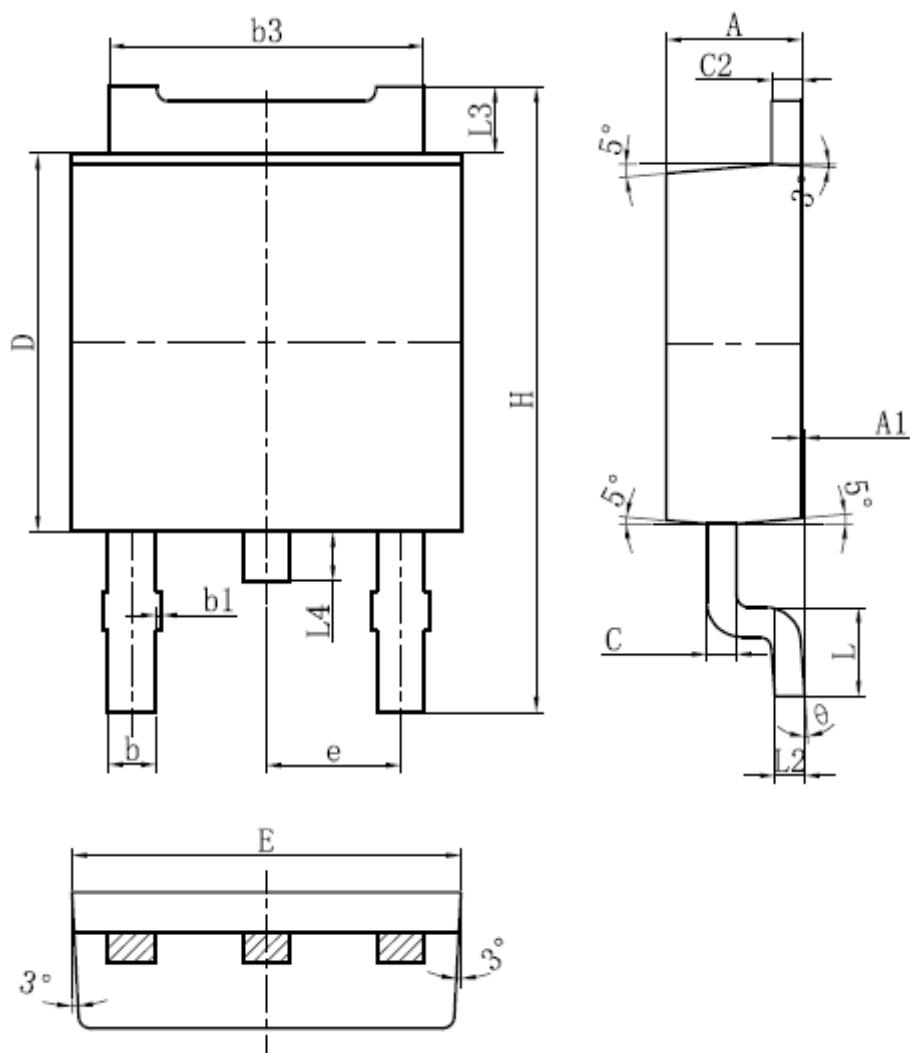


Switch Time Test Circuit:

Switch Waveform:


Transfer Characteristic

Capacitance

On Resistance vs. Junction Temperature

Breakdown Voltage vs. Junction Temperature



DPAK MECHANICAL DATA:


Symbol	MIn.	Normal	Max.
E	6.55	6.6	6.65
L	1.40	1.5	1.60
L2	-	0.51BSC	-
L3	0.93	1.08	1.23
L4	0.7	0.8	0.9
D	6.05	6.1	6.15
H	9.9	10.1	10.3
b	0.763	0.813	0.863
b1	0	-	0.1
b3	5.28	5.33	5.38
e	2.23	2.28	2.33
A	2.25	2.3	2.35
A1	0	0.05	0.10
C	0.498	0.508	0.518
C2	0.498	0.508	0.518
θ	0	-	8°

NOTE:

1. Package body size exclude flash and gate burrs.
2. Dimension L Is measured In gage plane.
3. Tolerance 0.10mm unless otherwise specified.
4. Controlling dimension is millimeter. Converted inch dimension are not necessarily exact.