

General Description

The MAX14591 evaluation kit (EV kit) is a fully assembled and tested circuit board that demonstrates the functionality of the MAX14591 high-speed, open-drain capable logic-level translator in both the 8-bump WLP and 8-pin TDFN packages. The EV kit enables direct evaluation of the device by multiple jumper-selectable methods. The highly configurable PCB allows the user to evaluate each package separately or both at once. Input power to the EV kit is provided by a micro-USB, type-B connector or an external 5V power supply. On-board LDO regulators provide the appropriate voltage for each component, and potentiometers allow the user to adjust the power supply for either side of the level translator independently.

Features and Benefits

- Proven PCB Layout
 - Decrease Evaluation Time
- Fully Assembled and Tested
- On-Board Adjustable Oscillators
 - Evaluate Without External Function Generator
- Jumper-Selectable Open-Drain and Push-Pull Buffers Enable Simple Evaluation

Ordering Information appears at end of data sheet.

Quick Start

Required Equipment

- MAX14591 EV kit
- Digital voltmeter (DVM)
- USB power source or another 5V external power supply
- Oscilloscope and at least one scope probe

Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation and begin evaluation:

- 1) If using a USB bus to power the board, connect the included micro-USB cable between the micro-USB, type-B connector (J1) and the USB power source, such as a computer or dedicated USB charging port, and install a shunt on jumper JU4 shorting pins 1-2.
- 2) If using an external power source to power the board, connect the external power supply at the VBUS test point (TP26) and install a shunt on jumper JU4 shorting pins 2-3.
- 3) Connect the DVM between GND (TP6) and V_{CC} (TP24). Adjust the first potentiometer (POT1) until the desired voltage for V_{CC} appears on the DVM by turning the screw on the potentiometer to the right or to the left.
- 4) Connect the DVM between GND (TP6) and V_L (TP25). Adjust the second potentiometer (POT2) until the desired voltage for V_L appears on the DVM by turning the screw on the potentiometer to the right or to the left. Note that V_L should be lower than V_{CC} .
- 5) Connect the jumpers in the desired configuration, based on the descriptions in Table 1.
- 6) After implementing the desired configuration, connect the oscilloscope probe to the output evaluated to observe the translated voltage of the input signal.

Table 1. Jumper Configuration (JP1–JP7, JP9–JP15, JP17–JP25)

JUMPER	SHUNT POSITION	DESCRIPTION
JP1	1-2	Pullup resistor connect for I/OVL2 of U2. Connects a 1kΩ pullup resistor between V _L and I/OVL2.
	Not installed	Pullup resistor disconnect for I/OVL2 of U2. Disconnects the 1kΩ pullup resistor between V _L and I/OVL2.
JP2	1-2	Connects open-drain buffer to driving signal bus for channel I/OVL1. The open-drain buffer is driven by the output of DS1090-16 (U4). The frequency of the signal is adjustable using POT3.
	1-3	Connects external source connected at TP9 to driving signal bus for channel I/OVL1.
	1-4	Connects push-pull buffer to driving signal bus for channel I/OVL1. The push-pull buffer is driven by the output of DS1090-1 (U5). The frequency of the signal is adjustable using POT4.
JP3	1-2	Pullup resistor connect for I/OVCC2 of U2. Connects a 1kΩ pullup resistor between V _{CC} and I/OVCC2.
	Not installed	Pullup resistor disconnect for I/OVCC2 of U2. Disconnects the 1kΩ pullup resistor between V _{CC} and I/OVCC2.
JP4	1-2	Power to the board supplied at the micro-USB connector (J1).
	2-3	Power to the board supplied at the external VBUS test point (TP26).
JP5	1-2	Connects the open-drain buffer to driving signal bus for channel I/OVL2. The open-drain buffer is driven by the output of DS1090-16 (U4). The frequency of the signal is adjustable using POT3.
	1-3	Connects external source connected at TP13 to driving signal bus for channel I/OVL2.
	1-4	Connects push-pull buffer to driving signal bus for channel I/OVL2. The push-pull buffer is driven by the output of DS1090-1 (U5). The frequency of the signal is adjustable using POT4.
JP6	1-2	Connects the \overline{TS} pin of U1 to V _L , placing the device's I/O pins in normal operating mode.
	2-3	Connects the \overline{TS} pin of U1 to GND, placing the device's I/O pins in high-impedance, three-state mode.
JP7	1-2	Pullup resistor connect for I/OVCC1 of U1. Connects a 1kΩ pullup resistor between V _{CC} and I/OVCC1.
	Not installed	Pullup resistor disconnect for I/OVCC1 of U1. Disconnects the 1kΩ pullup resistor between V _{CC} and I/OVCC1.
JP9*	1-2	Connects I/OVCC1 of U1 to the driving signal bus for channel I/OVCC1.
	Not installed	Disconnects I/OVCC1 of U1 from the driving signal bus for channel I/OVCC1.
JP10*	1-2	Connects I/OVCC1 of U2 to the driving signal bus for channel I/OVCC1.
	Not installed	Disconnects I/OVCC1 of U2 from the driving signal bus for channel I/OVCC1.
JP11	1-2	Pullup resistor connect for I/OVL1 U1. Connects a 1kΩ pullup resistor between V _L and I/OVL1.
	Not installed	Pullup resistor disconnect for I/OVL1 of U1. Disconnects the 1kΩ pullup resistor between V _L and I/OVL1.
JP12	1-2	Connects open-drain buffer to driving signal bus for channel I/OVCC1. The open-drain buffer is driven by the output of DS1090-16 (U4). The frequency of the signal is adjustable using POT3.
	1-3	Connects external source connected at TP16 to driving signal bus for channel I/OVCC1.
	1-4	Connects push-pull buffer to driving signal bus for channel I/OVCC1. The push-pull buffer is driven by the output of DS1090-1 (U5). The frequency of the signal is adjustable using POT4.

Table 1. Jumper Configuration (JP1–JP7, JP9–JP15, JP17–JP25) (continued)

JUMPER	SHUNT POSITION	DESCRIPTION
JP13	1-2	Pullup resistor connect for I/OVL2 of MAX14591EWA+ (U1). Connects a 1kΩ pullup resistor between V _L and I/OVL2.
	Not installed	Pullup resistor disconnect for I/OVL2 of MAX14591EWA+ (U1). Disconnects the 1kΩ pullup resistor between V _L and I/OVL2.
JP14	1-2	Pullup resistor connect for I/OVCC2 of MAX14591EWA+ (U1). Connects a 1kΩ pullup resistor between V _{CC} and I/OVCC2.
	Not installed	Pullup resistor disconnect for I/OVCC2 of MAX14591EWA+ (U1). Disconnects the 1kΩ pullup resistor between V _{CC} and I/OVCC2.
JP15*	1-2	Connects I/OVCC2 of U1 to the driving signal bus for channel I/OVCC2.
	Not installed	Disconnects I/OVCC2 of U1 from the driving signal bus for channel I/OVCC2.
JP17	1-2	Connects open-drain buffer to driving signal bus for channel I/OVCC2. The open-drain buffer is driven by the output of DS1090-16 (U4). The frequency of the signal is adjustable using POT3.
	1-3	Connects external source connected at TP17 to driving signal bus for channel I/OVCC2.
	1-4	Connects push-pull buffer to driving signal bus for channel I/OVCC2. The push-pull buffer is driven by the output of DS1090-1 (U5). The frequency of the signal is adjustable using POT4.
JP18	1-2	Pullup resistor connect for I/OVL1 of U2. Connects a 1kΩ pullup resistor between V _L and I/OVL1.
	Not installed	Pullup resistor disconnect for I/OVL1 of U2. Disconnects the 1kΩ pullup resistor between V _L and I/OVL1.
JP19	1-2	Pullup resistor connect for I/OVCC1 of U2. Connects a 1kΩ pullup resistor between V _{CC} and I/OVCC1.
	Not installed	Pullup resistor disconnect for I/OVCC1 of U2. Disconnects the 1kΩ pullup resistor between V _{CC} and I/OVCC1.
JP20*	1-2	Connects I/OVCC2 of U2 to the driving signal bus for channel I/OVCC2.
	Not installed	Disconnects I/OVCC2 of U2 from the driving signal bus for channel I/OVCC2.
JP21*	1-2	Connects I/OVL2 of U1 to the driving signal bus for channel I/OVL2.
	Not installed	Disconnects I/OVL2 of U1 from the driving signal bus for channel I/OVL2.
JP22*	1-2	Connects I/OVL2 of U2 to the driving signal bus for channel I/OVL2.
	Not installed	Disconnects I/OVL2 of U2 from the driving signal bus for channel I/OVL2.
JP23*	1-2	Connects I/OVL1 of U1 to the driving signal bus for channel I/OVL1.
	Not installed	Disconnects I/OVL1 of U1 from the driving signal bus for channel I/OVL1.
JP24	1-2	Connects \overline{TS} pin of U2 to V _L , placing the device's I/O pins in normal operating mode.
	2-3	Connects \overline{TS} pin of U2 to GND, placing the device's I/O pins in high-impedance three-state mode.
JP25*	1-2	Connects I/OVL1 of U2 to the driving signal bus for channel I/OVL1.
	Not installed	Disconnects I/OVL1 of U2 from the driving signal bus for channel I/OVL1.

*The following pairs are mutually exclusive. Do not connect both of any of the following pairs at the same time: JP9 and JP23, JP10 and JP25, JP15 and JP21, and JP20 and JP22.

Detailed Description of Hardware

The MAX14591 EV kit is a fully assembled and tested circuit board that demonstrates the functionality of the MAX14591 high-speed, open-drain capable logic-level translator in both the 8-bump WLP and 8-pin TDFN packages. The EV kit features enables direct evaluation of the device by multiple jumper-selectable methods. The highly configurable PCB allows the user to evaluate each package separately or both at once. Input power to the EV kit is provided by a micro-USB, type-B connector or an external 5V power supply. On-board LDO regulators provide the appropriate voltage for each component, and potentiometers allow the user to adjust the power supply for either side of the level translator independently. The EV kit's PCB is designed with 1oz copper.

Power Supply

The EV kit is powered by a user-supplied 5V external DC power supply connected between the VBUS test point (TP26) and GND, or the USB bus provided at the micro-USB connector (J1). The power supply is then converted into three independent voltages. The pin-selectable output voltage of the MAX8902A (U3) provides a 4.6V supply for peripherals such as the NC7WZ07 open-drain buffer, as well as for the DS1090 EconOscillators™. Two separate

MAX8902B ICs are used to generate the power for the V_{CC} and V_L supplies on the MAX14591. The V_{CC} supply is generated by U6, which also provides power to the push-pull buffer for the V_{CC} channels (U10). The V_L supply is generated by U7, which also provides power to the push-pull buffer for the V_L channels (U8).

On-Board Oscillators

The EV kit features two on-board oscillators to generate input signals to the device. The DS1090-1 (U5) is used to generate a potentiometer-adjustable clock from 4MHz to 8MHz, while the DS1090-16 (U4) generates a potentiometer adjustable clock from 250kHz to 500kHz. These clock signals can be connected to individual channels using 4-way jumpers JP2, JP5, JP12, and JP17 (Table 1).

Push-Pull and Open-Drain Evaluation

Each channel can be driven in either push-pull mode or open-drain mode. For evaluation of push-pull operation or low-speed open-drain operation, use the on-board oscillators. Simply connect the open-drain buffer or push-pull buffer through one of the 4-way jumpers to the channel to be driven to begin evaluation. See Table 1 for jumper configurations. For high-speed open-drain operation, an external function generator is required.

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C3, C4, C6, C9, C11	6	10 μ F \pm 10%, 6.3V X5R ceramic capacitors (0805)
C2, C5, C10	3	0.01 μ F \pm 10%, 16V X7R ceramic capacitors (0603)
C7, C8, C12, C13–C18	8	0.1 μ F \pm 10%, 16V X7R ceramic capacitors (0603)
C14, C19	2	1 μ F \pm 10%, 16V X5R ceramic capacitors (0603)
D1	1	Red LED (0805) Stanley Electric BR1112H-TR
J1	1	Micro USB, type-B receptacle Hirose ZX62D-B-5PA8
JP1, JP3, JP7, JP9–JP11, JP13–JP15, JP18–JP23, JP25	16	2-pin, single-row headers

DESIGNATION	QTY	DESCRIPTION
JP2, JP5, JP12, JP17	4	4-pin headers
JP4, JP6, JP24	3	3-pin, single-row headers
POT1, POT2	2	500k Ω \pm 10%, 0.25W potentiometers Murata PV37W504C01B00
POT3, POT4	2	50k Ω \pm 10%, 0.25W potentiometers Murata PV37W503C01B00
R1	1	470 Ω \pm 5% resistor (0805)
R2	1	1.5k Ω \pm 1% resistor (0805)
R3	1	120k Ω \pm 1% resistor (0805)
R4, R5	2	43k Ω \pm 5% resistors (0805)
R6	1	80.6k Ω \pm 1% resistor (0805)
R7	1	68k Ω \pm 1% resistor (0805)

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Component List (continued)

DESIGNATION	QTY	DESCRIPTION
R8, R9, R18, R19	4	100kΩ ±5% resistors (0805)
R10–R17	8	1kΩ ±1% resistors (0805)
TP4–TP8	5	Black test points
TP9, TP10, TP13, TP16, TP17, TP22	6	White test points
TP11, TP12, TP14, TP15, TP18–TP21	8	Yellow test points
TP23–TP26	4	Red test points
U1	1	High-speed, open-drain capable logic-level translator (8 WLP) Maxim MAX14591EWA+
U2	1	High-speed, open-drain capable logic-level translator (8 TDFN-EP*) Maxim MAX14591ETA+
U3	1	Low-noise LDO regulator with pin-selectable output voltage Maxim MAX8902AATA+

DESIGNATION	QTY	DESCRIPTION
U4	1	Low-frequency, spread- spectrum EconOscillator Maxim DS1090U-16+
U5	1	Low-frequency, spread- spectrum EconOscillator Maxim DS1090U-1+
U6, U7	2	Low-noise LDO regulators with resistor-selectable output voltage Maxim MAX8902BATA+
U8, U10	2	Tiny logic ultra-high-speed dual inverters Fairchild NC7WZ04P6X
U9, U11	2	Tiny logic ultra-high-speed dual buffers Fairchild NC7WZ07P6X
—	17	Shunts
—	1	PCB: MAX14591 EVKIT

*EP = Exposed pad.

Component Suppliers

SUPPLIER	PHONE	WEBSITE
Hirose Electric Co., Ltd.	—	www.hirose-connectors.com
Murata Americas	800-241-6574	www.murataamericas.com
Stanley Electric Co., Ltd.	—	www.stanley-components.com

Note: Indicate that you are using the MAX14591 when contacting these component suppliers.

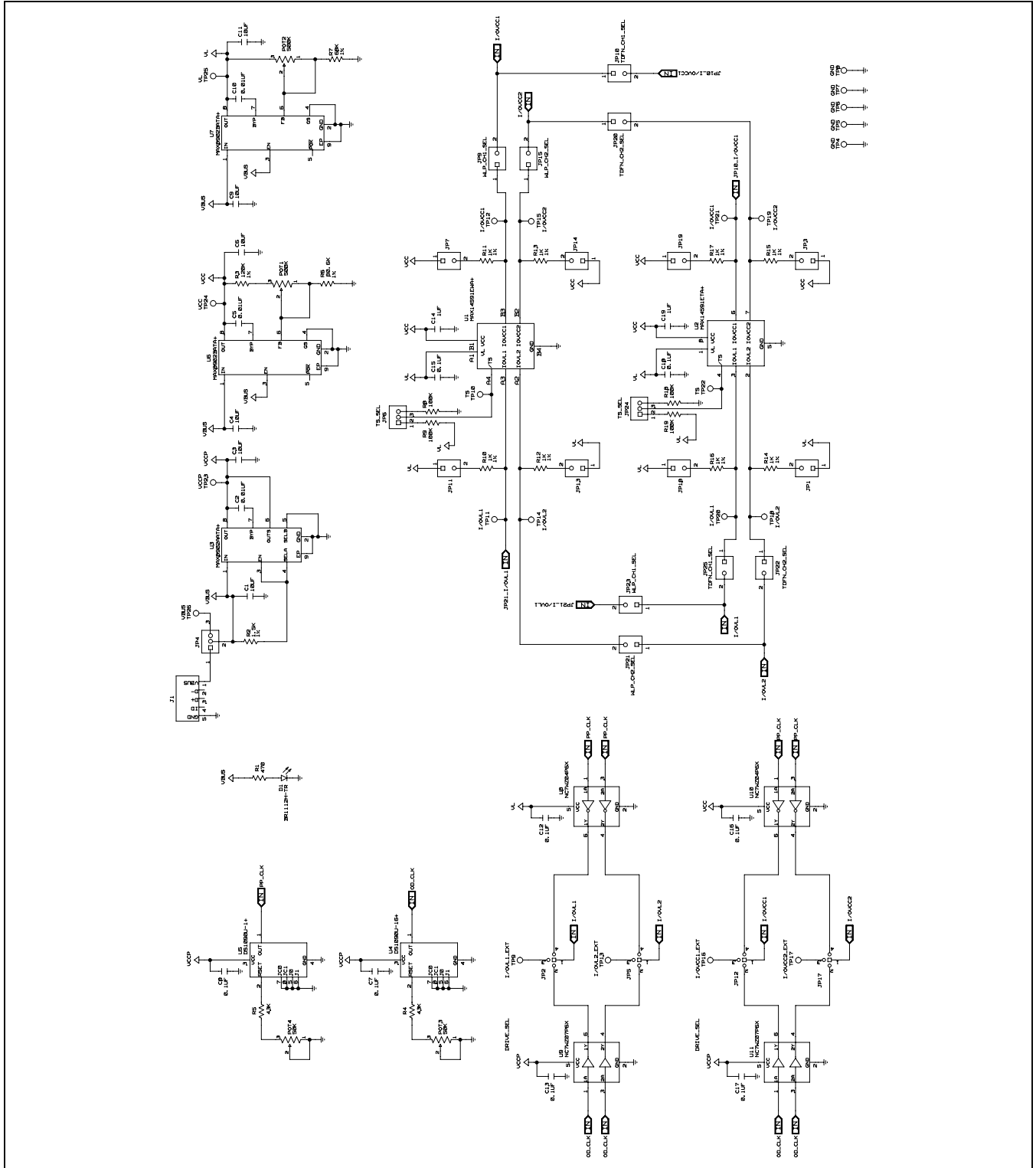


Figure 1. MAX14591 EV Kit Schematic

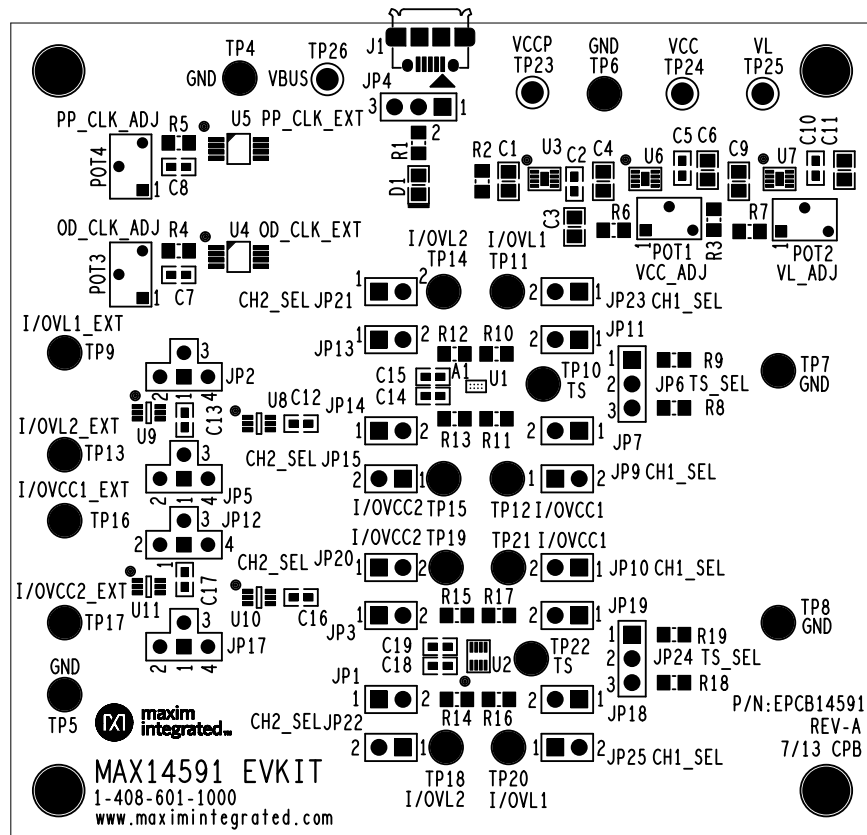


Figure 2. MAX14591 EV Kit Component Placement Guide

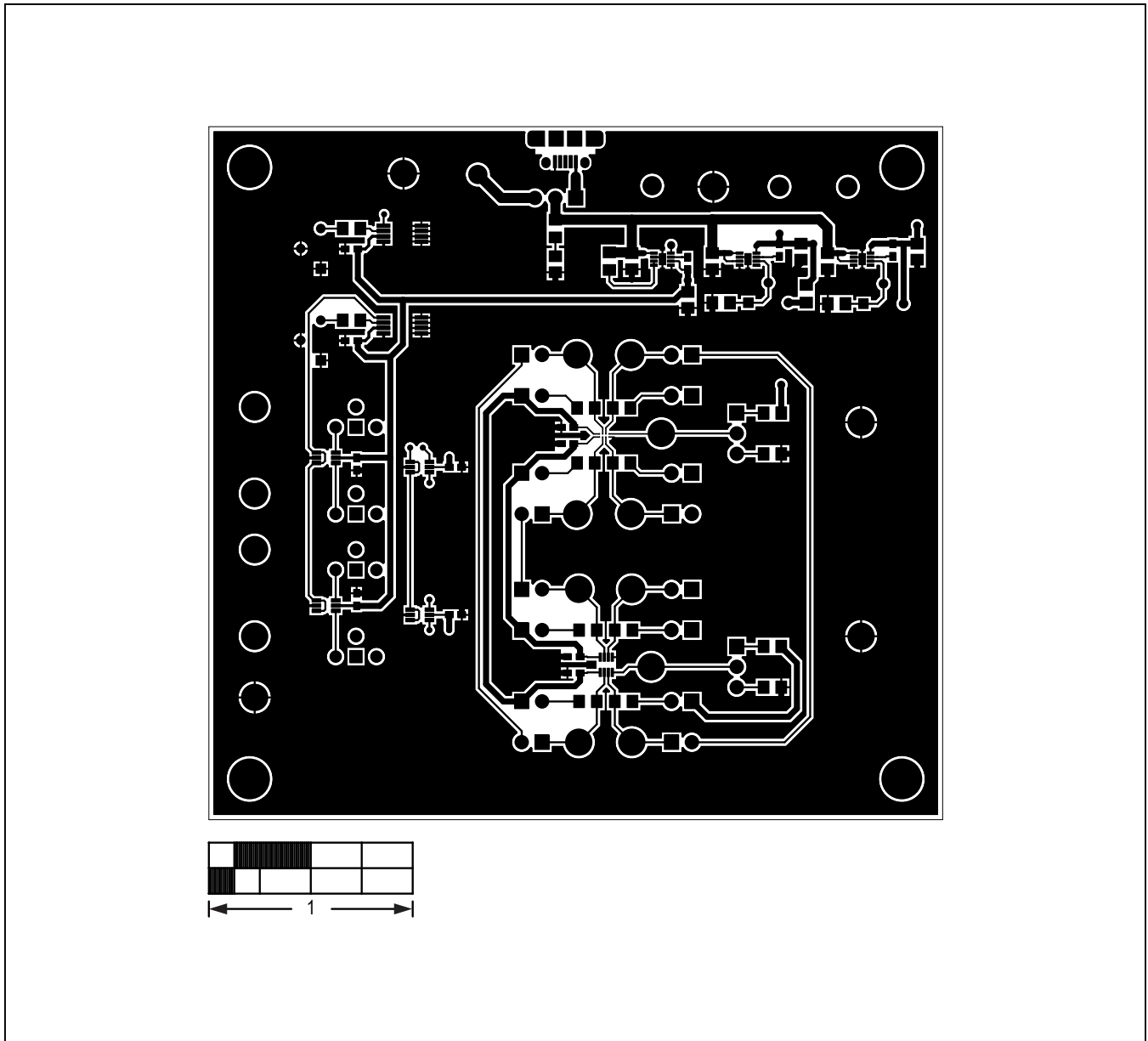


Figure 3. MAX14591 EV Kit Layout—Component Side

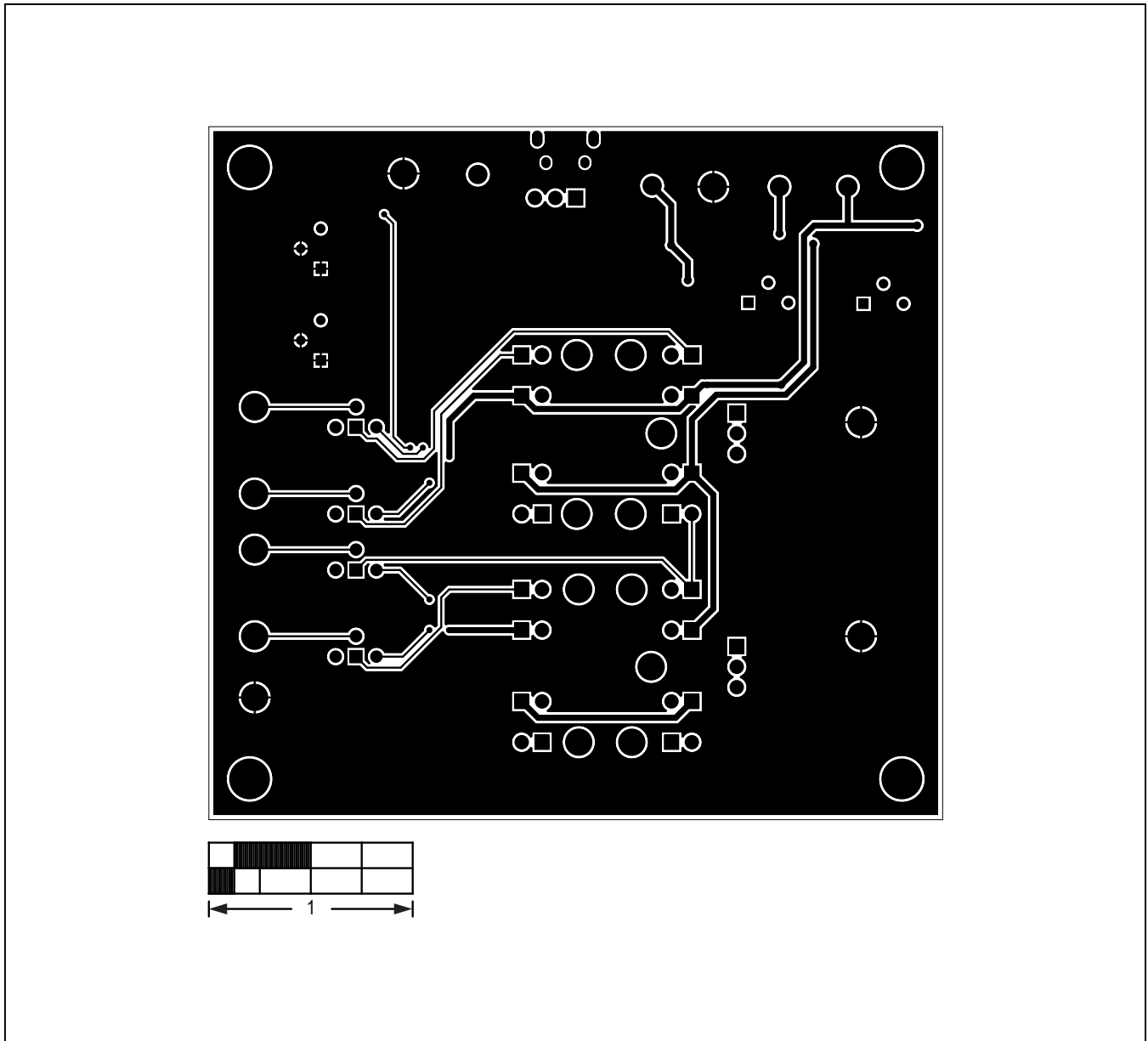


Figure 4. MAX14591 EV Kit Layout—Solder Side

Ordering Information

PART	TYPE
MAX14591EVKIT#	EV Kit

#Denotes RoHS compliant.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/13	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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