



SPN2038

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN2038 is the N-Channel logic enhancement mode power field effect transistor which is produced with high cell density DMOS trench technology. The SPN2038 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

FEATURES

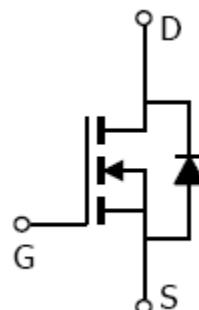
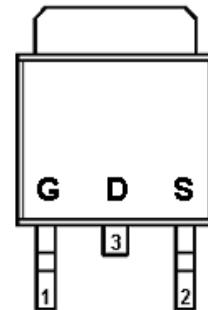
- ◆ 20V/14A, $R_{DS(ON)} = 16m\Omega$ @ $V_{GS} = 4.5V$
- ◆ 20V/7A, $R_{DS(ON)} = 22m\Omega$ @ $V_{GS} = 2.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

TO-252



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN2038T252RGB	TO-252	SPN2038

※ SPN2038T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	20	V
Gate –Source Voltage	V _{GSS}	±16	V
Continuous Drain Current	T _c =25°C	ID	A
	T _c =100°C		
Pulsed Drain Current	I _{DM}	70	A
Power Dissipation	P _D	25	W
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	5	°C/W



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, ID=250uA	20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , ID=250uA	0.5		1.2	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±16V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =16V, V _{GS} =0V			1	uA
		V _{DS} =16V, V _{GS} =0V T _J =55°C			5	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =4.5V	28			A
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =4.5V, ID=14A		0.016	0.02	Ω
		V _{GS} =2.5V, ID=7A		0.022	0.028	
Forward Transconductance	g _{fs}	V _{DS} =5V, ID=14A		30		S
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, V _{GS} =4.5V ID=14A		9.8		nC
Gate-Source Charge	Q _{gs}			2.1		
Gate-Drain Charge	Q _{gd}			3		
Input Capacitance	C _{iss}	V _{DS} =15, V _{GS} =0V f=1MHz		772		pF
Output Capacitance	C _{oss}			83		
Reverse Transfer Capacitance	C _{rss}			79		
Turn-On Time	t _{d(on)}	V _{DD} =10V, ID=14A, V _{GS} =4.5V, R _G =3.3Ω		4		nS
	t _r			12.5		
Turn-Off Time	t _{d(off)}			20		
	t _f			8		



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TYPICAL CHARACTERISTICS

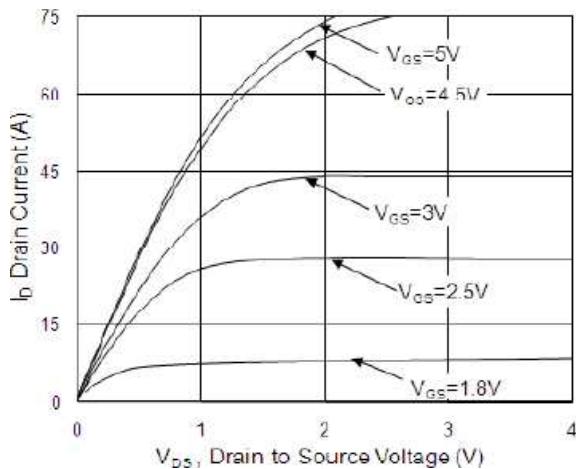


Fig. 1 Typical Output Characteristics

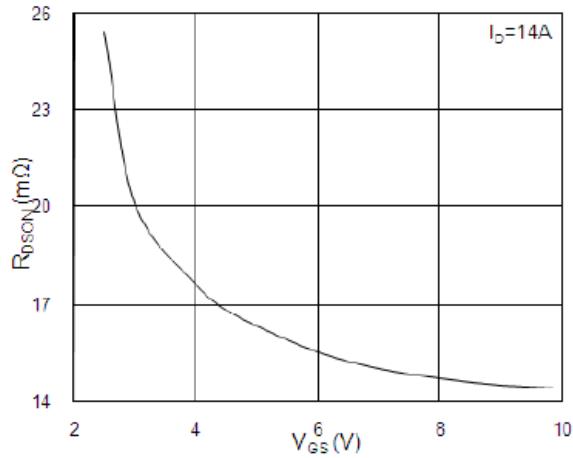


Fig. 2 On-Resistance vs Gate Voltage

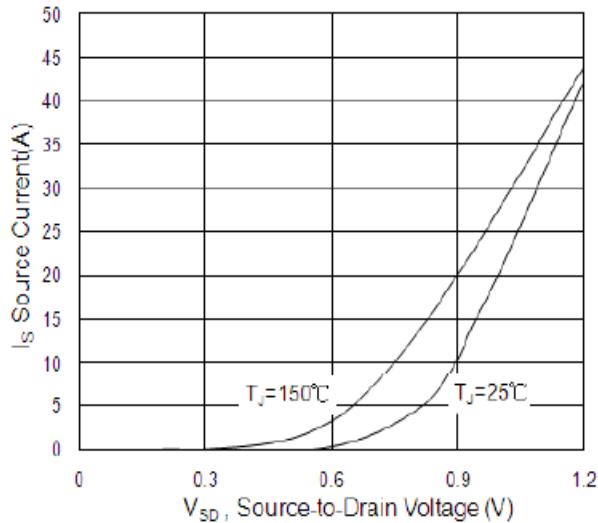


Fig. 3 Forward Characteristics

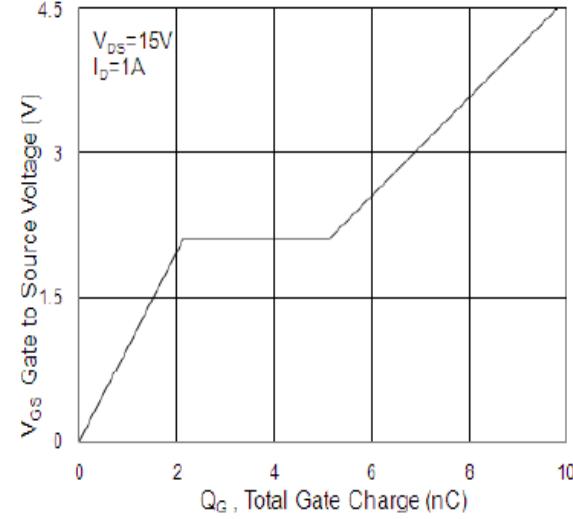


Fig. 4 Total Gate Charge

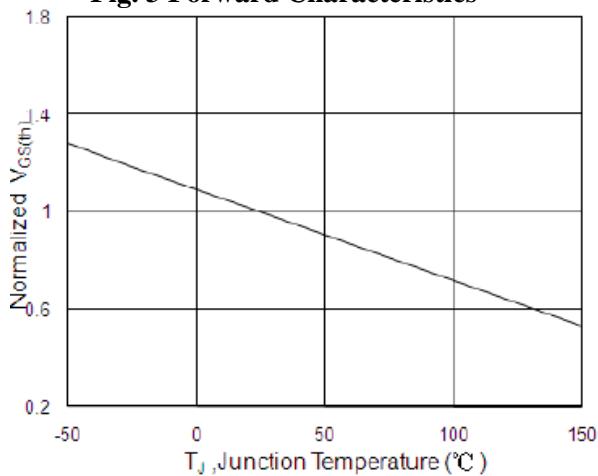


Fig. 5 V_{GS} vs Temperature

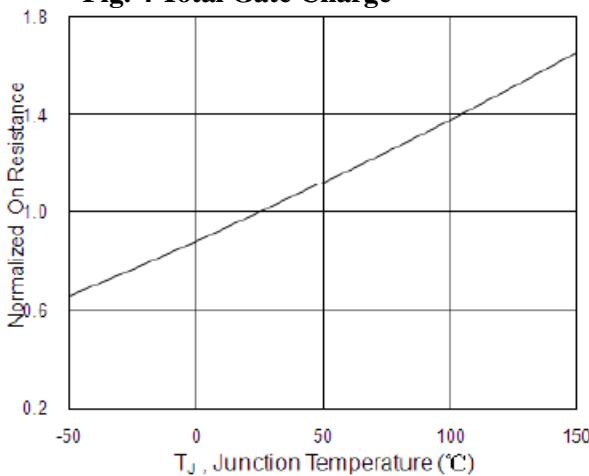


Fig. 6 $R_{DS(on)}$ vs Temperature



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TYPICAL CHARACTERISTICS

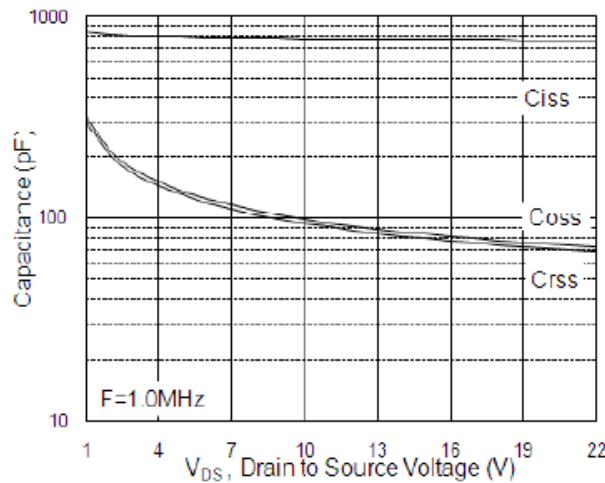


Fig. 7 Capacitance vs Vds

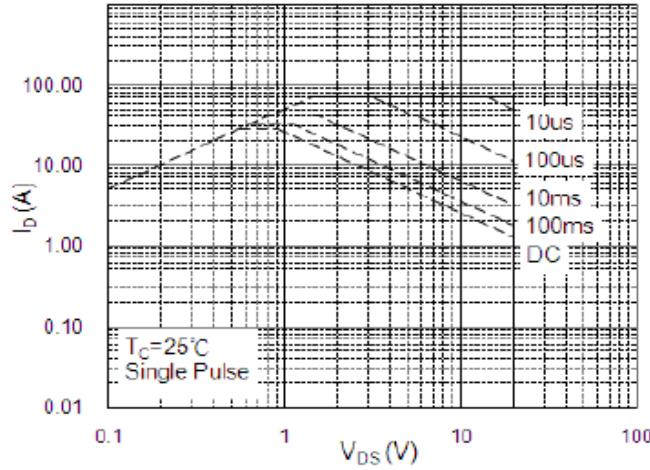


Fig. 8 Safe Operation Region

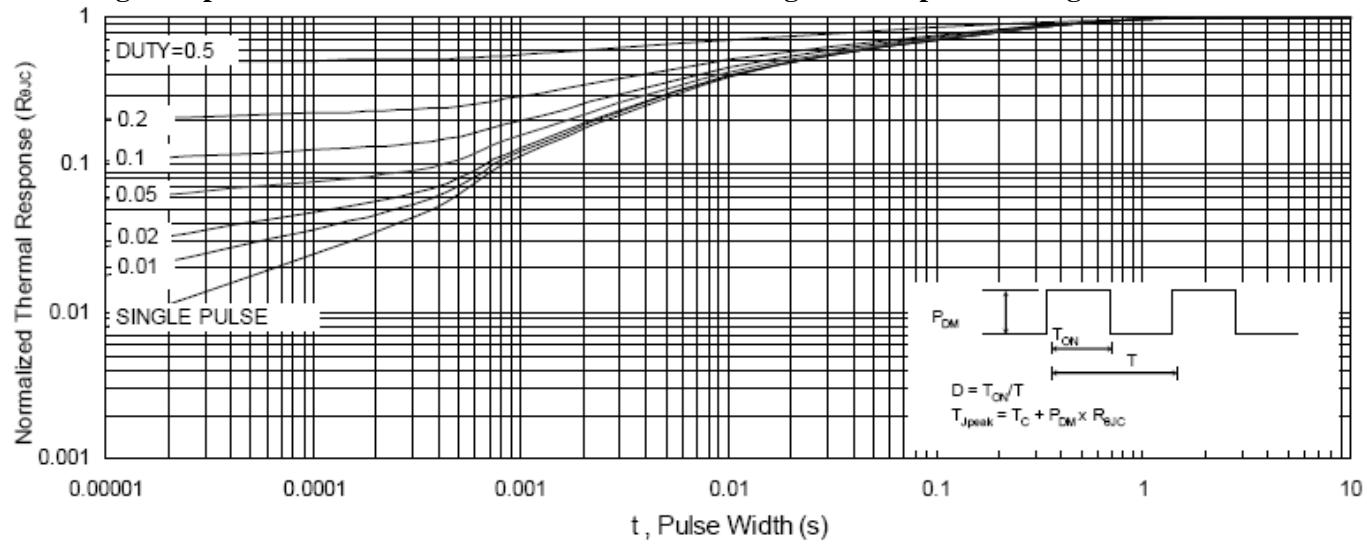


Fig. 9 Maximum Transient Thermal Impedance

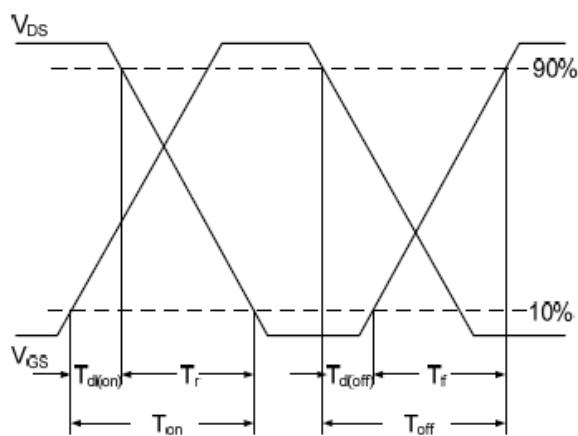


Fig. 10 Switching Time Waveform

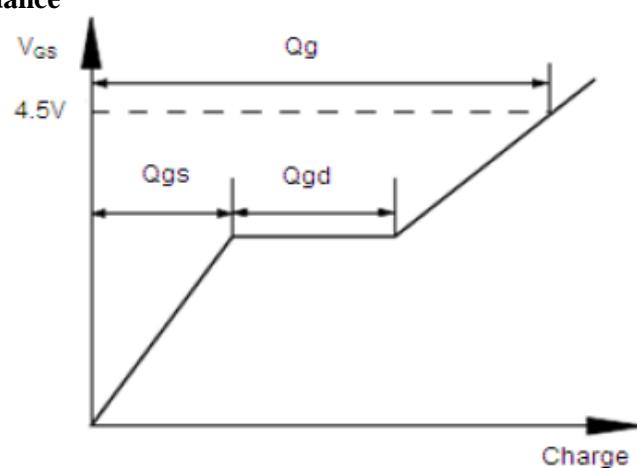


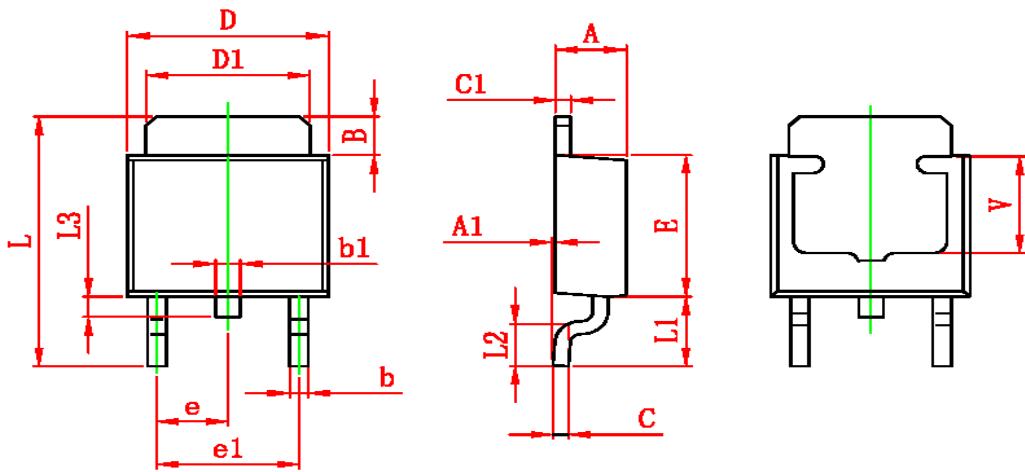
Fig. 11 Gate Charge Waveform



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TO-252 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.350	0.650	0.014	0.026
V	3.80 REF		0.150 REF	



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