Engineering Specification

Type 15.0 QXGA Color TFT/LCD Module
Model Name:IAQX10M

Document Control Number : OEM I-910M-03

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Sales Support
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ii Record of Revision

Date	Document Revision	Page	Summary
November 13,2001	OEM I-910M-01	All	First Edition for customer. Based on Internal Spec. EC H31229 as of November 9,2001.
March 12,2002	OEM I-910M-02		Based on Internal Spec. EC H31230 as of February 20,2002.
		4	To update Handling Precautions.
		6	To update following items. • Weight • Physical Size • White Luminance • Power Consumption (VDD Line) • Lamp Power Consumption To add Note for Temperature Range.
		7	To eliminate Optional part in the diagram.
		9	To update following items. • Max. value of Response Time • Color Chromaticity • White Luminance (ICFL)
		11	To update Interface Signal Connector.
		12,13	To update Interface Signal Description.
		14-18	To update Signal Electrical Characteristics for LVDS Receiver.
		19	To add Recommended Guidelines for Motherboard PCB Design and Cable Selection.
		22	To update Parameter guide line for CFL Inverter.
		26	To update Typ. value of Power Consumption.
		28,29	To update Reference Drawings.
June 17,2002	OEM I-910M-03		Based on Internal Spec. EC H31231 as of May 10,2002.
		4	To update Handling Precautions.
		13	To update Electrical Characteristics.
		15	To update Switching Characteristics.
		22	To delete 5.0[mA] lamp condition.
		24	To update Timing Characteristics.

1.0 Handling Precautions

- If any signals or power lines deviate from the power on/off sequence, it may cause shorten the life of the LCD module.
- The LCD panel and the CFL are made of glass and may break or crack if dropped on a hard surface, so please handle them with care.
- CMOS-ICs are included in the LCD panel. They should be handled with care, to prevent electrostatic discharge.
- Do not press the reflector sheet at the back of the LCD module to any directions.
- Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
- Please handle care when mount in the system cover. Mechanical damage for lamp cable and for lamp connector may cause safety problems.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.5, IEC60950 or UL60950), or be applied exemption conditions of flammability requirements (4.7.3.4, IEC60950 or UL60950) in an end product.
- The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL1950).
- The fluorescent lamp in the liquid crystal display(LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Never apply detergent or other liquid directly to the screen.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth; do not use solvents or abrasives.
- Do not touch the front screen surface in your system, even bezel.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporationg this product.

2.0 General Description

This specification applies to the Type 15.0 Color TFT/LCD Module 'IAQX10M'.
This module is designed for a display unit of a monitor application.
The screen format and electrical interface are intended to support the QXGA(2048(H) x 1536(V)) screen.
Support color is native 262K colors(RGB 6-bit data driver).
All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.
This module does not contain an inverter card for backlight.

2.1 Characteristics

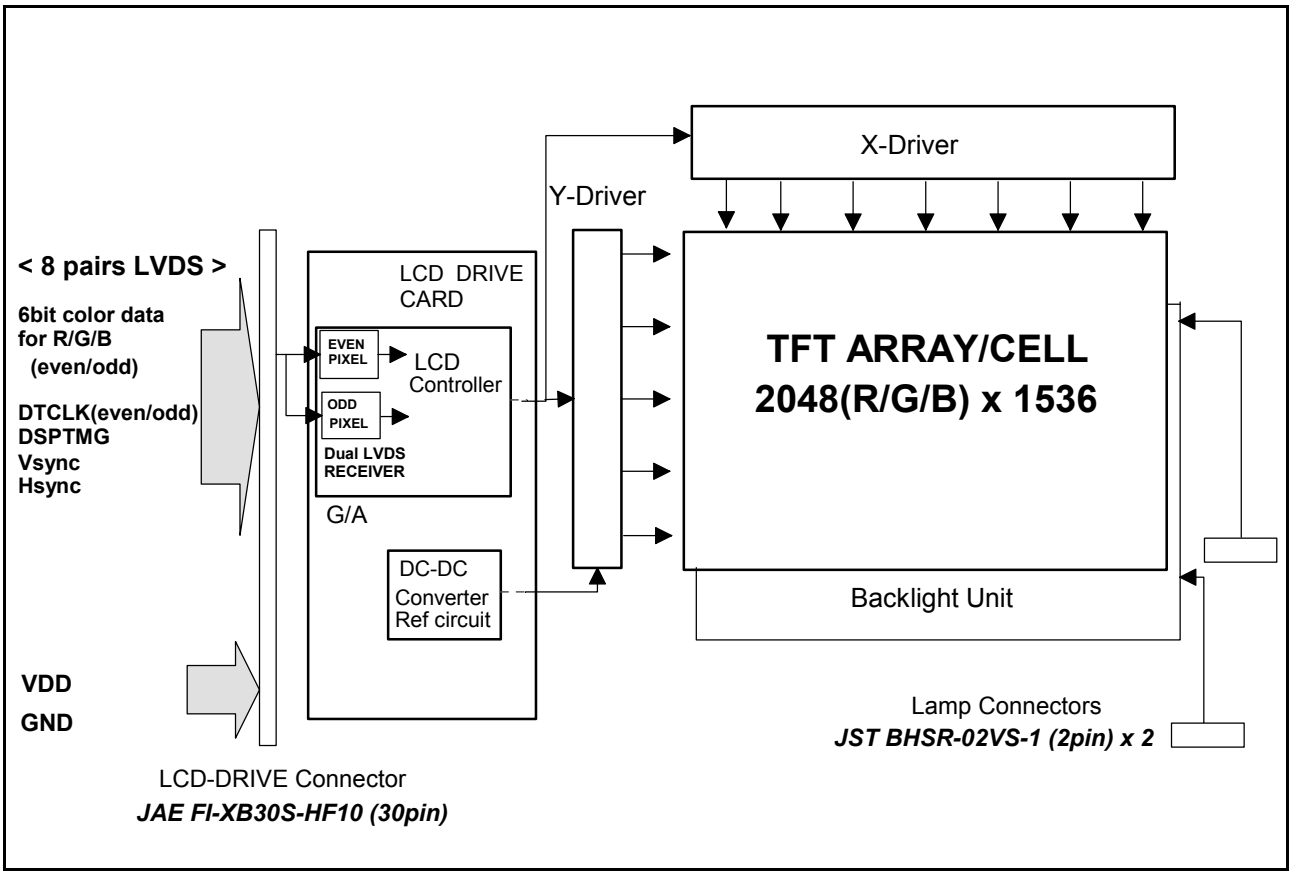
The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	380
Pixels H x V	2048(x3) x 1536
Active Area [mm]	304.1(H) x 228.1(V)
Pixel Pitch [mm]	0.1485(per one triad) x 0.1485
Pixel Arrangement	R,G,B Vertical Stripe
Weight [grams]	1065 Typ., 1100 Max.
Physical Size [mm]	326.0(W) x 244.5(H) x 13.0(D) Typ./13.3(D) Max.
Display Mode	Normally Black
Support Color	Native 262K colors(RGB 6-bit data driver)
White Luminance [cd/m^2] ICFL=7.0mA	200 Typ. (center) 180 Typ. (5 points average)
Contrast Ratio	400 : 1 Typ.
Optical Rise Time + Fall Time [msec]	60 Typ.
Nominal Input Voltage VDD [Volt]	+3.3 Typ.
Power Consumption [Watt](VDD Line)	4.1 Typ., 5.2 Max.
Lamp Power Consumption [Watt] ICFL=7.0mA	8.6 Typ. (W/o inverter loss)
Electrical Interface	8 pairs LVDS(Even/Odd R/G/B Data(6bit), 3sync signals, Clock)
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 **(Note)** -20 to +60

Note : Max. Operating Temperature 50 degree C in the Spec means the temperature measured for the point of the front surface of the LCD glass cell.

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 15.0 Color TFT/LCD Module.
The first LVDS port transmits even pixels while the second LVDS port transmits odd pixels.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	V	
Input Voltage on FlatLink pins	-	-0.3	+2.6	V	
Input Signal Voltage on all other pins	VIN	-0.3	VDD+0.3	V	
CFL Ignition Voltage	Vs	-	+1,600	Vrms	**(Note 2)**
CFL Current	ICFL	-	+8.5	mAms	
CFL Peak Inrush Current	ICFLP	-	+20	mA	
Operating Temperature	TOP	0	+50	deg.C	**(Note 1)**
Operating Relative Humidity	HOP	8	95	%RH	**(Note 1)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 1)**
Storage Relative Humidity	HST	5	95	%RH	**(Note 1)**
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.
Note 2 : Duration : 50msec Max. Ta=0 degree C

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≧10 (Left) Vertical (Upper) K≧10 (Lower)	85 85 85 85	- - - -
Contrast ratio		400	-
Response Time	Rising	30	60 Max.
(ms)	Falling	30	60 Max.
Color	Red x	0.569	-
Chromaticity	Red y	0.332	-
(CIE)	Green x	0.312	-
	Green y	0.544	-
	Blue x	0.149	-
	Blue y	0.132	-
	White x	0.313	-
	White y	0.329	-
White Luminance (cd/m^2) ICFL 7.0 mA		200 Typ. (Center) 180 Typ. (5 points average)	

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30S-HF10
Mating Receptacle Manufacture	JAE
Mating Receptacle/Part Number	FI-X30M

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Interface Signal Connector

Signal Connector Pin Assignment

Pin #	Signal Name	Pin #	Signal Name
1	GND	16	GND
2	VDD	17	ReCLKIN-
3	VDD	18	ReCLKIN+
4	Reserved **(Note 1)**	19	GND
5	Reserved **(Note 1)**	20	RoIN0-
6	VDD	21	RoIN0+
7	VDD	22	GND
8	ReIN0-	23	RoIN1-
9	ReIN0+	24	RoIN1+
10	GND	25	GND
11	ReIN1-	26	RoIN2-
12	ReIN1+	27	RoIN2+
13	GND	28	GND
14	ReIN2-	29	RoCLKIN-
15	ReIN2+	30	RoCLKIN+

Note :

1. 'Reserved' pins are not allowed to connect any other line.
2. Voltage levels of all input signals are LVDS compatible (except VDD). Refer to "Signal Electrical Characteristics for LVDS", for voltage levels of all input signals.

5.3 Interface Signal Description

The module uses a pair of LVDS receiver SN75LVDS86(Texas Instruments) compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84/85 or compatible.

PIN #	SIGNAL NAME	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	Reserved	Reserved
5	Reserved	Reserved
6	VDD	+3.3V Power Supply
7	VDD	+3.3V Power Supply
8	ReIN0-	Negative LVDS differential data input (Even R0-R5, G0)
9	ReIN0+	Positive LVDS differential data input (Even R0-R5, G0)
10	GND	Ground
11	ReIN1-	Negative LVDS differential data input (Even G1-G5, B0-B1)
12	ReIN1+	Positive LVDS differential data input (Even G1-G5, B0-B1)
13	GND	Ground
14	ReIN2-	Negative LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
15	ReIN2+	Positive LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
16	GND	Ground
17	ReCLKIN-	Negative LVDS differential clock input (Even)
18	ReCLKIN+	Positive LVDS differential clock input (Even)
19	GND	Ground
20	RoIN0-	Negative LVDS differential data input (Odd R0-R5, G0)
21	RoIN0+	Positive LVDS differential data input (Odd R0-R5, G0)
22	GND	Ground
23	RoIN1-	Negative LVDS differential data input (Odd G1-G5, B0-B1)
24	RoIN1+	Positive LVDS differential data input (Odd G1-G5, B0-B1)
25	GND	Ground
26	RoIN2-	Negative LVDS differential data input (Odd B2-B5)
27	RoIN2+	Positive LVDS differential data input (Odd B2-B5)
28	GND	Ground
29	RoCLKIN-	Negative LVDS differential clock input (Odd)
30	RoCLKIN+	Positive LVDS differential clock input (Odd)

Note :

1. Input signals of odd and even clock shall be the same timing.
2. The module uses a 100ohm resistor between positive and negative data lines of each receiver input.
3. Even: First Pixel , Odd: Second Pixel
4. 'Reserved' pins are not allowed to connect any other line.

SIGNAL NAME	Description
+RED 5 (ER5/OR5) +RED 4 (ER4/OR4) +RED 3 (ER3/OR3) +RED 2 (ER2/OR2) +RED 1 (ER1/OR1) +RED 0 (ER0/OR0) (EVEN/ODD)	RED Data 5 (MSB) RED Data 4 RED Data 3 RED Data 2 RED Data 1 RED Data 0 (LSB) Red-pixel Data: Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 (EG5/OG5) +GREEN 4 (EG4/OG4) +GREEN 3 (EG3/OG3) +GREEN 2 (EG2/OG2) +GREEN 1 (EG1/OG1) +GREEN 0 (EG0/OG0) (EVEN/ODD)	GREEN Data 5 (MSB) GREEN Data 4 GREEN Data 3 GREEN Data 2 GREEN Data 1 GREEN Data 0 (LSB) Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 (EB5/OB5) +BLUE 4 (EB4/OB4) +BLUE 3 (EB3/OB3) +BLUE 2 (EB2/OB2) +BLUE 1 (EB1/OB1) +BLUE 0 (EB0/OB0) (EVEN/ODD)	BLUE Data 5 (MSB) BLUE Data 4 BLUE Data 3 BLUE Data 2 BLUE Data 1 BLUE Data 0 (LSB) Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK (EVEN/ODD)	Data Clock: The typical frequency is 82.125MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG (DSP)	When the signal is high, the pixel data shall be valid to be displayed.
VSYNC (V-S)	Vertical Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
HSYNC (H-S)	Horizontal Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
VDD	Power Supply
GND	Ground

Note : Output signals from any system shall be Hi-Z state when VDD is off.

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

Each signal characteristics are as follows;

Electrical Characteristics

Parameter	Symbol	Min	Max	unit	Conditions
Differential Input High Threshold	Vth		+100	[mV]	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100		[mV]	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100	600	[mV]	
Common Mode Input Voltage	Vic	$0.6 + \frac{\|Vid\|}{2}$	$2.0 - \frac{\|Vid\|}{2}$	[V]	Vth-Vtl=200mV
Common Mode Voltage Offset	△Vcm	-50	+50	[mV]	Vth-Vtl=200mV

Note:

- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD (see Figure Measurement system).

Figure. Voltage Definitions

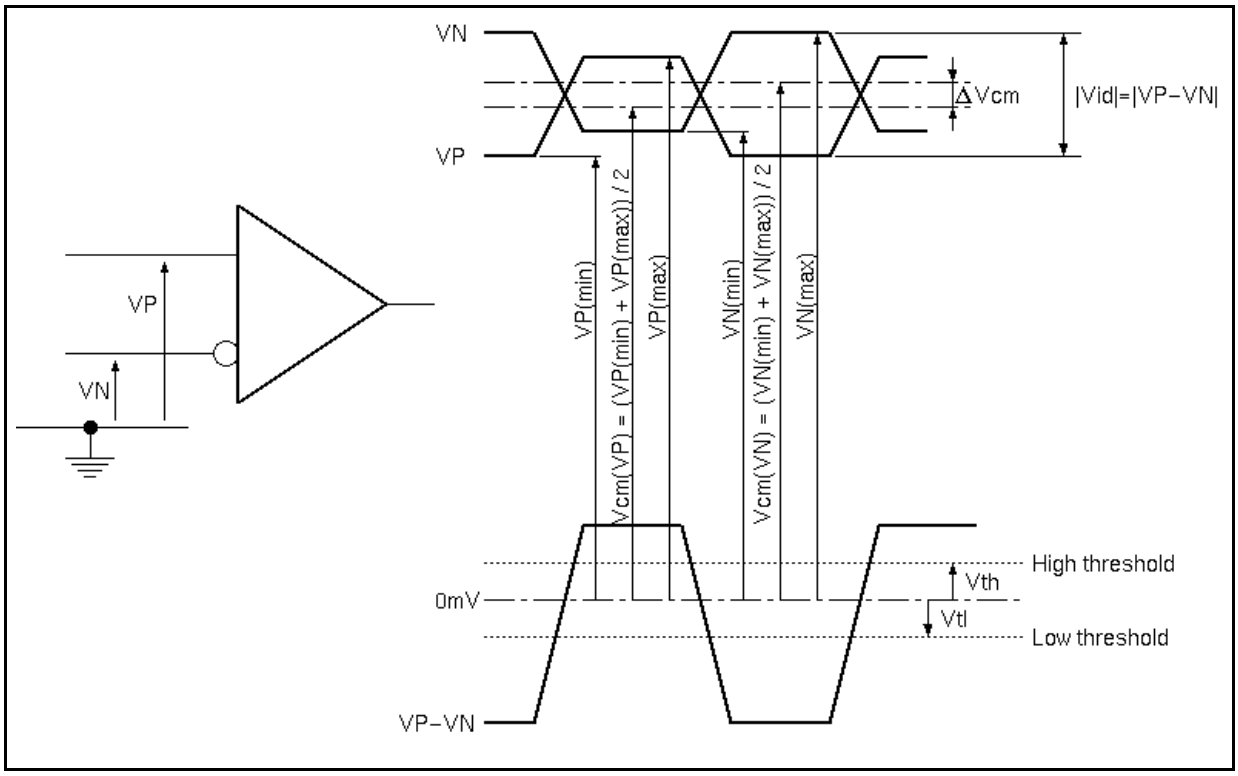
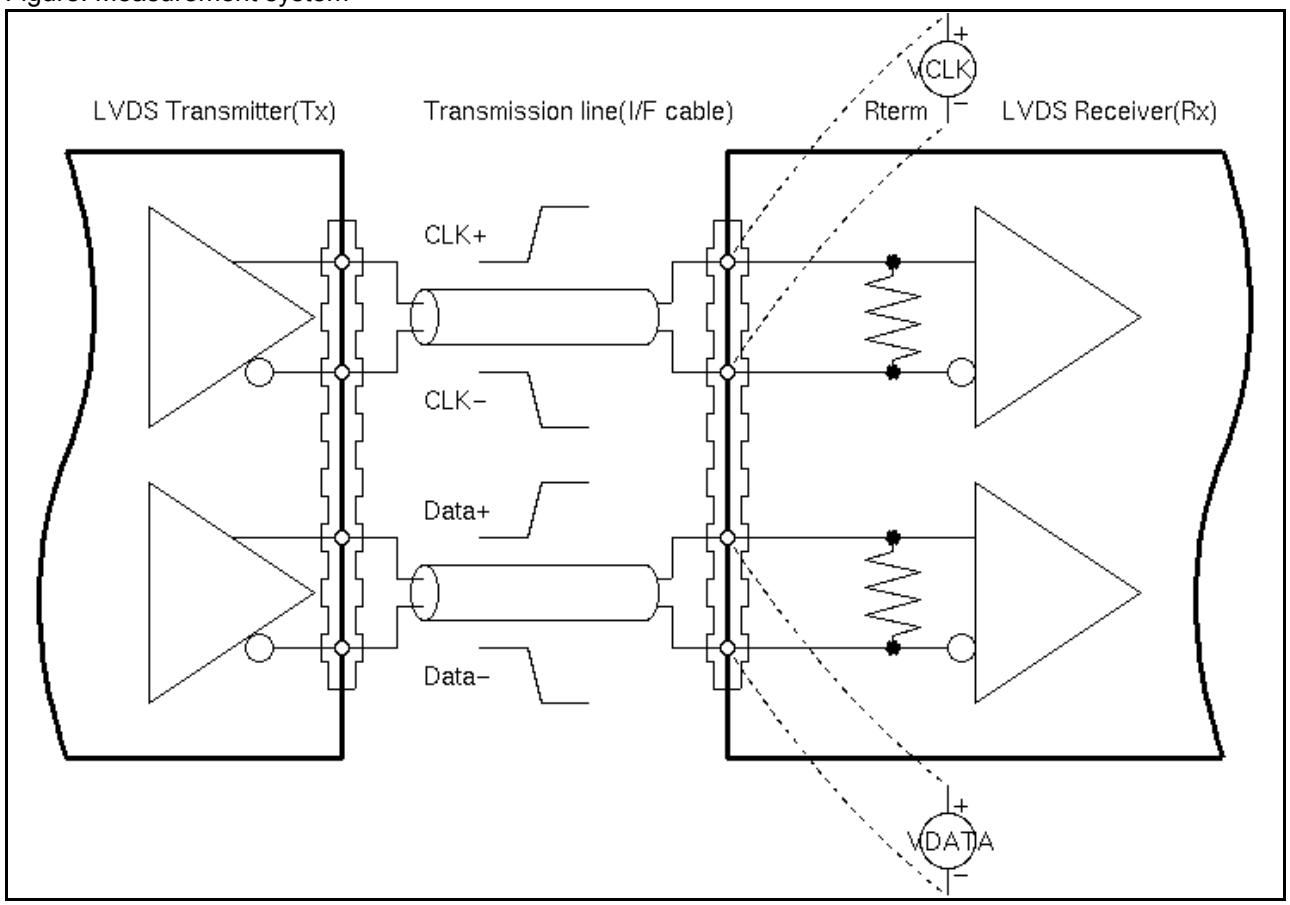


Figure. Measurement system



Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	50.0	82.125	86.6	MHz	
Cycle Time	tc	11.5	12.2	20.0	ns	
Data Setup Time **(Note 2)**	Tsu	500			ps	fc = 82.125MHz, tCCJ < 50ps, Vth-Vtl=200mV, Vcm=1.2V, △Vcm=0
Data Hold Time **(Note 2)**	Thd	500			ps	
Cycle-to-cycle jitter **(Note 3)**	tCCJ	-150		+150	ps	fc = 82.125MHz
Cycle Modulation Rate**(Note 4)**	tCJavg			20	ps/clk	fc = 82.125MHz
Skew Time between ReCLKIN and RoCLKIN	Tskeoclk			tc/7	ns	fc = 82.125MHz
LVDS Input Data Position 1	tLIDP1	-500	0	500	ps	fc = 82.125MHz **(Note 5)**
LVDS Input Data Position 2	tLIDP0	tc/7-500	tc/7	tc/7+500	ps	
LVDS Input Data Position 3	tLIDP6	2tc/7-500	2tc/7	2tc/7+500	ps	
LVDS Input Data Position 4	tLIDP5	3tc/7-500	3tc/7	3tc/7+500	ps	
LVDS Input Data Position 5	tLIDP4	4tc/7-500	4tc/7	4tc/7+500	ps	
LVDS Input Data Position 6	tLIDP3	5tc/7-500	5tc/7	5tc/7+500	ps	
LVDS Input Data Position 7	tLIDP2	6tc/7-500	6tc/7	6tc/7+500	ps	

Note :

1. All values are at VDD=3.3V, Ta=25 degree C.
2. See figure "Timing Definition" and "Timing Definition(detail A)" for definition.
3. Jitter is the magnitude of the change in input clock period.
4. This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles.
   This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.
5. See figure "LVDS input Data Position".

Figure. Timing Definition (Even Port)

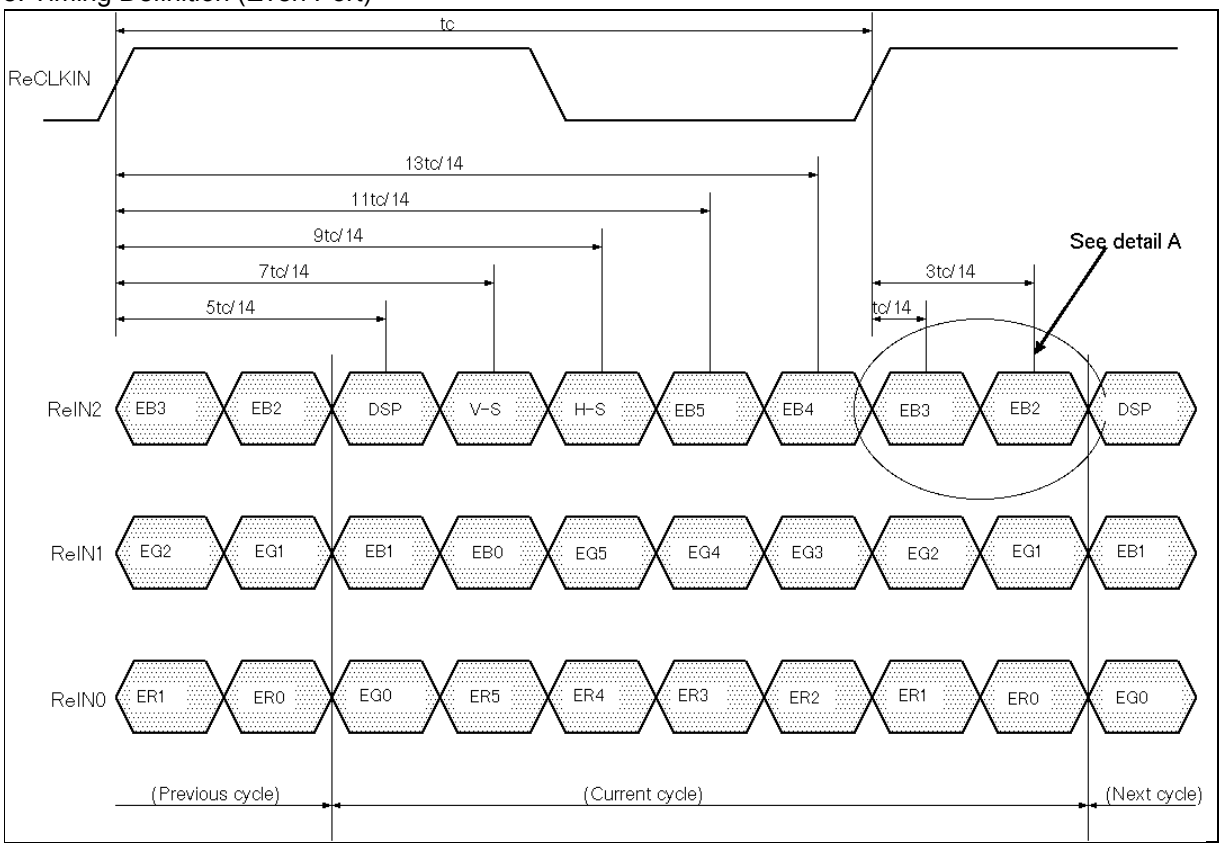


Figure. Timming Definition (Odd Port)

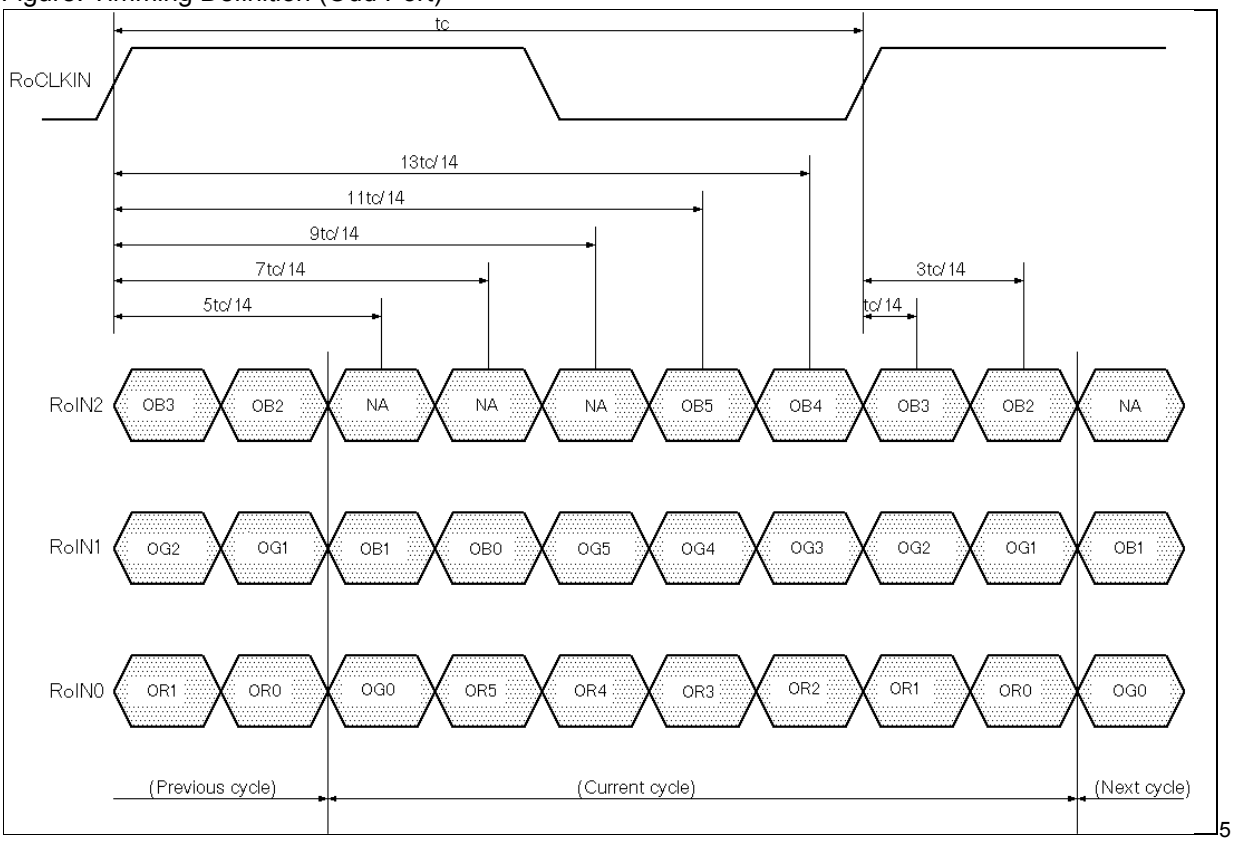


Figure. LVDS Input Data Position

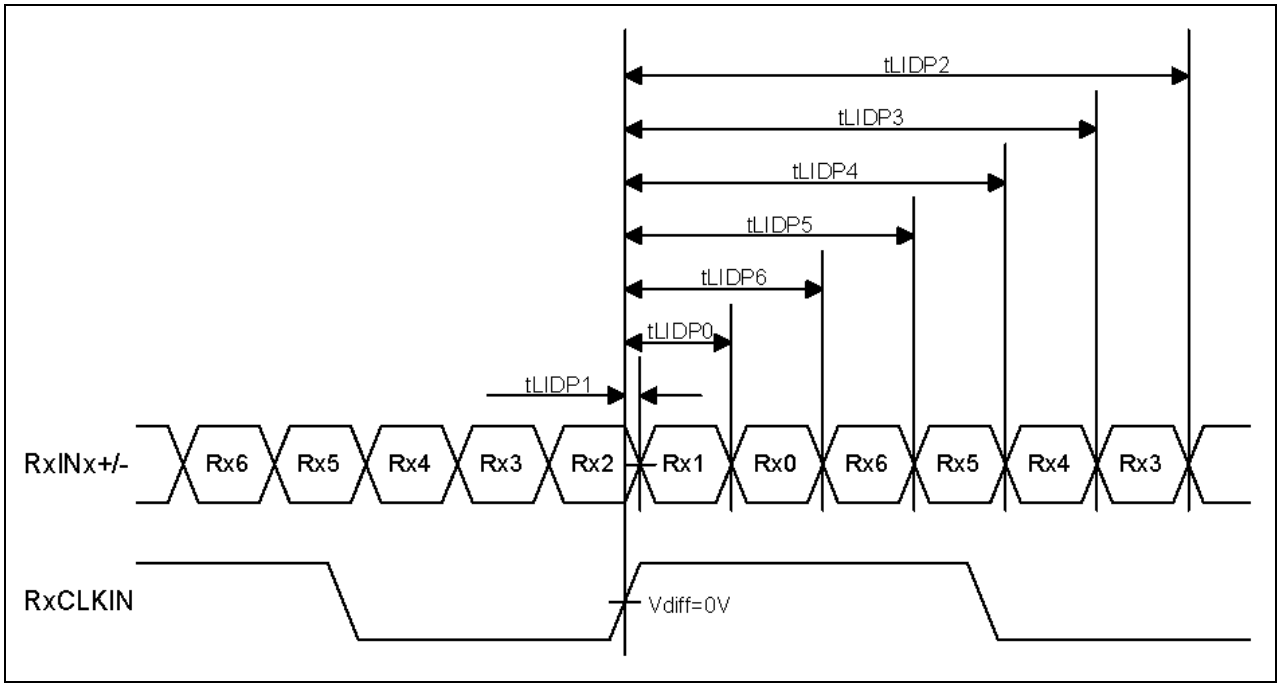
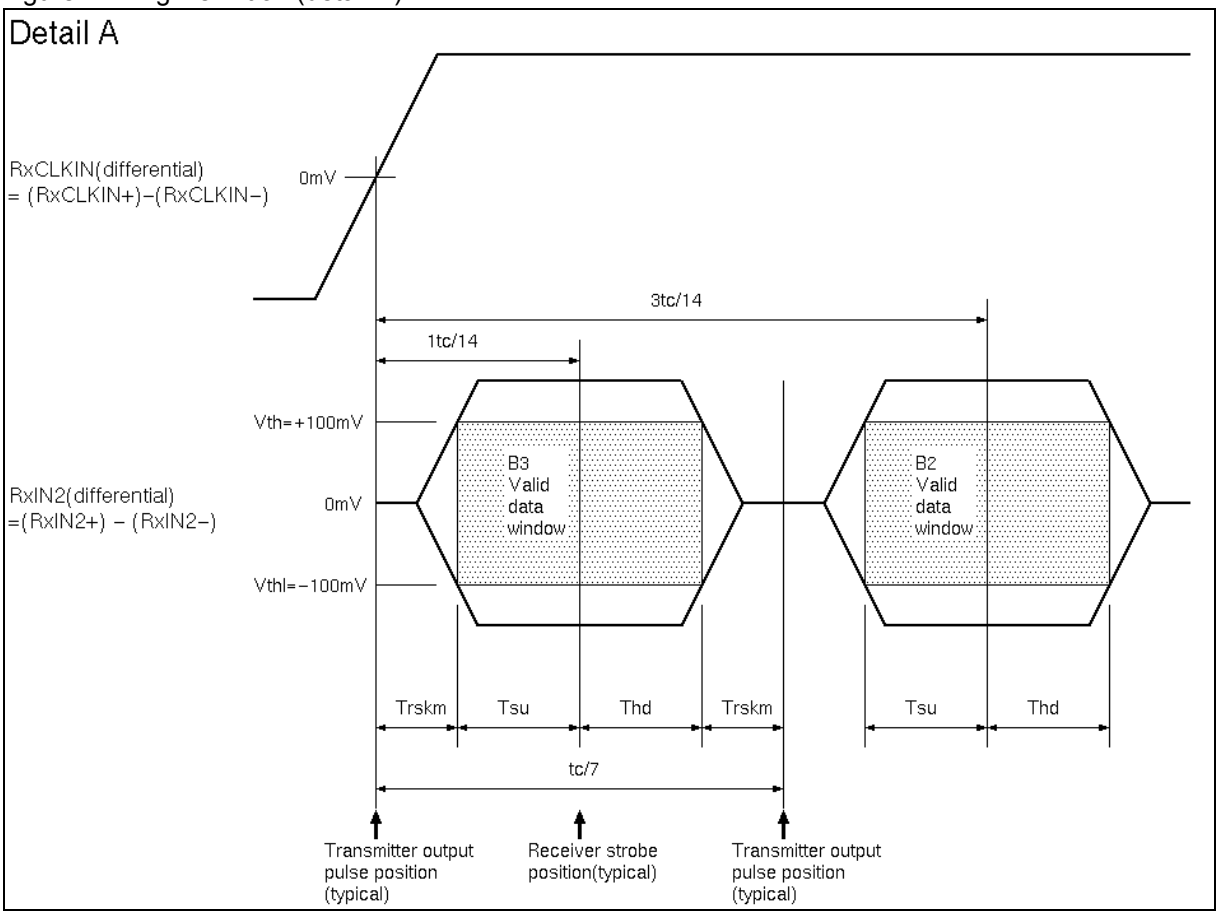


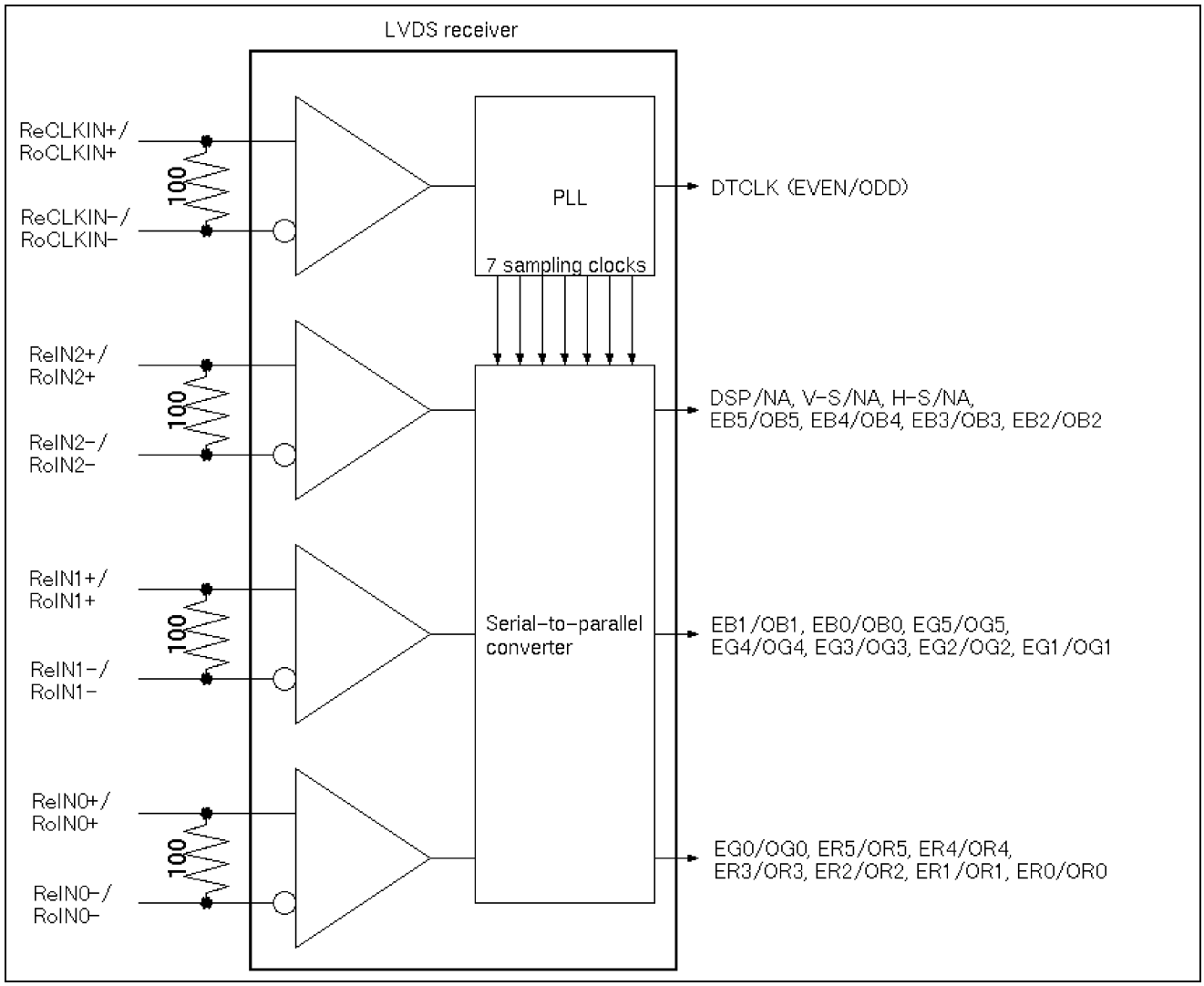
Figure. Timing Definition (detail A)



Note : Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

5.4.2 LVDS Receiver Internal Circuit

Below figure shows the internal block diagram of the LVDS receiver.



5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

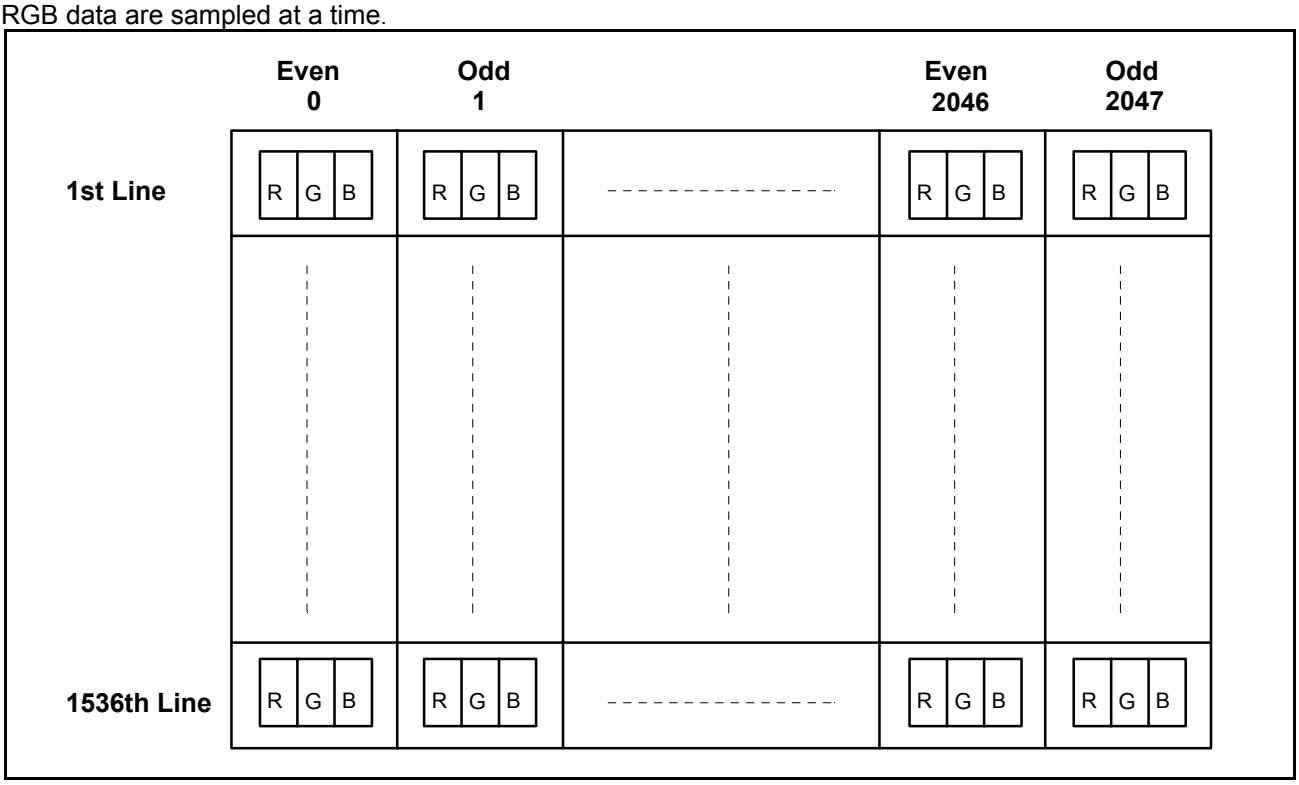
- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.

5.5 Signal for Lamp Connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image. Even and odd pair of RGB data are sampled at a time.



7.0 Parameter guide line for CFL Inverter

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
White Luminance (5 points average)	-	180	-	cd/m^2	(Ta=25 deg.C)
CFL current(ICFL)	3.0	7.0	7.5	mArms	(Ta=25 deg.C)
CFL Frequency(FCFL)	40		60	KHz	(Ta=25 deg.C) **(Note 1)**
CFL Ignition Voltage(Vs)	1,500	-	-	Vrms	(Ta= 0 deg.C) **(Note 3)**
CFL Voltage (Reference)(VCFL)	-	620	-	Vrms	(Ta=25 deg.C) **(Note 2)**
CFL Power consumption(PCFL)	-	8.6	9.5	W	(Ta=25 deg.C) **(Note 2)**

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

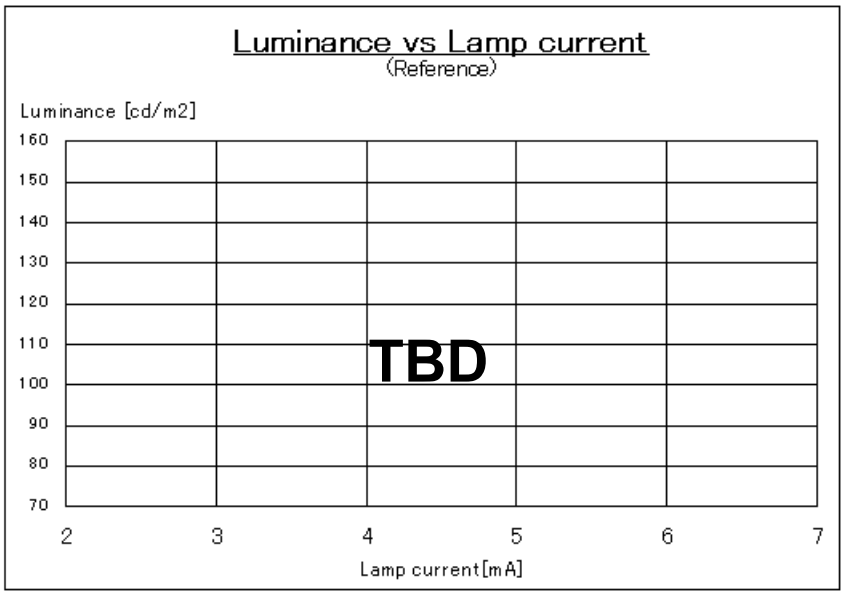
Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,500 voltage. Lamp units need 1,500 voltage minimum for ignition.

Note 4:

- All of characteristics listed are measured under the condition using the Test inverter.
- In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
- In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.
- Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
- Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
- It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4.0[mA].

The following chart is CFL current versus the luminance for your reference.



8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86(Texas Instruments) or equivalent.

8.1 Timing Characteristics

Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freqency	Fdck	50	82.125	86.6	[MHz]
		Tck	11.547	12.177	20.000	[ns]
+V-Sync	Frame Rate	Fv	-	49.266	-	[Hz]
		Tv	-	20.3	-	[ms]
		Nv	1542	1555	1662	[lines]
	V-Active Level	Tva	-	13.1	-	[us]
		Nva	1	1	124	[lines]
	V-Back Porch	Nvb	1	1	124	[lines]
	V-Front Porch	Nvf	1	17	124	[lines]
+DSPTMG	V-Line	m		1536		[lines]
+H-Sync	Scan Rate	Fh	-	76.6	-	[KHz]
		Th	-	13.1	-	[us]
		Nh	1064	1072	1407	[Tck]
	H-Active Level	Tha		0.097		[us]
		Nha	1	8	381	[Tck]
	H-Back Porch	Thb	1	32	381	[Tck]
	H-Front Porch	Thf	1	8	381	[Tck]
+DSPTMG	Display	Thd		12.469		[us]
+DATA	Data Even/Odd	n		2048		[dots]

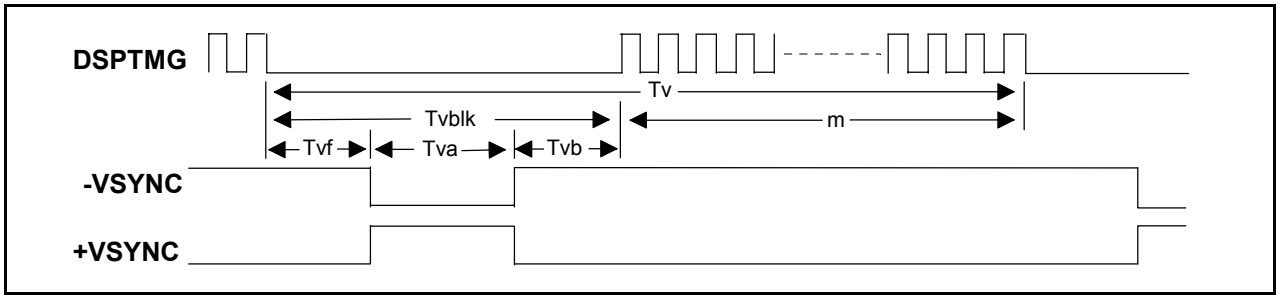
Note :

- Both positive Hsync and positive Vsync polarity is recommended
- When there are invalid timing, Display appears black pattern.
  Synchronous Signal Defects and enter Auto Refresh for LCD Module Protection Mode.

8.2 Timing Definition

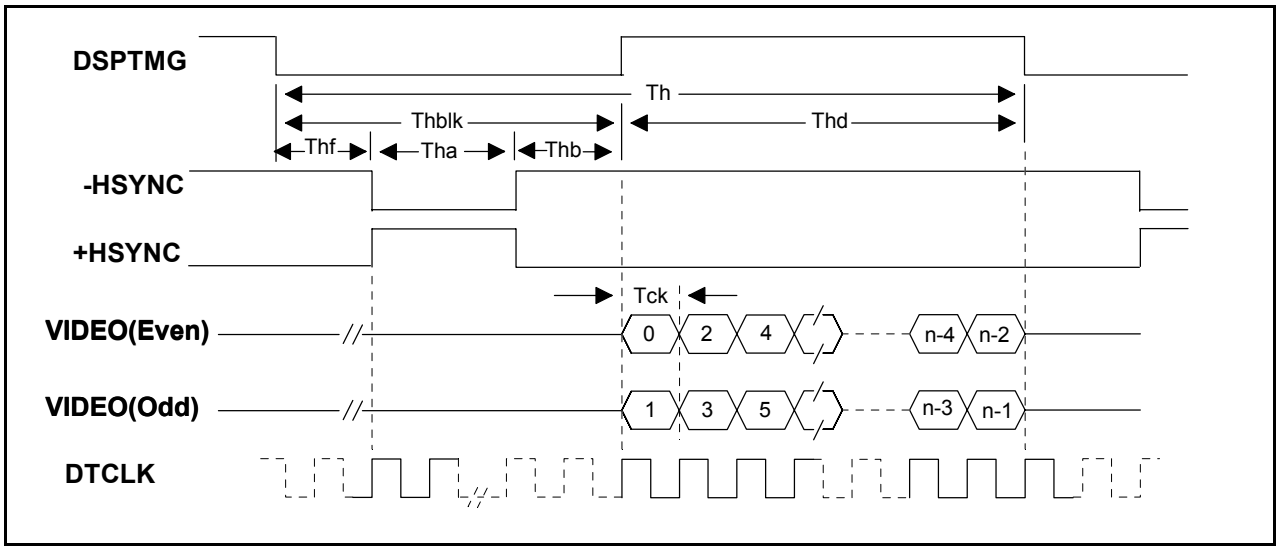
Vertical Timing

Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
2048 x 1536 at 50Hz (H line rate : 13.1 us)	0.248 ms (19 lines)	20.050 ms (1536 lines)	0.222 ms (17 lines)	20.298 ms (1555 lines)	0.013 ms (1 line)	0.013 ms (1 line)



Horizontal Timing

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
2048 x 1536 Dotclock : 164.250 MHz (82.125MHz x2)	0.584 us (96 dots)	12.469 us (2048 dots)	0.097 us (16 dots)	13.053 us (2144 dots)	0.097 us (16 dots)	0.390 us (64 dots)



9.0 Power Consumption

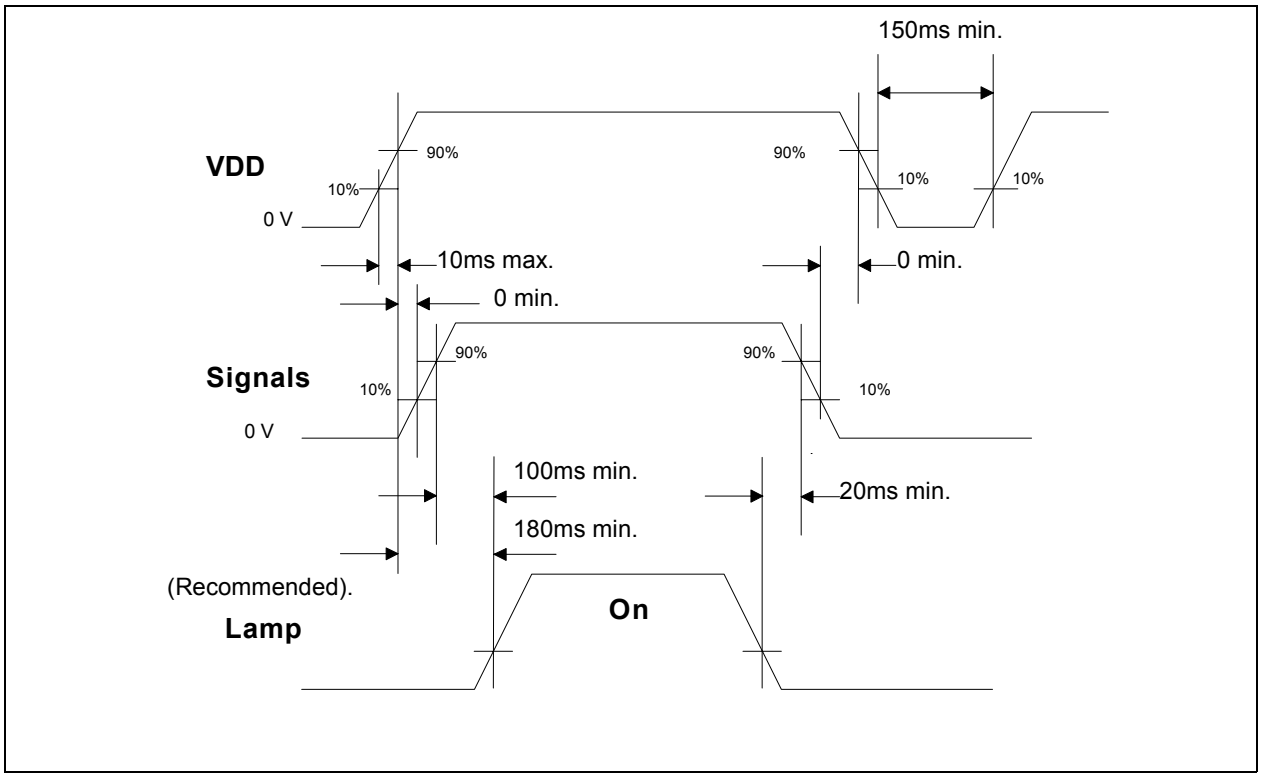
Input power specifications are as follows;

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	V	Load Capacitance 68uF
PDD	VDD Power			5.2	W	MAX Pattern **VDD=3.6V**
PDD	VDD Power		4.1		W	All White Pattern **VDD=3.3V**
IDD	VDD Current			1730	mA	MAX Pattern **VDD=3.0V**
IDD	VDD Current		1240		mA	All White Pattern **VDD=3.3V**
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

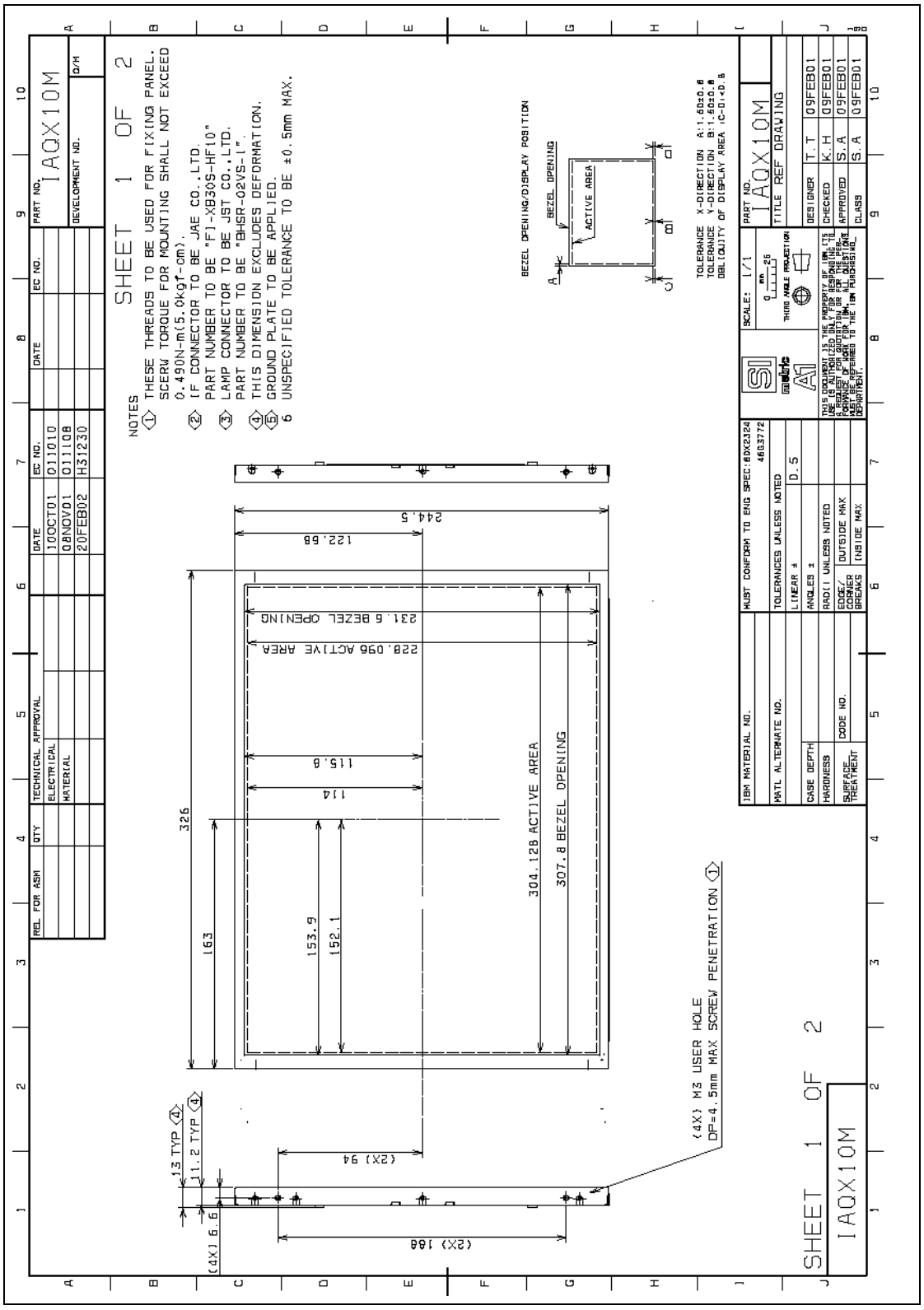
Note : Max Pattern:2 dot Vertical sub-pixel stripe.

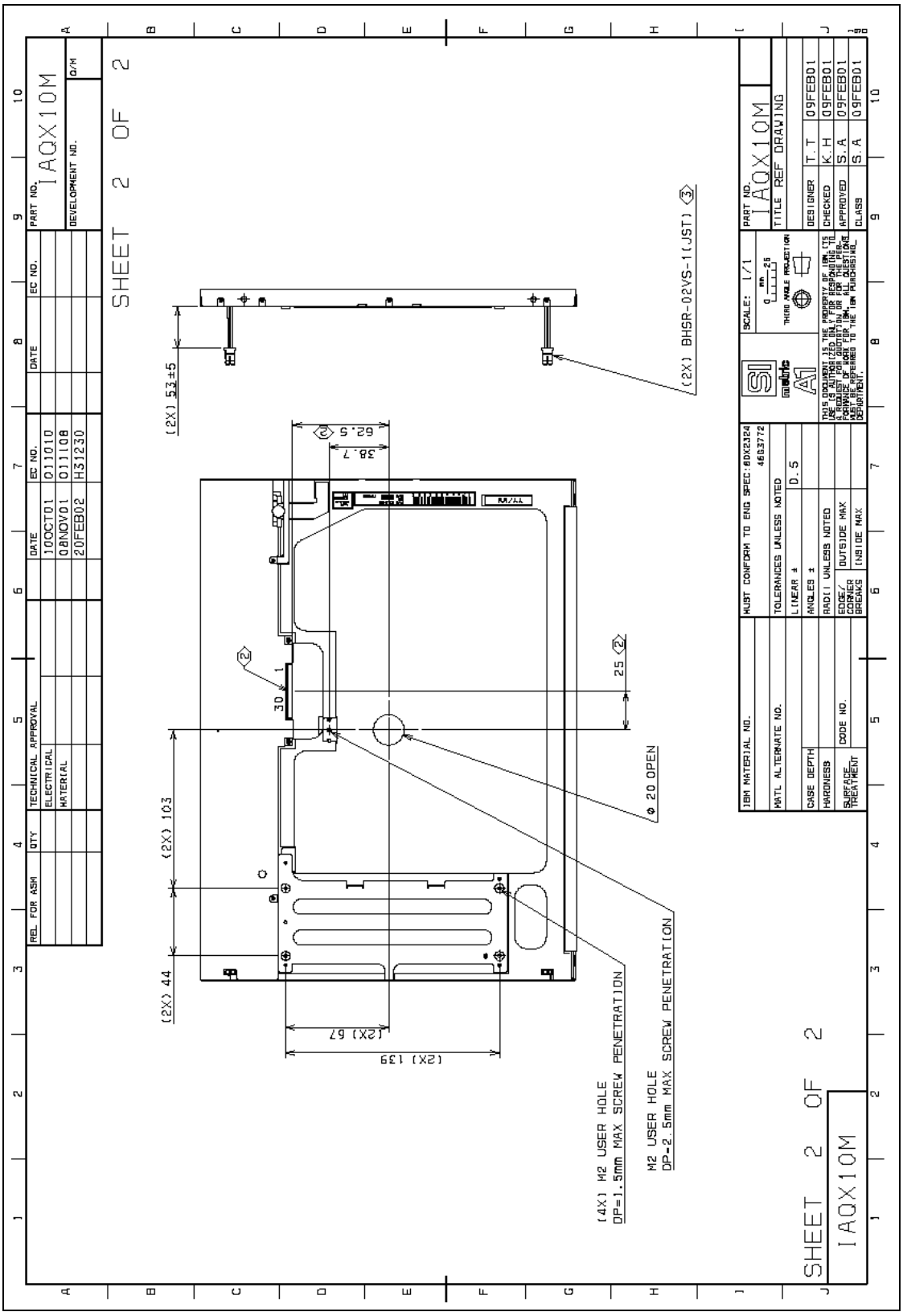
10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics





12.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

- This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment, CAN/CSA C22.2 No.950-00,UL60950, 3rd Edition, IEC 60950 (3rd. Ed.) and EN 60950 (3rd. Ed.), which would cover the component itself if submitted for Listing.
- CF Lamp circuit for this model should be supplied from Limited Current Circuit.
- The units are supplied by Limited Power Sources.
- The terminals and connectors are suitable for factory wiring only.
- The terminals and connectors have not been evaluated for field wiring.
- A suitable Electrical and Fire enclosure shall be provided.

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