M50944-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50944-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP.

This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50944-XXXSP and the M50944-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

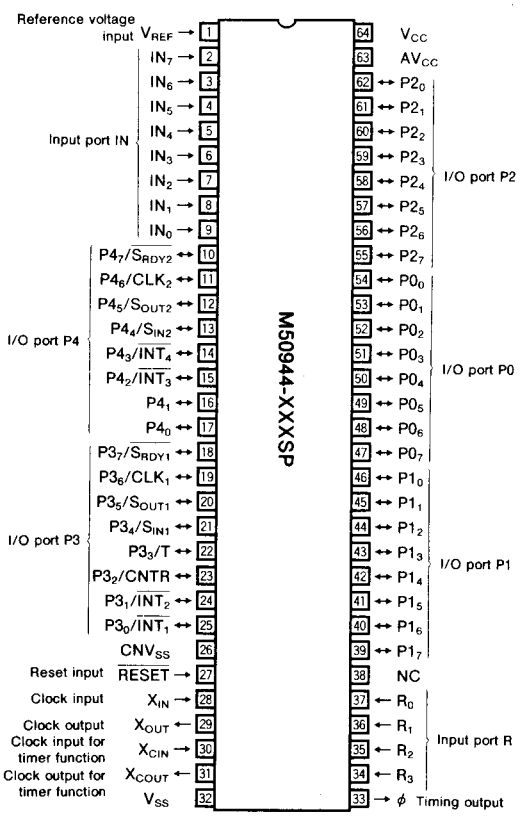
FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 12288 bytes
  RAM ..... 192 bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply $f(X_{IN})$=4MHz ..... 5V±10%
  $f(X_{IN})$=1MHz ..... 3~5.5V
- Power dissipation
  normal operation mode (at 4MHz frequency)
  ..... 15mW
  low-speed operation mode (at 32kHz frequency for clock function) 0.3mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 10 types, 5 vectors
- 8-bit timer ..... 7 (6 when used as serial I/O)
- Serial I/O ..... 8-bit×2
- Devider for serial I/O 1
- Interrupt request distinguish register ..... 8-bit×2
- Programmable I/O ports (Ports P3, P4) 16
- Middle-voltage programmable ports
  (Ports P0, P1, P2) 24
- Input ports (Ports R, IN) 12
- A-D converter 8-bit, 8-channel
- Two clock generator circuits
  (One is for main clock, the other is for clock function)

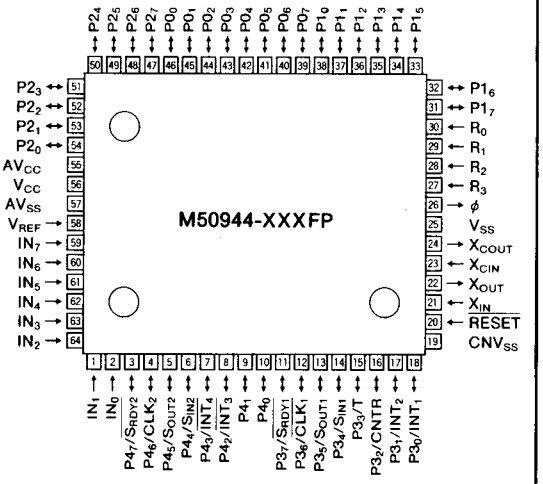
APPLICATION

Camera, Office automation equipment, VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



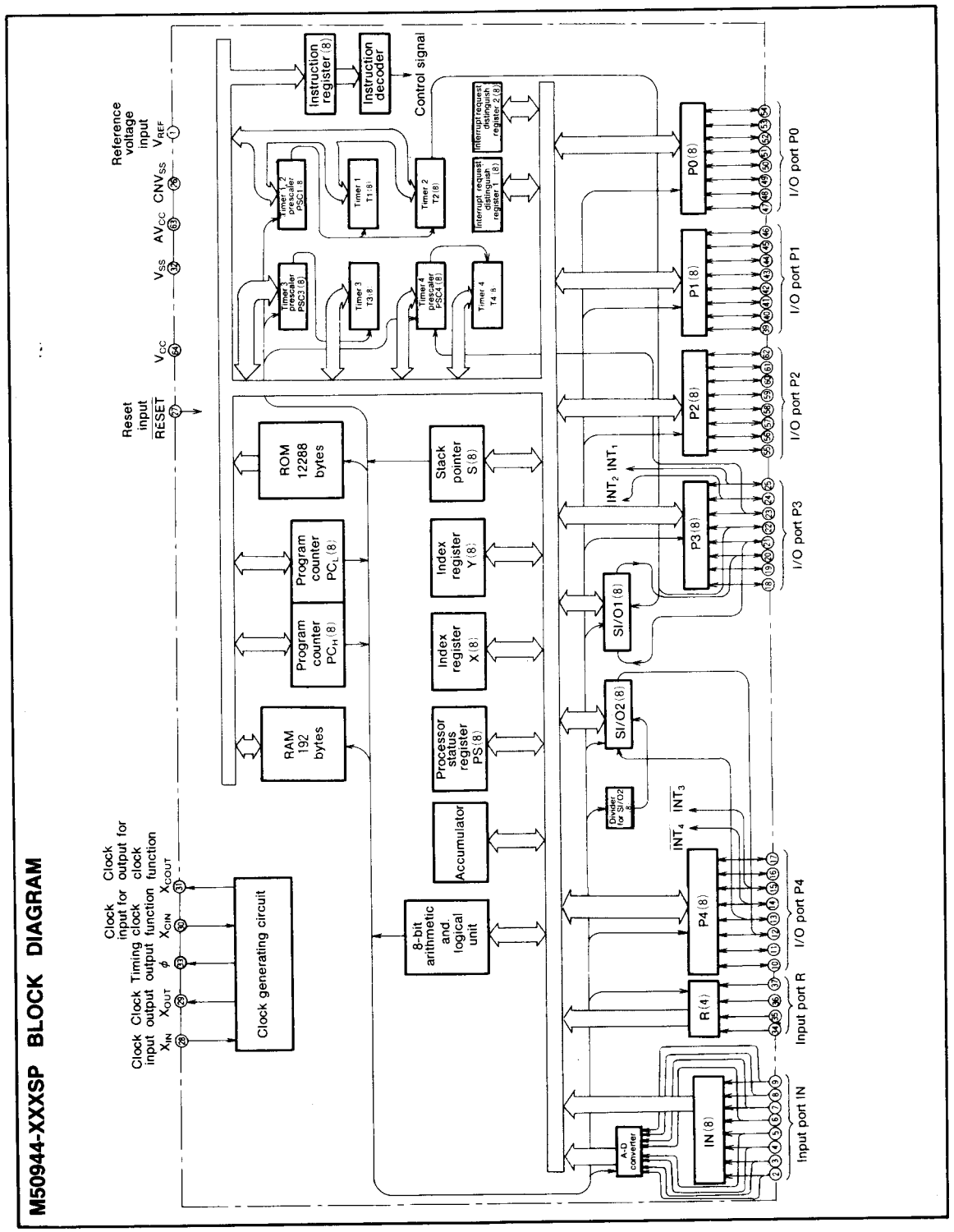
Outline 64P4B



Outline 64P6S

NC : No connection

M50944-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50944-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency).
Clock frequency			4.2MHz (main clock input), 32kHz (for clock function)
Memory size	ROM		12288bytes
	RAM		192bytes
Input/Output ports	P0, P1, P2, P3, P4	I/O	8-bit×5
	IN	Input	8-bit×1
	R	Input	4-bit×1
Serial I/O			8-bit×2
Timers			8-bit prescaler×3+8-bit timer×4 (3 when serial I/O is used)
Subroutine nesting			96 levels (max.)
Interrupt			Four external interrupts, Four timer interrupts (or three timers, one serial I/O)
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator).
Supply voltage			5V±10%(at f(X_{IN})=4MHz), 3.0~5.5V(at f(X_{IN})≤1.0MHz)
Power dissipation	At high-speed operation		15mW (at f(X_{IN})=4MHz).
	At low-speed operation		0.3mW (at f(X_{CIN})=32kHz).
	At stop mode		1μA (at clock stop)
Input/Output Characteristics	Input/Output voltage		5V (ports P3, P4)
			12V (ports P0, P1, P2)
	Output current		10mA (ports P0, P1, P2: middle voltage N-channel open drain output).
			−5~10mA (ports P3, P4: CMOS tri-state output)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M50944-XXXSP		64-pin shrink plastic molded DIP
	M50944-XXXFP		64-pin shrink plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% at f(X_{IN})=4MHz and 3.0~5.5V below f(X_{IN})=1.0MHz to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillatior to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-ch open drain. A pull-up transistor is built-in between the V_{CC} pin and this port.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port with CMOS output. The other functions are basically the same as port P0. $P3_0$, $P3_1$, $P3_2$ and $P3_3$ pins are in common with INT_2, INT_1, CNTR and T respectively. When serial I/O_1 is used, $P3_4$, $P3_5$, $P3_6$ and $P3_7$ work as S_{IN1}, S_{OUT1}, CLK1 and $\overline{S_{RDY1}}$ pin respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. $P4_2$ and $P4_3$ pins are in common with $\overline{INT_3}$ and $\overline{INT_4}$ respectively. When serial I/O_2 is used, $P4_4$, $P4_5$, $P4_6$ and $P4_7$ work as S_{IN2}, S_{OUT2}, CLK_2 and $\overline{S_{RDY2}}$ pin respectively.
R_0~R_3	Input port R	Input	Port R is a 4-bit input port.
IN_0~IN_7	Analog input port IN	Input	Port IN is the analog input pin to the A-D converter. It also has a dual function and works as a normal input port.
AV_{CC}, AV_{SS} (Note)	Voltage input for A-D		This is the power supply input pin for the A-D conveter.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D conveter.

Note. This pin is for flat package only.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50944-XXXSP is shown in Figure 1. Addresses $D000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 12288 bytes. Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (See interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses 0000_{16} to $00BF_{16}$ are assigned for the built-in RAM which consists of 192 bytes of static RAM. This RAM is used as the stack during subroutine calls and interrupts, in addition to data storage.

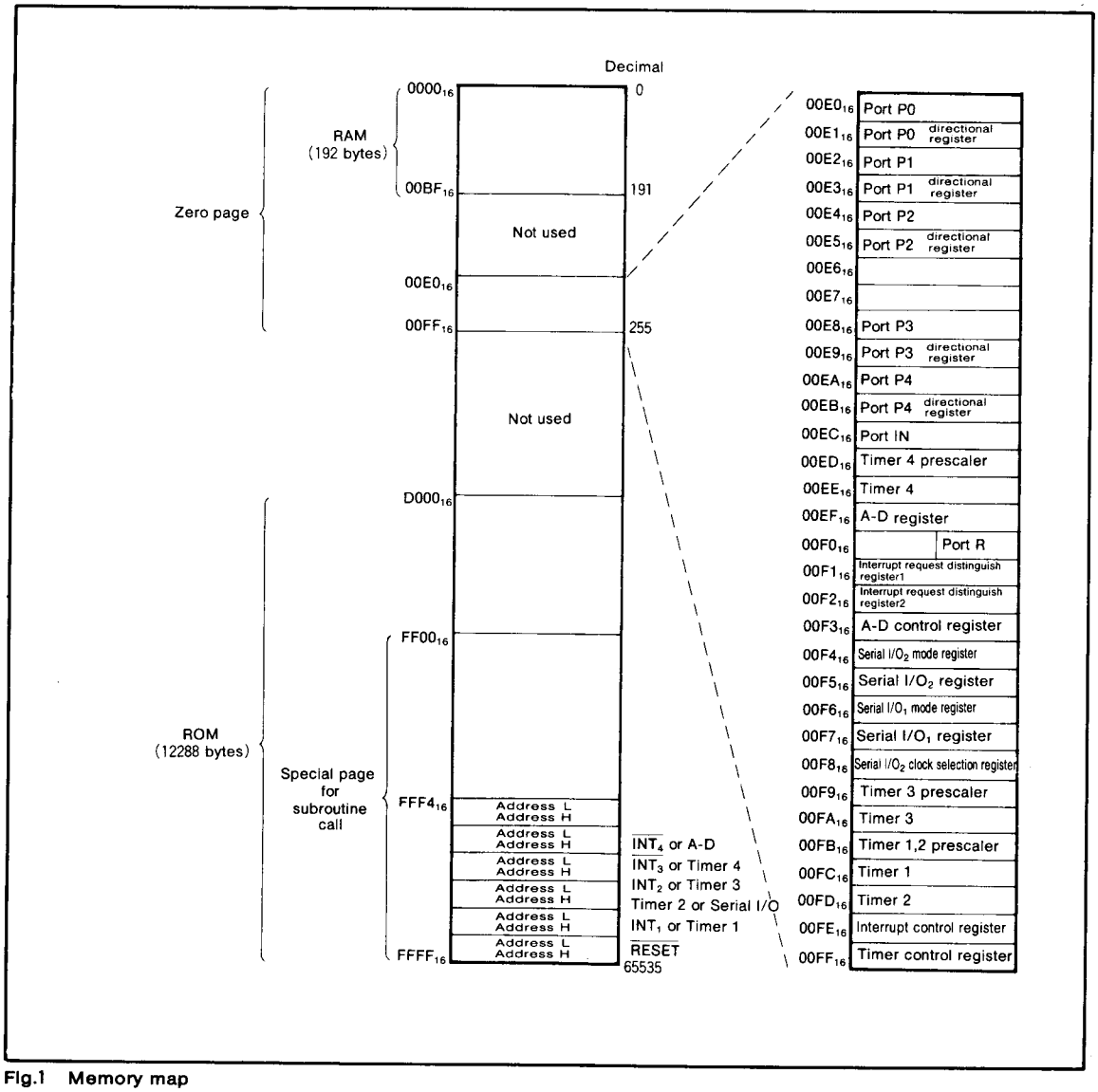


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., is executed mainly through the accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register. In the index regsiter X addressing mode, the value of the OPERAND added to the contents of the index register X specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGSITER Y (Y)

The index register Y is an 8-bit register. In the index register Y addressing mode, the value of the OPERAND added to the contents of the index register Y specifies the real address.

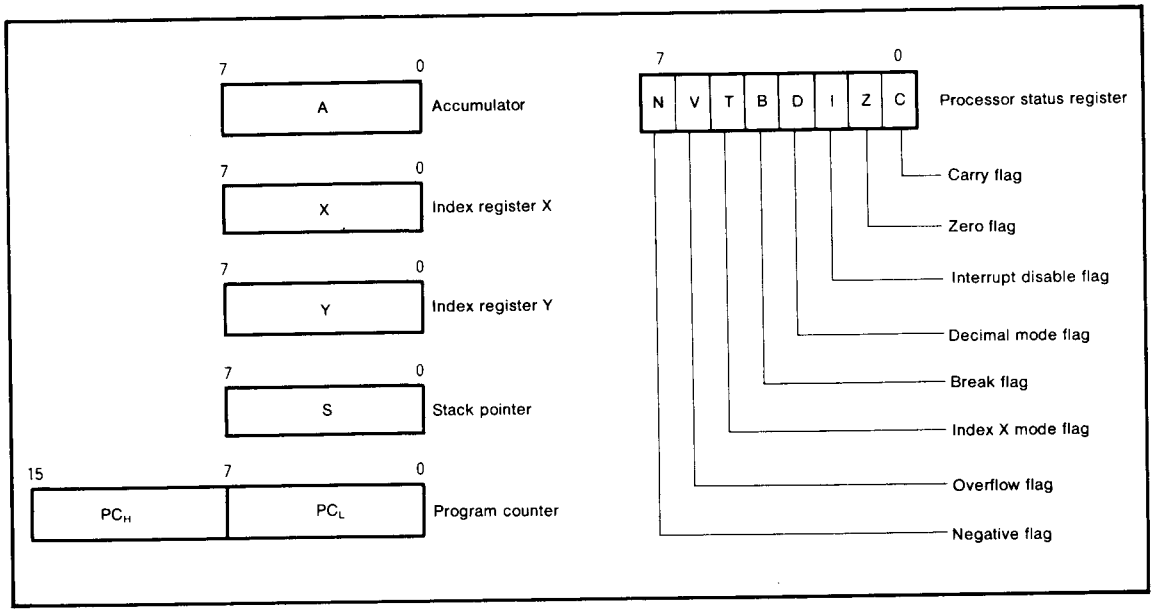


Fig.2 Register structure

STACK POINTER (S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed into the stack first, the stack pointer is decremented, and then the lower 8 bits of the program counter is pushed into the stack. Next the contents of the processor status register is pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is popped off the stack in reverse order from above.

The accumulator is never pushed into the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the accumulator to its previous value is accomplished by the Pop Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and popped to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the program counter is pushed into the stack. Therefore, any registers that should not be destroyed should be pushed into the stack manually. To return from a subroutine call, the RTS instruction is used.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The 8-bit PS is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic Logic Unit (ALU) immediately after an operation. It is also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "0". If the result is not zero, the zero flag will be set to "1".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt is accepted, this flag is automatically set to "1" to prevent from other interrupts until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the B flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the T flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the V flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the N flag. There are no instuctions for directly setting or resetting the N flag.

INTERRUPT

The M50944-XXXSP can be interrupted from ten sources; INT_1 or timer 1, timer 2 or serial I/O_1, INT_2 or timer 3, $\overline{INT_3}$ or timer 4, $\overline{INT_4}$ or A-D or BRK instruction. The value of bit 2 of the serial I/O_1 mode register (address $00F6_{16}$) determines whether the interrupt is from timer 2 or from serial I/O_1. When bit 2 is "1" the interrupt is from serial I/O_1, and when bit 2 is "0" the interrupt is from timer 2. Also, when bit 2 is "1", parts of port 3 are used for serial I/O_1. Bit 7 and bit 5 of the interrupt request distinguish regisrer 1 (address $00F1_{16}$) distinguish whether the interrupt request is from INT_1 pin or timer 1. When bit 7 is "1", the interrupt is requested from INT_1 pin and bit 5 is "1", the interrupt is requested from timer 1. Bit 3 and bit 1 of the interrupt request distinguish register 1 (address $00F1_{16}$) distinguish whether the interrupt request is from INT_1 pin or timer 1. When bit 3 is "1", the interrupt is requested from INT_2 pin and bit 1 is "1", the interrupt is requested from timer 3. Also, bit 7 and bit 5 or bit 3 and bit 1 of the interrupt request distinguish register 2 distinguish whether the interrupt request is from $\overline{INT_3}$ pin or timer 4 and $\overline{INT_4}$ or A-D, respectively.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt. When an interrupt is accepted, the contents of certain registers are pushed into specified locations, as discussed in the stack pointer section, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

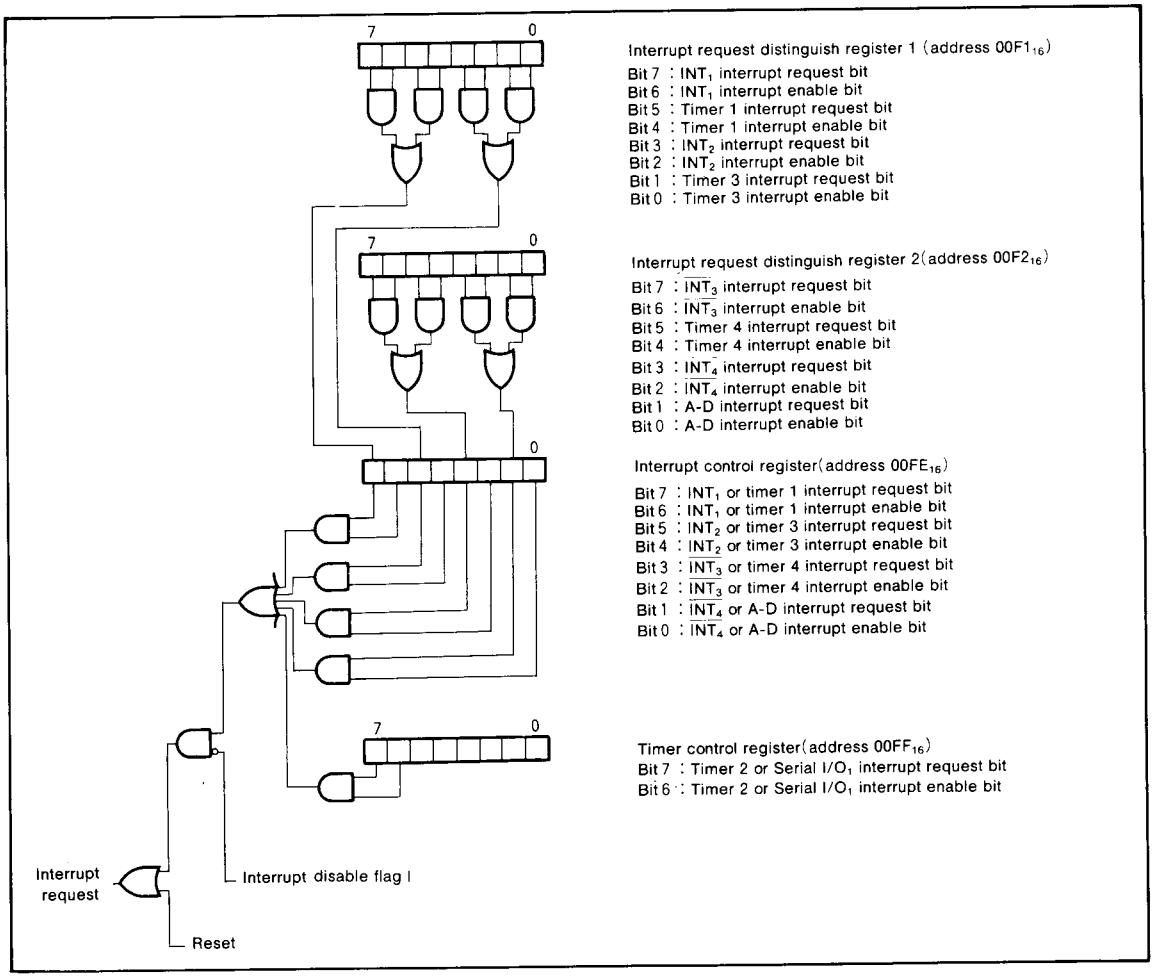


Fig. 3 Interrupt control

(1) When the level of INT_1, INT_2, $\overline{INT_3}$ or $\overline{INT_4}$ pin changed
(2) When the contents of timer 1, timer 2 (or the serial I/O_1 counter), or timer 4 goes to "0"

When the two interrupt requests, which are the same priority, are at the same sampling, the priority process is processed by interrupt request distinguish register 1 and 2.

These request bits can be reset by a program but can not be set. Since the BRK instruction interrupt and the A-D interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if A-D generated the interrupt.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$
INT_1 or timer 1	2	$FFFD_{16}$, $FFFC_{16}$
Timer 2 or serial I/O_1	3	$FFFB_{16}$, $FFFA_{16}$
INT_2 or timer 3	4	$FFF9_{16}$, $FFF8_{16}$
INT_3 or timer 4	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{INT_4}$ or A-D(BRK)	6	$FFF5_{16}$, $FFF4_{16}$

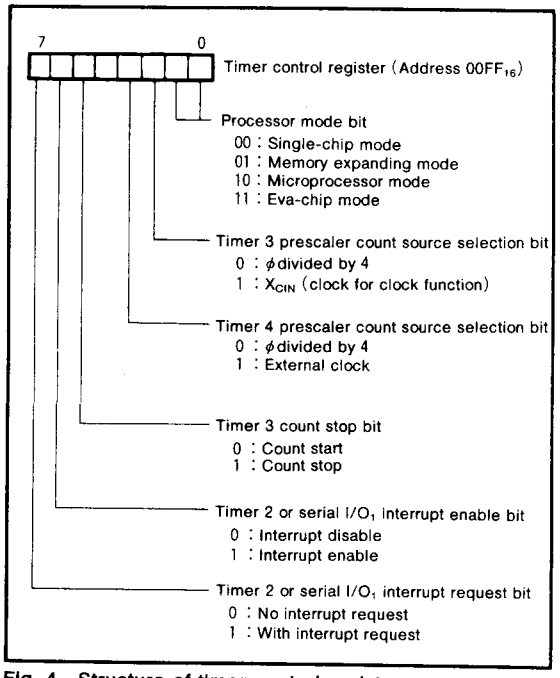


Fig. 4 Structure of timer control register

TIMER

The M50944-XXXSP has seven timers; timer 1, 2 prescaler, timer 1, timer 2, timer 3 prescaler, timer 3, timer 4 prescaler and timer 4. Interrupt from timer 2 cannot be used at using serial I/O (see serial I/O section).

A block diagram of timer 1 through 3 and timer 4 is shown in Figure 5 and Figure 6 respectively. The count source for timer 3 prescaler and timer 4 prescaler can be selected by using bit 2 and 3 of the timer control register (addres $00FF_{16}$), as shown in Figure 4.

All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is 1/(n +1), where n is the contents of timer latch.

Each timer has interrupt generating functions. The timer interrupt request bits (in the interrupt request distinguish register 1, the interrupt request distinguish register 2, the interrupt control register and the timer control register) is set at the next count pulse after the timer reaches "0". The interrupt distinguish register 1 and 2 are located at addresses $00F1_{16}$ and $00F2_{16}$ respectively.

The starting and stopping of timer 3 prescaler is controlled by bit 5 of the timer control register. If the corresponding bit is "0", the timer starts counting, when the corresponding bit is "1", the timer stops.

After a STP instruction is executed, timer 3 prescaler, timer 3, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 of the timer control register). This state is canceled if timer 3 interrupt request bit is set to "1", or if the system is reset, and it becomes a former count source decided with bit 2 of the timer control register. Before the STP instruction is executed, bit 5 of the timer control register must be set to "0", bit 0 of the interrupt request distinguish register 1 must be set to "1", bit 1 of the interrupt request distinguish register 1 must be set to "0", bit 4 of the interrupt control register must be set to "0" and bit 5 of the interrupt control register must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

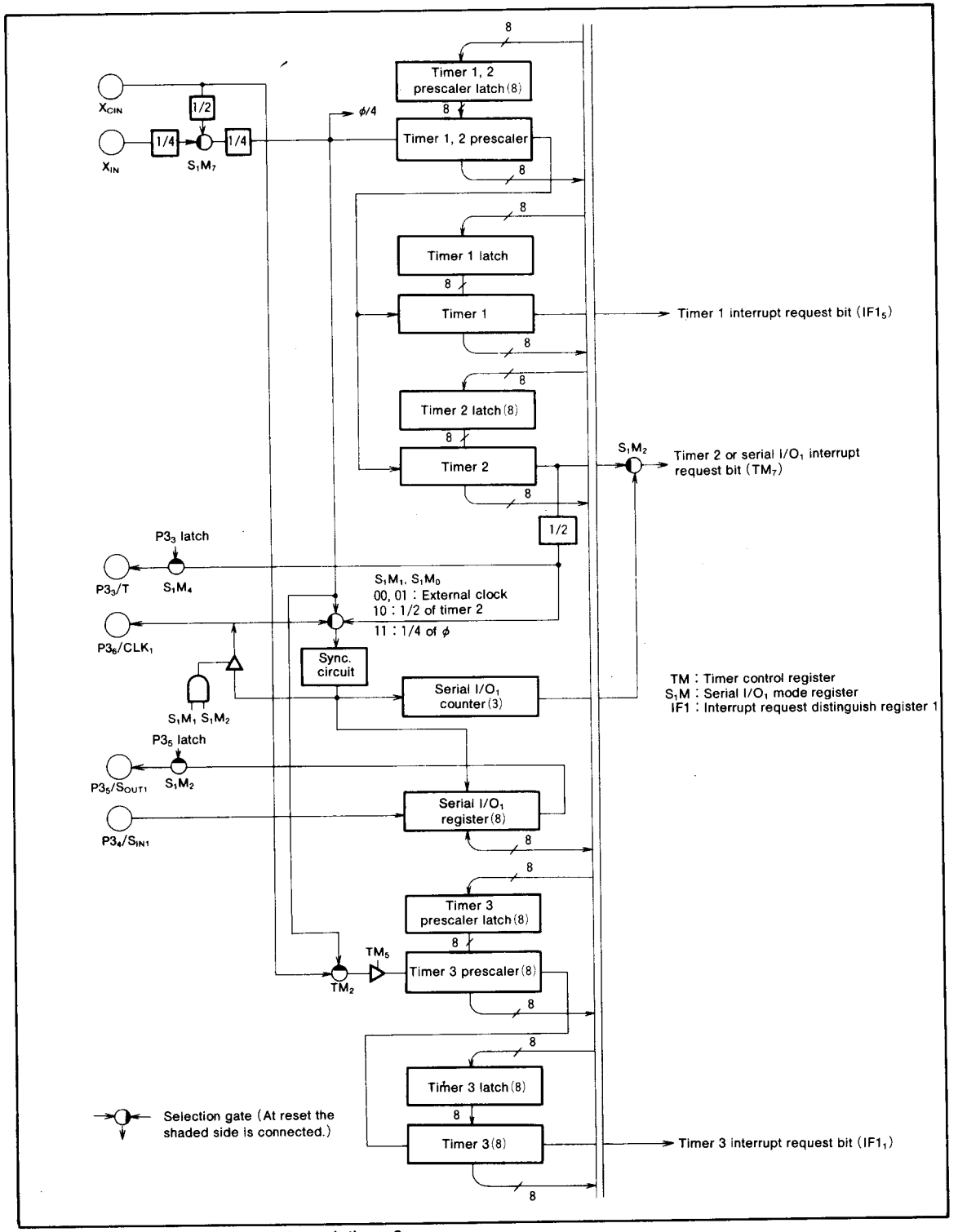


Fig. 5 Block diagram of timer 1 through timer 3

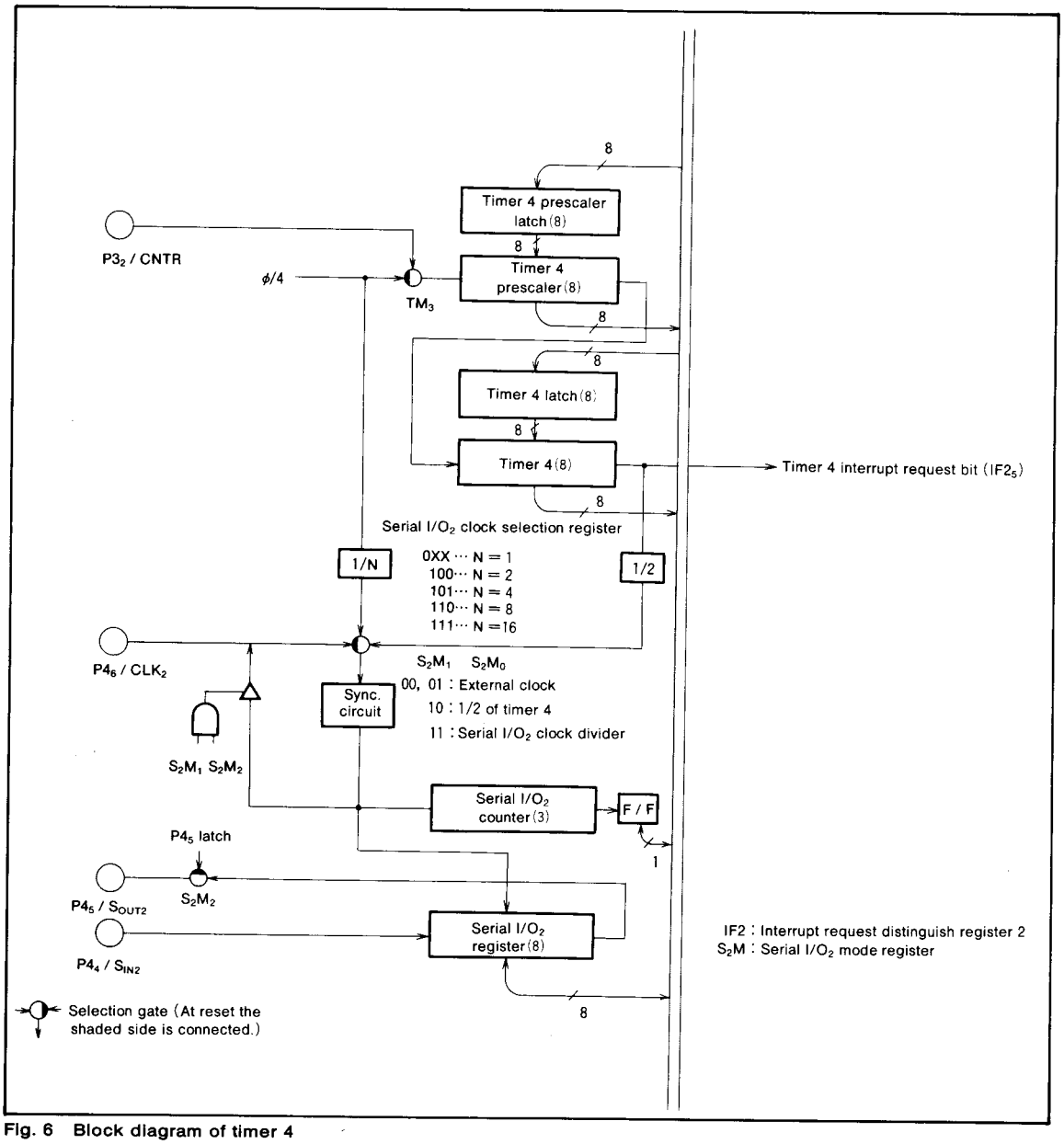


Fig. 6 Block diagram of timer 4

SERIAL I/O$_1$

A block diagram of the serial I/O$_1$ is shown in Figure 7. In the serial I/O$_1$ mode, the receive ready signal ($\overline{S_{RDY1}}$), synchronous input/output clock (CLK$_1$), and the serial I/O$_1$ (S_{OUT1}, S_{IN1}) pins are used as P3$_7$, P3$_6$, P3$_5$, and P3$_4$, respectively.

The serial I/O$_1$ mode register (address 00F6$_{16}$) is an 8-bit register. Bits 1 and 0 of this register are used to select a synchronous clock source. When these bits are [00] or [01], an external clock from P3$_6$ is selected. When these bits are [10], the overflow signal (from timer 2) divided by two becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", P3$_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous is selected, the clock is output from P3$_6$. If an external synchronous clock is selected, the clock is input to P3$_6$. And P3$_5$ will be a serial output and P3$_4$ will be a serial input. To use P3$_4$ as a serial input, set the directional register bit which corresponds to P3$_4$ to "0". For more information on the directional register, refer to the I/O pin section.

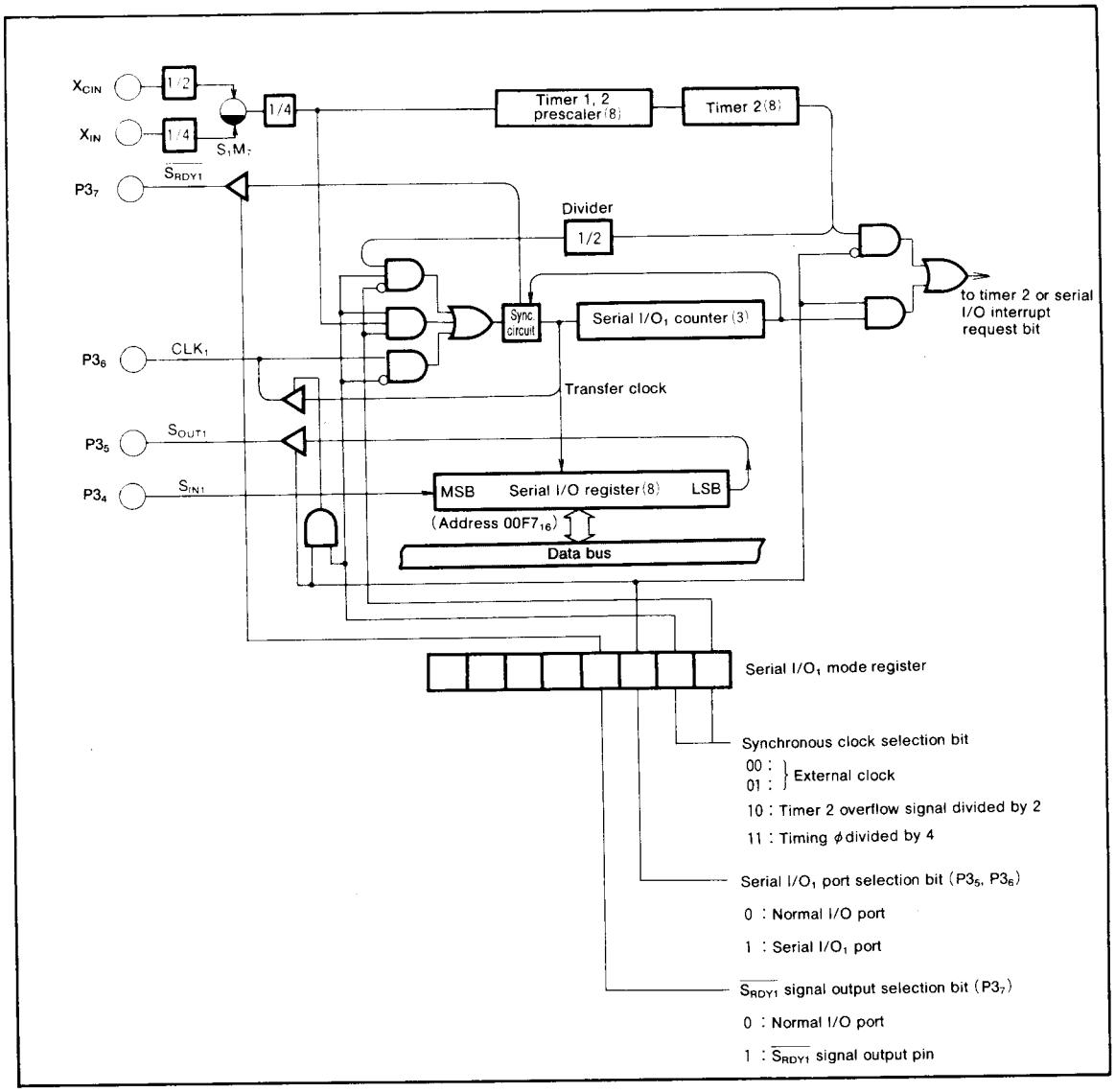


Fig. 7 Block diagram of serial I/O

To use the serial I/O_1, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O_1 counter instead of timer 1. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3 = "1", $\overline{S_{RDY1}}$) or used as a normal I/O pin (bit 3="0").

The function of the serial I/O_1 differs depending on the clock source; external clock or internal clock.

Internal Clock — The $\overline{S_{RDY1}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_1 register. After the falling edge of the write signal, the $\overline{S_{RDY1}}$ signal becomes low signaling that the M50944-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY1}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_1 counter is set to 7 when data is stored in the serial I/O_1 register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O_1 register will be shifted 1 bit. Data is output starting with the LSB. After the transfter clock has counted 8 times, the serial I/O_1 register will be empty and the transfter clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock — If an external clock is used, the interrupt request will be set after the transfter clock has counted 8 times but the transfter clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 8, and connections between two M50944-XXXSPs' are shown in Figure 9.

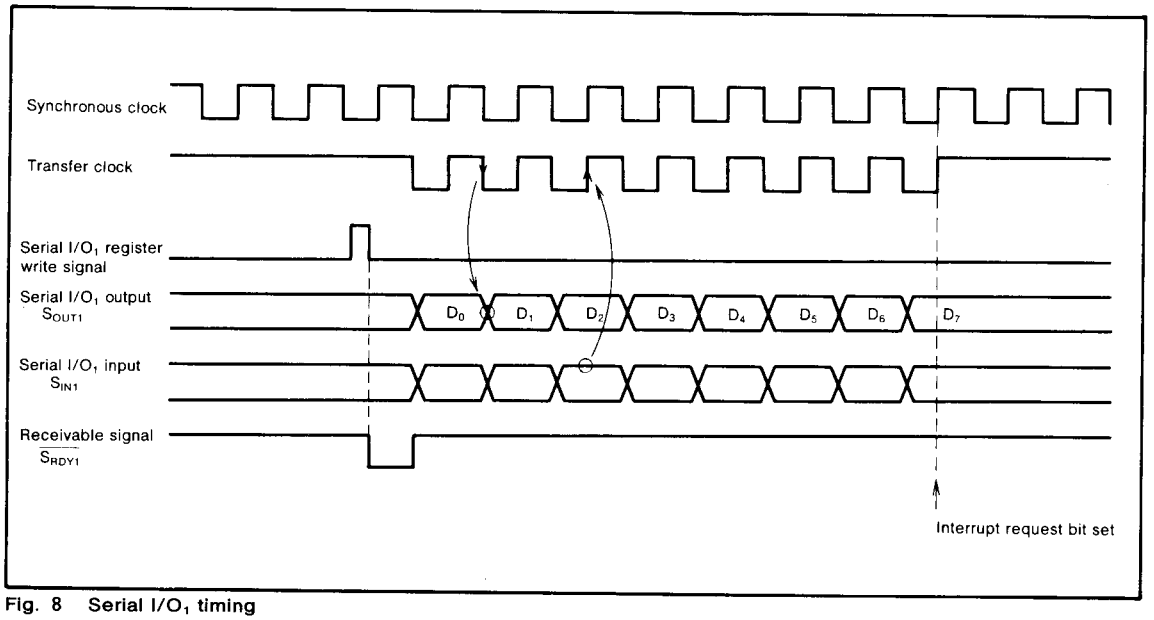


Fig. 8 Serial I/O_1 timing

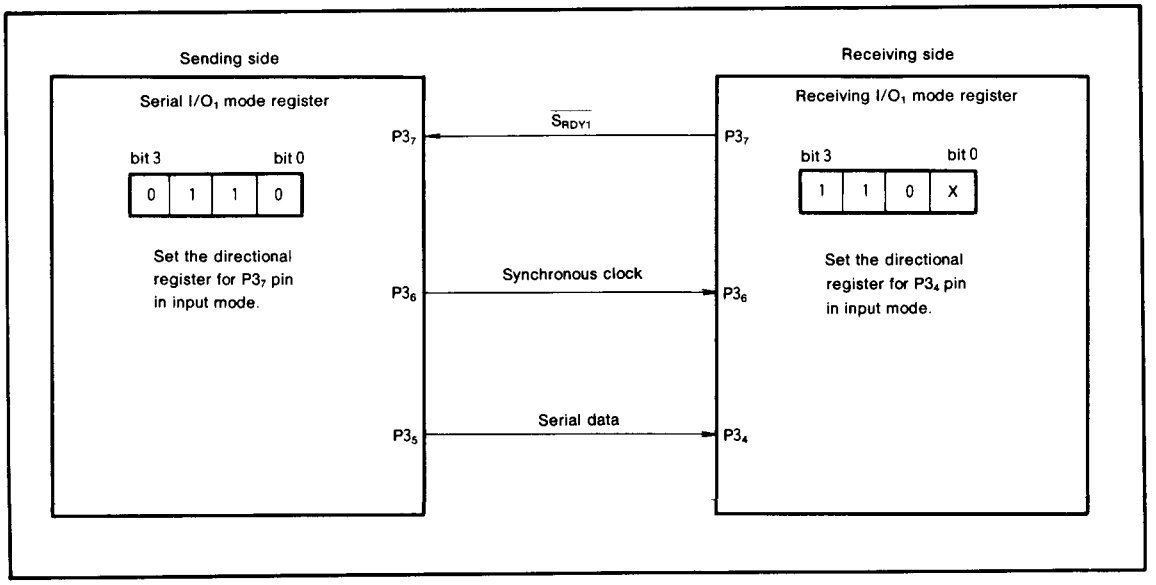


Fig. 9 Example of serial I/O$_1$ connection

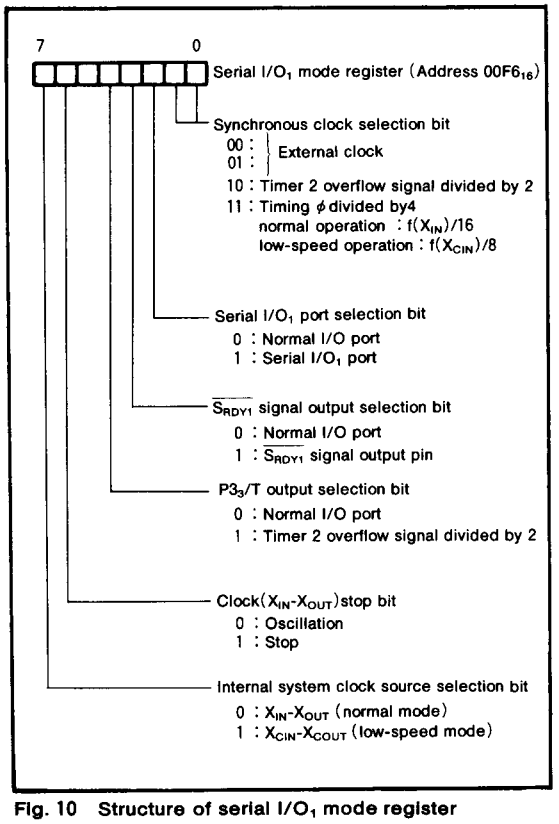


Fig. 10 Structure of serial I/O$_1$ mode register

SERIAL I/O_2

A block diagram of the serial I/O_2 is shown in Figure 11.

In the serial I/O_2 mode the receive ready signal ($\overline{S_{RDY2}}$), synchronous input /output clock (CLK_2), and the serial I/O_2 pins (S_{OUT2}, S_{IN2}) are used as $P4_7$, $P4_6$, $P4_5$, and $P4_4$, respectively.

The serial I/O_2 mode register (address $00F4_{16}$) is an 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P4_6$ is selected. When these bits are [10], the overflow signal from timer 4, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the timing ϕ divided by 4, becomes the clock.

Bit 2 and 3 decide whether parts of P4 will be used as a serial I/O_2 or not. When bit 2 is a "1", $P4_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P4_6$. If an external synchronous clock is selected, the clock is input to $P4_6$ and $P4_5$ will be a serial output and $P4_4$ will be a serial input. To use $P4_4$ as a serial input, set the directional register bit which corresponds to $P4_4$ to "0". For more information on the directional register, refer to the I/O pin section.

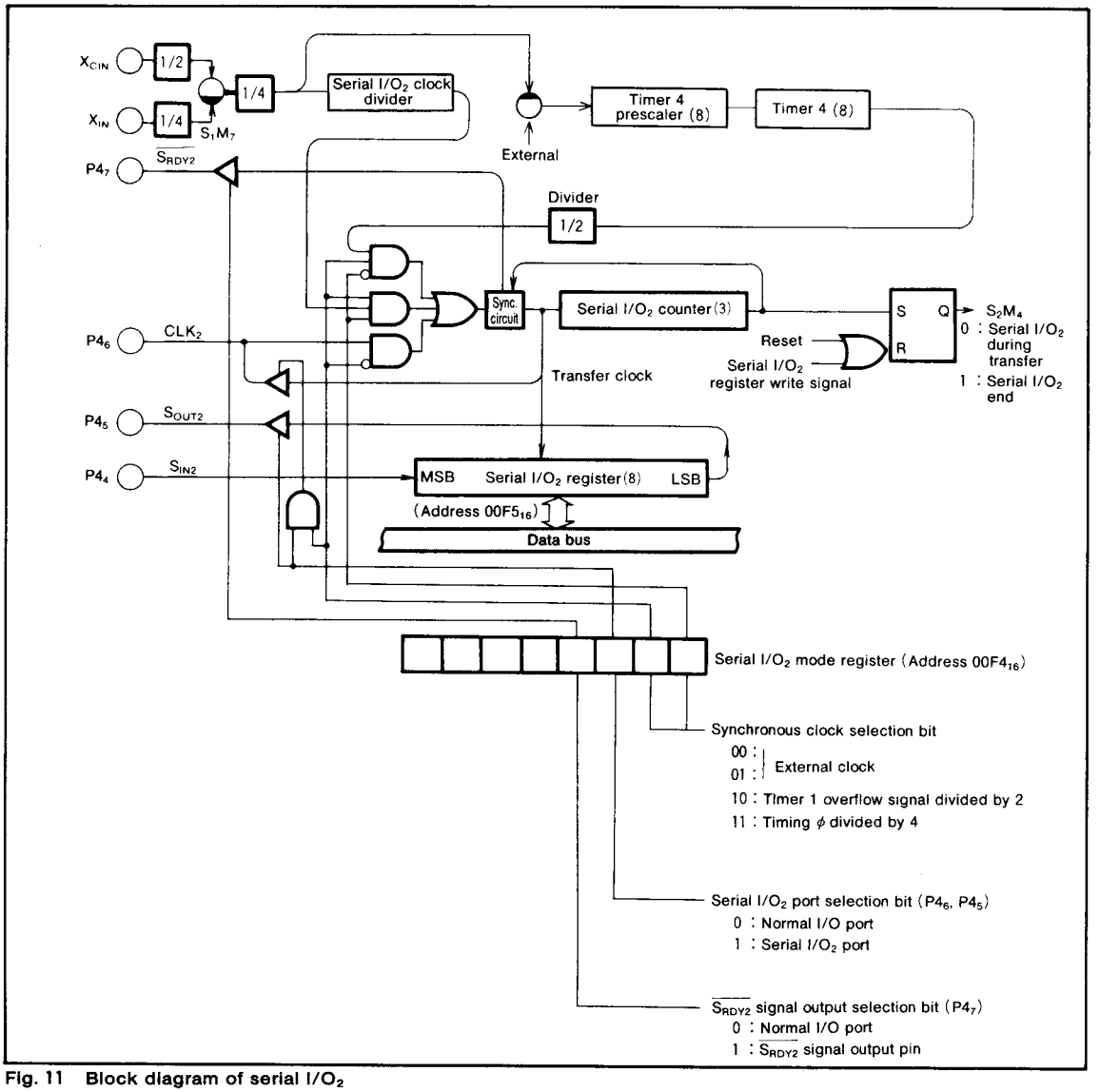


Fig. 11 Block diagram of serial I/O_2

To use the serial I/O_2, bit 2 needs to be set to "1", if it is "0" $P4_6$ will function as a normal I/O. Bit 3 determines if $P4_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY2}}$) or used as normal I/O pin (bit 3=0). The serial I/O_2 function is discussed below. The function of the serial I/O_2 differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY2}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_2 register (address $00F5_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY2}}$ signal becomes low signaling that the M50944-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY2}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_2 counter is set to 7 when data is stored in the serial I/O_2 register. At each falling edge of the transfer clock, serial data is output to $P4_5$. During the rising edge of this clock, data can be input from $P4_4$ and the data in the serial I/O_2 register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O_2 register will be empty and the transfer clock will remain at a high level. At this time the serial I/O_2 end bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 12.

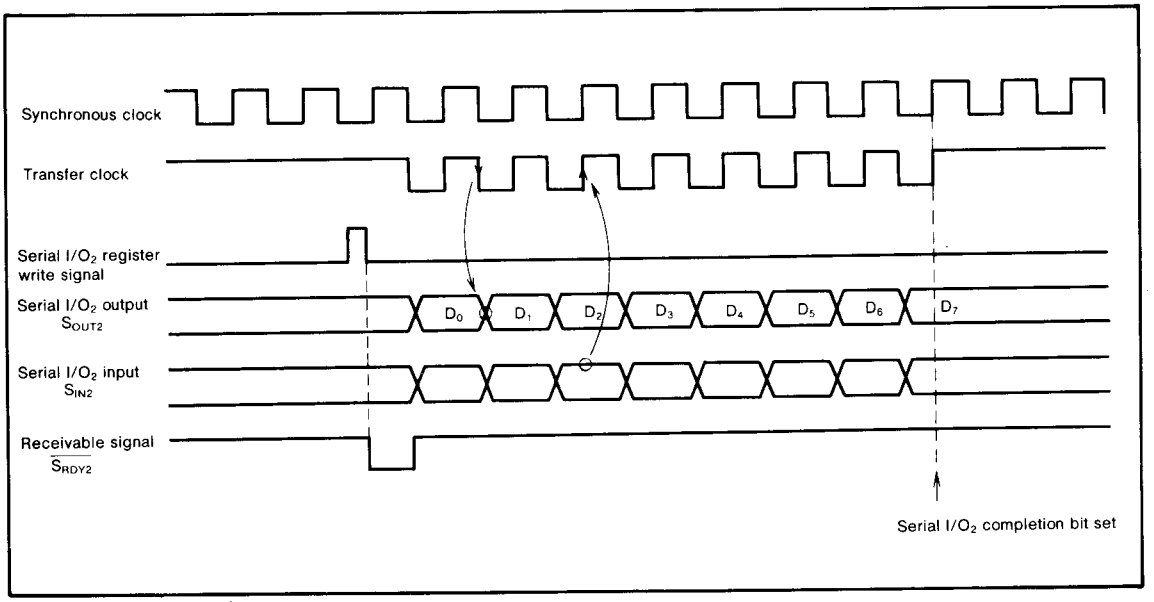


Fig. 12 Serial I/O_2 timing

A block diagram of clock divider for serial I/O_2 is shown in Figure 13. Bit 2, 1 and 0 of the serial I/O_2 clock selection register (address $00F8_{16}$) determine the dividing ratio of the serial I/O_2 clock. When these bits are [0XX], the timing ϕ divided by 4 is selected. When these bits are [100], [101], [110] and [111], the timing ϕ divided by 8, 16, 32 and 64 are selected respectively.

To use the clock divider for serial I/O_2, both bit 1 and bit 0 of the serial I/O_2 mode register (address $00F4_{16}$) need to be set to "1".

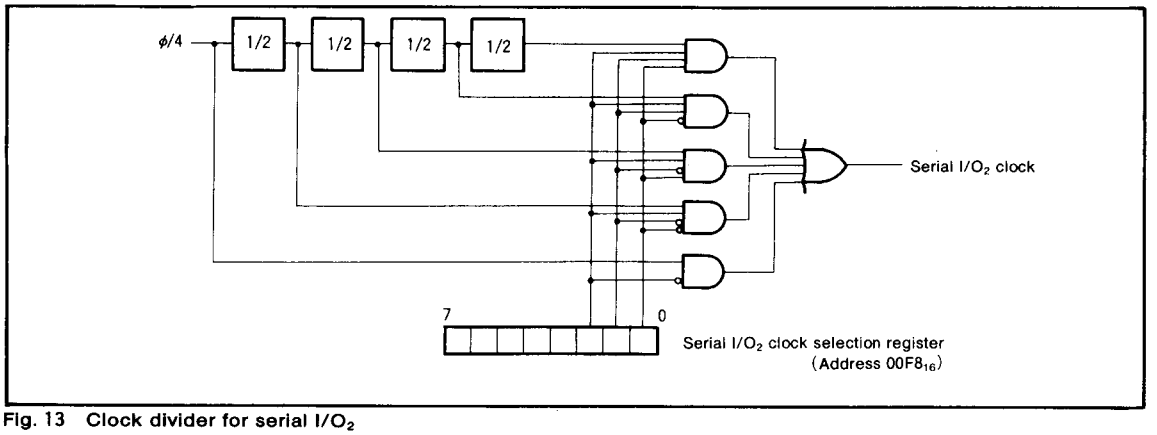


Fig. 13 Clock divider for serial I/O_2

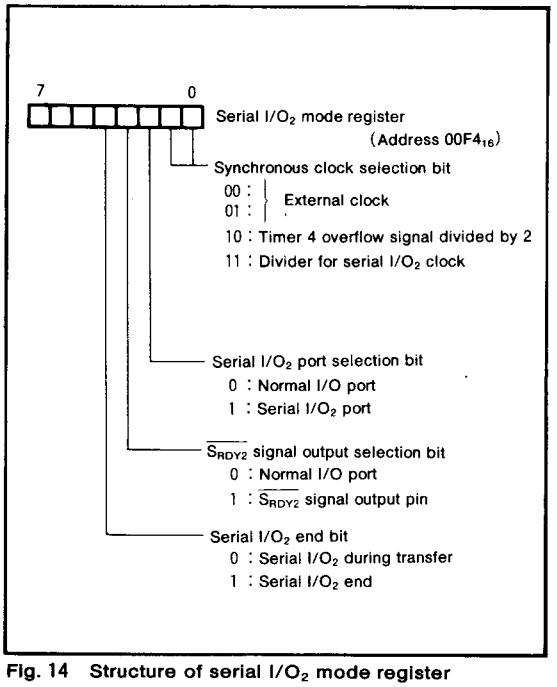


Fig. 14 Structure of serial I/O_2 mode register

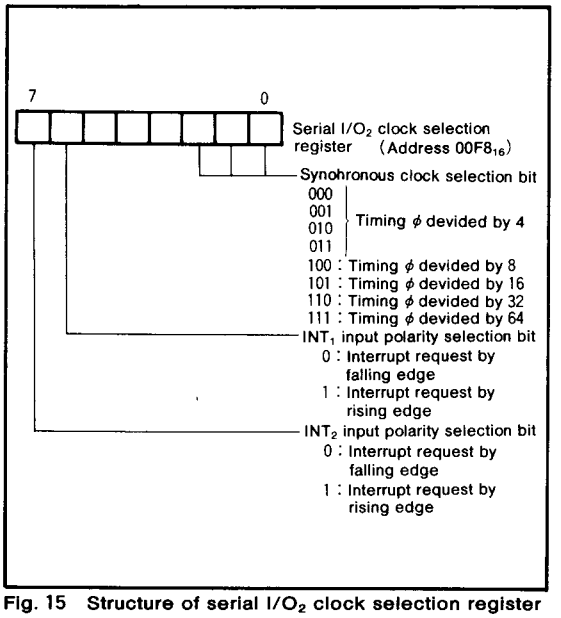


Fig. 15 Structure of serial I/O_2 clock selection register

A-D CONVERTER

The A-D converter circuit is shown in Figure 17. The analog input ports of the A-D converter ($IN_0 \sim IN_7$) are in common with the input ports of the data bus.

The 6-bit A-D control register is located at address $00F3_{16}$. One of the eight analog inputs is selected by bits 0, 1 and 2 of this register.

A-D conversion is accomplished by first selecting the analog channel (bit 0, 1 and 2) to be converted. The conversion is started when dummy data is written into address $00EF_{16}$. When the conversion is finished, an interrupt is generated by the A-D and the digital data can be read from the A-D register (address $00EF_{16}$). The end of the conversion is determined by either the A-D conversion end bit (bit 5 of the A-D control regiser) or an A-D interrupt request bit.

The A-D conversion can also be programmed for high or low speed conversions. This is accomplished by using the A-D conversion speed switch bit (bit 4 of the A-D control register). For more information on the electrical characteristics of the high and low speed conversions, refer to the electrical characteristics section.

Port IN can also be used as an input port by reading data into address $00EC_{16}$. However, this cannot be done during A-D conversions.

The A-D control register is shown in Figure 16.

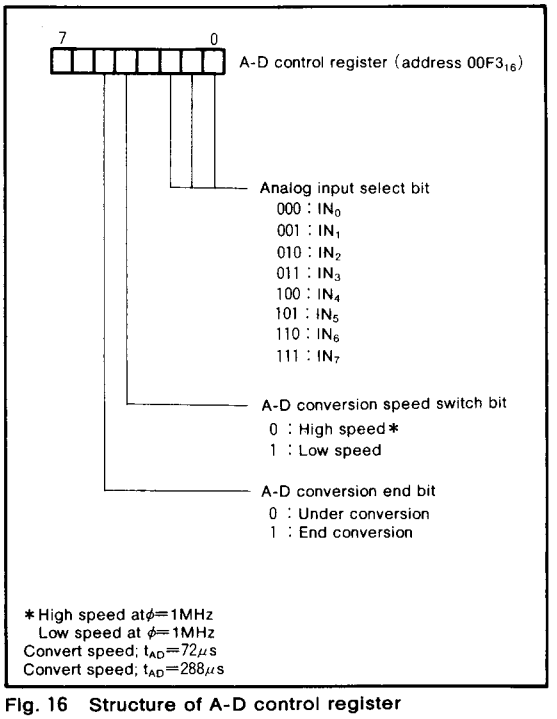


Fig. 16 Structure of A-D control register

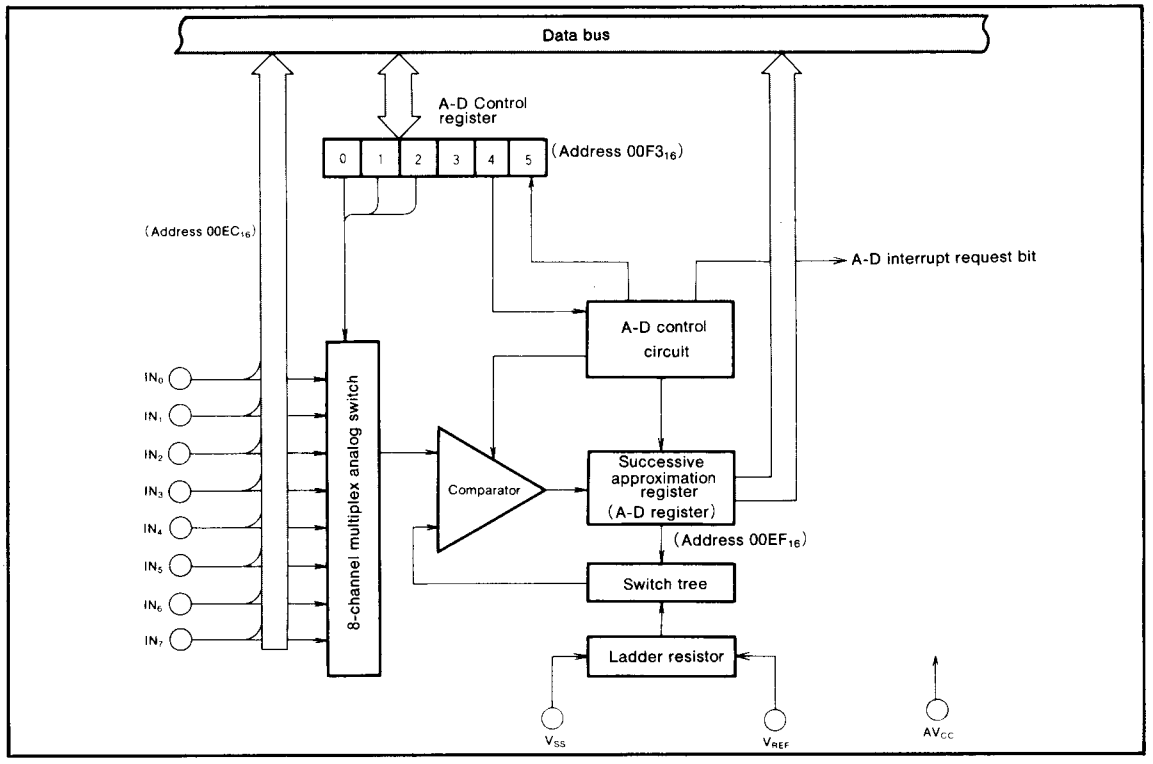


Fig. 17 A-D conversion circuit

RESET CIRCUIT

The M50944-XXXSP is reset according to the sequence shown in Figure 20. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 18.

An example of the reset circuit is shown in Figure 19.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

		Address	
(1)	Port P0 directional register	(D0) ($E1_{16}$) ···	00_{16}
(2)	Port P1 directional register	(D1) ($E3_{16}$) ···	00_{16}
(3)	Port P2 directional register	(D2) ($E5_{16}$) ···	00_{16}
(4)	Port P3 directional register	(D3) ($E9_{16}$) ···	00_{16}
(5)	Port P4 directional register	(D4) (EB_{16}) ···	00_{16}
(6)	Serial I/O_1 mode register	(S_1M)($F6_{16}$) ···	* * 0 0 0 0 0
(7)	Serial I/O_2 mode register	(S_2M)($F4_{16}$) ···	0 0 0 0 0
(8)	Serial I/O_2 clock selection register	($F6_{16}$)	0 0 0 0 0
(9)	A-D control register	($F3_{16}$)	1 0 0 0 0
(10)	Interrupt request distinguish register 1	(IF1)($F1_{16}$)	00_{16}
(11)	Interrupt request distinguish register 2	(IF2)($F2_{16}$) ···	00_{16}
(12)	Interrupt control register	(IM)(FF_{16}) ···	00_{16}
(13)	Timer control register	(TM)(FE_{16}) ···	00_{16}
(14)	Interrupt disable flag for processor status register	(PS) ···	1
(15)	Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
		(PC_L) ···	Contents of address $FFFE_{16}$

Since the contents both registers other than those listed above (Inclouding timer 1, timer 2, timer 3, and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

Note : * means mask option

Fig. 18 Internal state of microcomputer at reset

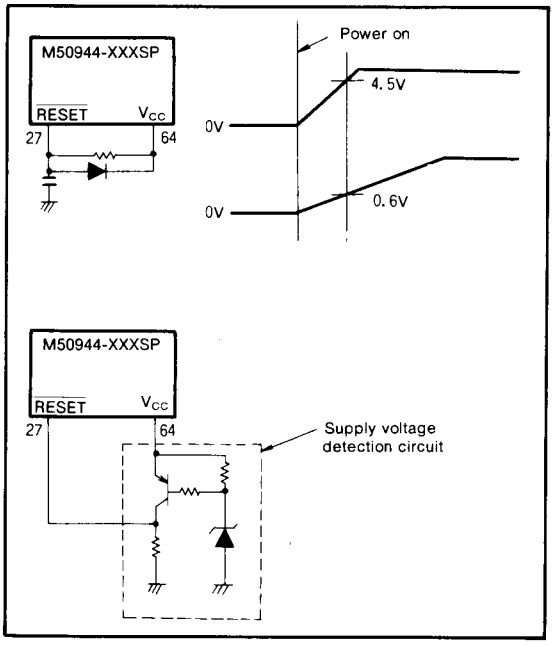


Fig. 19 Example of reset circuit

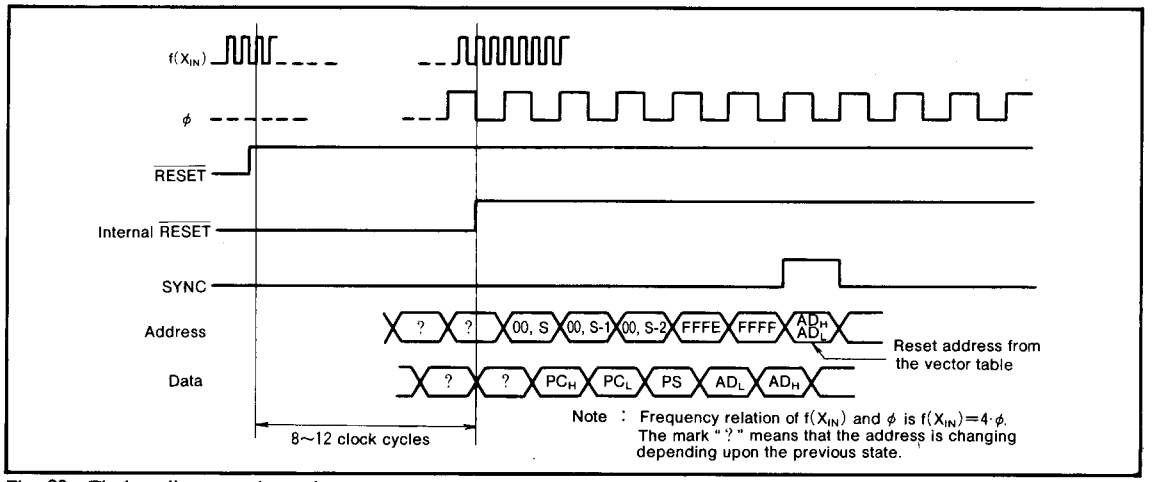


Fig. 20 Timing diagram at reset

MITSUBISHI ELECTRIC

I/O PORTS

(1) Port P0

Port P0 is an 8-bit output port with N-channel open drain and high voltage output. Each pin has a pull-up transistor option. As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$.

Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the high impedance state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

Depending on the status of the processor status register (bit 0 and bit 1 of address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode section.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode section.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's. For more details, see the processor mode section.

(4) Port P3

Port P3 is an 8-bit I/O port having CMOS output. Each pin is shared with serial I/O_1, timer overflow and external interrupt input functions. These functions remain the same even if the device is used in other modes.

(5) Port P4

Port P4 is an 8-bit I/O 'port with CMOS outputs. Each pin is shared with serial I/O_2, and external interrupt input functions. During all modes except single-chip mode, $P4_1$ and $P4_0$ function as both SYNC and $R/\overline{W}$ outputs as well as I/O ports (see processor mode section).

(6) Port R

Port R is a 4-bit input port.

(7) Port IN

Port IN is an 8-bit input port to the A-D converter. It can also be used as an input port by reading the input data into address $00EC_{16}$. However, this port cannot be read during A-D conversion.

(8) Clock ϕ output pin

This is the timing output pin. When selected the main clock (X_{IN}-X_{OUT}) as the internal system clock, the clock frequency divided by four is outputed. However, when selected the clock for clock function (X_{CIN}-X_{COUT}), the clock frequency divided by two is outputed.

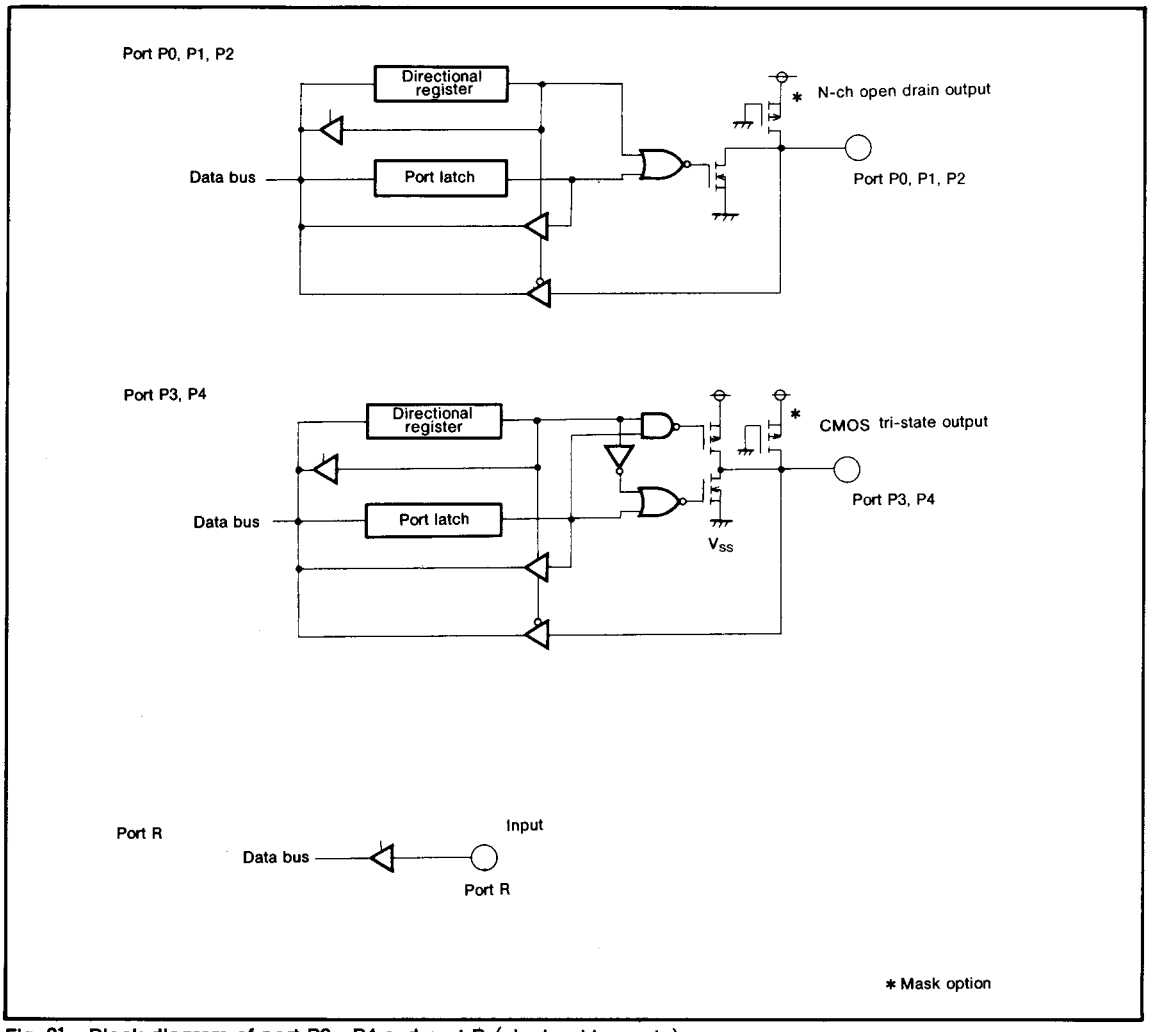


Fig. 21 Block diagram of port P0~P4 and port R (single-chip mode)

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 of address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, P0～P2 and P4 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports. Figure 23 shows the functions of ports P0～P2, and P4 corresponding to each mode.

The memory map of the single-chip mode is illustrated in Figure 1, and the other modes are shown in Figure 22. By connecting the CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode regsiter. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

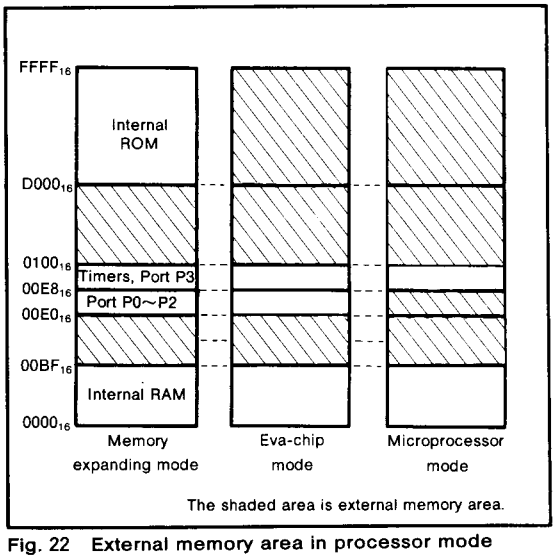


Fig. 22 External memory area in processor mode

(1) Single-chip mode (00)
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P4 will work as original I/O ports.

(2) Memory expanding mode (01)
The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.
The lower 8 bits of address data for port P0 is output when ϕ goes to the "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.
Port P1's higher 8 bits of address data are output when ϕ goes "H" state and as it changes back to the "L" state it retains its original I/O functions.
Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state.
Pins $P4_1$ and $P4_0$ output the SYNC and R/W control signals, respectively while ϕ is in the "H" state.
When in the "L" state, $P4_1$ and $P4_0$ retain their original I/O functions.
The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.
The SYNC is a synchronous signal which goes "H" state when it fetches the OP code.

(3) Microprocessor mode (10)
After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.
In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pin is lost. Port P2 becomes the data bus ($D_7 \sim D_0$) and loses its normal I/O functions. Port $P4_1$ and $P4_0$ become the SYNC and R/$\overline{W}$ pins respectively and the normal I/O functions are lost.

(4) Eva-chip mode (11)
When 10V is supplied to the CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. This mode has almost the same function as the memory expanding mode except that it needs all its programs to come from the outside (including ROM programs). The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

TM_1	0	0	1	1
TM_0	0	1	1	0
Mode / Port	Single-chip mode	Memory expanding mode	Eva-chip mode	Microprocessor mode
Port P0	φ Ports $P0_7$~$P0_0$ I/O Port	φ Ports $P0_7$~$P0_0$ Address A_7~A_0 / I/O Port	Same as left	φ Ports $P0_7$~$P0_0$ Address A_7~A_0
Port P1	φ Ports $P1_7$~$P1_0$ I/O Port	φ Ports $P1_7$~$P1_0$ Address A_{15}~A_8 / I/O Port	Same as left	φ Ports $P1_7$~$P1_0$ Address A_{15}~A_8
Port P2	φ Ports $P2_7$~$P2_0$ I/O Port	φ Ports $P2_7$~$P2_0$ I/O Port / Data D_7~D_0	Same as left	φ Ports $P2_7$~$P2_0$ Data D_7~D_0
Port P4	φ Ports $P4_7$~$P4_0$ I/O Port	φ Ports $P4_7$~$P4_2$ I/O Port Port $P4_1$ SYNC / I/O Port Port $P4_0$ R/$\overline{W}$ / I/O Port	Same as left	φ Ports $P4_7$~$P4_2$ I/O Port Port $P4_1$ SYNC Port $P4_0$ R/$\overline{W}$

Fig. 23 Processor mode and functions of ports P0~P2, P4

Table 2. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The M50944-XXXSP has two internal clock generating circuit. Figure 26 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of serial I/O_1 mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 24 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 25.

The M50944-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case, $\phi/4$ is selected as timer 3 prescaler input. Before executing the STP instruction, appropriate values must be set in timer 3 prescaler and timer 3 to enable the oscillator to stabilize when restarting oscillation. And the timer 3 count stop bit must be set to supply ("0"), timer 3 interrupt enable bit must be set to enable ("1"), and timer 3 interrupt request bit must be set to no request ("0"), INT_2 or timer 3 interrupt enable bit must be set to disable ("0") and INT_2 or timer 3 interrupt request bit must be set to no request ("0").

Oscillation is restarted (release the stop mode) when INT_1, INT_2, $\overline{INT_3}$, $\overline{INT_4}$, or serial I/O_1 interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($120\mu A$ max. at $f(X_{CIN}) = 32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O_2 mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 27 shows the transition of states for the system clock.

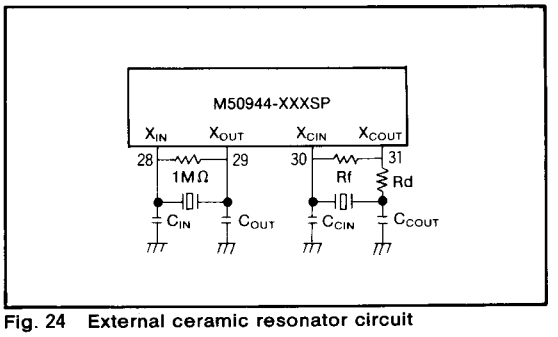


Fig. 24 External ceramic resonator circuit

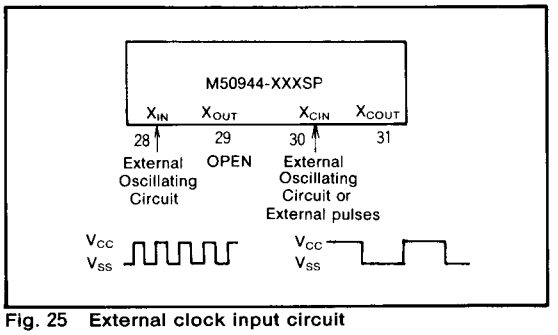


Fig. 25 External clock input circuit

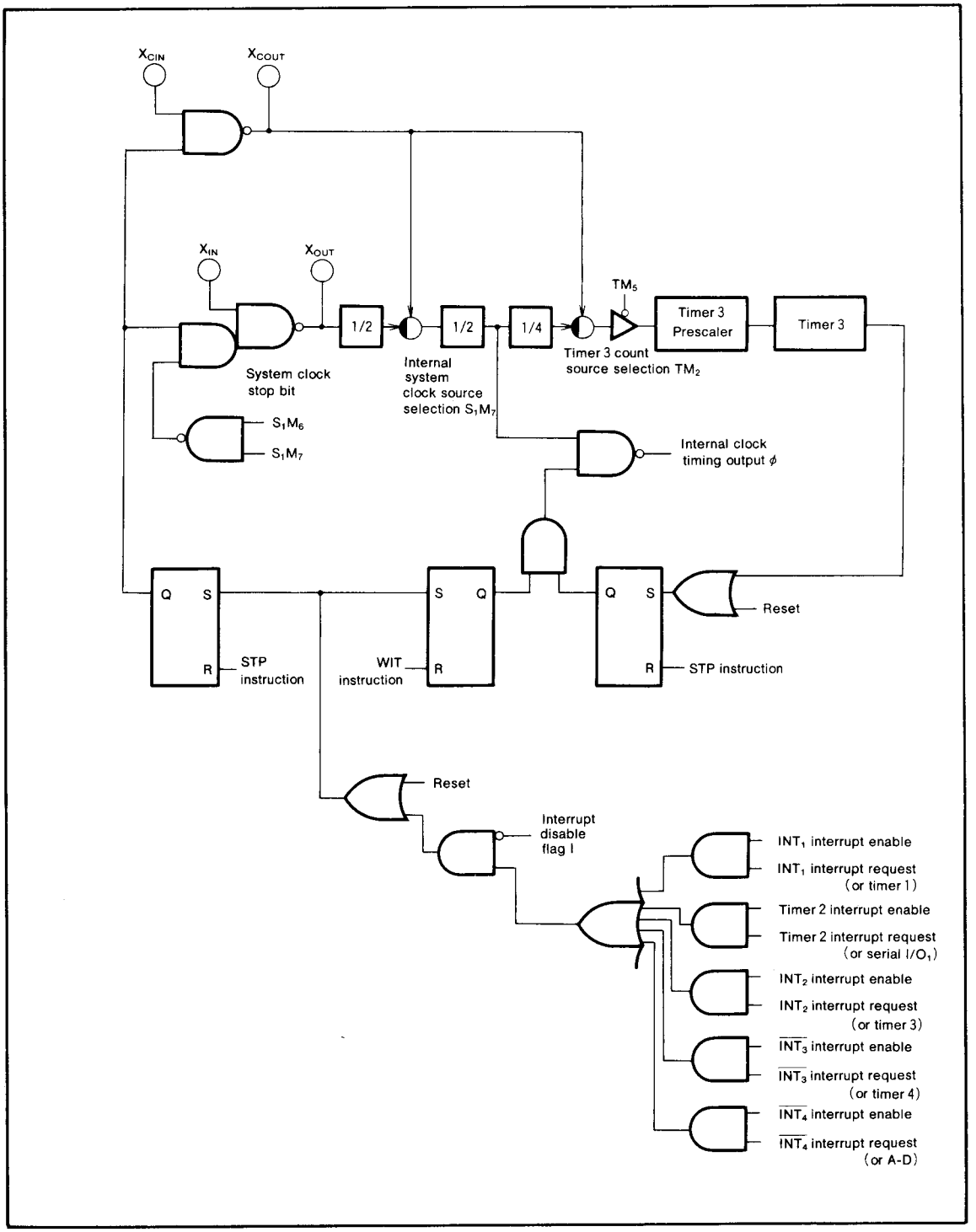
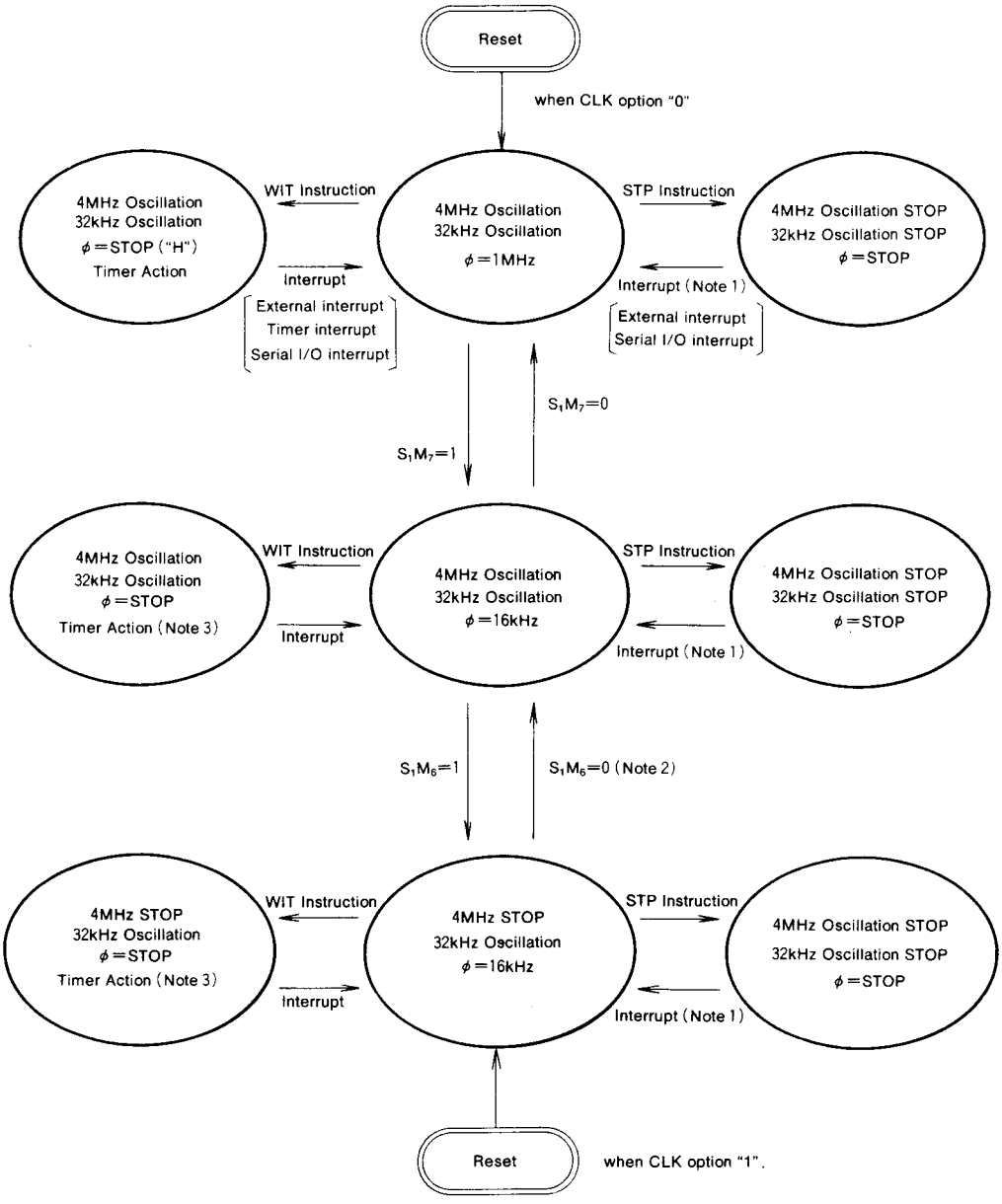


Fig. 26 Block diagram of clock generating circuit



Note 1. At recovery from the STP Instruction, wait time occurs automatically by connecting timer 3 prescaler and timer 3. This time is set by the program.

2. When $S_1M_6=1$, and unsystem clock is operated, a programmed wait time may be necessary to allow the oscillator stabilize.

3. When connected the clock divided by four as the count source of timer, frequency of count source is 4kHz.

Fig.27 Transition of states for the system clock

<An example of flow for system>

Normal operation

(1) When CLK option "0"
Power on reset
↓
Clock X and Clock for clock function X_C oscillation
↓
Internal system clock start (X →1/4→ φ)
↓
Program start from $\overline{\text{RESET}}$ vector
↓
Normal program ←Operation at 4 MHz
↓

(2) When CLK option "1"
Power on reset
↓
Clock for clock function X_C oscillation
↓
Internal system clock start (X_C →1/2→ φ)
↓
Program start from $\overline{\text{RESET}}$ vector
↓
Normal program ←Operation at 32.768kHz

Operation on the clock function only

Internal clock φ source switching X(4 MHz)→X_{CLK}(32.768kHz)(S_1M_7 : 0 → 1)
↓
Clock X halt (X_C in operation)(S_1M_6= 1)
↓
Internal clock halt (WIT instruction)
↓
Timer 1 (clock count) overflow
↓
Internal clock operation start (WIT instruction)
↓
Clock processing routine ← Operating at 32.768kHz
↓
Internal clock halt (WIT instruction)

Return from clock function

INT_1 or timer 1 , timer 2 or serial I/O_1, INT_2 or timer 3 $\overline{INT_3}$ or timer 4 , $\overline{INT_4}$
↓
Internal clock operation start (WIT instruction released)
↓
Program start from interrupt vector
↓
Clock X oscillation start (S_1M_6= 0)
↓
Oscillation rise time routine (software) ←Operating at 32.768kHz
↓
Internal clock φ souce switching (X_C→X)(S_1M_7 : 1 → 0)
↓
Normal program ←Operating at 4MHz

R A M backup function

STP instruction preparation (pushing registers)
↓
Timer 3 interrupt disable ($IF1_0$=1, IM_4=0), Timer 3 interrupt no request ($IF1_1$=0, IM_5=0)
↓
Timer 3 count stop bit resetting (TM_5 = 0)
↓
Clock X and clock function X_C halt (STP instruction)
↓
RAM backup status

Return from R A M backup function

Interrupts from INT_1, INT_2, $\overline{INT_3}$, $\overline{INT_4}$ or serial I/O_1
↓
Clock X and clock for clock function X_C oscillation start
↓
Timer 3 overflow (X/16 or X_C/8→timer 3 prescaler→timer 3)
(Automatically connected by the hardware)
↓
Internal system clock start (X/4 or X_C/2→φ)
↓
Program start from interrupt vector
↓
Normal program

PROGRAMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).(n=0~255)

(2) When the timer 1, timer 2, timer 3 or timer 4 is input the clock except $\phi/4$ or it divided by timer, read the contents of these timers either while the input of these timers are not changing or after counting of timers are stopped.

(3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD intructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) Notes on serial I/O_1

① Set "0" in the serial I/O_1 interrupt enable bit (bit 6 of address $00FF_{16}$) before setting the serial I/O_1 mode.

② Insert at least one instruction and set "0" in the serial I/O interrupt request bit (bit 7 of address $00FF_{16}$) after setting the serial I/O_1 mode.

③ Set "1" in the serial I/O_1 interrupt enable bit after the operation described in ②.

(7) The timer 3 prescaler and the timer 3 must be set the necessary value immediately before the execution of a STP instruction.

(8) The V_{REF} pin must be kept open or connected to V_{SS} at the low power dissipation mode.

(9) Use the LDA (immidiate, T = 1) instruction to modify the interrupt request distinguish register. SEB and CLB instructions can be used only when interrupts in the register are not generated at executing these instructions.

(10) Do not write any data into an address where no register nor port is assigned.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3 sets

Write the following option on the mask ROM cofirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-up transistor bit
- Clock source option at reset
- STP instruction

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output Transistors are at "OFF" state.	−0.3~7	V
V_I	Input voltage CNV_{SS}, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$		−0.3~13	V
V_I	Input voltage R_0~R_3, X_{IN}, X_{CIN}, $\overline{RESET}$		−0.3~7	V
V_I	Input voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7, V_{REF}		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P3_0$~$P3_7$,$P4_0$~$P4_7$, X_{COUT}, X_{OUT}, ϕ		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$		−0.3~13	V
P_d	Power Dissipation	T_a=25℃	1000(Note 1)	mW
Topr	Operating Temperature		−10~70	℃
Tstg	Storage Temperature		−40~125	℃

Note 1. 600mW for QFP type.

RECOMMEND OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	f(X_{IN})=4MHz	4.5	5	5.5	V
		f(X_{IN})≦1MHz	3	5	5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7,CNV_{SS}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage R_0~R_3		0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$		0.8V_{CC}		12	V
V_{IL}	"L" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	"L" input voltage R_0~R_3		0		0.12V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.16V_{CC}	V
$I_{OL(sum)}$	"L" sum output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$				60	mA
$I_{OH(sum)}$	"H" sum output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				−30	mA
$I_{OL(sum)}$	"L" sum output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				60	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$				20	mA
$I_{OH(peak)}$	"H" peak output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				−10	mA
$I_{OL(peak)}$	"L" peak output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				20	mA
$I_{OL(avg)}$	"L" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$				10	mA
$I_{OH(avg)}$	"H" average output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				−5	mA
$I_{OL(avg)}$	"L" average output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				10	mA
f(X_{IN})	Clock oscillating frequency	V_{CC}=5V			4.3	MHz
		V_{CC}=3V			1.1	
f(X_{CIN})	Clock oscillating frequency for clock function	V_{CC}=5V			500	kHz
		V_{CC}=3V			300	

Note 1. The maximum "H" input voltage for CNV_{SS} is +12V.
2. The duty cycle for these oscillation frequency is 50%.
3. When the low speed mode is used, the clock input oscillation frequency for the timer must satisfy the following expression : f(X_{CIN}) < f(X_{IN})/3
4. The avarage output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms cycle.
5. f(X_{CIN}) must be less than 50kHz when the external clock is to be used.

ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V±10%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OH}	"H" output voltage ϕ	V_{CC}=5V, I_{OH}=−2.5mA		3			V
		V_{CC}=3V, I_{OH}=−0.8mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{OL}	"L" output voltage ϕ	V_{CC}=5V, I_{OL}=2.5mA				2	V
		V_{CC}=3V, I_{OL}=0.8mA				1	
$V_{T+}-V_{T-}$	Hysteresis $P3_0/\overline{INT_1}$, $P3_1/\overline{INT_2}$, $P4_2/\overline{INT_3}$, $P4_3/\overline{INT_4}$	use as interrupt input	V_{CC}=5V	0.3		1	V
			V_{CC}=3V	0.15		0.7	
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5	0.7	V
		V_{CC}=3V			0.35		
$V_{T+}-V_{T-}$	Hysteresis $P3_6/CLK_1$, $P4_6/CLK_2$	use as CLK input	V_{CC}=5V	0.3		1	V
			V_{CC}=3V	0.15		0.7	
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	V_{CC}=5V		0.1		0.5	V
		V_{CC}=3V		0.06		0.3	
$V_{T+}-V_{T-}$	Hysteresis $P3_2$/CNTR	Use as CNTR input	V_{CC}=5V	0.3		1	V
			V_{CC}=3V	0.15		0.7	
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=0V without pull-up T_r.	V_{CC}=5V			−5	μA
			V_{CC}=3V			−4	
		V_I=0V, with pull-up T_r.	V_{CC}=5V	−35	−70	−140	
			V_{CC}=3V	−12	−25	−40	
I_{IL}	"L" input current IN_0~IN_7	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−4	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−4	
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=5V, without pull-up transistor				5	μA
I_{IH}	"H" input current IN_0~IN_7	V_I=5V, not use as analog input				5	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=5V				5	μA
I_{IH}	"H" input current V_{REF}	V_I=5V				5	mA
I_{CC}	Supply current	Open output ports, V_P=V_{CC}, Input port is V_{SS}, at normal operation.	X_{IN}=4MHz, V_{CC}=5V		3	6	mA
			X_{IN}=1MHz, V_{CC}=3V		0.4		
		Open output ports, V_P=V_{CC}, Input port is V_{SS}, at wait mode.	X_{IN}=4MHz, V_{CC}=5V		1		
			X_{IN}=1MHz, V_{CC}=3V		0.2		
		Open output ports, V_P=V_{CC}, Input port is V_{SS}, at normal operation, stop X_{IN} and X_{OUT}. X_{CIN}=32kHz.	V_{CC}=5V		60	200	μA
			V_{CC}=3V		25		
		Open output ports, V_P=V_{CC}, Input port is V_{SS}, at wait mode, stop X_{IN} and X_{OUT}, X_{CIN}=32kHz.	V_{CC}=5V		40		
			V_{CC}=3V		15		
		Stop all oscillation.	T_a=25℃, V_{CC}=5V		0.1	1	
			T_a=25℃, V_{CC}=3V		0.06		
			T_a=70℃, V_{CC}=5V		1	10	
			T_a=70℃, V_{CC}=3V		0.6		
I_{ACC}	Supply current for A-D	at A-D converting time			2	4	mA
V_{RAM}	RAM retention voltage	at clock stop		2		5.5	V

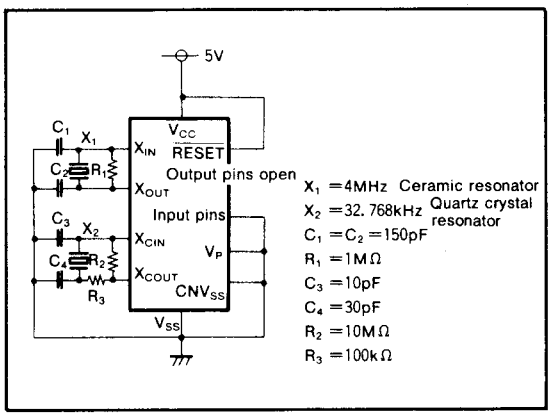


Fig. 28 Test circuit for measuring supply current

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.12V			±3	LSB
R_{LADDER}	Ladder resistor value		1			kΩ
t_{CONV}	Conversion time	High-speed : ϕ=1MHz			72	μs
		Low-speed : ϕ=1MHz			288	
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}= 5 V±10%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		270			ns
$t_{su(RD-\phi)}$	Port R input setup time		270			ns
$t_{su(IND-\phi)}$	Port IN input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{h(\phi-RD)}$	Port R input hold time		20			ns
$t_{h(\phi-IND)}$	Port IN input hold time		20			ns
$t_{C(X_{IN})}$	External clock input cycle time (X_{IN})		230			ns
$t_{W(X_{IN})}$	External clock input pulse width (X_{IN})		75			ns
$t_{C(X_{CIN})}$	External clock input cycle time (X_{CIN})		2			ms
$t_{W(X_{CIN})}$	External clock input pulse width (X_{CIN})		1			ms
t_r	External clock rising edge time				25	ns
t_f	External clock falling edge time				25	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 29			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 29			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P4_0Q)}$	Port $P4_0$ data output delay time				200	ns
$t_{d(\phi-P4_0QF)}$	Port $P4_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P4_1Q)}$	Port $P4_1$ data output delay time				200	ns
$t_{d(\phi-P4_1QF)}$	Port $P4_1$ data output delay time				200	ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 29			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

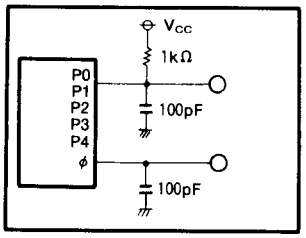
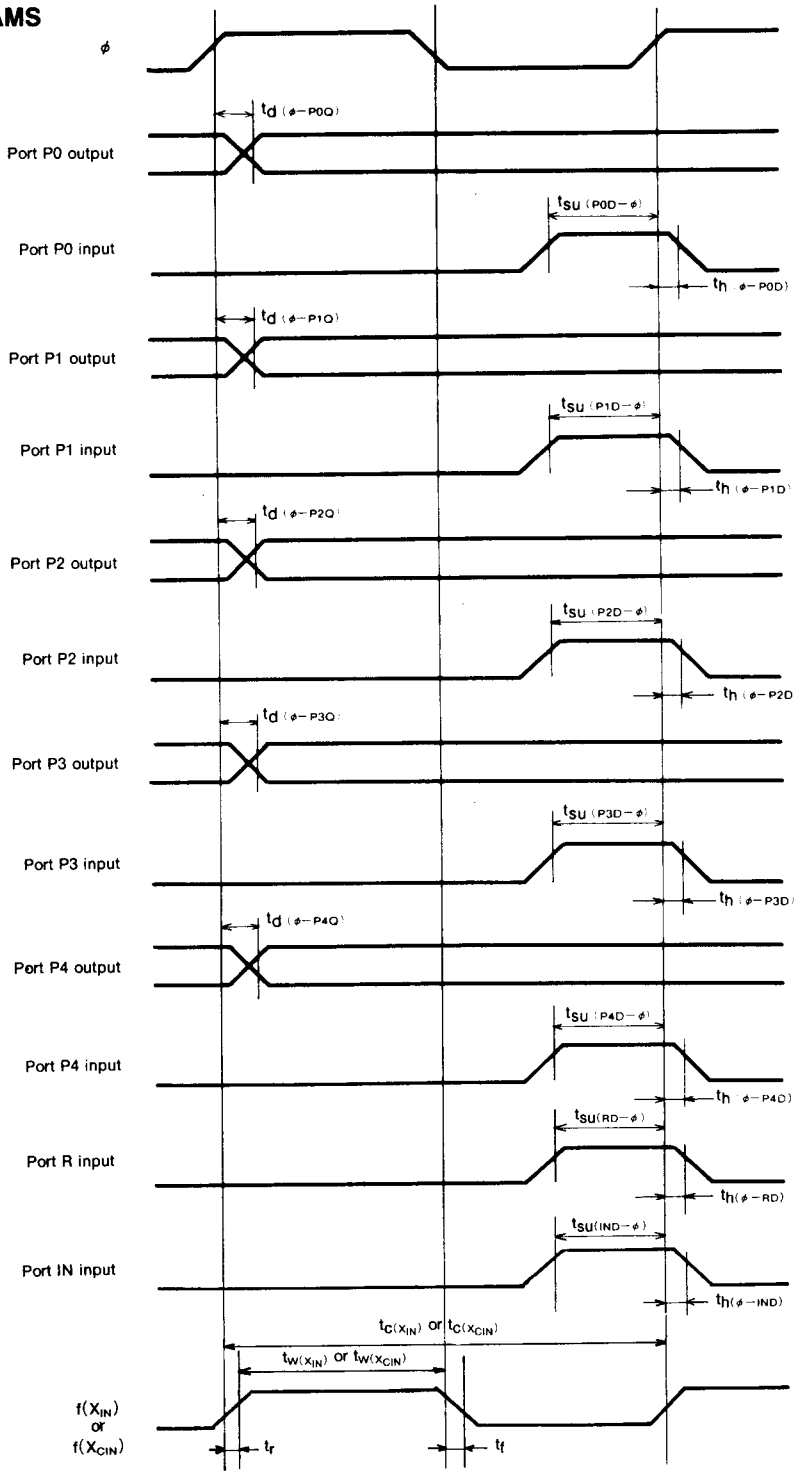


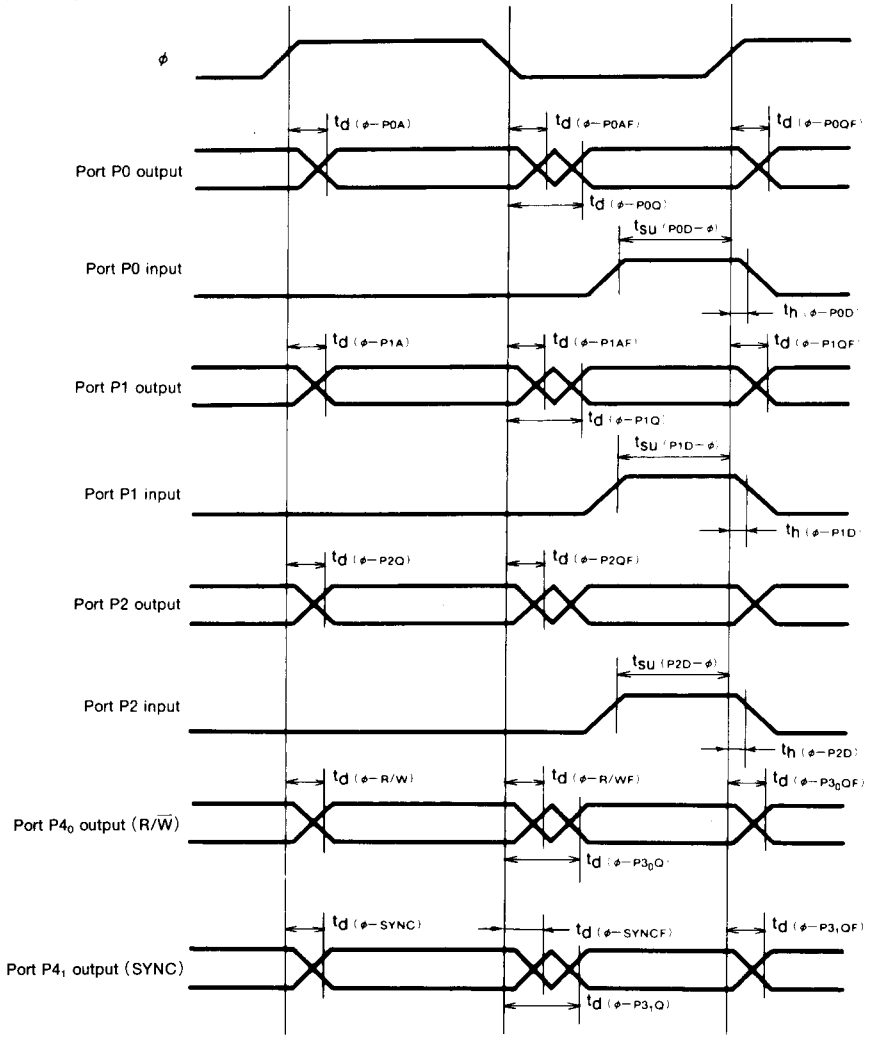
Fig. 29 Test circuit of ports P0~P4

TIMING DIAGRAMS

In single-chip mode



In memory expanding mode and eva-chip mode



In microprocessor mode