MITSUBISHI LSIs

M5M417805CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMs with Hyper page mode fuction, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417805CXX-5,-5S	50	13	25	13	90	655
M5M417805CXX-6,-6S	60	15	30	15	110	540
M5M417805CXX-7,-7S	70	20	35	20	130	475

XX=J,TP

- Standard 28 pin SOJ,28 pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  - 5.5mW (Max) ..... CMOS input level
  - 1.1mW (Max)* ..... CMOS input level
- Operating power dissipation
  - M5M417805CXX-5,-5S ..... 800mW (Max)
  - M5M417805CXX-6,-6S ..... 660mW (Max)
  - M5M417805CXX-7,-7S ..... 580mW (Max)
- Self refresh capability*
  - Self refresh current ..... 200 μA(Max)
- Hyper page mode (1024-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.

  Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})

* : Applicable to self refresh version (M5M417805CJ,TP-5S,-6S, -7S :option) only

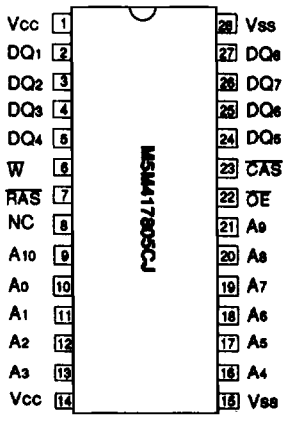
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

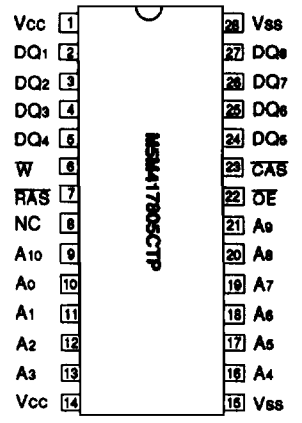
PIN DESCRIPTION

Pin name	Function
A_0~A_{10}	Address inputs
DQ_1~DQ_8	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 28P0N-A (400mil SOJ)



Outline 28P3N-C (400mil TSOP)

NC: NO CONNECTION

MITSUBISHI ELECTRIC

FUNCTION

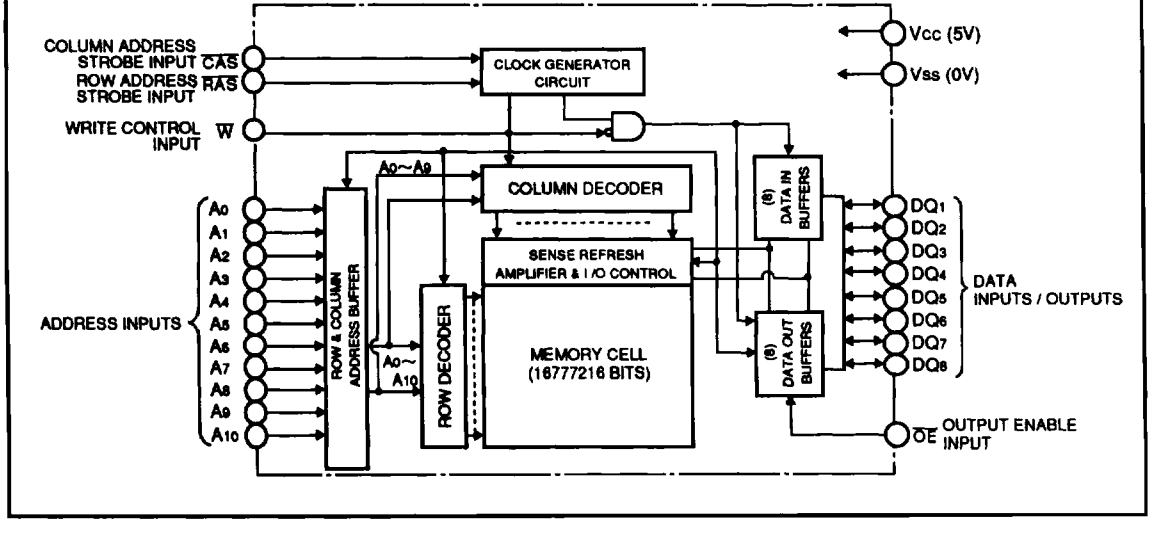
In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M417805CJ, TP provides a number of other functions,e.g., $\overline{RAS}$-only refresh,and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	−1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : $V_{IL(min)}$ is −2.0V when undershoot width is less than 25ns.(Undershoot width is with respect to Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ +6.5V, Other inputs pins=0V	−10		10	μA
$I_{CC1\,(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M417805C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M417805C-6,-6S				120	
		M5M417805C-7,-7S				105	
I_{CC2}	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc−0.2V, output open			0.5	
$I_{CC3\,(AV)}$	Average supply current from Vcc,$\overline{RAS}$ only refresh mode (Note 3,5)	M5M417805C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M417805C-6,-6S				120	
		M5M417805C-7,-7S				105	
$I_{CC4\,(AV)}$	Average supply current from Vcc Hyper Page Mode (Note 3,4,5)	M5M417805C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			140	mA
		M5M417805C-6,-6S				115	
		M5M417805C-7,-7S				90	
$I_{CC6\,(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M417805C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M417805C-6,-6S				120	
		M5M417805C-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1\,(AV)}$, $I_{CC3\,(AV)}$,$I_{CC4\,(AV)}$, and $I_{CC6\,(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1\,(AV)}$ and $I_{CC4\,(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5: Under condition of column address being changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

CAPACITANCE (Ta=0～70℃ , Vcc = 5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I\,(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHZ V_I=25mVrms			5	pF
$C_{I\,(CLK)}$	Input capacitance, clock inputs				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

PRELIMINARY

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc = 5V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$ high	(Note 13)	5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$ high	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns
tDOH	Output hold time from $\overline{CAS}$ low		5		5		5		ns

Note 6:An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-only refresh cycles or by $\overline{CAS}$ before $\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods(greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIH (min) or lower than VIL (max) except $\overline{RAS}$ transition time.
7:Measured with a load circuit equivalent to 100pF.
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).
8:Assumes that tRCD ≧tRCD(max) and tASC ≧tASC(max) and tCP≧ tCP(max).
9:Assumes that tRCD≦tRCD(max) and tRAD≦tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
10:Assumes that tRAD≧ tRAD(max) and tASC≦tASC(max).
11:Assumes that tCP ≦tCP(max) and tASC≧tASC(max).
12:tOEZ (max) ,tWEZ(max) ,tOFF(max) and tREZ(max)defines the time at which the output achieves the high impedance state (IOUT≦ | ±10 μA |) and is not reference to VOH(min) or VOL(max).
13:Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc = 5V ±10%, Vss=0V, unless otherwise noted, See notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note16)	18	32	20	38	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note20)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note20)	13		15		20		ns
tT	Transition time	(Note21)	1	50	1	50	1	50	ns

Note 14:The timing requirements are assumed tT =2ns.
15:VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
16:tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
17:tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
18:tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
19:Either tDZC or tDZO must be satisfied.
20:Either tRDD or tCDD or tODD must be satisfied.
21:tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 22)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time		13		18		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	(Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low		8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		8		10		13		ns
tWP	Write pulse width		8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note23)	109		133		161		ns
tRAS	$\overline{RAS}$ low pulse width		75	10000	89	10000	107	10000	ns
tCAS	$\overline{CAS}$ low pulse width		38	10000	44	10000	57	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		82		99		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		38		44		57		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note24)	28		32		42		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note24)	65		77		92		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note24)	40		47		57		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		13		15		20		ns

Note 23: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

24: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≥tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≥tCWD(min), tRWD≥tRWD (min), tAWD≥tAWD(min) and tCPWD ≥tCPWD(min) (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Hyper page Mode Cycle
(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time (Note26)	20		25		30		ns
tHPRWC	Hyper Page Mode read write / read modify write cycle time	57		66		79		ns
tRAS	$\overline{RAS}$ low pulse width for read or write cycle (Note27)	65	100000	77	100000	92	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note28)	8	13	10	16	13	16	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24)	43		50		60		ns
tCHOL	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
tOEPE	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
tWPE	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
tHAWD	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
tHCOD	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
tHAOD	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
tHPOD	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: tHPC(min) is specified in the case of read-only and early write-only in Hyper Page Mode.
27: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.
28: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
tCAS	$\overline{CAS}$ low pulse width	17		17		22		ns
tRSR	Read setup time before $\overline{RAS}$ low	5		5		5		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Hidden Refresh Cycle (Note 30)

Symbol	Parameter	Limits						Unit
		M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRSR	Read setup time before $\overline{RAS}$ low	5		5		5		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 30: Read, early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases tRSR and tRHR should be satisfied.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70℃ , Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC8\ (AV)}$	Average supply current from Vcc Slow - Refresh cycle (note 6)	M5M417805C (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS} \leq 0.2V$ $\overline{OE}$ & $\overline{WE} \leq 0.2V$ or $\overline{OE}$ & $\overline{WE} \geq$ Vcc-0.2V $A_0 \sim A_{10} \leq 0.2V$ or $A_0 \sim A_{10} \geq$ Vcc-0.2V t_{REF}=128ms (2048 cycles) output = OPEN $t_{RAS}=t_{RAS}$min. ~1 μs			500	μA
$I_{CC9\ (AV)}$*	Average supply current from Vcc Self - Refresh cycle (note 6)	M5M417805C (S)	$\overline{RAS}$= $\overline{CAS}$ ≤ 0.2V output = OPEN			200	μA

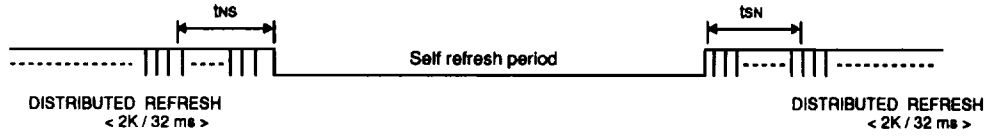
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=5V±10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M417805C-5S		M5M417805C-6S		M5M417805C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	−50		−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leq 32$ms and $t_{SN} \leq$ 32 ms.



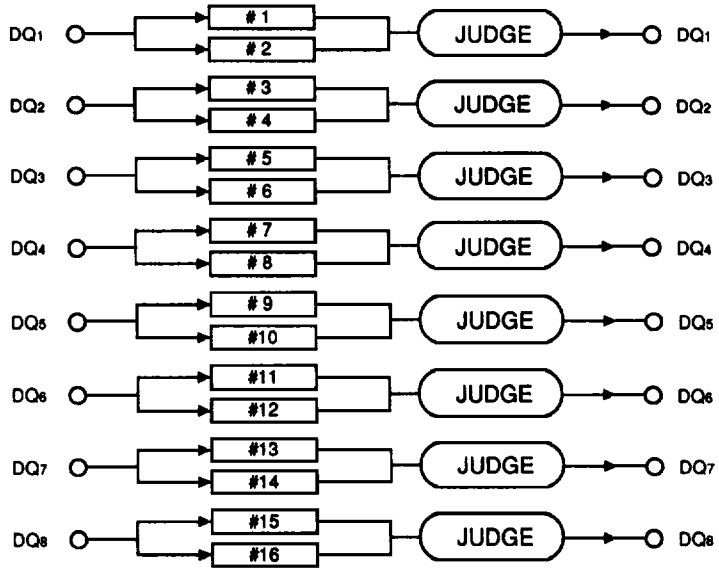
(2) In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leq 32$ ms.

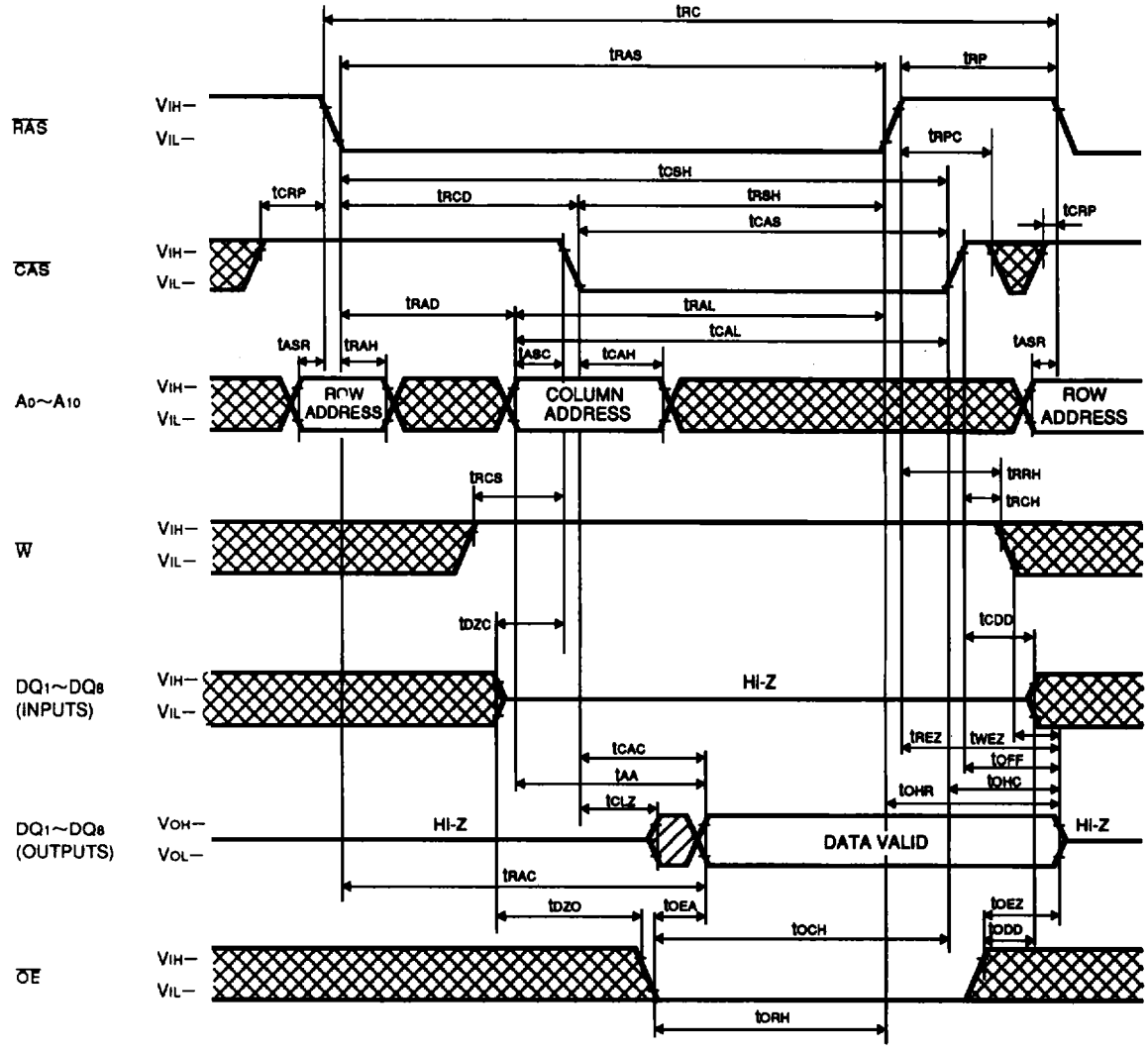
TEST Mode SET Cycle (Note 31)

Symbol	Parameter	Limits						Unit
		M5M417805C-5,-5S		M5M417805C-6,-6S		M5M417805C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 31: The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth) . No addressing of CA_0 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 32)
Read Cycle

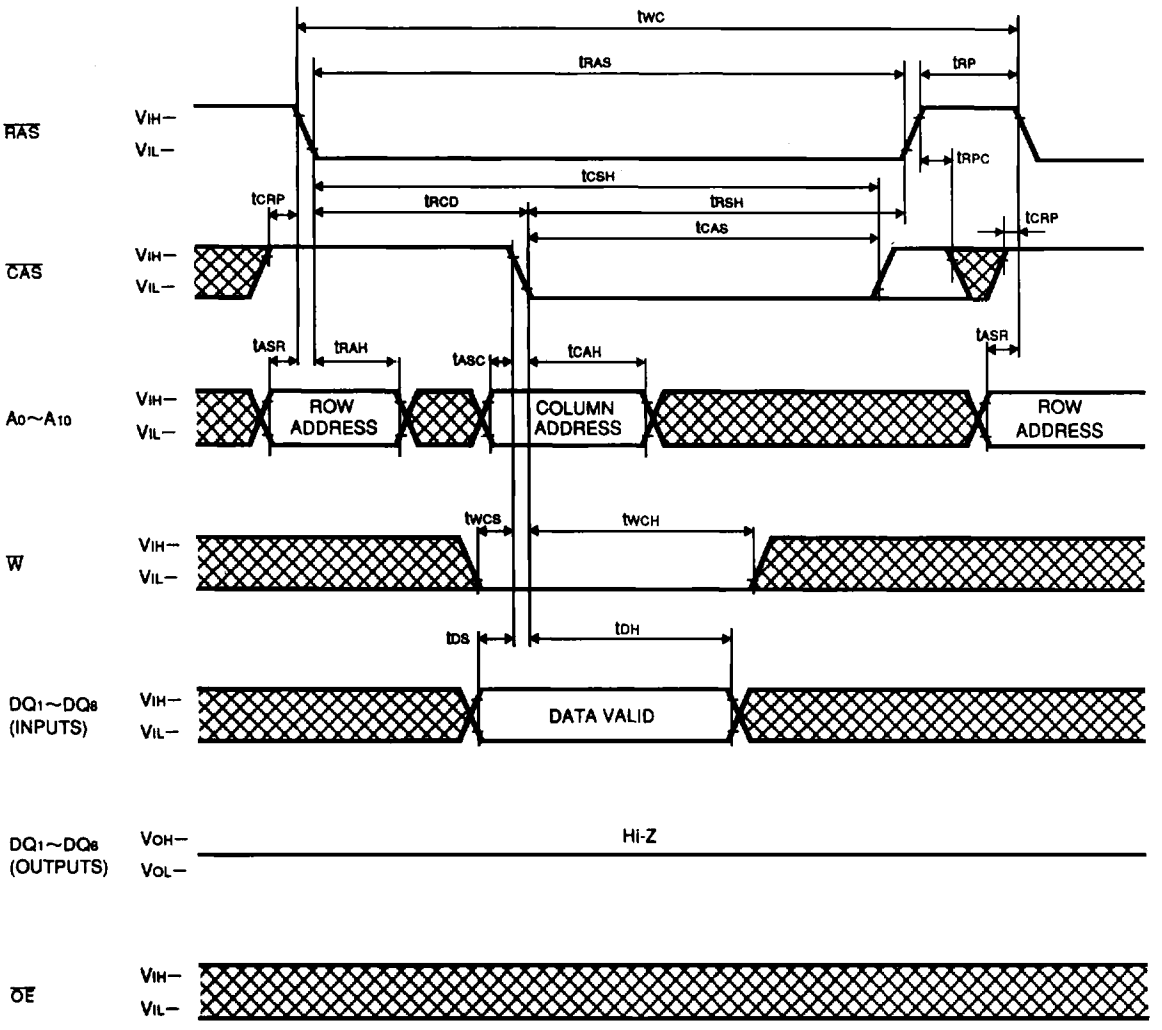


Note 32

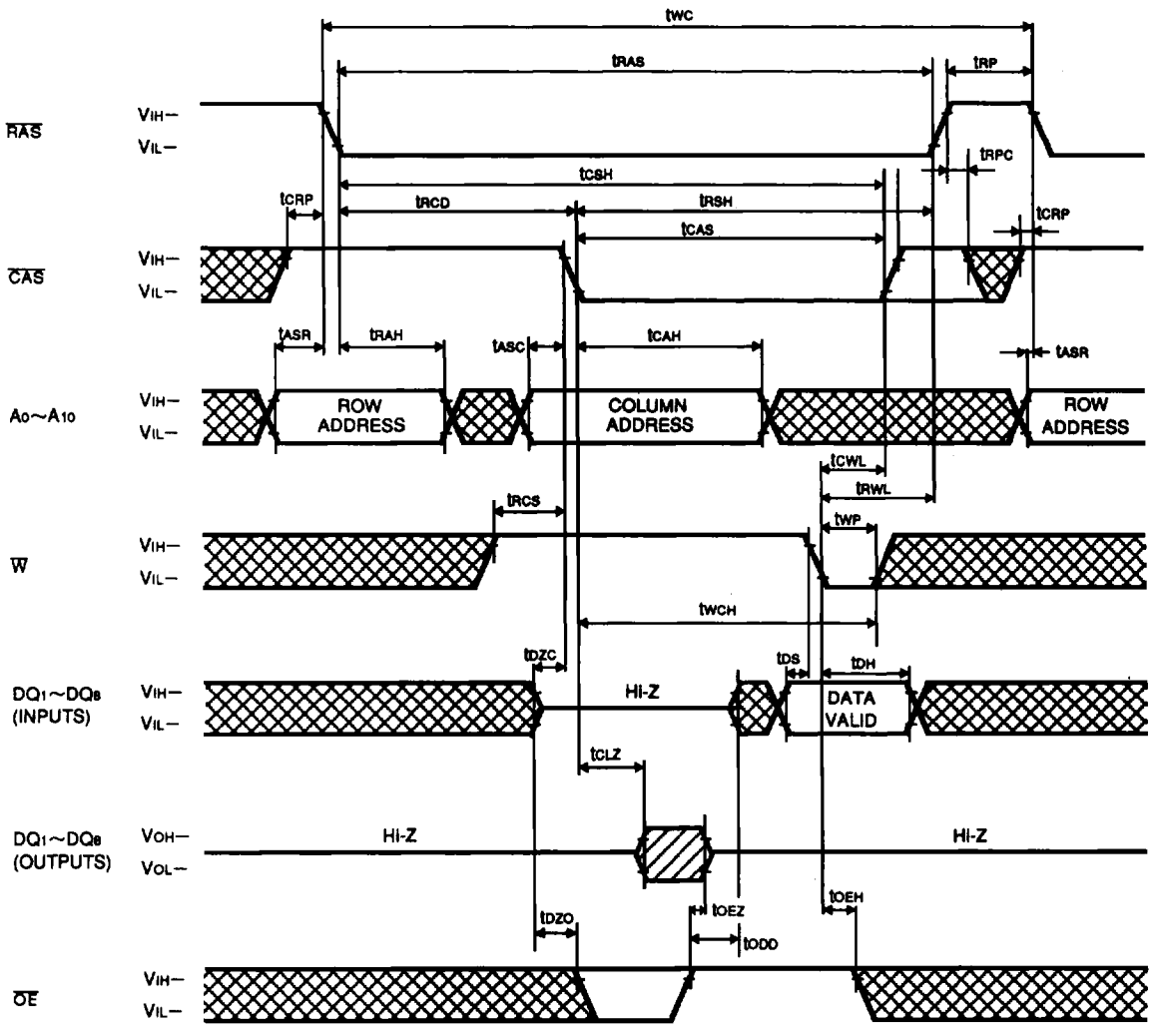
Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

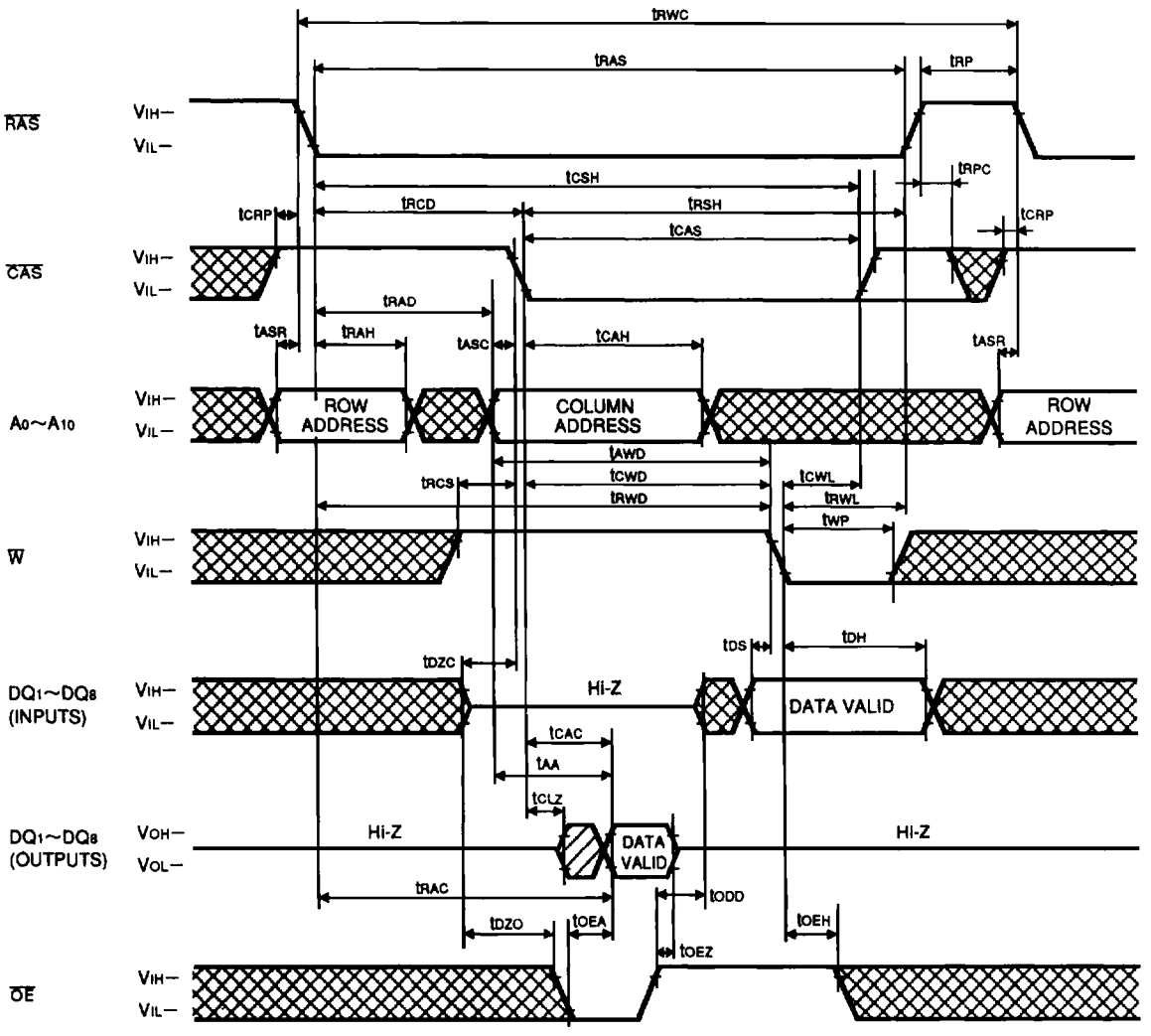
Early Write Cycle



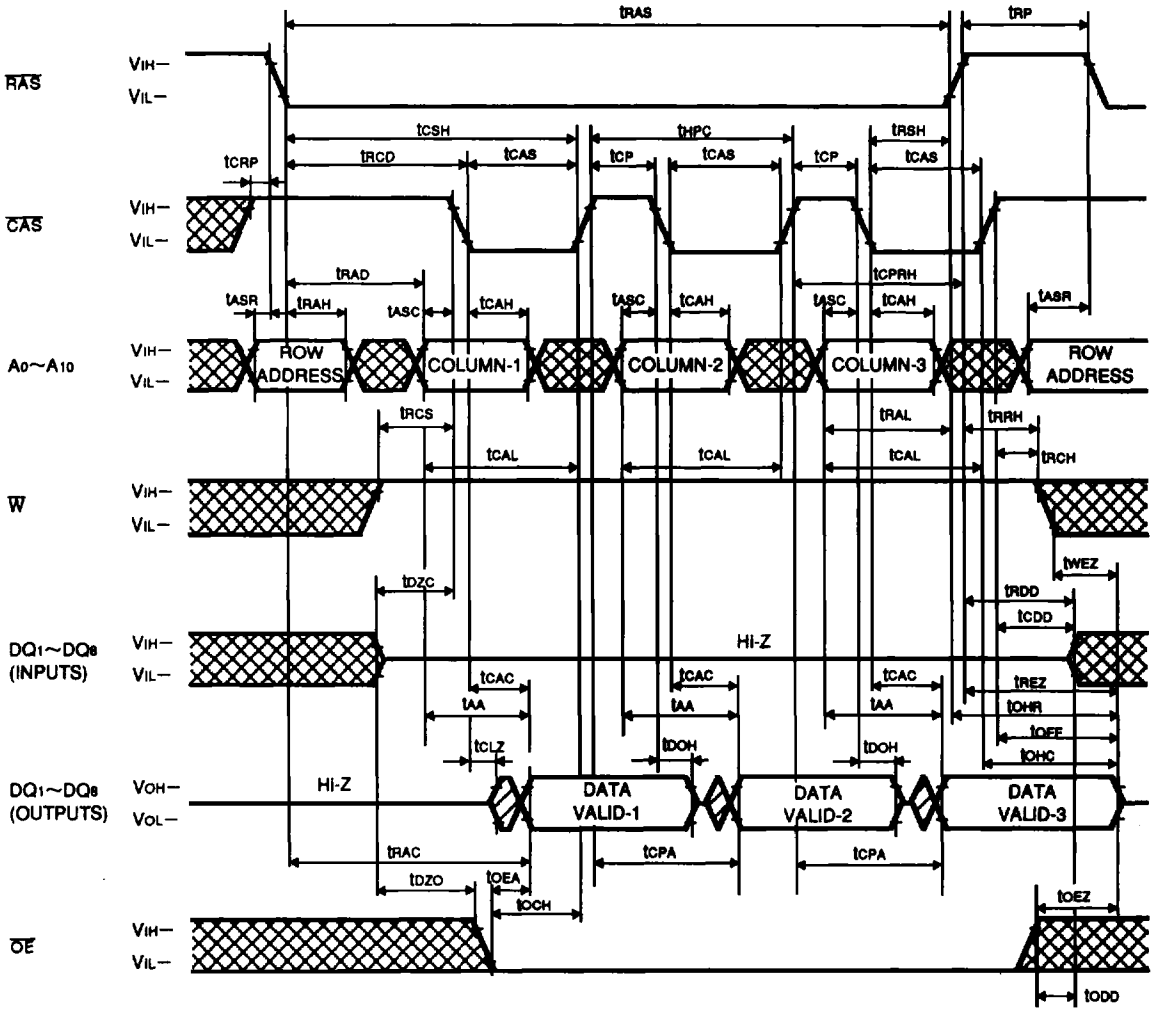
Delay d Write Cycle



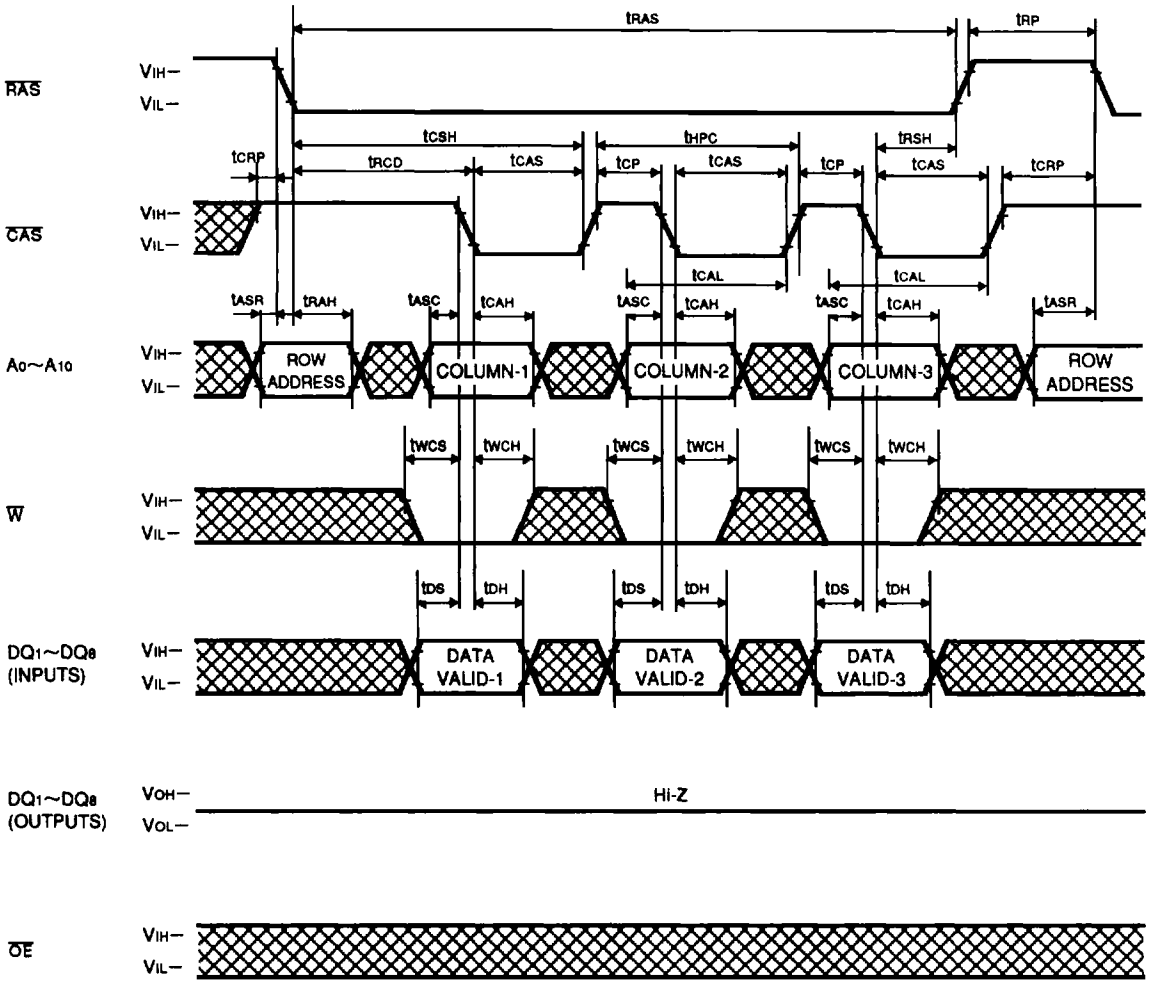
Read-Write, Read-Modify-Write Cycle



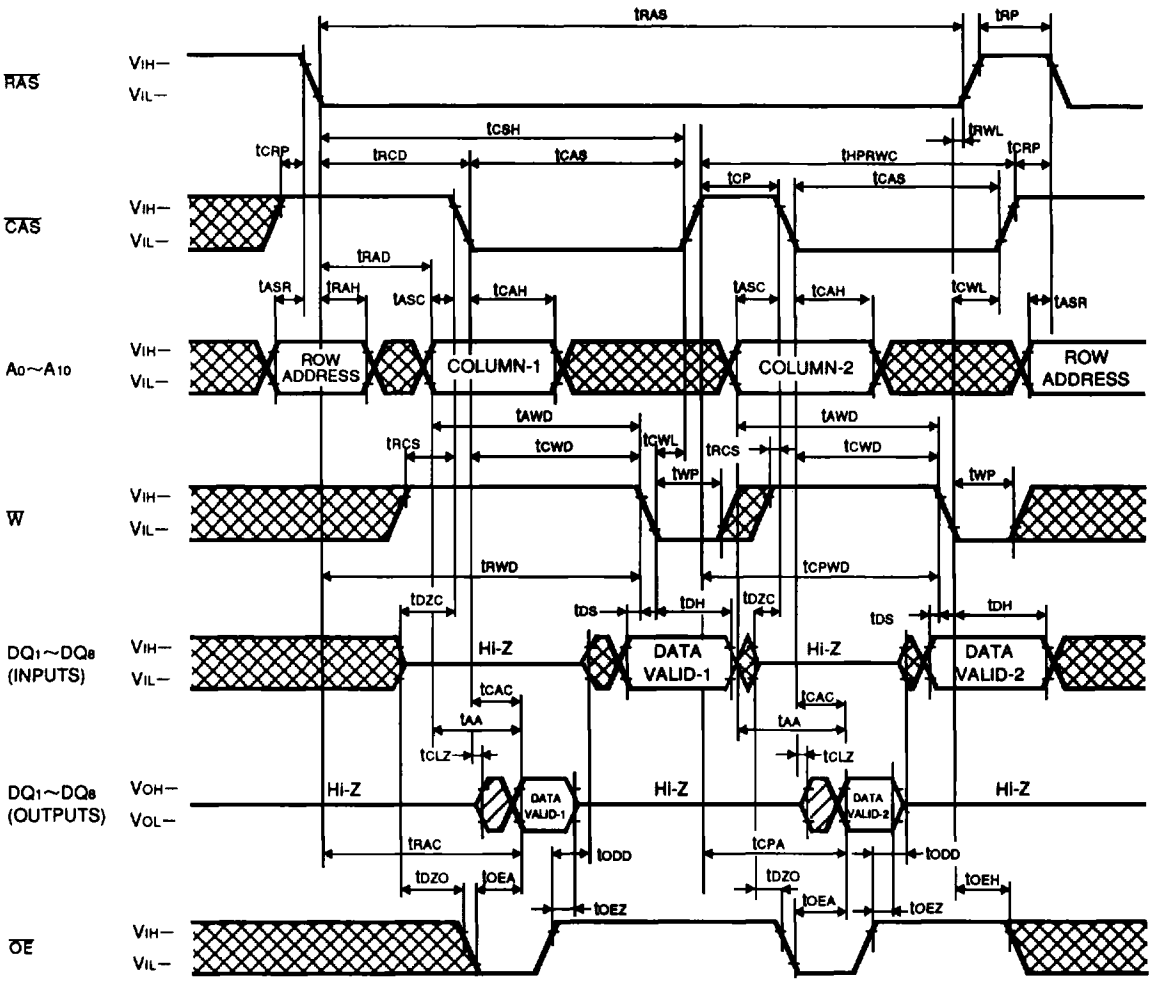
Hyper Page Mode Read Cycle



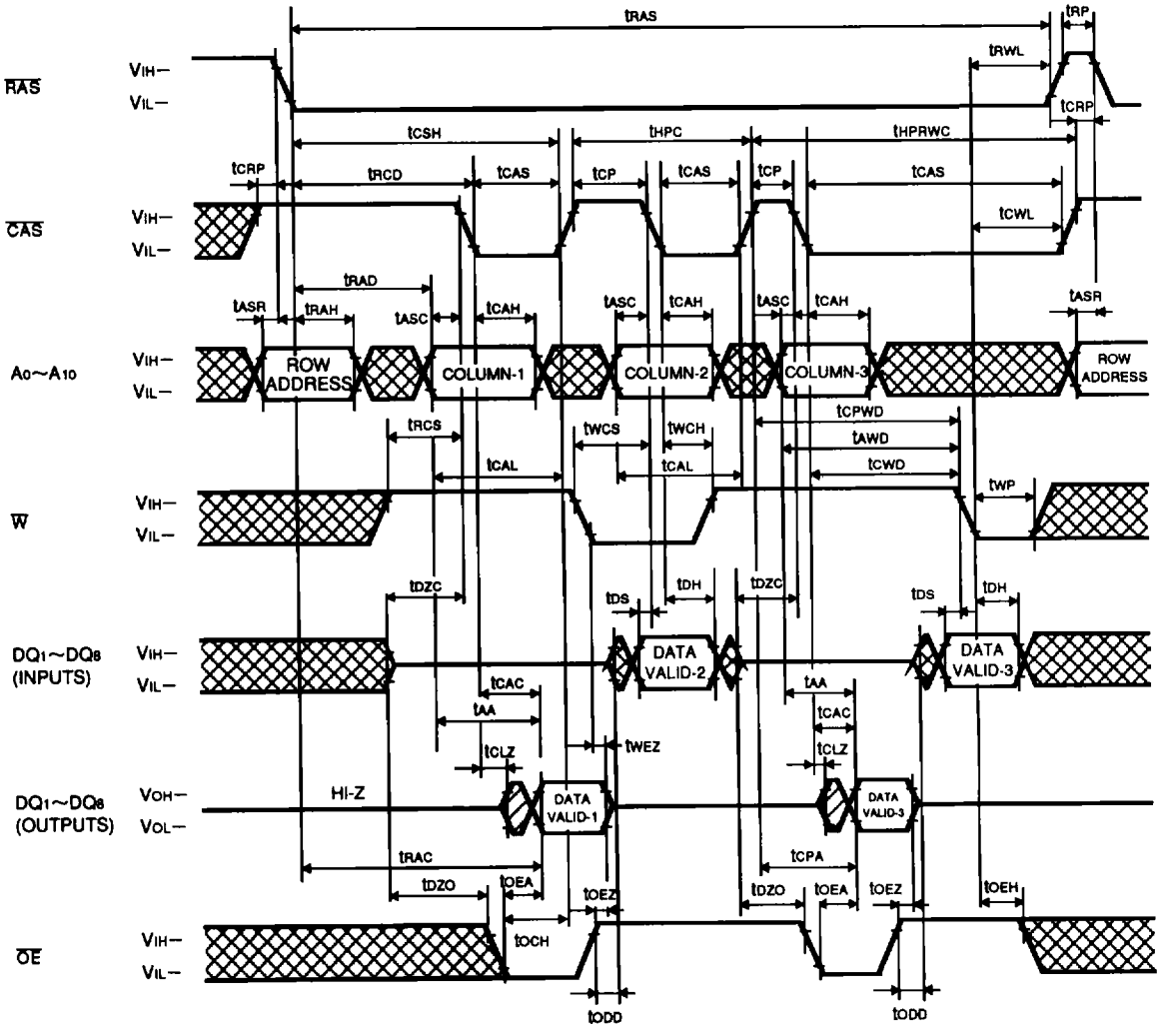
Hyper Page Mode Early Write Cycle



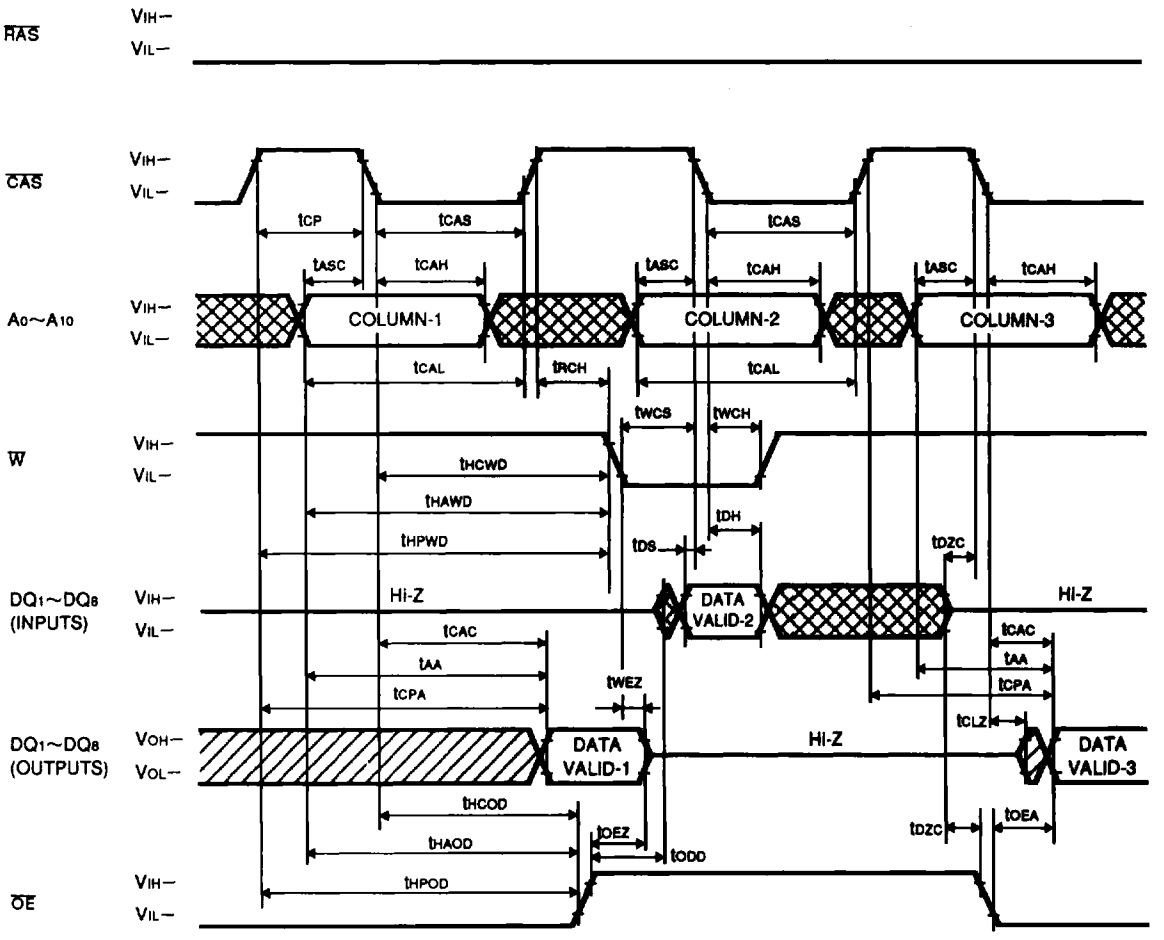
Hyper Page Mode Read-Write,Read-Modify-Write Cycle



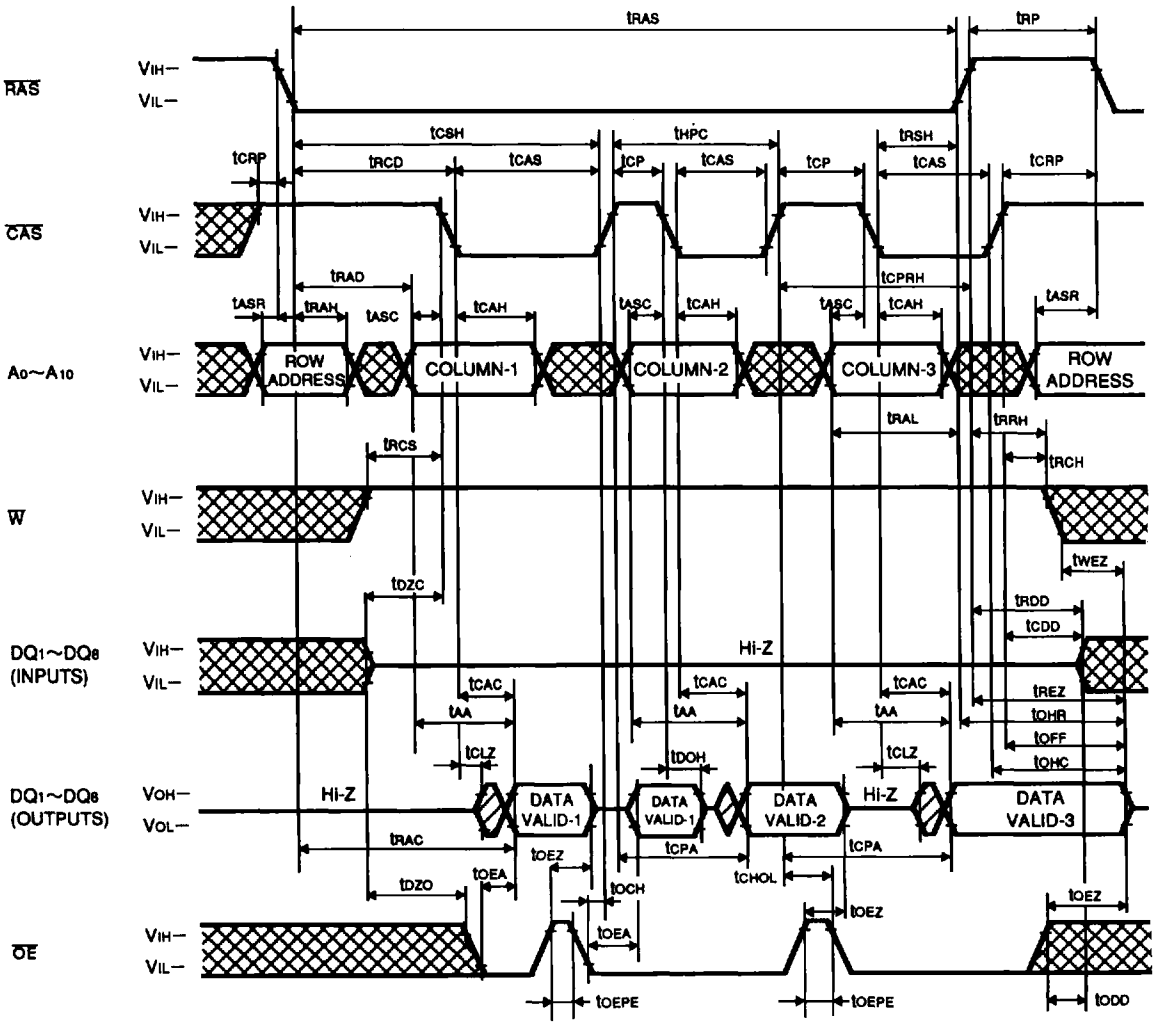
Hyper Page Mode Mix Cycle (1)



Hyper Page Mode Mix Cycle (2)

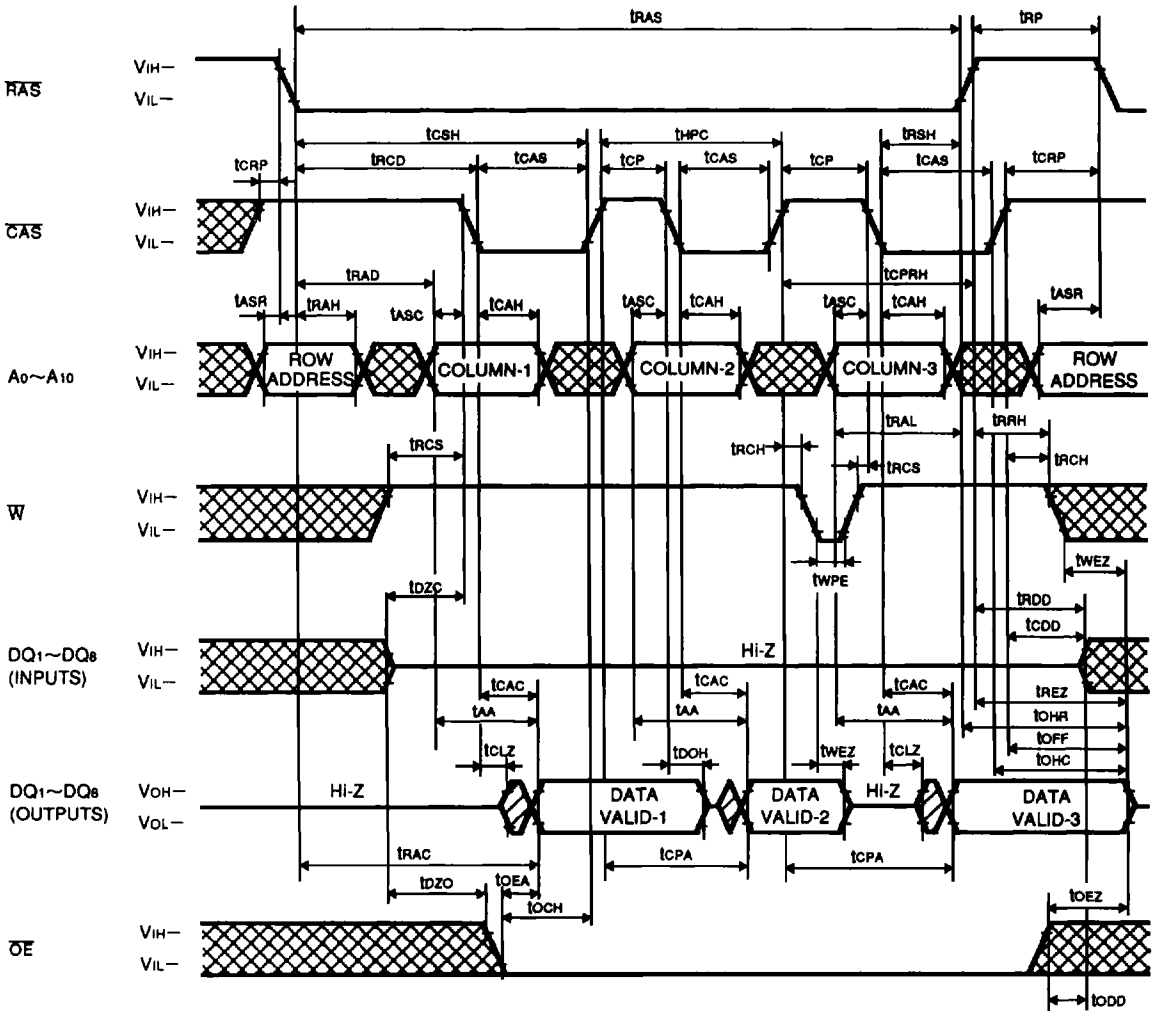


Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



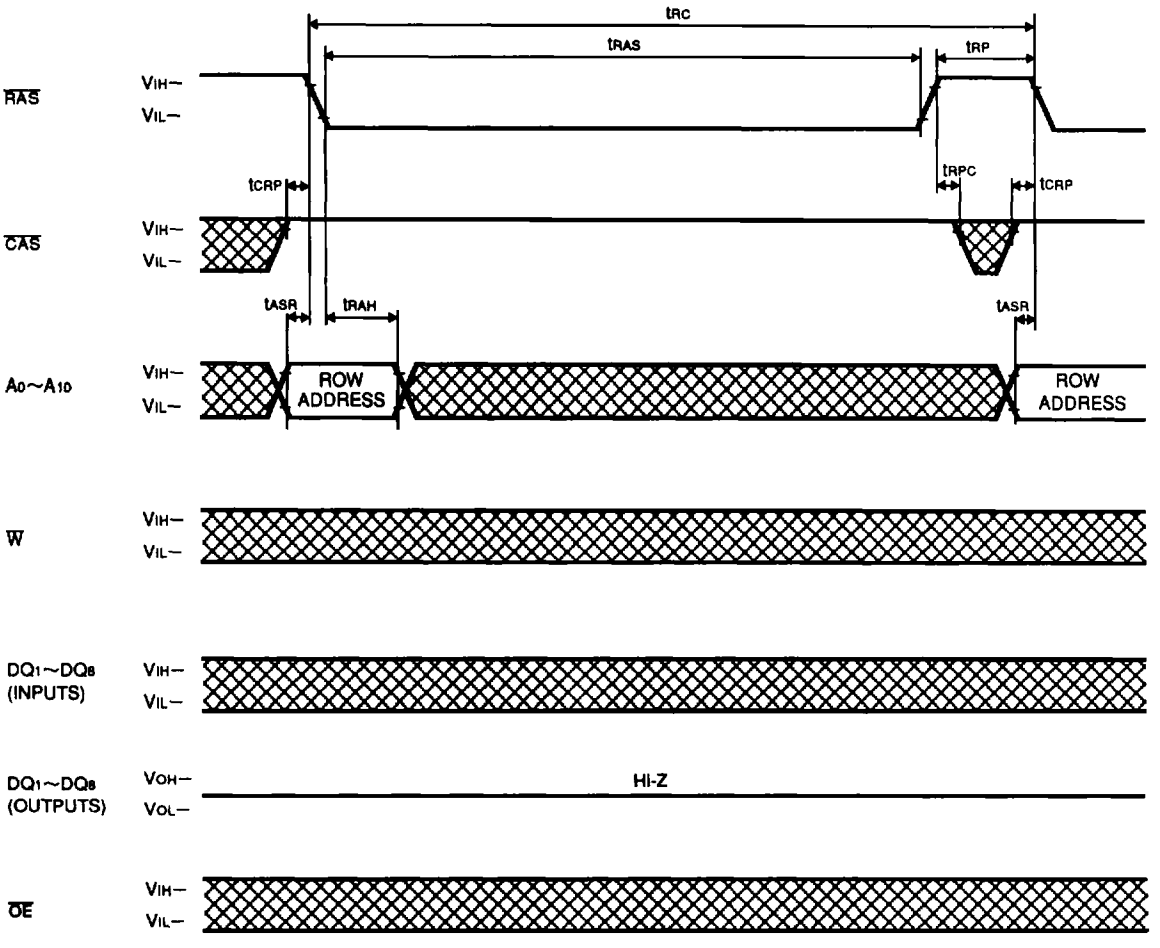
PRELIMINARY

Hyper Page Mode Read Cycle (HI-Z control by $\overline{W}$)

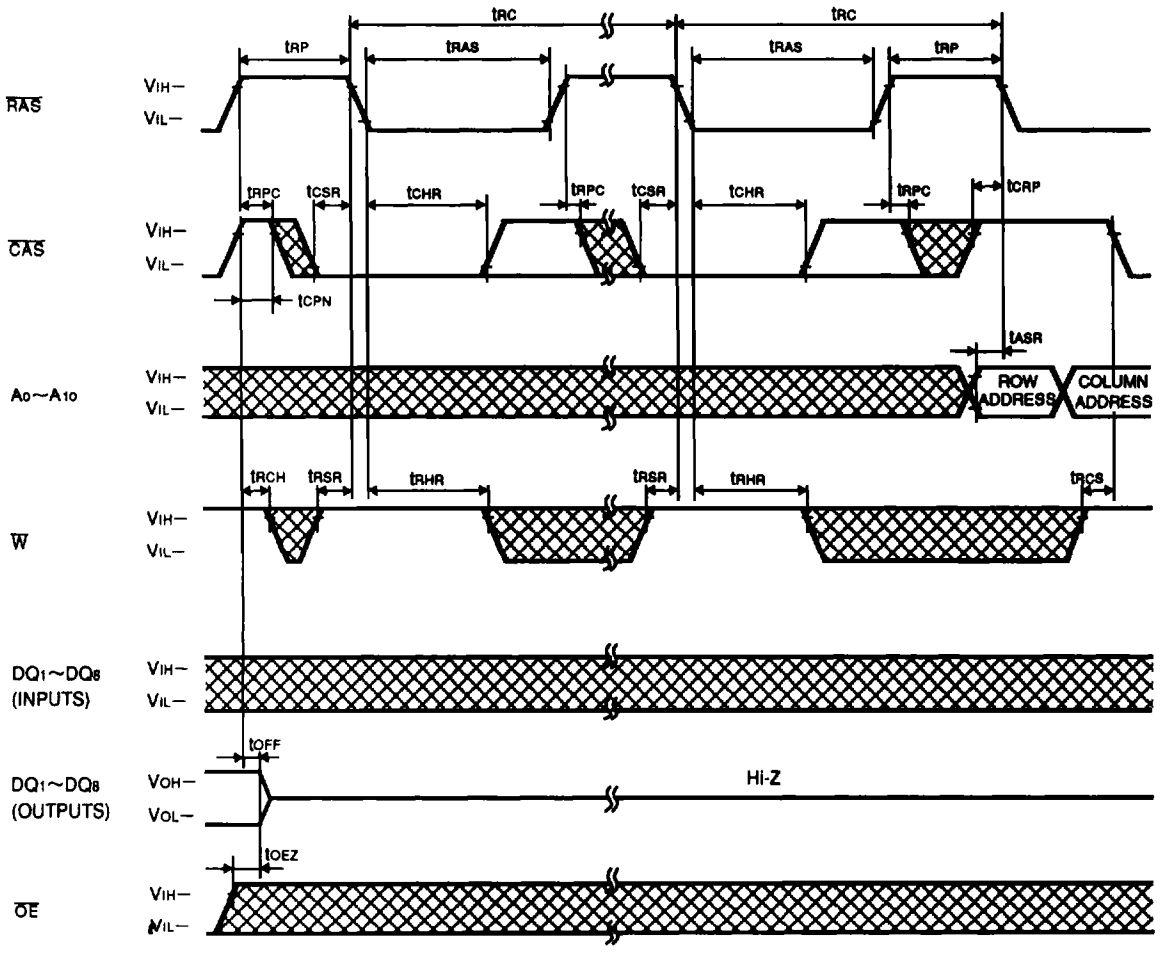


MITSUBISHI ELECTRIC

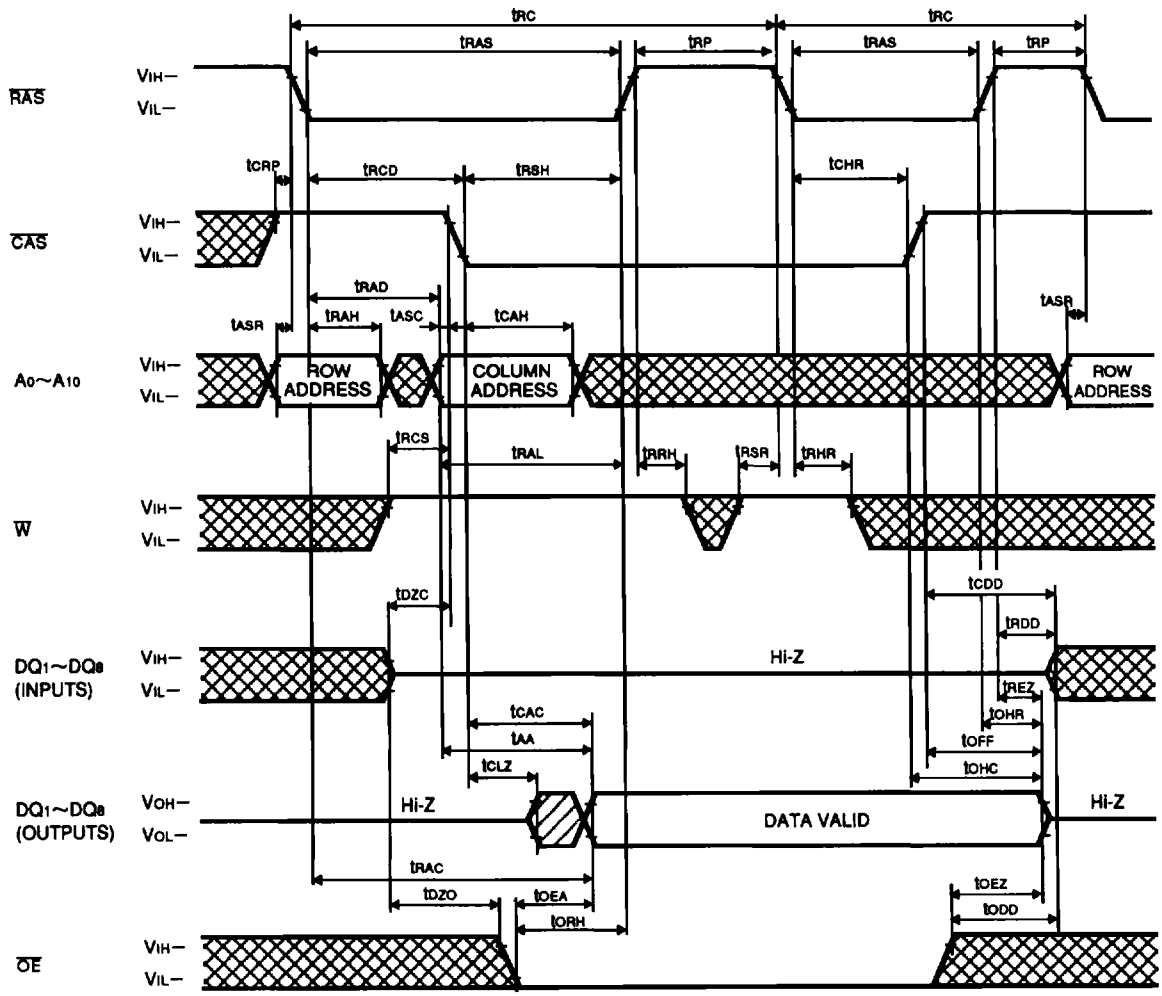
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle

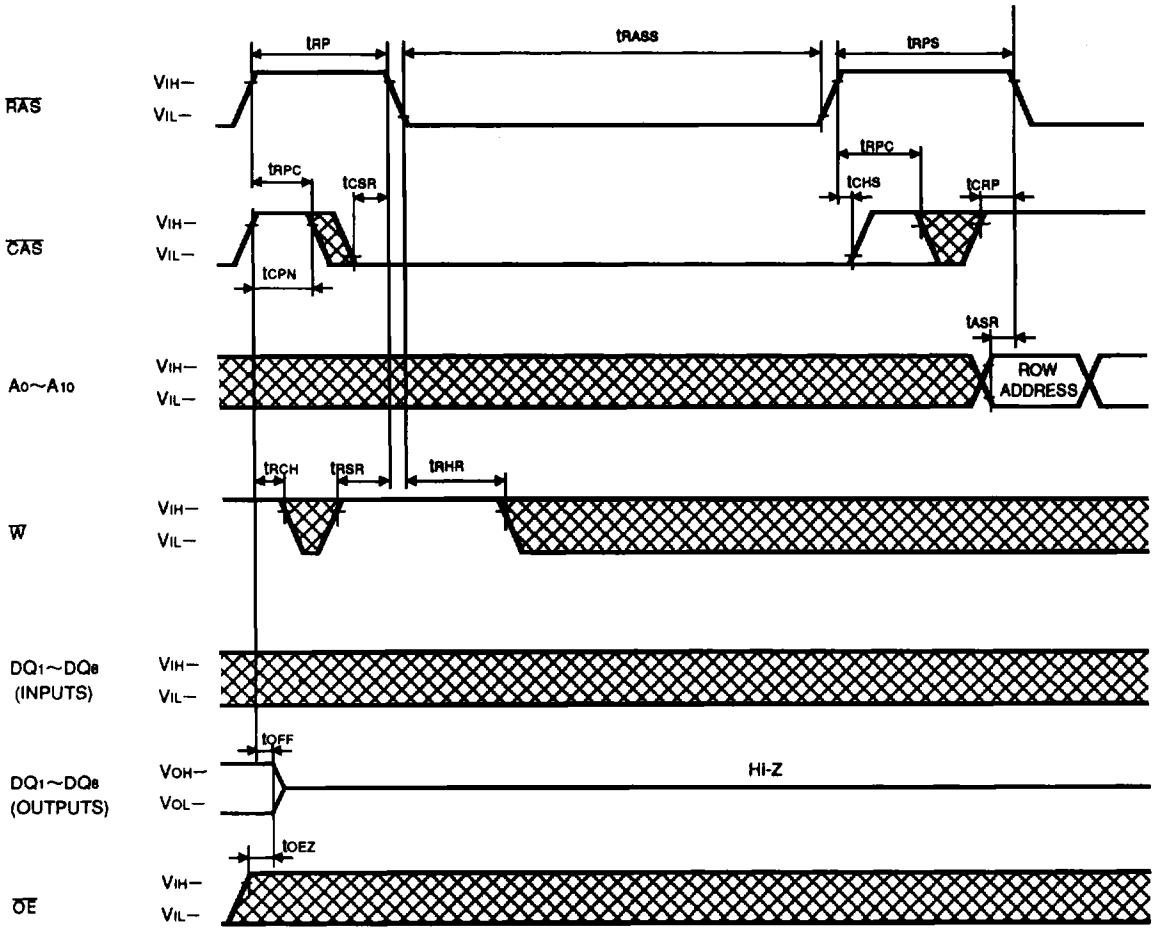


Hidden Refresh Cycle (Read) (Note 33)

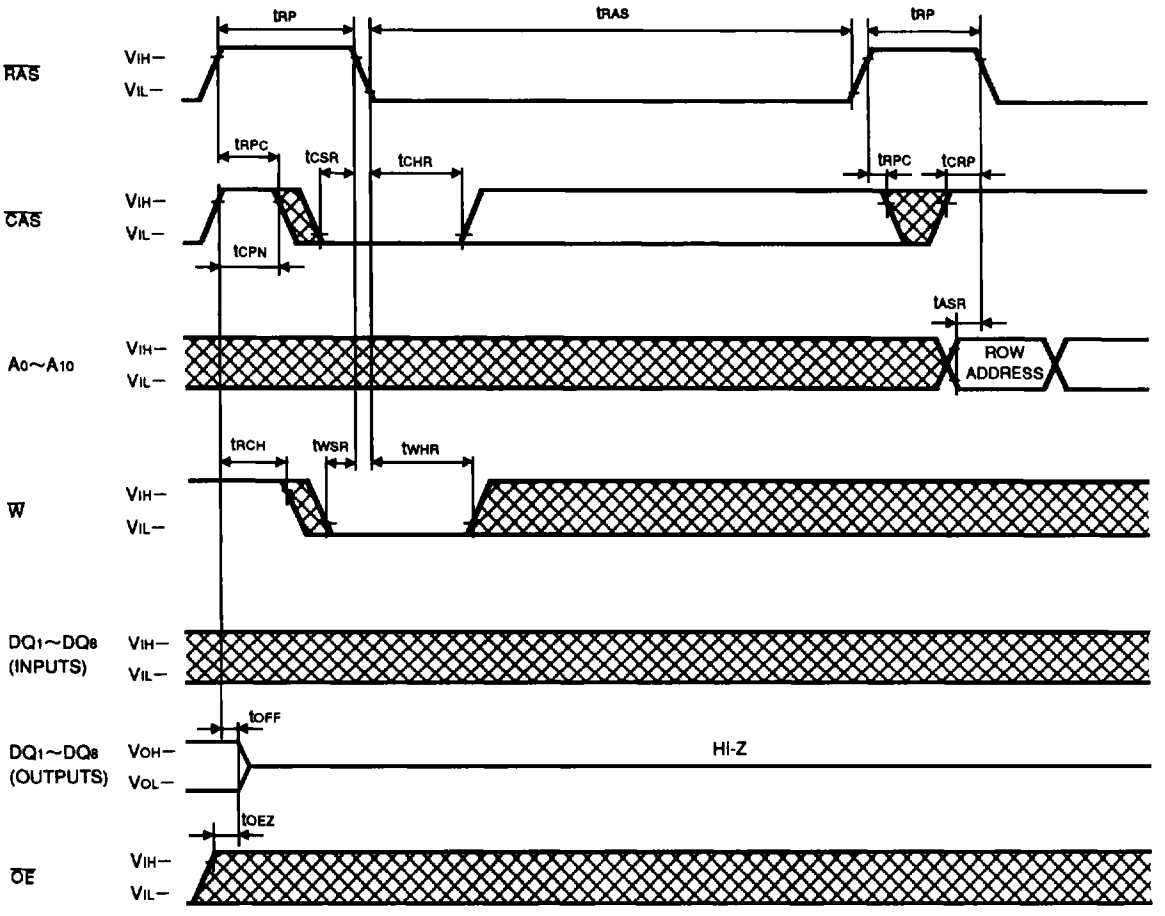


Note 33: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
In all cases tRSR and tRHR should be satisfied.

Self Refresh Cycle



TEST Mode SET Cycle



Note 34: This cycle can be used for initialized cycle after power-up , however entried into Test Mode.