RF5603

3.0V TO 5.0V, 3.3GHz TO 3.8GHz LINEAR POWER AMPLIFIER

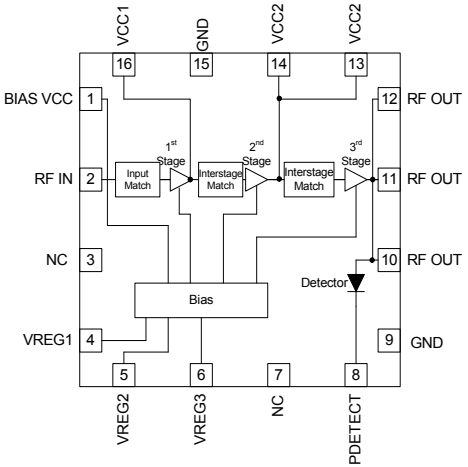
Package Style: QFN, 16-Pin, 3mmx3mmx0.45mm

Features

- Single 3.0V to 5.0V Supply
- 32dB Small Signal Gain (Typ.)
- 2.75% EVM (RMS) at 24dBm, 3.3V
- 2.5% EVM (RMS) at 26dBm, 5.0V
- Internal Power Detector

Applications

- Final Stage PA for Medium Power 3.3GHz to 3.8GHz WiMAX Systems
- Driver Amp for Higher Power WiMAX Access Points



Functional Block Diagram

Product Description

The RF5603 is a linear power amplifier IC designed specifically for WiMAX medium power applications. The device is manufactured on an advanced InGaP Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 802.16e transmitters. The device is provided in a 3mmx3mmx0.45mm, 16-pin, leadless chip carrier with a backside ground. The RF5603 is designed to maintain linearity over a wide range of conditions and power outputs.

Ordering Information

RF5603	3.0V to 5.0V, 3.3GHz to 3.8GHz Linear Power Amplifier
RF5603L33PCK-410	3.3GHz to 3.6GHz WiMAX Fully Assembled PCB at 3.3V
RF5603H33PCK-410	3.6GHz to 3.8GHz WiMAX Fully Assembled PCB at 3.3V
RF5603L50PCK-410	3.3GHz to 3.6GHz WiMAX Fully Assembled PCB at 5.0V
RF5603H50PCK-410	3.6GHz to 3.8GHz WiMAX Fully Assembled PCB at 5.0V

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF Applied)	-0.5 to +5.25	V
Supply Voltage (No RF Applied)	-0.5 to +6.0	V
DC Supply Current	1000	mA
Input RF Power	+10*	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	MSL1, 260C rating, 3X reflow	

*Note: Maximum input power with a 50Ω load.

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Compliance WiMAX IEEE802.16e					Nominal Condition T=25 °C, V_{CC}=3.3V, V_{REG}=2.85V, Freq=Full frequency range, using a standard IEEE802.16e 16QAM 10MHz BW waveform at 37% duty cycle unless otherwise noted
Frequency Range	3.3		3.6	GHz	
	3.6		3.8	GHz	
Output Power	23	24		dBm	Over temperature -40°C to +85°C
EVM		2.75	4	%	At Rated Output Power
Current					
Operating		425	500	mA	At P_{OUT}=24dBm, V_{CC}=3.3V, across V_{REG} 2.75V to 2.95V
Quiescent		250	300	mA	V_{CC}=3.3V, V_{REG}=2.85V, RF=Off
I_{REG}		5	10	mA	Across all conditions
Leakage		0.5	1	uA	V_{CC}=3.3V, V_{REG}=0V, RF=Off
Gain	29	32.5	36	dB	At Rated Output Power, across V_{REG} 2.75V to 2.95V
Gain Variation over Temperature			±2.5	dB	-40°C to +85°C
Low Gain Mode (Gain Reduction)		TBD		dB	At V_{CC}=3.3V, V_{REG} 1 and 3=2.85V, V_{REG} 2=Low and Temp=25°C (In this mode the gain of the power amplifier drop by TBD typical from its original gain)
Power Detector	10		29	dBm	Useable power detection range
Input Return Loss		-15	-10	dB	
Output P1dB		TBD		dB	With CW signal at V_{CC}=3.3V
Turn-On Time from Setting of VREG		0.5	1	usec	Output stable to within 90% of final gain
Compliance WiMAX IEEE802.16e					Nominal Condition T=25 °C, V_{CC}=5.0V, V_{REG}=2.85V, Freq=Full frequency range, using a standard IEEE802.16e 16QAM 10MHz BW waveform at 37% duty cycle unless otherwise noted
Frequency Range	3.3		3.6	GHz	
	3.6		3.8	GHz	
Output Power	24.5	26		dBm	Over temperature -40°C to +85°C
EVM		2.5	3.5	%	At Rated Output Power

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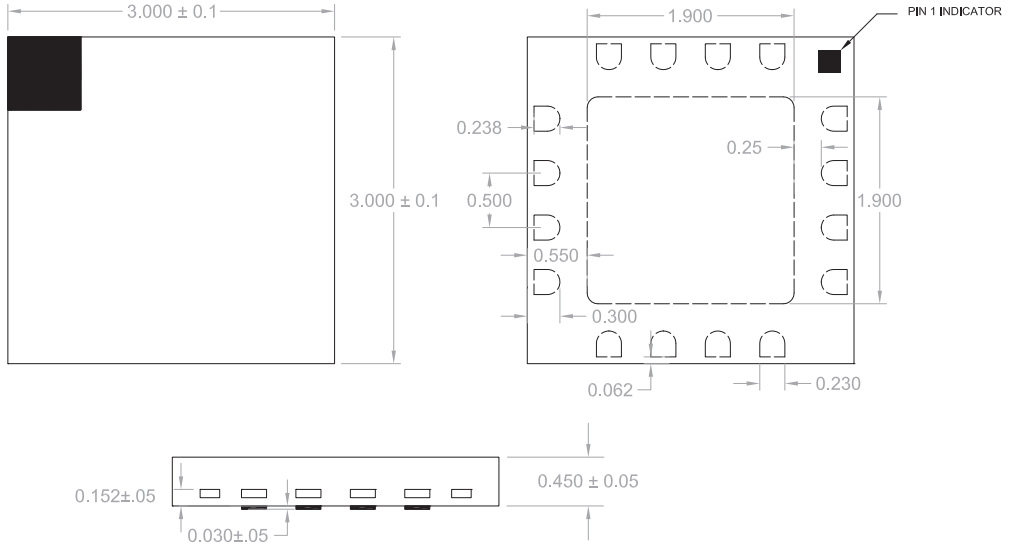
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Compliance WiMAX IEEE802.6e, cont.					Nominal Condition T=25 °C, V_{CC}=5.0V, V_{REG}=2.85V, Freq=Full frequency range and duty cycle=37.09% unless otherwise specified.
Current					
Operating		580	700	mA	At P_{OUT}=26dBm, V_{CC}=5.0V, across V_{REG} 2.75V to 2.95V
Quiescent		370	420	mA	V_{CC}=5.0V, V_{REG}=2.85V, RF=Off
I_{REG}		5	10	mA	Across all conditions
Leakage		0.5	1	uA	V_{CC}=5.0V, V_{REG}=0V, RF=Off
Gain	31	34	37	dB	At Rated Output Power, across V_{REG} 2.75V to 2.95V
Gain Variation Over Temperature			±2.5	±dB	-40°C to +85°C
Low Gain Mode (Gain Reduction)		TBD		dB	At V_{CC}=5.0V, V_{REG} 1 and 3=2.85V, V_{REG2}=Low and Temp=25°C (In this mode the gain of the power amplifier drops by TBD typical from its original gain)
Power Detector	10		29	dBm	Useable power detection range
Input Return Loss		-15	-10	dB	
Output P1dB		TBD		dB	With CW signal at V_{CC}=5.0V
Turn-On Time from Setting of V_{REG}		0.5	1	usec	Output stable to within 90% of final gain

Pin	Function	Description
1	BIAS VCC	Supply voltage for the bias reference and control circuits. May be connected with VCC1 and VCC2 as long as V_{CC} does not exceed $5.0V_{DC}$ in this configuration.
2	RF IN	RF input, internally matched and DC block is provided.
3, 7, 9, 15	NC	Not connected. May be connected to ground.
4	VREG1	First stage input bias voltage. This pin requires a regulated supply to maintain nominal bias current.
5	VREG2	Second stage input bias voltage. This pin requires a regulated supply to maintain nominal bias current.
6	VREG3	Third stage input bias voltage. This pin requires a regulated supply to maintain nominal bias current.
8	P DETECT	Power detector provides an output voltage proportional to the RF output power level.
10, 11, 12	VCC3/ RF OUT	RF output and bias for the output stage. Output is externally matched to 50Ω and needs DC block.
13, 14	VCC2	Second stage supply voltage.
16	VCC1	First stage supply voltage.
Pkg Base	GND	Ground connection. The back side of the package should be connected to the ground plane through as short a connection as possible, e.g., PCB vias under the device are recommended.

Package Outline



NOTES:
1 Shaded Area is Pin 1 Indicator

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PCB Design Requirements

PCB Surface Finish

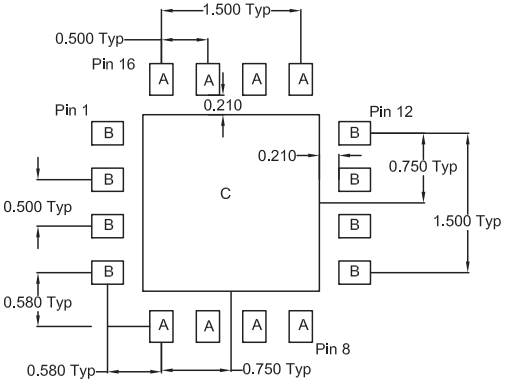
The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

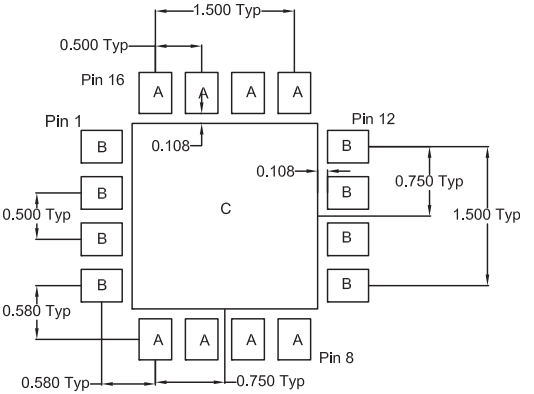
PCB Metal Land and Solder Mask Pattern

A = 0.250 x 0.340 (mm) Typ
B = 0.340 x 0.250 (mm) Typ
C = 1.900 (mm) Sq



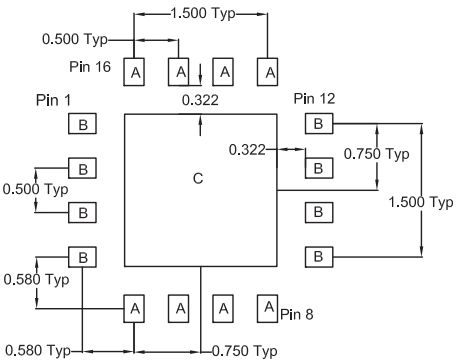
PCB METAL LAND PATTERN

A = 0.352 x 0.442 (mm) Typ
B = 0.442 x 0.352 (mm) Typ
C = 2.030 (mm) Sq



PCB SOLDER MASK PATTERN

A = 0.225 x 0.306 (mm) Typ
B = 0.306 x 0.225 (mm) Typ
C = 1.710 (mm) Sq



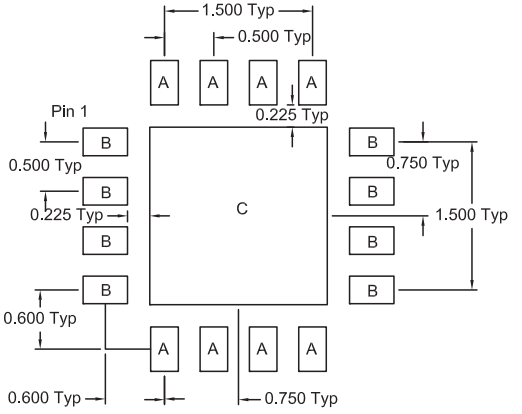
PCB STENCIL PATTERN

Thermal vias for center slug “C” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application. Example of the number and size of vias can be found on the RFMD evaluation board layout.

PCB Metal Land and Solder Mask Pattern

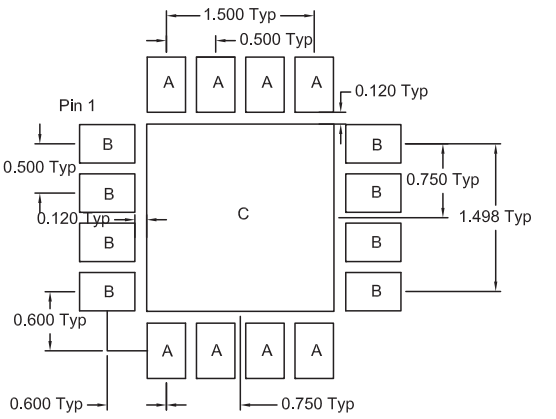
Note: If it is desired to build the same PCB to accommodate the RF5602 as well as the RF5623/RF5603 use the following PCB Patterns.

A = 0.280 x 0.450 (mm) Typ
B = 0.450 x 0.280 (mm) Typ
C = 1.800 (mm) Sq



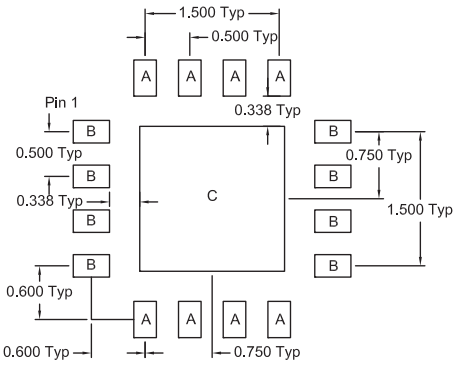
PCB METAL LAND PATTERN

A = 0.390 x 0.560 (mm) Typ
B = 0.560 x 0.390 (mm) Typ
C = 1.900 (mm) Sq



PCB SOLDER MASK PATTERN

A = 0.252 x 0.405 (mm) Typ
B = 0.405 x 0.252 (mm) Typ
C = 1.620 (mm) Sq



PCB STENCIL PATTERN

Note: Thermal vias for center slug “C” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application. Example of the number and size of vias can be found on the RFMD evaluation board layout.

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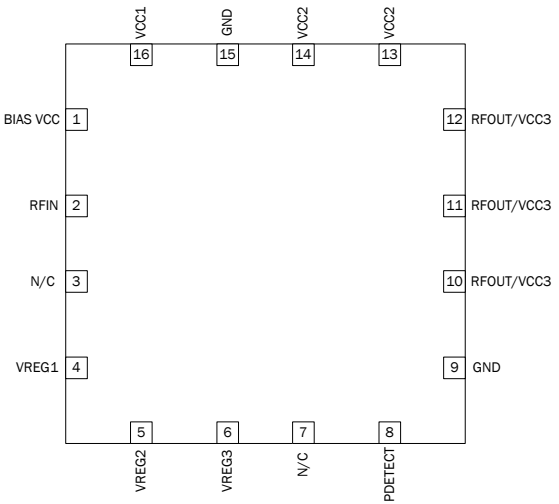
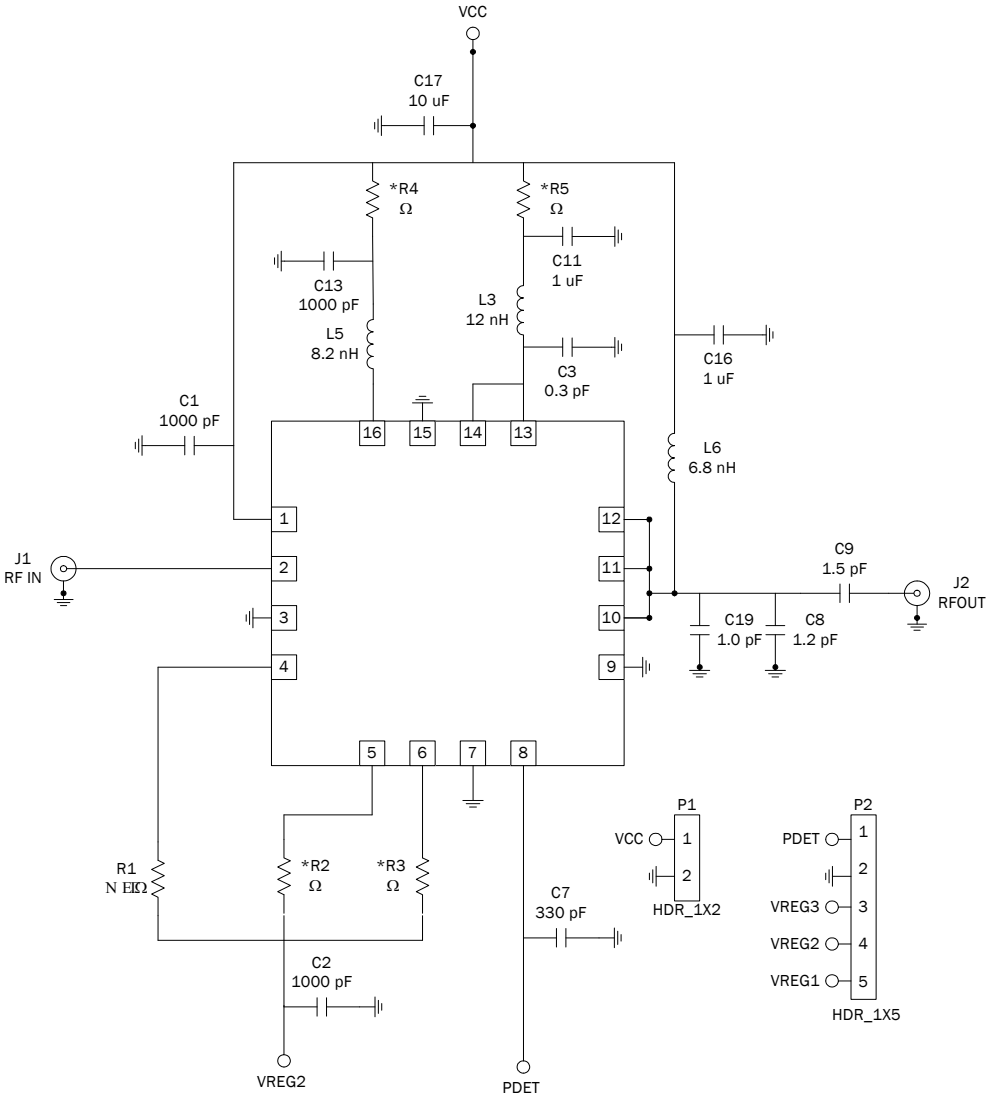
Pin Out


VCC1
GND
VCC2
VCC2
16
15
14
13
BIAS VCC 1
RFIN 2
N/C 3
VREG1 4
12 RFOUT/VCC3
11 RFOUT/VCC3
10 RFOUT/VCC3
9 GND
5
6
7
8
VREG2
VREG3
N/C
PDETECT

3.3GHz to 3.6GHz Schematic



*	VCC(V)	R1(Ohms)	R2(Ohms)	R3(Ohms)	R4(Ohms)	R5(Ohms)
	3.3	220	180	56	0	0
	5.0	220	75	0	56	5.1

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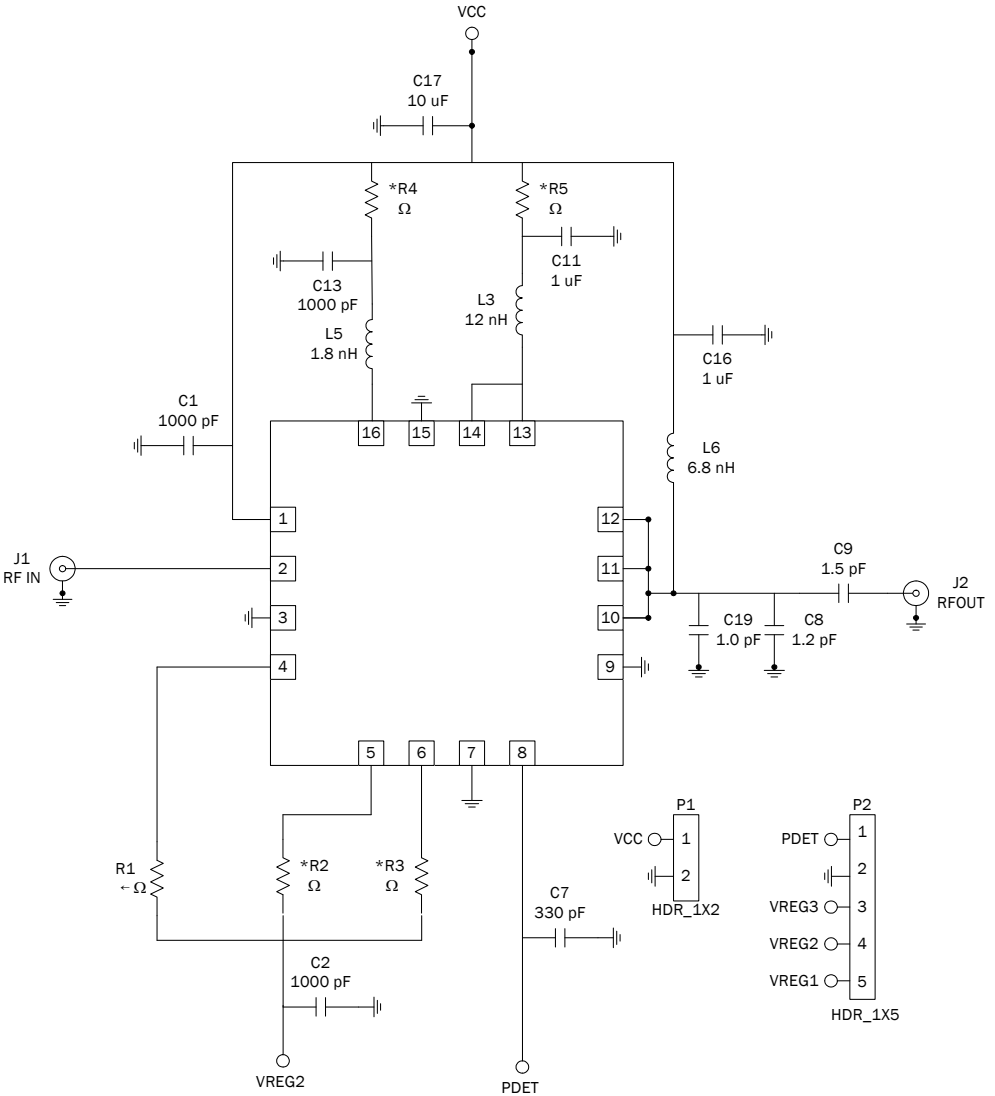
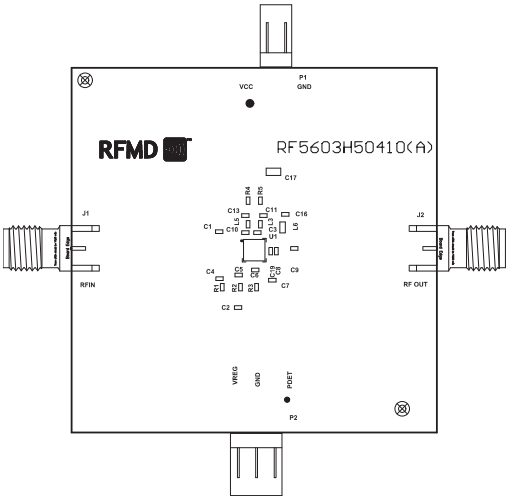
3.6GHz to 3.8GHz Schematic



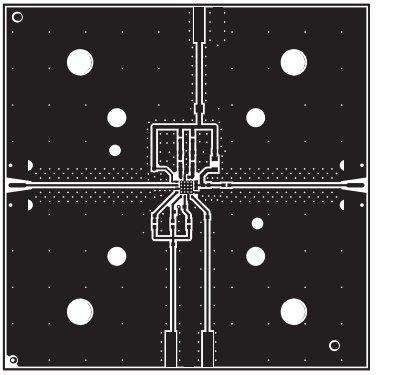
*

VCC(V)	R1(Ohms)	R2(Ohms)	R3(Ohms)	R4(Ohms)	R5(Ohms)
3.3	220	180	56	0	0
5.0	220	75	0	56	5.1

Evaluation Board Layout



Assembly



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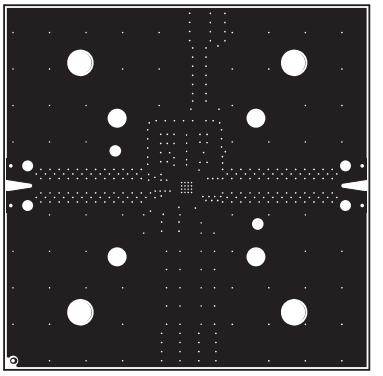
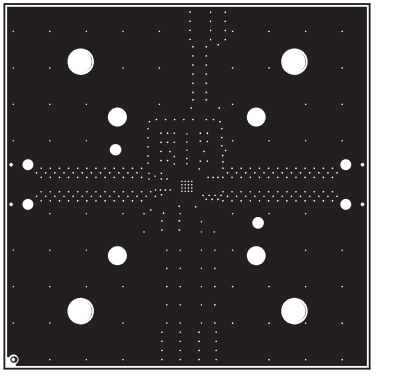


Inner 1



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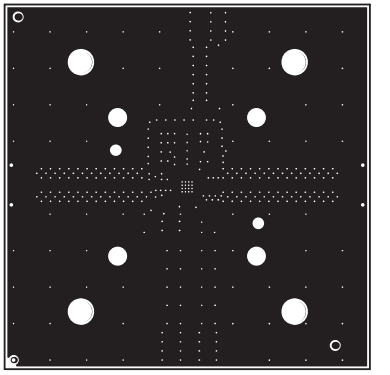

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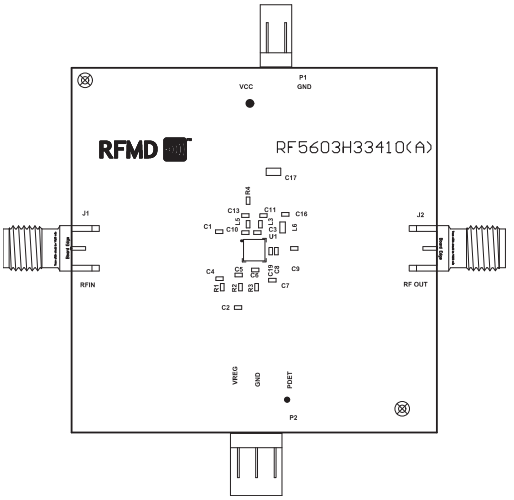
Evaluation Board Layout



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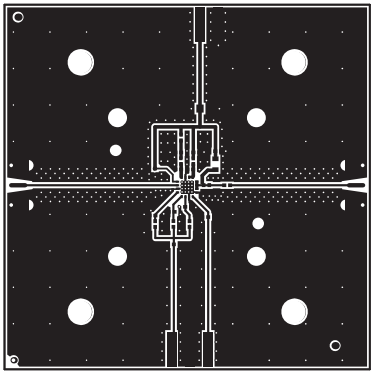

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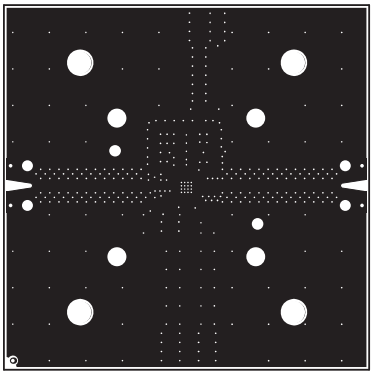

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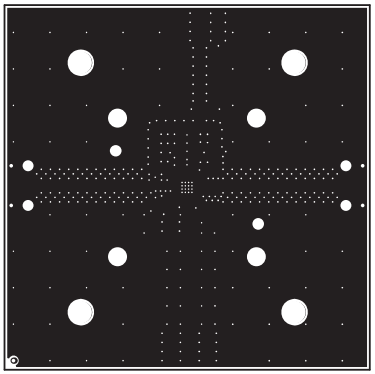

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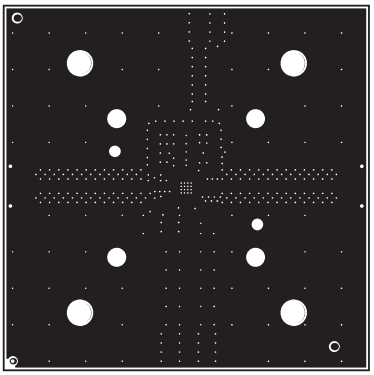

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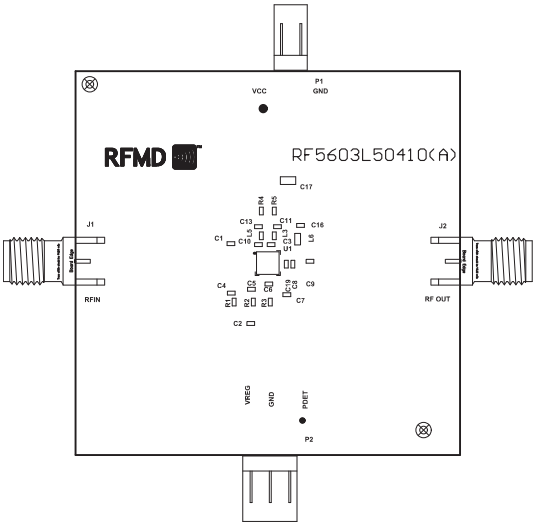
Evaluation Board Layout



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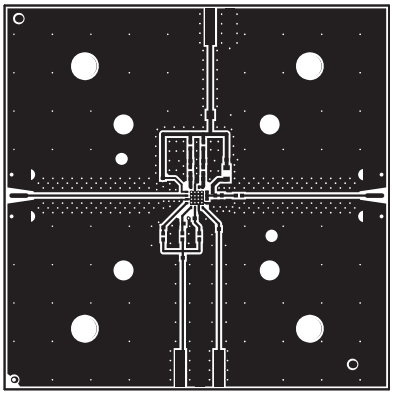

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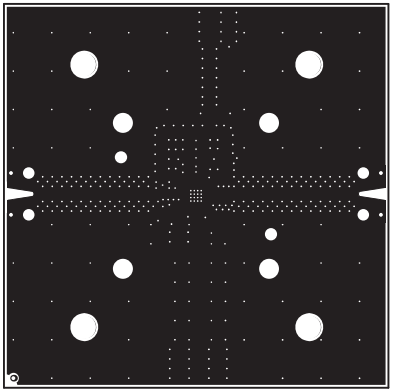

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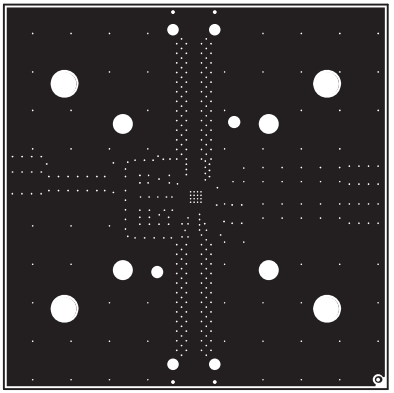

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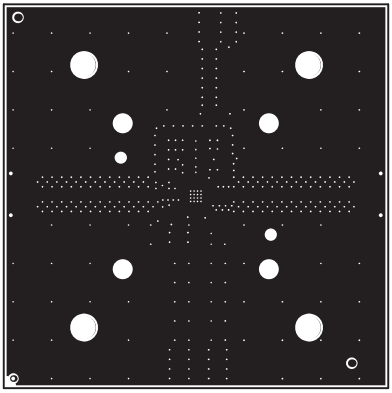

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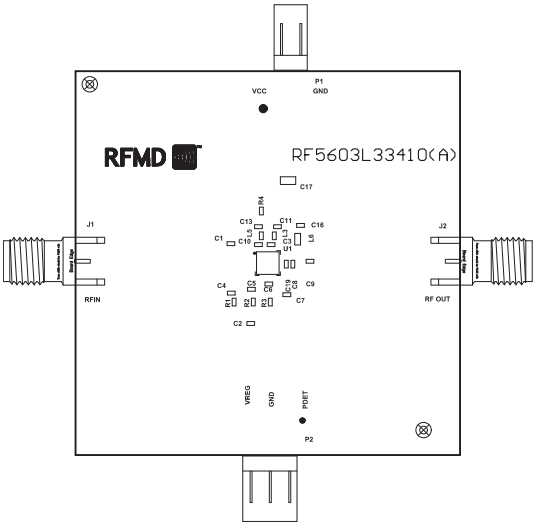
Evaluation Board Layout



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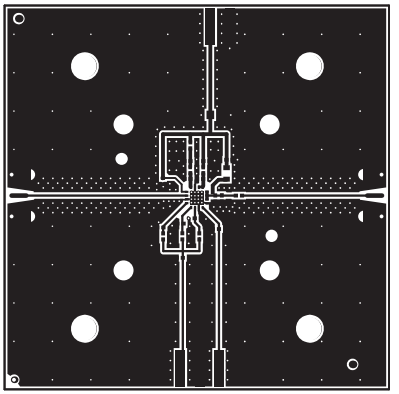

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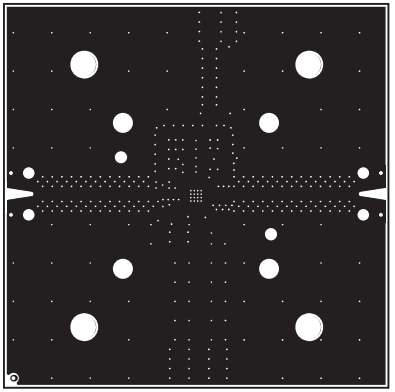

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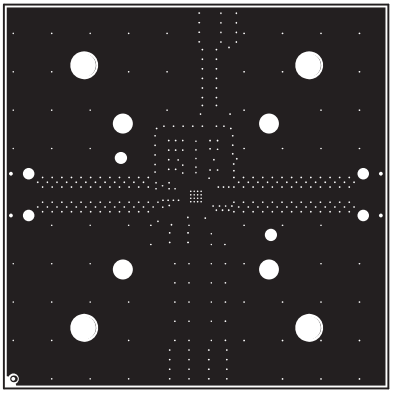

Inner 2

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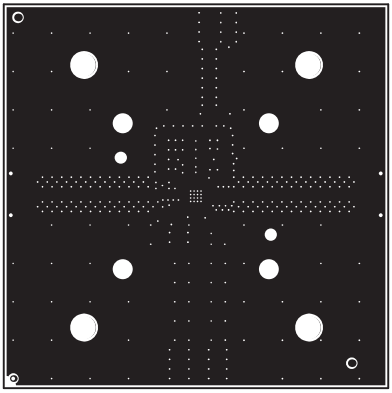

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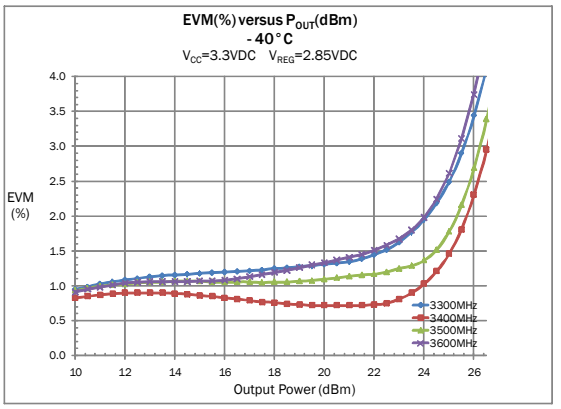
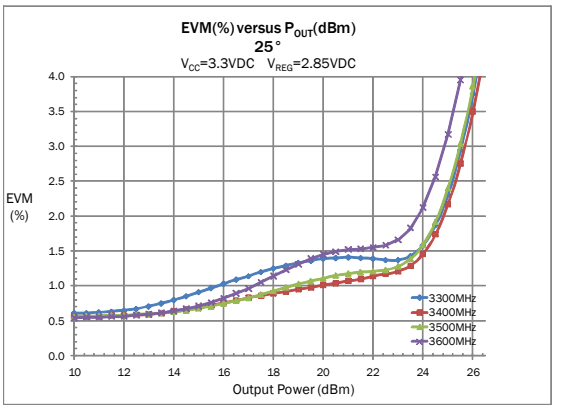
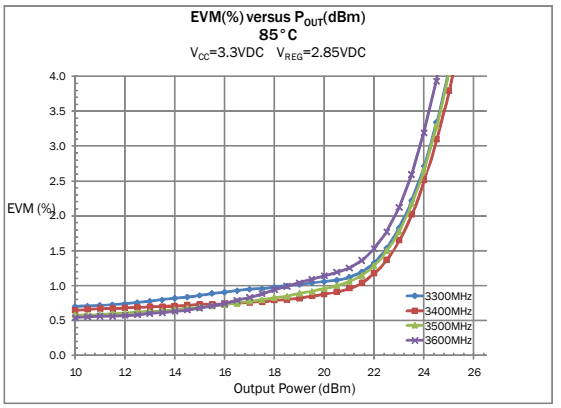
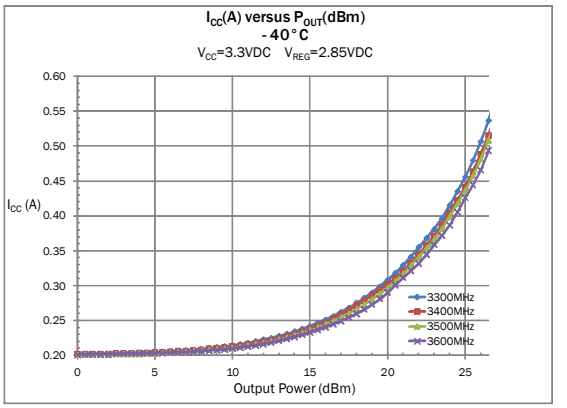
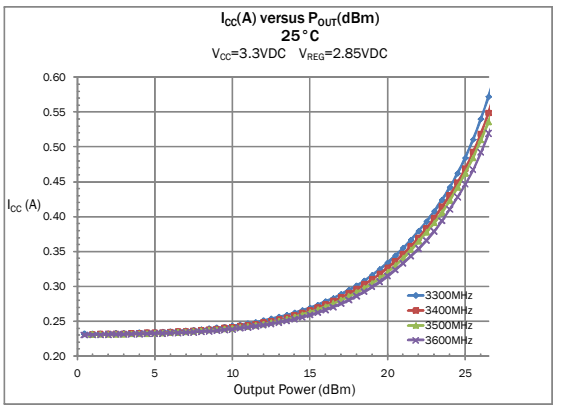
3.3GHz to 3.6GHz

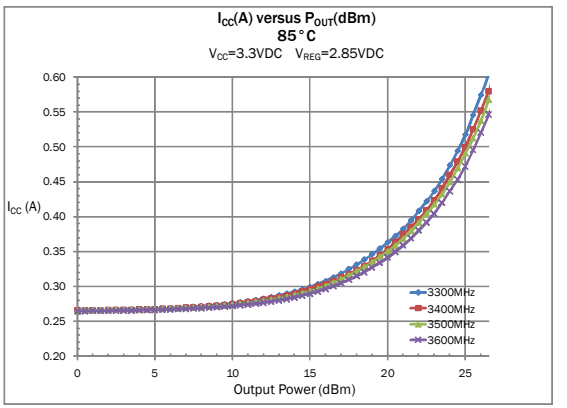












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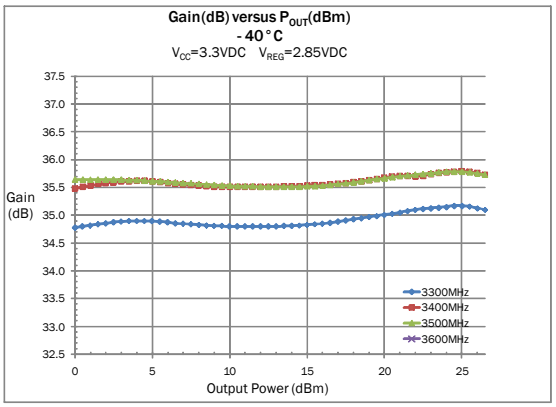
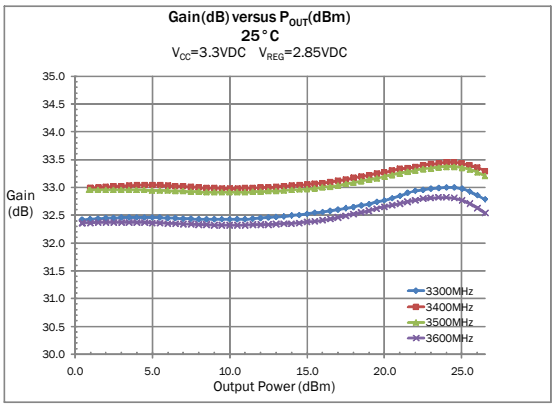
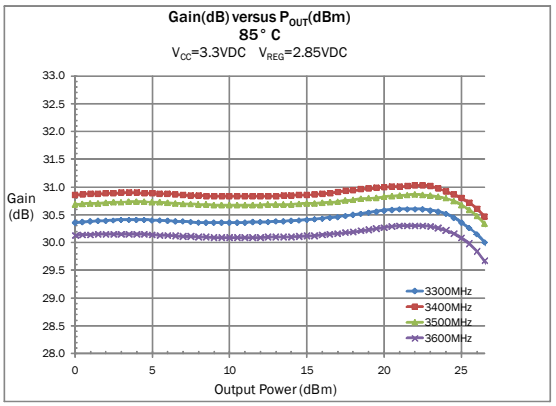
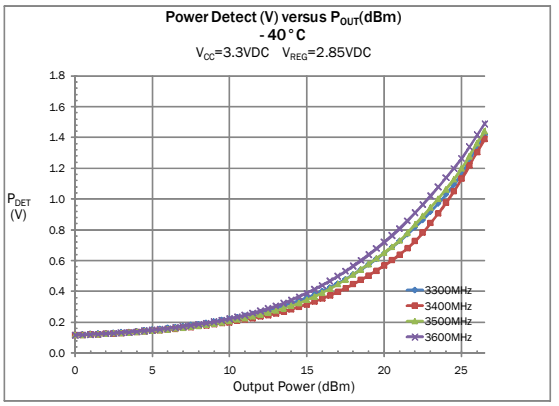
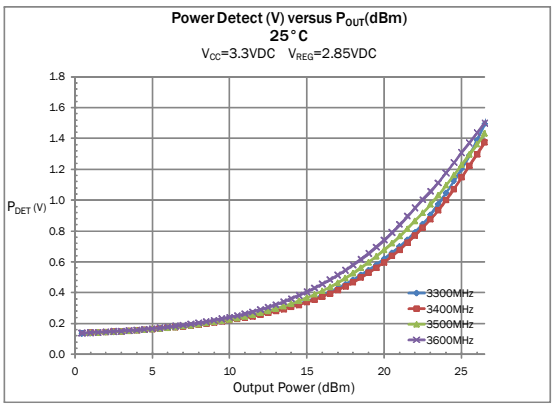
3.3GHz to 3.6GHz

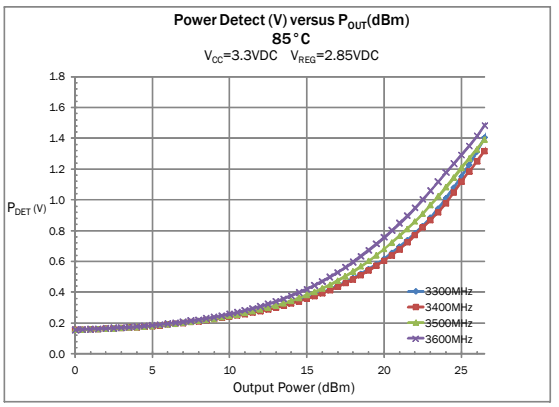




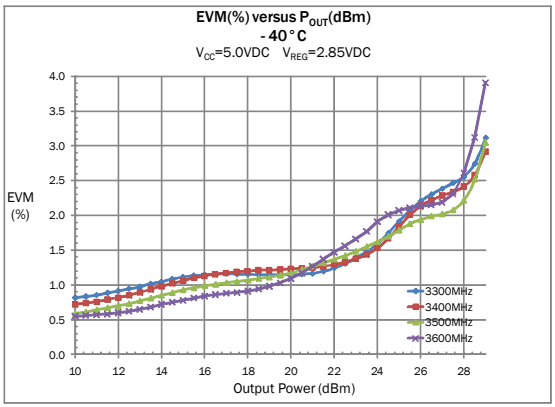


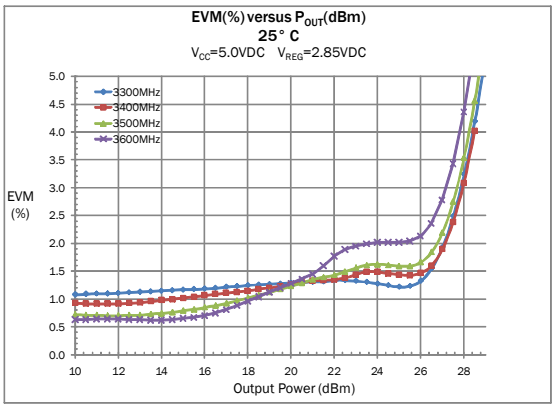


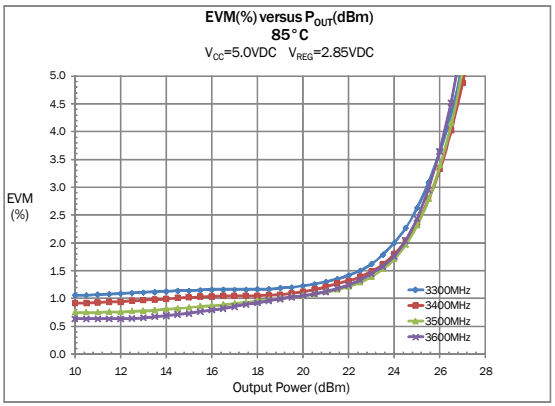


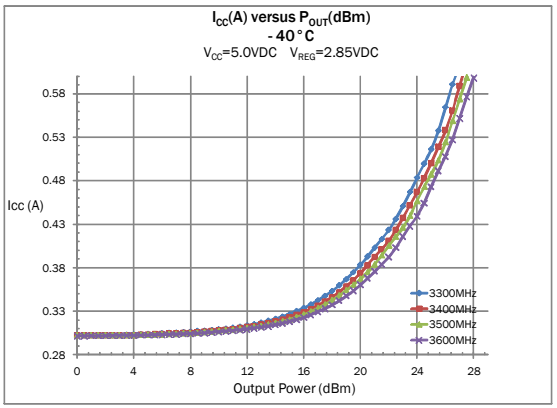


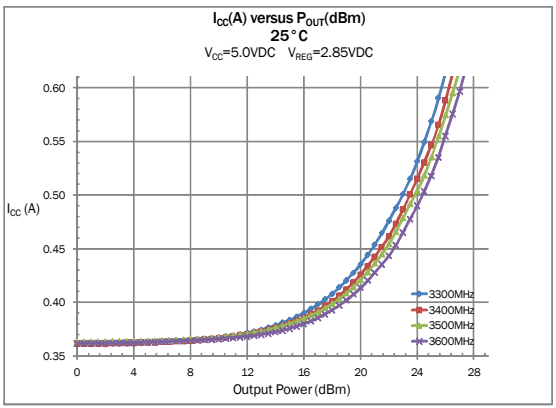
3.3GHz to 3.6GHz

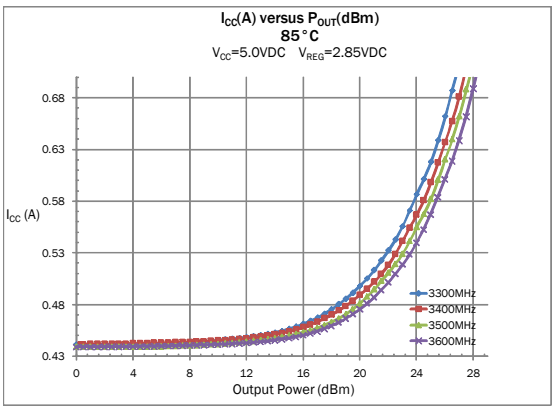












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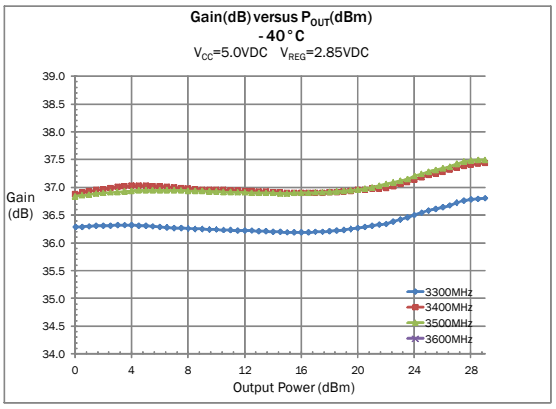
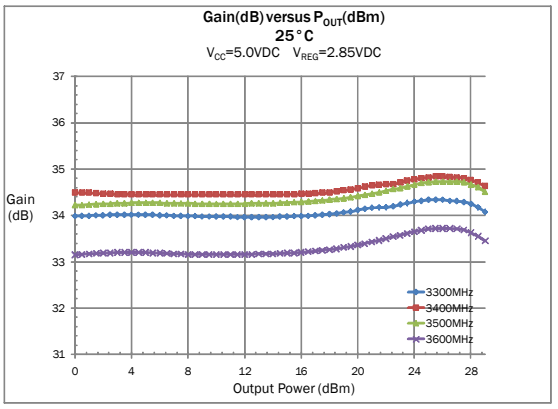
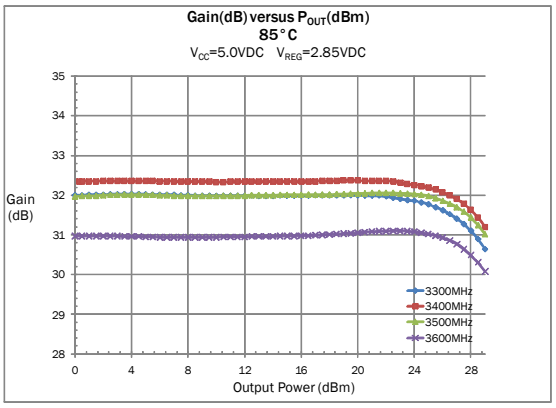
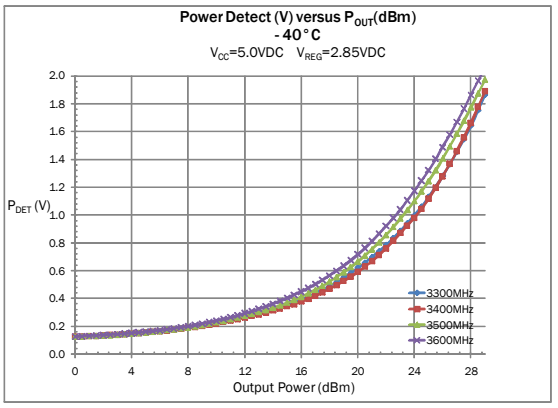
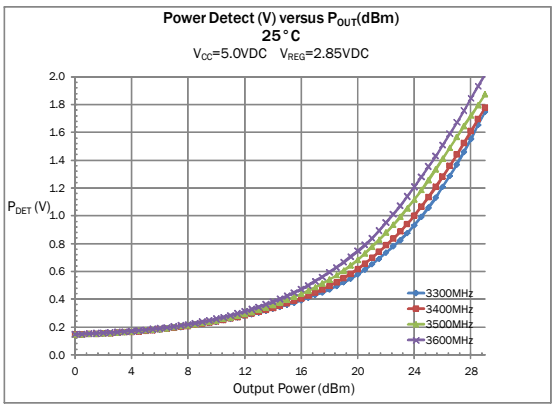
3.3GHz to 3.6GHz

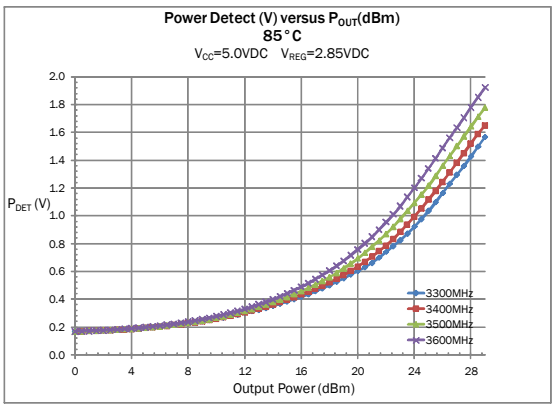




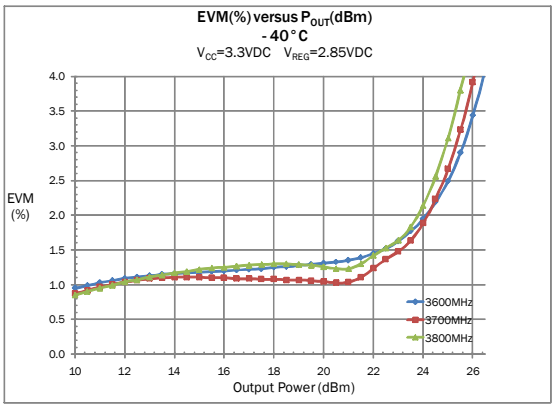


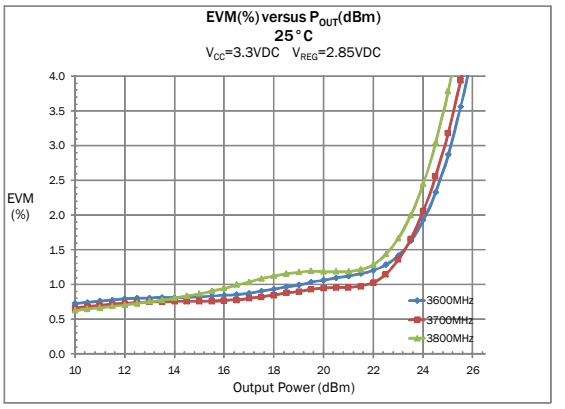


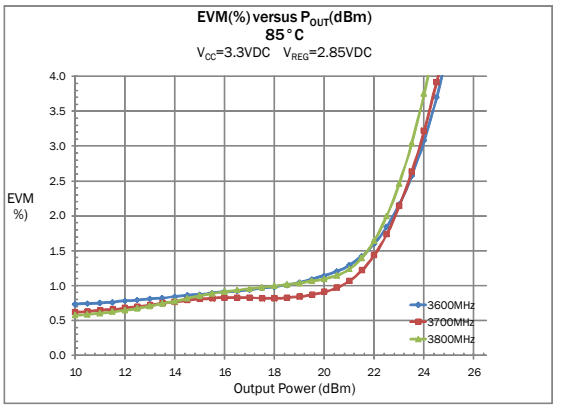


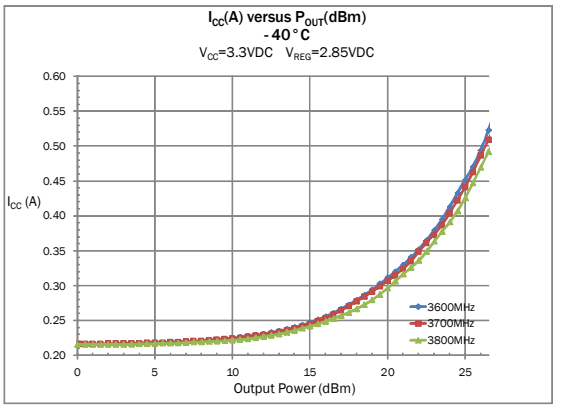


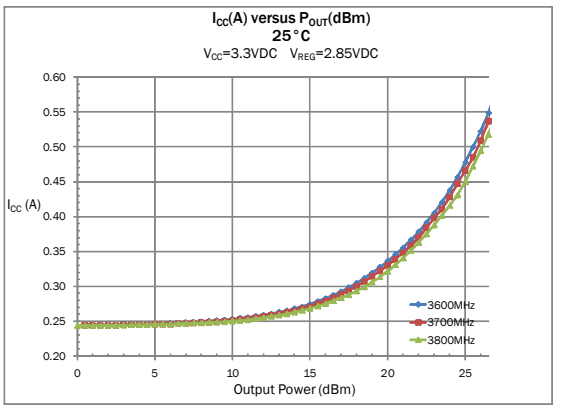
3.6GHz to 3.8GHz

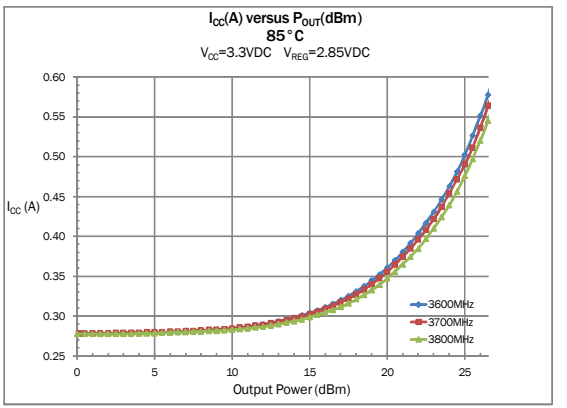












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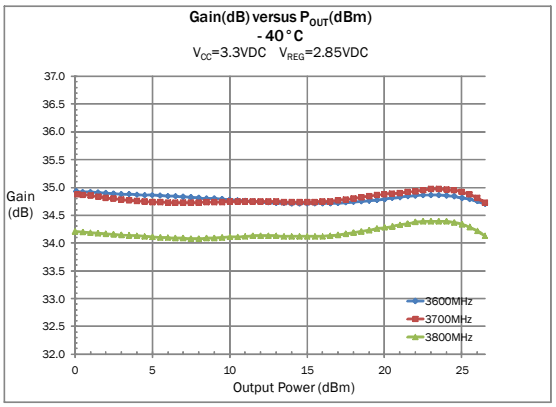
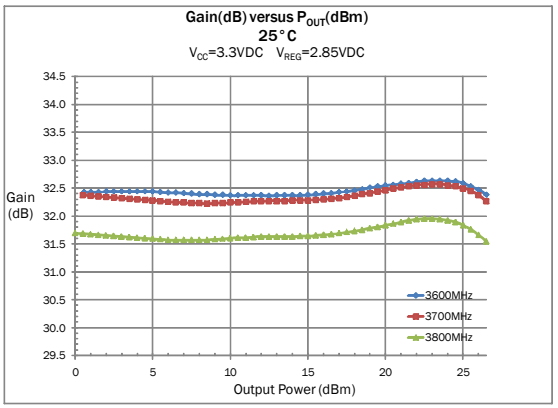
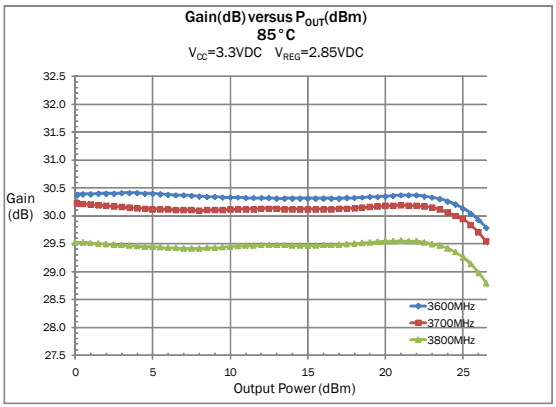
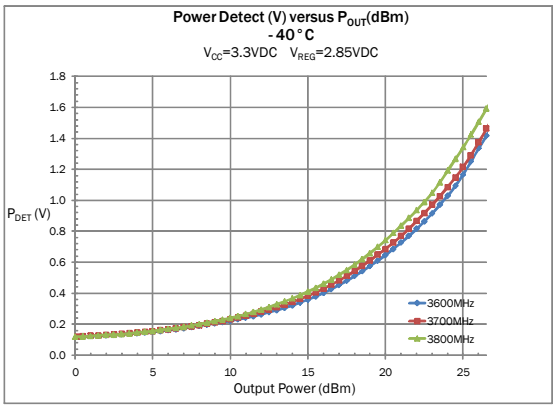
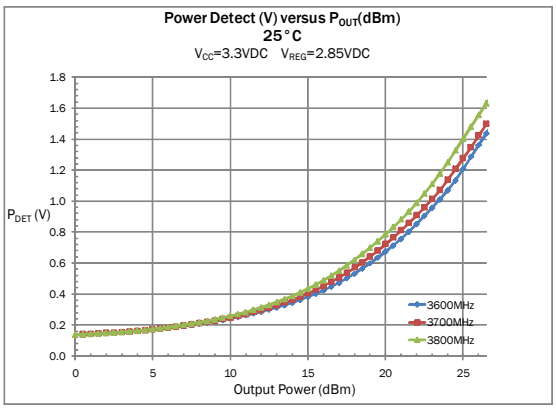
3.6GHz to 3.8GHz

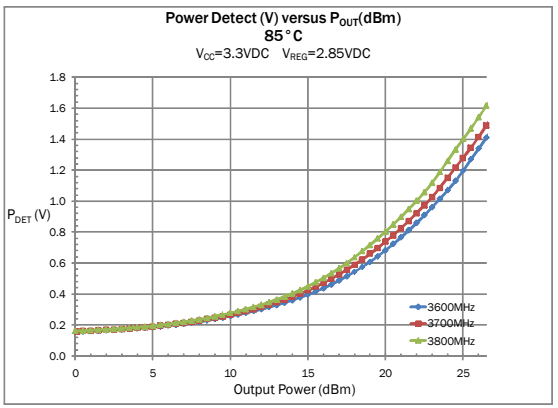




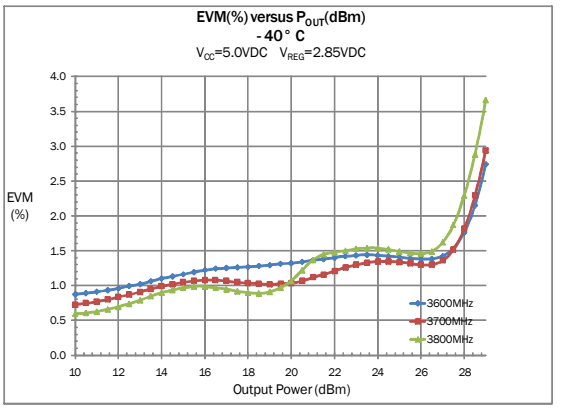


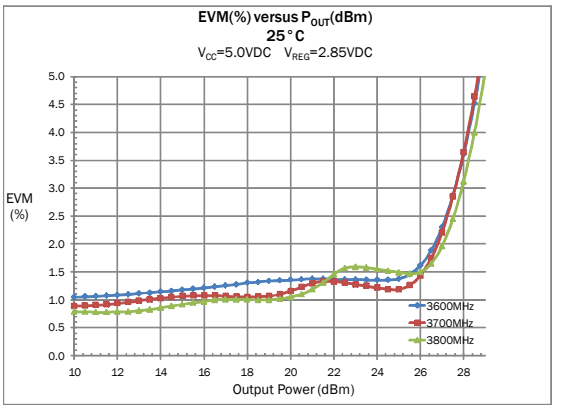


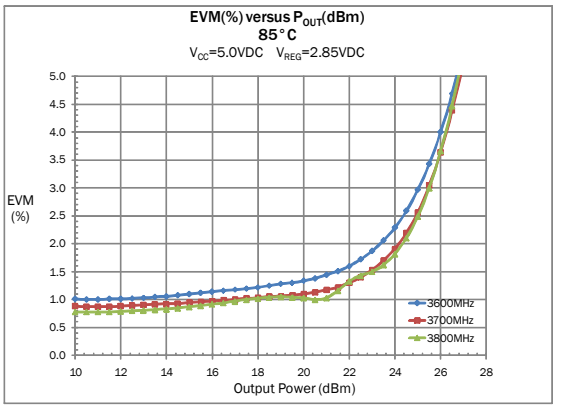


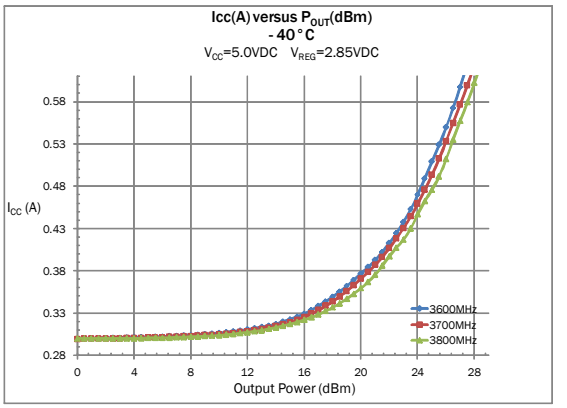


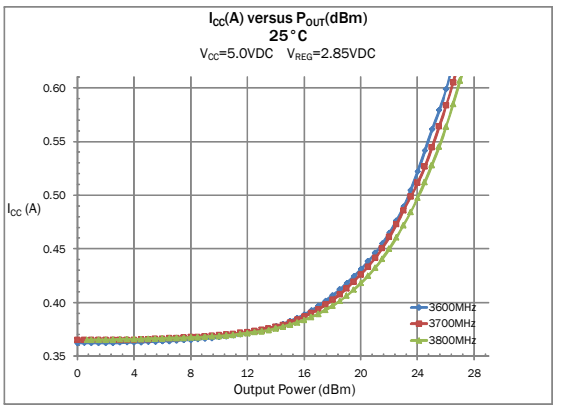
3.6GHz to 3.8GHz

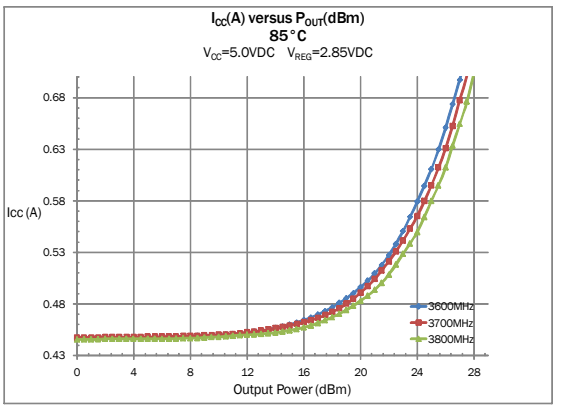












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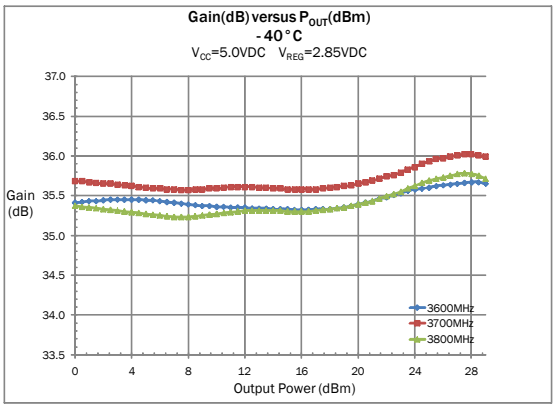
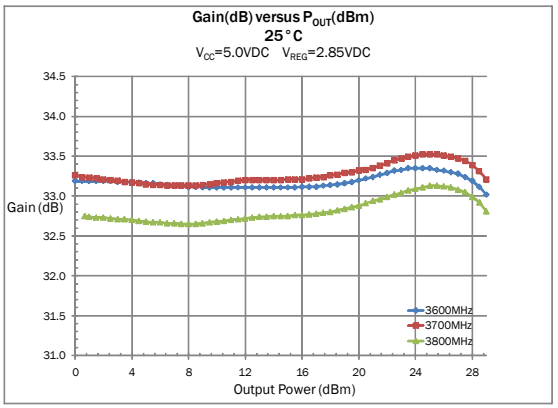
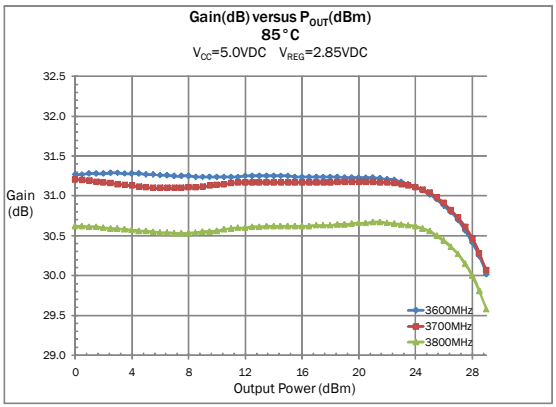
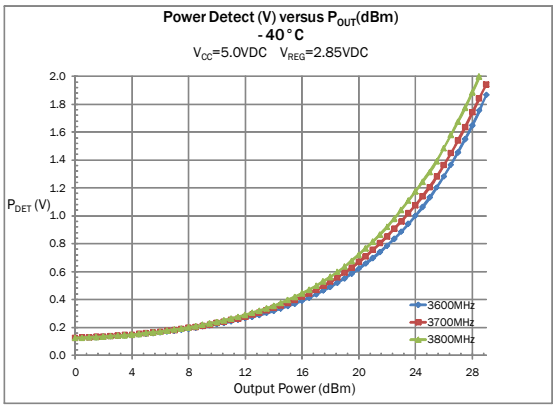
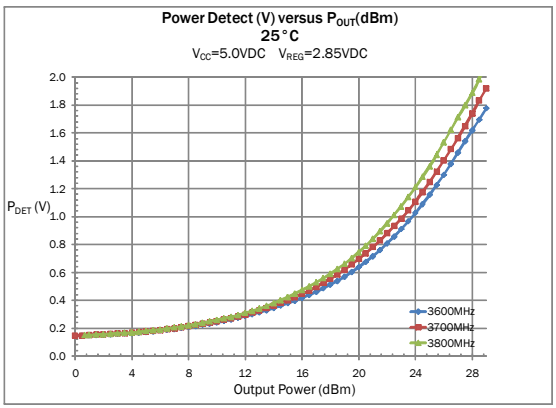
3.6GHz to 3.8GHz

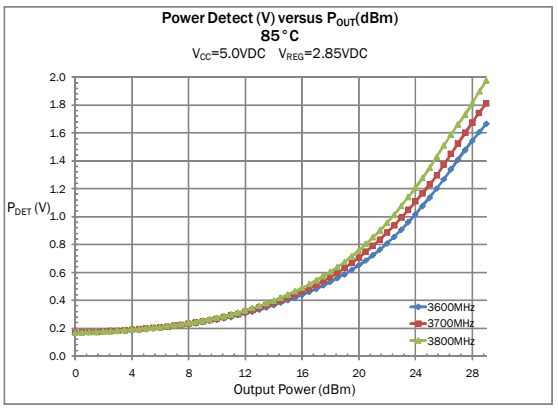












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