

SPP3401

DESCRIPTION

The SPP3401 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

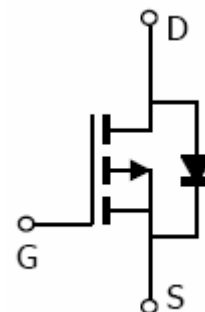
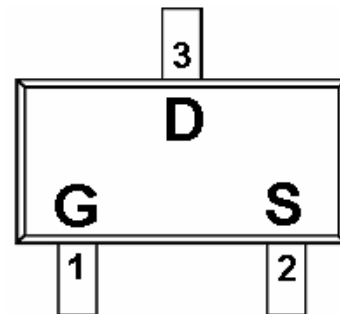
FEATURES

- ◆ -30V/-4.0A, $R_{DS(ON)}=55m\Omega@V_{GS}=-10V$
- ◆ -30V/-3.2A, $R_{DS(ON)}=65m\Omega@V_{GS}=-4.5V$
- ◆ -30V/-1.2A, $R_{DS(ON)}=75m\Omega@V_{GS}=-2.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23-3L package design

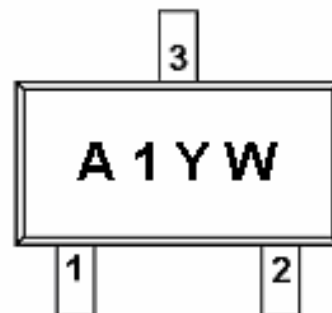
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23-3L)



PART MARKING



Y : Year Code
W : Week Code

SPP3401

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3401S23RG	SOT-23-3L	A1YW

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPP3401S23RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-30	V
Gate –Source Voltage	V _{GSS}	±12	V
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-4.0
		TA=70°C	-3.2
Pulsed Drain Current	I _{DM}	-15	A
Continuous Source Current(Diode Conduction)	I _S	-1.0	A
Power Dissipation	P _D	TA=25°C	1.25
		TA=70°C	0.8
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	120	°C/W

SPP3401

ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4		-1.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq -5V, V_{GS}=-10V$	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-4.0A$		0.045	0.055	Ω
		$V_{GS}=-4.5V, I_D=-3.2A$		0.050	0.065	
		$V_{GS}=-2.5V, I_D=-1.2A$		0.060	0.075	
Forward Transconductance	g_{fs}	$V_{DS}=-5.0V, I_D=-4.0A$		10		S
Diode Forward Voltage	V_{SD}	$I_S=-1.0A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-15V, V_{GS}=-10V$ $I_D=-4.0A$		14	21	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			3.7		
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		540		pF
Output Capacitance	C_{oss}			131		
Reverse Transfer Capacitance	C_{rss}			105		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=15\Omega$ $I_D=-1.0A, V_{GEN}=-10V$ $R_G=6\Omega$		10	15	ns
	t_r			15	25	
Turn-Off Time	$t_{d(off)}$			31	50	
	t_f			20	30	