Preliminary

3.3V LVDS 1:4 Clock Fanout Buffer AK8181G

Features

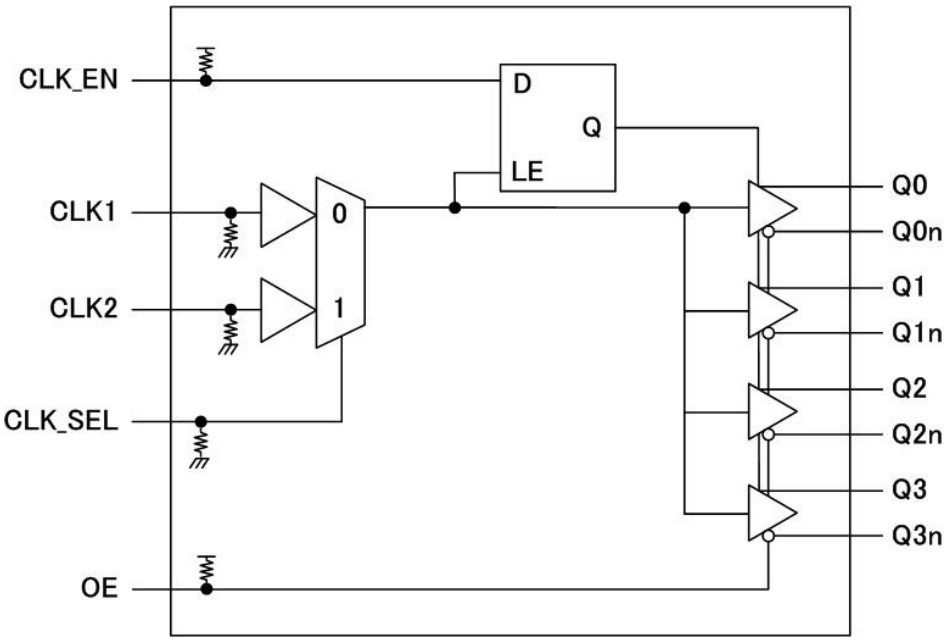
- Four differential 3.3V LVDS outputs
- Selectable two LVCMOS/LVTTL clock inputs
- Clock output frequency up to 650MHz
- Translates LVCMOS/LVTTL input signals to LVDS levels
- Output skew : 30ps (maximum)
- Part-to-part skew : 500ps (maximum)
- Propagation delay : 2.2ns (maximum)
- Additive phase jitter(RMS): 0.1ps (typical)
- Operating Temperature Range: -40 to +85℃
- Package: 20-pin TSSOP (Pb free)
- Pin compatible with ICS8545I

Description

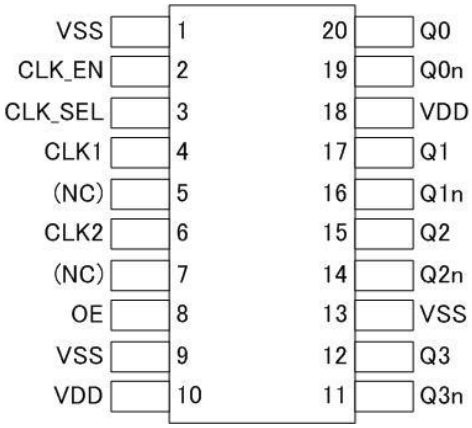
The AK8181G is a member of AKM's LVDS clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8181G distributes 4 buffered clocks.

AK8181G are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew. The AK8181G is available in a 20-pin TSSOP package.

Block Diagram



Pin Descriptions



Package: 20-Pin TSSOP(Top View)

Pin No.	Pin Name	Pin Type	Pullup down	Description
1	VSS	PWR	---	Negative power supply
2	CLK_EN	IN	Pull up	Synchronizing clock output enable (LVCMOS/LVTTL) Pin is connected to VDD by internal resistor. (typ. 51kΩ) High (Open): clock outputs follow clock input. Low: Q outputs are forced low, Qn outputs are forced high.
3	CLK_SEL	IN	Pull down	CLK Select Input (LVCMOS/LVTTL) Pin is connected to VSS by internal resistor. (typ. 51kΩ) High: selects CLK2 input Low (Open): selects CLK1 input
4	CLK1	IN	Pull down	Single-ended clock input Pin is connected to VSS by internal resistor. (typ. 51kΩ)
5	NC	--	---	No connect
6	CLK2	IN	Pull down	Single-ended clock input Pin is connected to VSS by internal resistor. (typ. 51kΩ)
7	NC	--	---	No connect
8	OE	IN	Pull up	Output enable. Controls enabling and disabling of outputs Q0, Q0n through Q3, Q3n. Pin is connected to VDD by internal resistor. (typ. 51kΩ)
9	VSS	PWR	---	Negative power supply
10	VDD	PWR	---	Positive power supply
11, 12	Q3n, Q3	OUT	---	Differential clock output (LVDS)
13	VSS	PWR	---	Negative power supply
14, 15	Q2n, Q2	OUT	---	Differential clock output (LVDS)
16, 17	Q1n, Q1	OUT	---	Differential clock output (LVDS)
18	VDD	PWR	---	Positive power supply
19, 20	Q0n, Q0	OUT	---	Differential clock output (LVDS)

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8181G	AK8181G	Tape and Reel	20-pin TSSOP	-40 to 85 °C

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.5 to VDD+0.5	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 150	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

(2) VSS=0V

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD	VDD±5%	3.135	3.3	3.465	V

(1) Power of 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}			4		pF
Input Pullup Resistor	R_{PU}			51		kΩ
Input Pulldown Resistor	R_{PD}			51		kΩ

Power Supply Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Current	I_{DD}	CLK1 = input 650MHz CLK2 = open			47	mA
		CLK1 = open CLK2 = input 650MHz			47	mA

DC Characteristics (LVCMOS/LVTTL)

All specifications at VDD=3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage		V_{IH}		2.0		VDD+0.3	V
Input Low Voltage	CLK1, CLK2	V_{IL}		-0.3		1.3	V
	CLK_SEL, OE, CLK_EN,			-0.3		0.8	V
Input High Current	CLK_SEL	I_H	Vin=VDD=3.465V			150	µA
	CLK_EN, OE		Vin=VDD=3.465V			5	µA
Input Low Current	CLK_SEL	I_L	Vin=VSS, VDD=3.465V	-5			µA
	CLK_EN, OE		Vin=VSS, VDD=3.465V	-150			µA

DC Characteristics (Differential)

All specifications at VDD=3.3V±5%, VSS=0V, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Differential Output Voltage	V_{OD}		200	280	360	mV
V_{OD} Magnitude Change	ΔV_{OD}				40	mV
Offset Voltage	V_{OS}		1.125	1.25	1.375	V
V_{OS} Magnitude Change	ΔV_{OS}			5	25	mV
High Impedance Leakage Current	I_{OZ}	OE = Low	-10		+10	µA
Differential Output Short Circuit Current	I_{OSD}			-3.5	-5	mA
Output Voltage High	V_{OH}			1.34	1.6	V
Output Voltage Low	V_{OL}		0.9	1.06		V

AC Characteristics

All specifications at VDD=3.3V±5%, VSS=0V, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Frequency	f_{OUT}				650	MHz
Propagation Delay (1)	t_{PD}		0.7		2.2	ns
Output Skew (2) (3)	$t_{sk(O)}$				30	ps
Part-to-Part Skew (3) (4)	t_{skPP}				500	ps
Buffer Additive Jitter, RMS (5)	t_{jit}	156.25MHz (12kHz – 20MHz)		0.1		ps
Output Rise/Fall Time (5)	t_r, t_f	20% to 80% @50MHz	100		500	ps
Output Duty Cycle	DC_{OUT}		45		55	%

All parameters measured at f ≤ 650MHz unless noted otherwise.

The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

(1) Measured from VDD/2 of the input to the differential output crossing point.

(2) Defined as skew between outputs at the same supply voltage and with equal load conditions.

(3) This parameter is defined in accordance with JEDEC Standard 65.

(4) Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

(5) Design value.

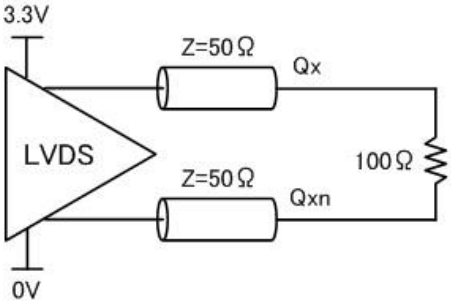


Figure 1 3.3V Output Load Test Circuit

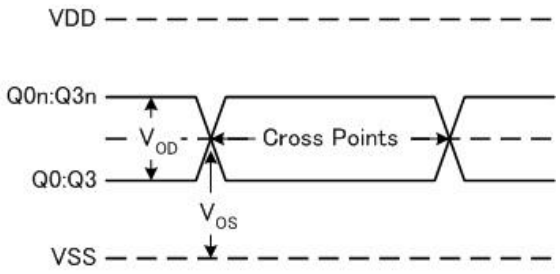


Figure 2 Differential Output Level

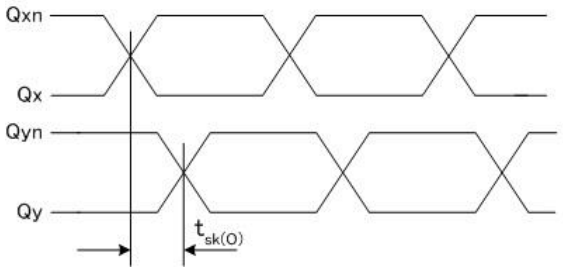


Figure 3 Output Skew

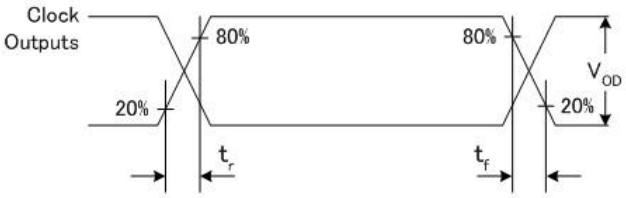


Figure 4 Output Rise/Fall Time

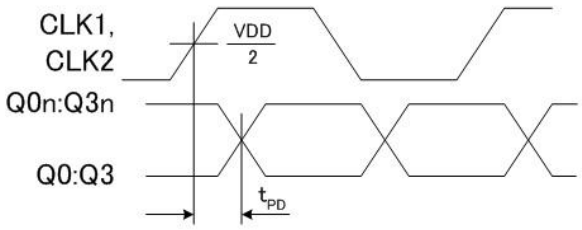


Figure 5 Propagation Delay

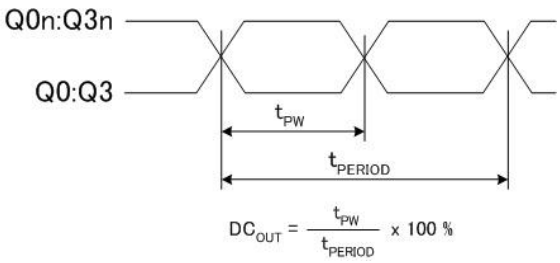


Figure 6 Output Duty/ Pulse Width/ Period

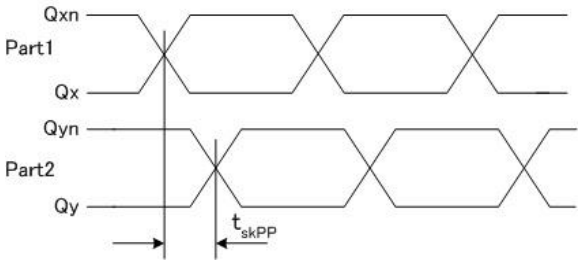


Figure 7 Part-to-Part Skew

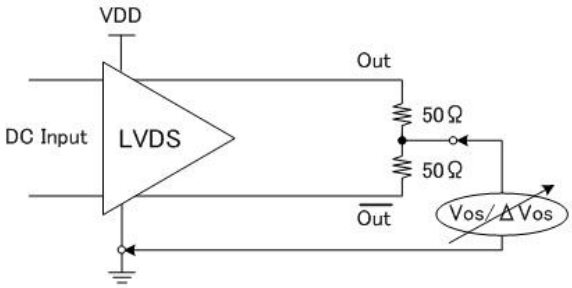


Figure 8 Offset Voltage Setup

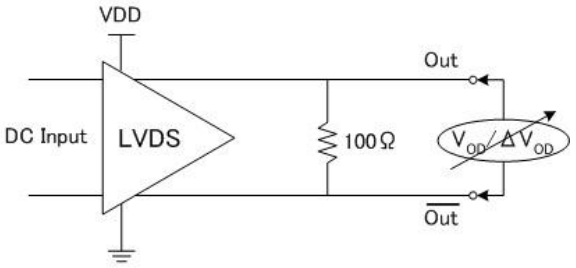


Figure 9 Differential Output Voltage Setup

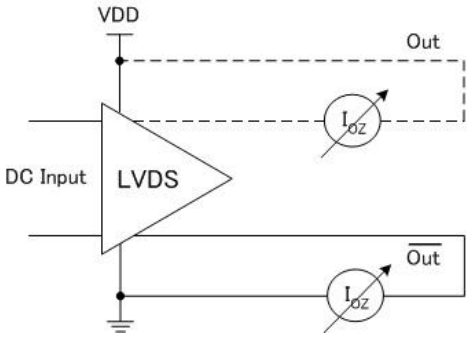


Figure 10 High Impedance Leakage Current Setup

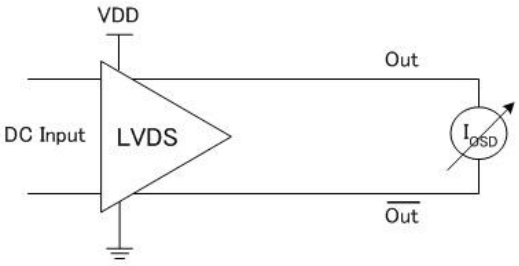


Figure 11 Differential Output Short Circuit Setup

Function Table

The following table shows the inputs/outputs clock state configured through the control pins.

Table 1: Control Input Function Table

Inputs				Outputs	
OE	**CLK_EN**	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**Q0n:Q3n**
1	0	0 (Open)	CLK1	Disabled: Low	Disabled: High
1	0	1	CLK2	Disabled: Low	Disabled: High
1	1 (Open)	0 (Open)	CLK1	Enabled	Enabled
1	1 (Open)	1	CLK2	Enabled	Enabled
0	Don't care	Don't care	---	Hi-Z	Hi-Z

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 12. In the active mode, the state of the outputs are a function of the CLK1 and CLK2 inputs as described in Table 2.

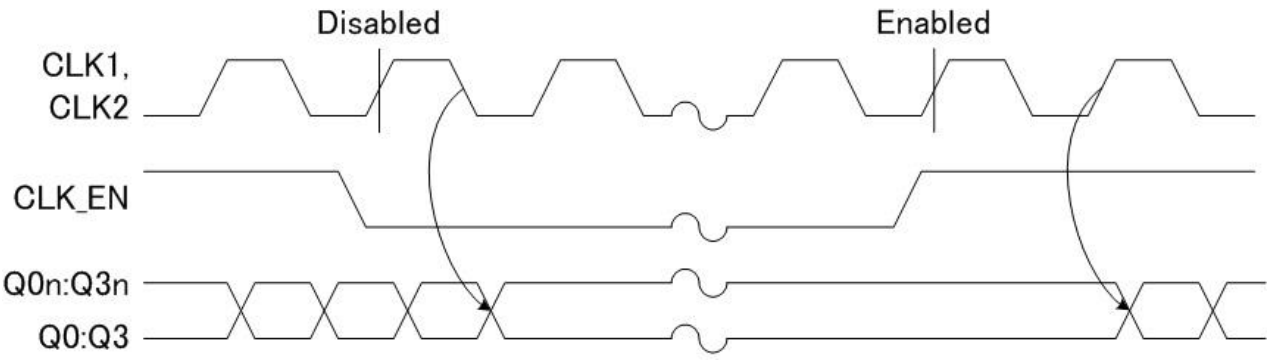


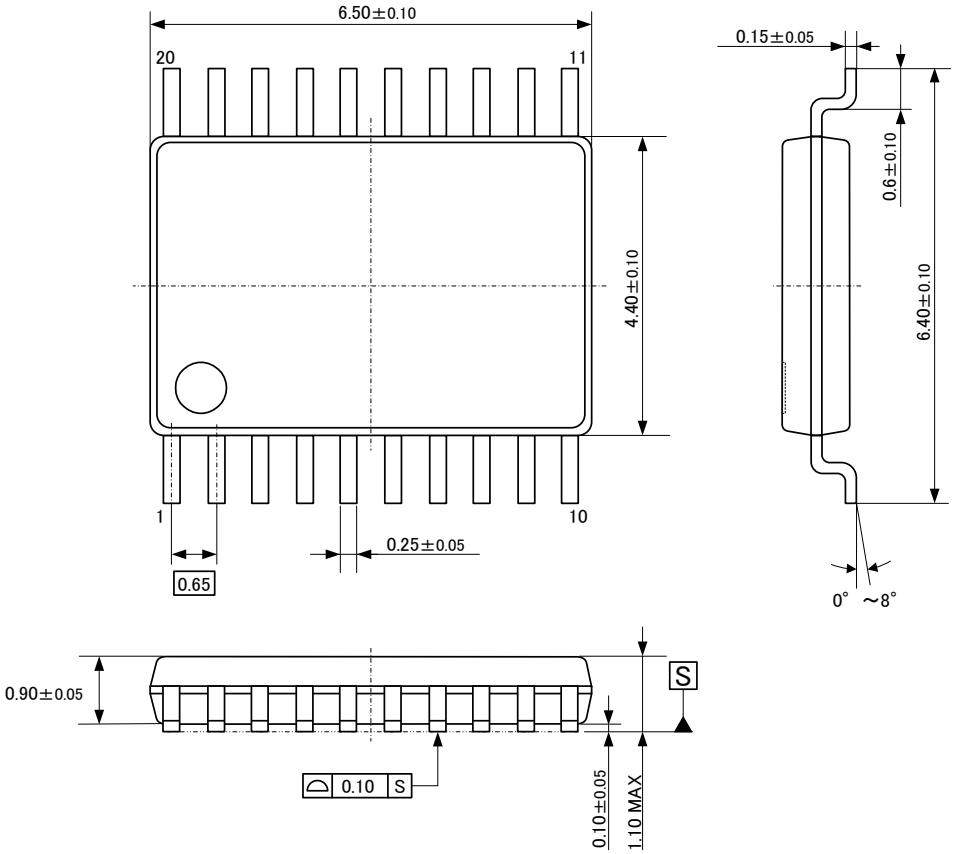
Figure 12 CLK_EN Timing Diagram

Table 2: Clock Input Function Table

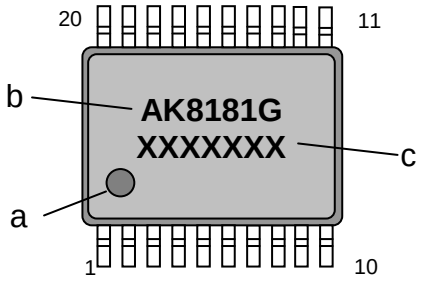
Inputs	Outputs	
CLK1/2	**Q0 : Q3**	**Q0n : Q3n**
0	Low	High
1	High	Low

Package Information

- **Mechanical data : 20pin TSSOP**

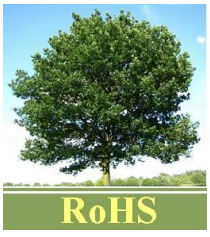


- **Marking**



a: #1 Pin Index
b: Part number
c: Date code (7 digits)

- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

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