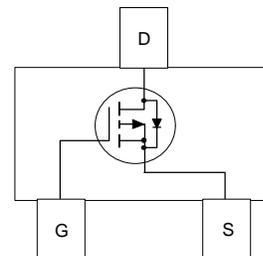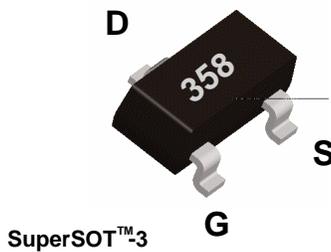# FDN358P

General Description

SuperSOT™-3 P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -1.5 A, -30 V, $R_{DS(ON)} = 0.125\ \Omega$ @ $V_{GS} = -10$ V
  $R_{DS(ON)} = 0.20\ \Omega$ @ $V_{GS} = -4.5$ V.

- High power version of industry SOT-23 package: identical pin out to SOT-23; 30% higher power handling capability.

- High density cell design for extremely low $R_{DS(ON)}$.

- Exceptional on-resistance and maximum DC current capability.

| SuperSOT™-3 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16 |

D 358 **S** **G**

SuperSOT™-3

Absolute Maximum Ratings $T_A = 25^{\circ}C$ unless other wise noted

Symbol	Parameter		FDN358P	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain/Output Current - Continuous		-1.5	A
	- Pulsed		-5	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)		250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)		75	°C/W

TY Semicondutor® TY

Electrical Characteristics (T_A = 25 $^{\circ}$C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA		-30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 $^{\circ}$C			-28		mV/ $^{\circ}$C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V				-1	µA
			T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA		-1	-1.5	-2	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 $^{\circ}$C			3		mV/ $^{\circ}$C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -1.5 A			0.11	0.125	Ω
			T_J =125°C		0.15	0.21	
		V_{GS} = -4.5 V, I_D = -1.2 A			0.175	0.2	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V		-5			A
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -1.5 A			7		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz			270		pF
C_{oss}	Output Capacitance				150		pF
C_{rss}	Reverse Transfer Capacitance				45		pF
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -15 V, I_D = -1 A, V_{GS} = -10 V, R_{GEN} = 6 Ω			8	16	ns
t_r	Turn - On Rise Time				7	14	ns
$t_{D(off)}$	Turn - Off Delay Time				17	27	ns
t_f	Turn - Off Fall Time				10	1.8	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -1.5 A, V_{GS} = -10 V			6.5	9.1	nC
Q_{gs}	Gate-Source Charge				1		nC
Q_{gd}	Gate-Drain Charge				1.1		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current					-0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.42 A (Note 2)			-0.74	-1.2	V

Note:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Typical $R_{\theta JA}$ using the board layouts shown below on FR-4 PCB in a still air environment :

a. 250°C/W when mounted on 0.02 in^2 pad of 2oz Cu.

a

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq$ 300µs, Duty Cycle $\leq$ 2.0%.