HIGH-SPEED CMOS QUAD 2-INPUT MULTIPLEXER

IDT74FCTL2257T

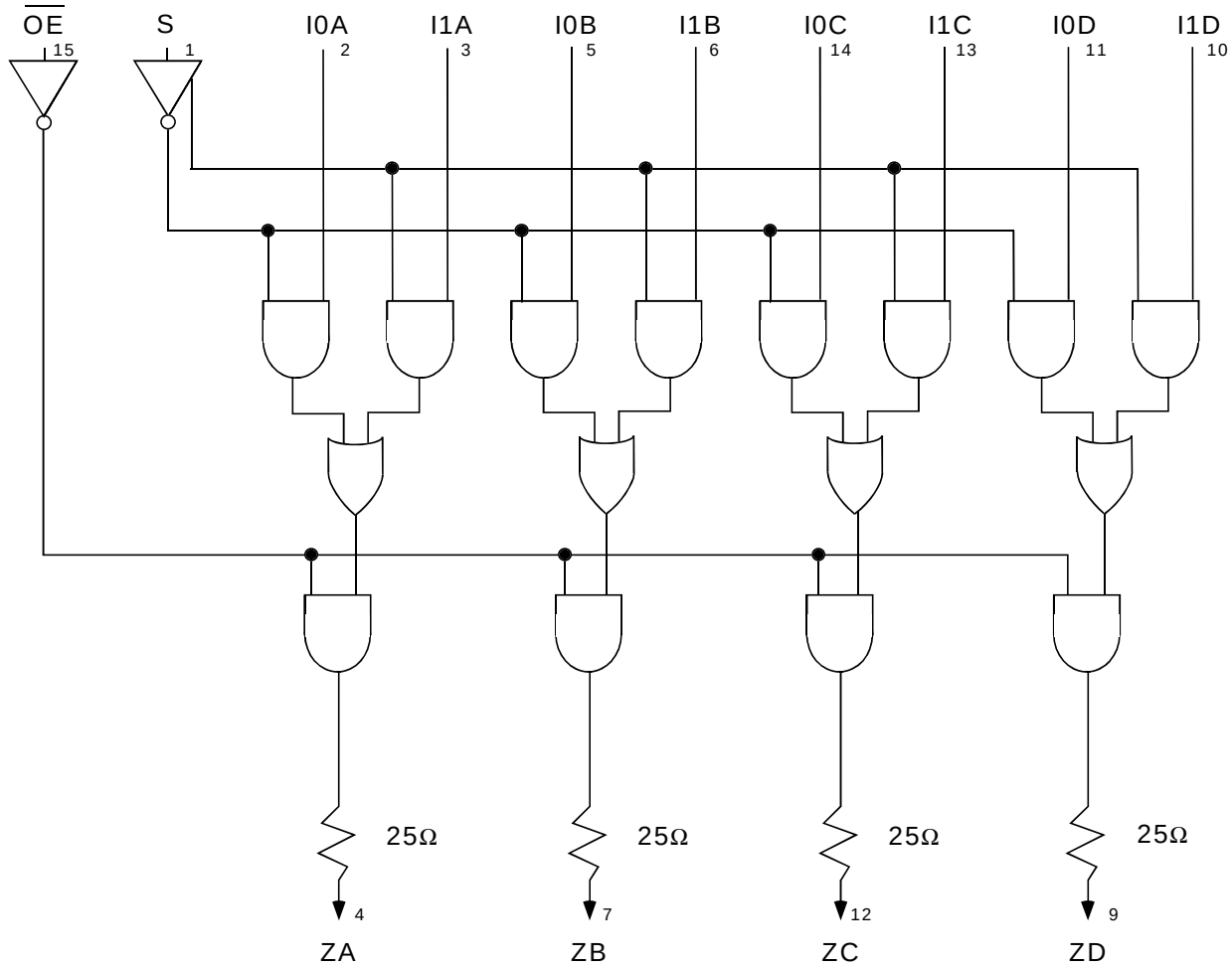
FEATURES:

- Pin and function compatible to the Quality QS74FCT Family
- Extended commercial range of –40°C to +85°C
- CMOS power levels: <7.5mW static
- Available in PDIP, SOIC and QSOP packages
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A and C speed grades with 4.3ns for C
- I_{OL} = 12mA

DESCRIPTION:

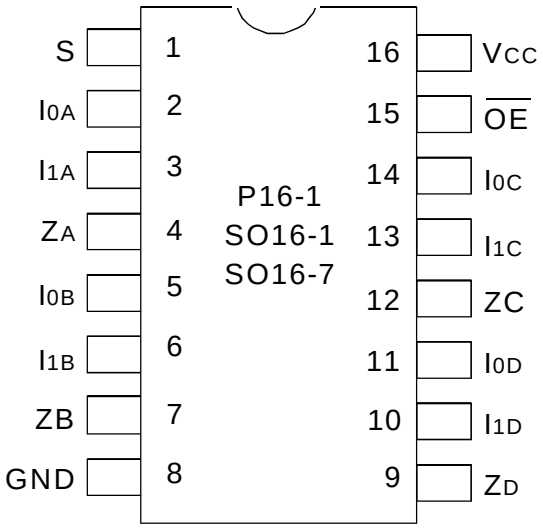
The IDT74FCTL2257T is a 25Ω resistor output version of a high-speed CMOS TTL-compatible, quad, 2-input multiplexer, useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



EXTENDED COMMERCIAL TEMPERATURE RANGE **SEPTEMBER 1999**

PIN CONFIGURATION



PDIP/ SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to +7	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current	120	mA
I_{IK}	Continuous Clamp Current,	– 20	mA
I_{OK}	V_I < 0 or V_O < 0	– 50	mA

FCTL

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

FCTL

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I_{0A} - I_{0D}	Source O Data Inputs
I_{1A} - I_{1D}	Source I Data Inputs
$\overline{OE}$	Enable Input (Active LOW)
S	Select Input
Z_A - Z_D	Outputs

FUNCTION TABLE(1)

Inputs				Outputs
$\overline{OE}$	S	I_0	I_1	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

NOTE:
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Extended Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV_T	Input Hysteresis	V_{TLH} - V_{THL} for all inputs		—	0.2	—	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	0 ≤ V_{IN} < Vcc	—	—	5	µA
I_{IL}	Input LOW Current						
I_{OZ}	Off-State Output Current (Hi-Z)	V_{CC} = Max.	0 ≤ V_{IN} ≤ Vcc	—	—	5	µA
I_{OR}	Current Drive	V_{CC} = Max., V_{OUT} = 2.0V[2]		50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25°C		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -15mA	2.4	—	—	V
V_{OL}	Output LOW Voltage (25Ω)	V_{CC} = Min.	I_{OL} = 12mA	—	—	0.5	V
R_{OUT}	Output Resistance (25Ω)	V_{CC} = Min.	I_{OL} = 12mA	20	28	40	Ω

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:
Extended Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[2] freq = 0	—	2	mA
I_{CCD}	Supply Current per Input per MHz	V_{CC} = Max. Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or Vcc[3,4]	—	0.25	mA/MHz

FCTL

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE(1)

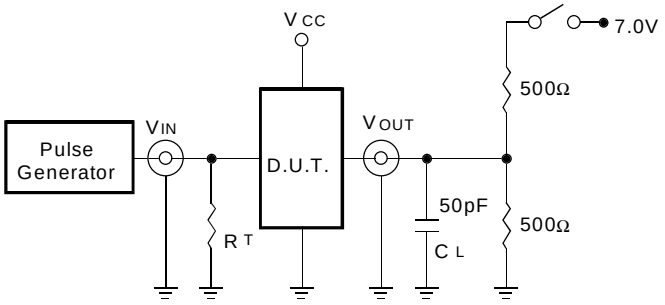
Following Conditions Apply Unless Otherwise Specified:
Extended Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	74FCTL2257T		74FCTL2257AT		74FCTL2257CT		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Ixx to Zx	1.5	6	1.5	5	1.5	4.3	ns
t_{PLH} t_{PHL}	Propagation Delay S to Zx	1.5	10.5	1.5	7	1.5	5.2	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Zx	1.5	8.5	1.5	7	1.5	6	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Zx	1.5	6	1.5	5.5	1.5	5	ns

NOTES:
1. C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



Octal link

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

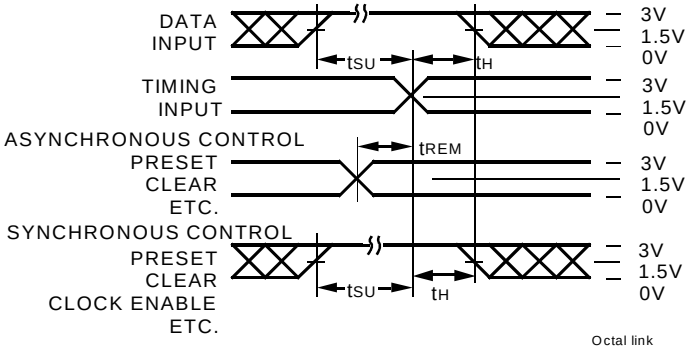
FCTL

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

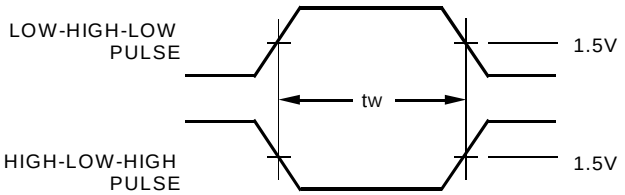
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



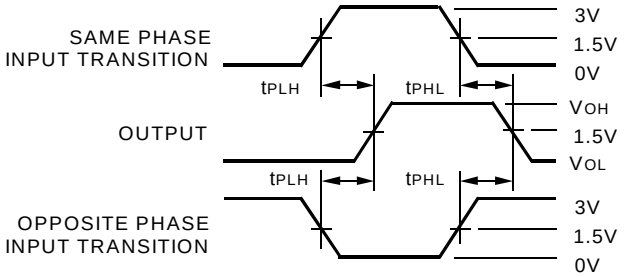
Octal link

PULSE WIDTH



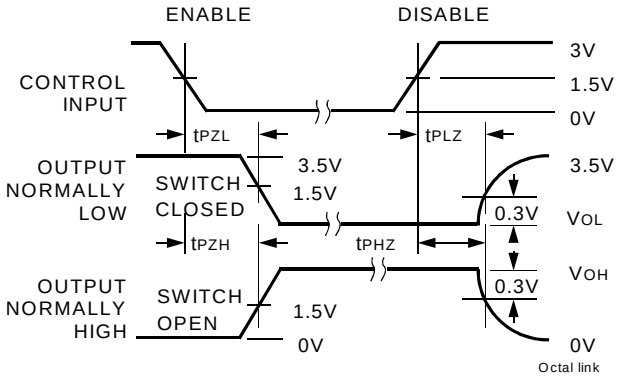
Octal link

PROPAGATION DELAY



Octal link

ENABLE AND DISABLE TIMES

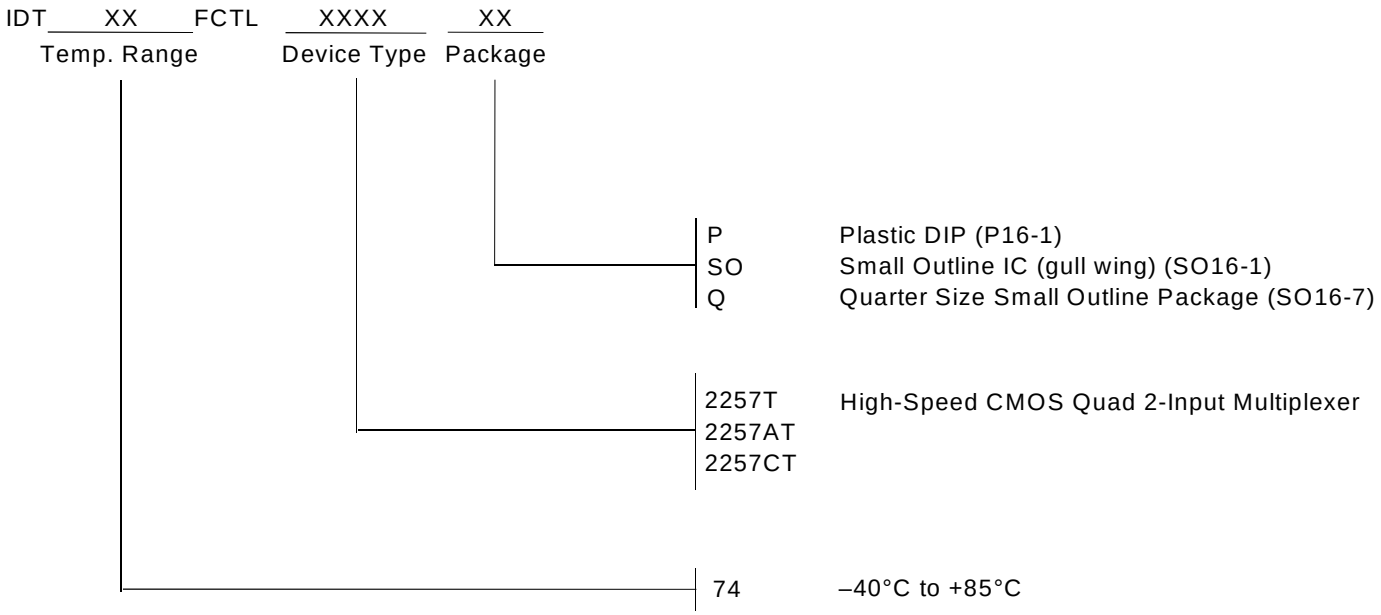


Octal link

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

**To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.*