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ML610Q485

8-bit Microcontroller

GENERAL DESCRIPTION

This LSI is a high performance CMOS 8-bit microcontroller equipped with an 8-bit CPU nX-U8/100 and integrated with peripheral functions such as synchronous serial port, UART, melody driver, and Analog compartor.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipe line architecture parallel processing. Additionally, it adopts the low-/high-speed dual clock system, standby mode, and process that prohibits leak current at high temperatures, and is most suitable for battery-driven applications.
MTP version can rewrite programs on-board, which can contribute to reduction in product development TAT. The flash memory incorporated into this MTP version implements the mask ROM-equivalent low-voltage operation (1.25V or higher) and low-power consumption (typically 5uA at low-speed operation), enabling volume production by the MTP version. For industrial use, ML610Q485P with the extended operating ambient temperature ranging from -40°C to 85°C are available.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit length instruction
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    30.5 μs (@ 32.768 kHz system clock)
    2 μs (@ 500 kHz system clock)
    0.25 μs (@ 4 MHz system clock)

- Internal memory
  - Internal 32KByte flash memory (16K x 16 bits) (including unusable 1K Byte TEST area)
  - Internal 2KByte RAM (2048 x 8 bits)

- Interrupt controller
  - 1 non-maskable interrupt source:
    Internal source: 1 (Watchdog Timer)
  - 28 maskable interrupt sources:
    Internal source: 16 (SSIO0, Timer0, Timer1, Timer 2, Timer 3, Timer C, Timer D, UART0, Melody 0, PWM0, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz, Analog Comparator, RTC)
    External source: 12 (P00, P01, P02, P03, P50, P51, P52, P53, P54, P55, P56, P57)
    (One interrupt request is generated from P50 to P57 interrupt sources.)

- Time base counter
  - Low-speed time base counter x 1 channel
    Frequency compensation (Compensation range: Approx. -488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter x 1 channel

- Real time clock
  – Year, month, day, hour, minute, and second registers
  – Adjustable to compensate for crystal variations
  – Automatic leap year correction
  – Regular interrupts (0.5 sec, 1 sec, 1 minute)

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s)

- Timers
  - 8 bits x 6 channels [also available is 16-bit x 3 configuration (using Timers 0-1, 2-3, or C-D)]
  - Clock frequency measurement function mode (16-bit configuration using Timers 2 and 3 x 1 channel only)
  - The timer C and timer D are controlled by the external trigger.
  - The timer C and timer D are used for the one-shot timer mode.

- PWM
  - Resolution 16 bits × 1 channel

- Capture
  - Time base capture x 2 channels (4096 Hz to 32 Hz)

- Synchronous serial port
  - Master/slave selectable × 1 channel
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- Analog Comparator
  - Operating voltage: V_{DD}=1.8V～3.6V
  - Common mode input voltage: 0.2V～VDD－0.2V
  - Input offset voltage: 30mV(max)
  - Interrupt allow edge selection and sampling selection
  - The RC discharged type A/D convertor is configured with the timers C and D.
  - The temperature measurement function using built-in temperature sensor.
    Temperature measurement range: -20°C to +70°C (P version:-40°C to +85°C)
  - The reference voltage can be switched between CMPP0, CMPP1, CMPM0, CMPM1, 1/4VDD, 1/2VDD, temperature sensor and the internal 0.7V voltage source.

- General-purpose ports
  - Input-only port: 4 channels (including secondary functions)
  - Output-only port: 6 channels (including secondary functions)
  - Input/output port: 16 channels (including secondary functions)

- Random Number Generator
  - Ring oscillator based entropy source

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow
  - Reset by the low-speed oscillation stop detection

- Clock
  - Low-speed clock (Operation of this LSI is not guaranteed under a condition with no supply of low-speed crystal oscillation clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock
    Built-in RC oscillation (500 kHz, 4 MHz)

- Power management
  - HALT mode: Suspends the instruction execution by CPU (peripheral circuits are in operating states)
  - STOP mode: Stops the low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - High-speed clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block control function: Completely stops the operation of any function block circuit that is not used (resets registers and stops clock)
  - When LSCLK is selected for system clock, the power consumption can be reduced by using halver circuit.

- Shipment

- Chip (Die) -	Low-speed oscillation stop detect reset	Operating temperature	Product availability
ML610Q485-xxxWA	Yes	-20°C to +70°C	Yes
ML610Q485P-xxxWA	Yes	-40°C to +85°C	Yes

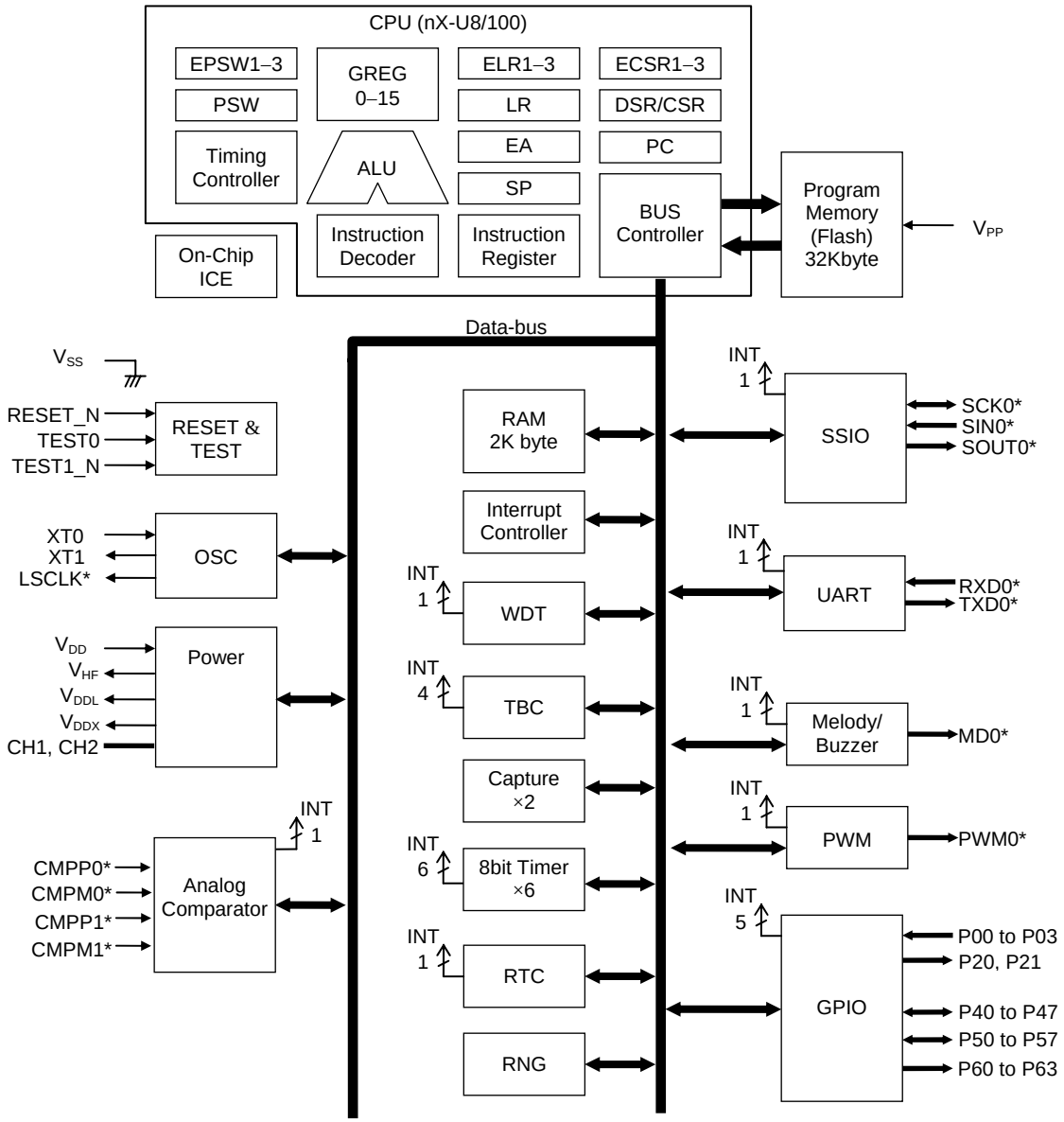
- 48 pin plastic TQFP -	Low-speed oscillation stop detect reset	Operating temperature	Product availability
ML610Q485-xxxTB	Yes	-20°C to +70°C	-
ML610Q485P-xxxTB	Yes	-40°C to +85°C	-

xxx: ROM code number (xxx of the blank product is NNN)
Q: MTP version
P: Wide range temperature version (P version)
WA: Chip (Die)
TB: TQFP

- Guaranteed Operation Range
  – Operating temperature: -20°C to +70°C (P version: -40°C to +85°C)
  – Operating voltage: V_{DD} = 1.25V to 3.6V (2.4V to 3.6V used halver circuit)

BLOCK DIAGRAM

Block Diagram of ML610Q485

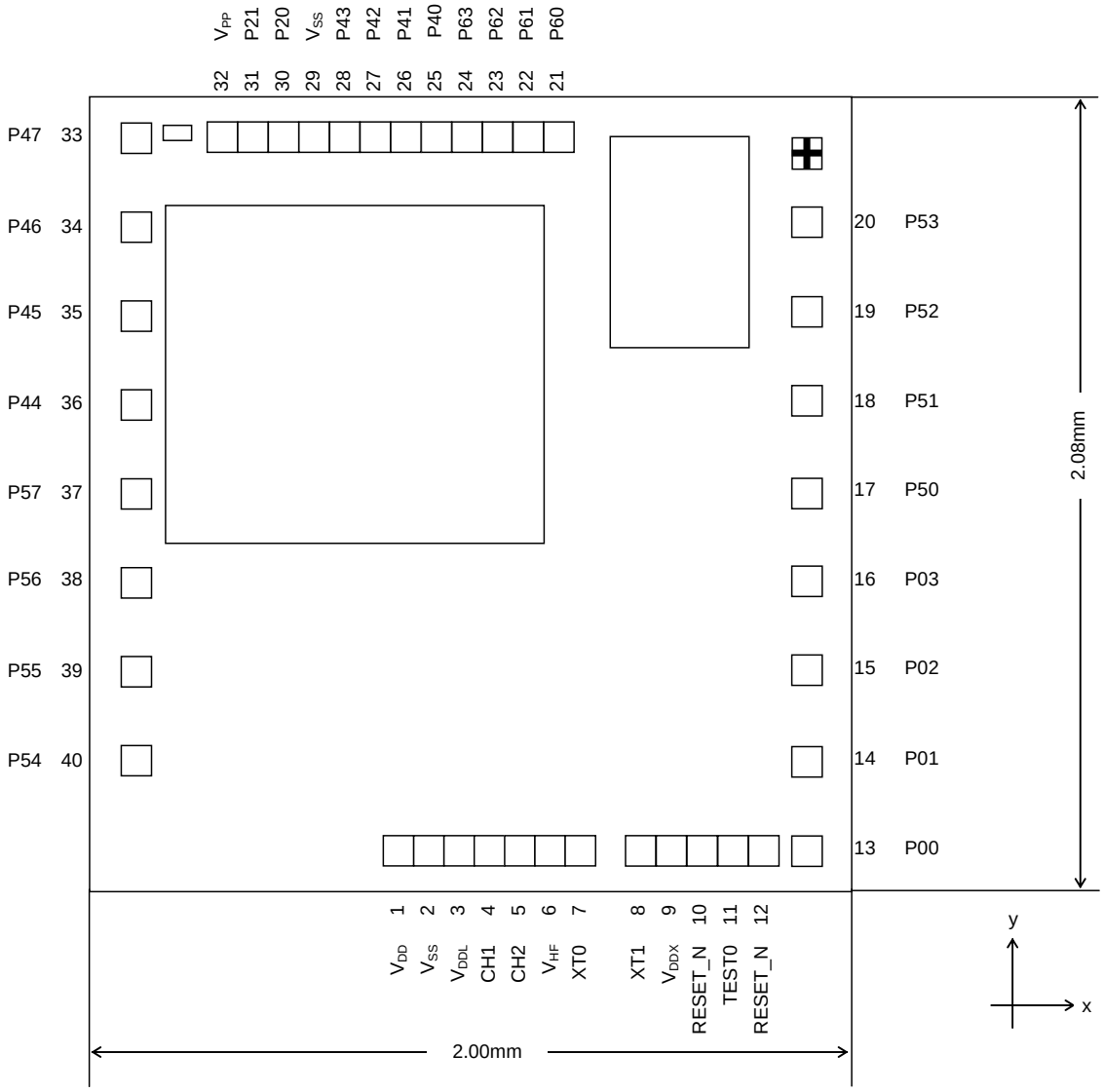


* Secondary function or Tertiary function

Figure 1 ML610Q485 Block Diagram

CHIP PAD LAYOUT

ML610Q485 Chip Pad Layout & Dimension



Chip size: 2.00mm × 2.08mm
PAD count: 40 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

Figure 2 ML610Q485 Chip Pin Layout & Dimension

PAD COORDINATES

ML610Q485 Pad Coordinates

Table 1 ML610Q485 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610Q485		PAD No.	Pad Name	ML610Q485	
		X (µm)	Y (µm)			X (µm)	Y (µm)
1	V_{DD}	-193	-934	21	P60	230	934
2	V_{SS}	-113	-934	22	P61	150	934
3	V_{DDL}	-33	-934	23	P62	70	934
4	CH1	47	-934	24	P63	-10	934
5	CH2	127	-934	25	P40	-90	934
6	V_{HF}	207	-934	26	P41	-170	934
7	XT0	287	-934	27	P42	-250	934
8	XT1	447	-934	28	P43	-330	934
9	V_{DDX}	527	-934	29	V_{SS}	-410	934
10	RESET_N	607	-934	30	P20	-490	934
11	TEST0	687	-934	31	P21	-570	934
12	TEST1_N	767	-934	32	V_{PP}	-650	934
13	P00	879	-934	33	P47	-879	934
14	P01	879	-699	34	P46	-879	699
15	P02	879	-464	35	P45	-879	464
16	P03	879	-229	36	P44	-879	229
17	P50	879	6	37	P57	-879	-6
18	P51	879	241	38	P56	-879	-241
19	P52	879	476	39	P55	-879	-476
20	P53	879	711	40	P54	-879	-711

PIN LIST

PAD No.	Primary function			Secondary function or Tertiary function			
	Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
2,29	V_{SS}	—	Negative power supply pin	—	—	—	—
1	V_{DD}	—	Positive power supply pin	—	—	—	—
6	V_{HF}	—	Power supply pin for halver circuit (internally generated)	—	—	—	—
3	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—
9	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—
32	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—
4	CH1	—	Capacitor connection pin for halver circuit	—	—	—	—
5	CH2	—	Capacitor connection pin for halver circuit	—	—	—	—
11	TEST0	I/O	Test pin	—	—	—	—
12	TEST1_N	I	Test pin	—	—	—	—
10	RESET_N	I	Reset input pin	—	—	—	—
7	XT0	I	Low-speed clock oscillation pin	—	—	—	—
8	XT1	O	Low-speed clock oscillation pin	—	—	—	—
13	P00/EXI0/ CAP0/TPRUN0	I	Input port, External interrupt, Capture 0 input Timer C/Timer D external trigger input	—	—	—	—
14	P01/EXI1/ CAP1/TPRUN1	I	Input port, External interrupt, Capture 1 input Timer C/Timer D external trigger input	—	—	—	—
15	P02/EXI2/ RXD0/TPRUN2	I	Input port, External interrupt, UART0 received data Timer C/TimerD external trigger input	—	—	—	—
16	P03/EXI3/ TPRUN3	I	Input port, External interrupt Timer C/Timer D external trigger input	—	—	—	—
30	P20/LED0	O	Output port	Secondary	LSCLK	O	Low-speed clock output
31	P21/LED1	O	Output port	Secondary	OUTCLK	O	High-speed clock output
25	P40	I/O	Input/output port	—	—	—	—
				Tertiary	SIN0	I	SSIO0 data input
26	P41	I/O	Input/output port	—	—	—	—
				Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
27	P42	I/O	Input/output port	Secondary	RXD0	I	UART data input
				Tertiary	SOUT0	O	SSIO0 data output
28	P43	I/O	Input/output port	Secondary	TXD0	O	UART data output
				Tertiary	PWM0	O	PWM output
36	P44/T02P0CK/ TCDRUN	I/O	Input/output port, Timer 0/Timer 2/PWM 0 external clock input Timer C/Timer D external trigger Input	—	—	—	—
				Tertiary	SIN0	I	SSIO0 data input
35	P45/T13CK/ TCDRUN	I/O	Input/output port, Timer 1/Timer 3 external clock input Timer C/Timer D external trigger input	—	—	—	—
				Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
34	P46/TCCK	I/O	Input/output port, Timer C external clock input	—	—	—	—
				Tertiary	SOUT0	O	SSIO0 data output
33	P47/TDCK	I/O	Input/output port, Timer D external clock input	—	—	—	—
17	P50/EXI8	I/O	Input/output port, External interrupt	Secondary	MD0	O	Melody 0 output
18	P51/EXI8	I/O	Input/output port, External interrupt	—	—	—	—
19	P52/EXI8	I/O	Input/output port, External interrupt	—	—	—	—

PAD No.	Primary function			Secondary function or Tertiary function			
	Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
20	P53/EXI8	I/O	Input/output port, External interrupt	—	—	—	—
40	P54/EXI8/ CMPP0	I/O	Input/output port, External interrupt Analog comparator noninverting input0 pin	—	—	—	—
39	P55/EXI8/ CMPP1	I/O	Input/output port, External interrupt Analog comparator noninverting Input1 pin	—	—	—	—
38	P56/EXI8/ CMPM0	I/O	Input/output port, External interrupt Analog comparator inverting input0 pin	—	—	—	—
37	P57/EXI8/ CMPM1	I/O	Input/output port, External interrupt Analog comparator inverting Input1 pin	—	—	—	—
21	P60	O	Output port	—	—	—	—
22	P61	O	Output port	—	—	—	—
23	P62	O	Output port	—	—	—	—
24	P63	O	Output port	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal resonator is connected to this pin. Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS}. (see appendix C measuring circuit 1)	—	—
XT1	O		—	—
LSCLK	O	Low-speed clock output. Assigned to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00 to P03	I	General-purpose input port.	Primary	Positive
General-purpose output port				
P20, P21	O	General-purpose output port. This cannot be used as the general output port when used as the secondary function.	Primary	Positive
P60 to P63	O	General-purpose output port.	Primary	Positive
General-purpose input/output port				
P40 to P47	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary or tertiary function.	Primary	Positive
P50 to P57	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
External interrupt				
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00 to P03 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. Assigned to the primary function of the P50 to P57 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. This pin is used as the primary function of the P44 pin.	Primary	—
T13CK	I	External clock input pin used for both Timer 1 and Timer 3. This pin is used as the primary function of the P45 pin.	Primary	—
TCCK	I	External clock input pin used for Timer C. This pin is used as the primary function of the P46 pin.	Primary	—
TDCK	I	External clock input pin used for Timer D. This pin is used as the primary function of the P47 pin.	Primary	—
TCDRUN	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P44 pin or the P45 pin.	Primary	—
TPRUN0	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P00 pin.	Primary	—
TPRUN1	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P01 pin.	Primary	—
TPRUN2	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P02 pin.	Primary	—
TPRUN3	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P03 pin.	Primary	—
LED drive				
LED0, LED1	O	N-channel open drain output pins to drive LED. This pin is used as the primary function of the P20 and the P21 pins.	Primary	Positive /negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P50 pin.	Secondary	Positive/ negative
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 pin.	Tertiary	Positive
T02P0CK	I	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
Analog Comparator				
CMPP0	I	Analog comparator noninverting input0 pin. This pin is used as the primary function of the P54.	Primary	—
CMPP1	I	Analog comparator noninverting input1 pin. This pin is used as the primary function of the P55.	Primary	—
CMPM0	I	Analog comparator inverting input0 pin. This pin is used as the primary function of the P56.	Primary	—
CMPM1	I	Analog comparator inverting input1 pin. This pin is used as the primary function of the P57.	Primary	—
Test				
TEST0	I/O	Pin for testing. A pull-down resistor is internally connected.	—	Positive
TEST1_N	I	Pin for testing. A pull-up resistor is internally connected.	—	Negative
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{HF}	—	Positive power supply pin (internally generated) for Halver. Capacitor C_{HF} (see measuring circuit 1) should be connected between this pin and V_{SS}.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors C_L (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—
V_{DDX}	—	Positive power supply pin (internally generated) for low-speed oscillation. Capacitor C_X (see measuring circuit 1) should be connected between this pin and V_{SS}.	—	—
CH1	—	Capacitor connection pin for halver circuit. Capacitor C_{H12} (see measuring circuit 1) are connected between CH1 and CH2.	—	—
CH2	—		—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.	—	—

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2 Termination of Unused Pins

Pin	Recommended pin handling
V_{PP}	Open
RESET_N	Open
TEST0	Open
TEST1_N	Open
P00 to P03	V_{DD} or V_{SS}
P20, P21	Open
P40 to P47	Open
P50 to P57	Open
P60 to P63	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS}= 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	-0.3 to +4.6	V
Power supply voltage 2	V_{PP}	Ta=25°C	-0.3 to +9.5	V
Power supply voltage 3	V_{DDL}	Ta=25°C	-0.3 to +3.6	V
Input voltage	V_{IN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port 4 to 6, Ta=25°C	-12 to +11	mA
Output current 2	I_{OUT2}	Port 2, Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	0.9	W
Storage temperature	T_{STG}	—	-55 to +150	°C

Recommended Operating conditions

(V_{SS}= 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	without P version	-20 to +70	°C
		P version	-40 to +85	
Operating voltage	V_{DD}	f_{OP}=30k to 625kHz	1.25 to 3.6	V
		f_{OP}=30k to 5MHz	1.8 to 3.6	
		f_{OP}=30k to 36kHz, Used Halver	2.4 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD}=1.25 to 3.6V	30k to 625k	Hz
		V_{DD}=1.8 to 3.6V	30k to 5.0M	
		V_{DD}=2.4 to 3.6V, Used Halver	30k to 36k	
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitance	C_{DL}	—	3 to 18	pF
	C_{GL}	—	3 to 18	
V_{DDL} pin external capacitance	C_L	—	2.2±30%	µF
V_{DDX} pin external capacitance	C_X	—	0.1±30%	µF
V_{HF} pin external capacitance	C_{HF}	—	0.1±30%	µF
Pin-to-pin (CH1 to CH2) external capacitance	C_{H12}	—	0.1±30%	µF

Operating conditions of FlashROM

(VSS= 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase	2.75 to 3.6	V
	V_{DDL}	At write/erase[*1]	2.5 to 2.75	
	V_{PP}	At write/erase	7.7 to 8.3	
Rewrite count	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

[*1]: When writing to and erasing on the flash Memory, the voltage in the specified range needs to be supplied to the V_{DDL} pin. The V_{PP} pin has an internal pull-down resistor.

Operation conditions of Comparator

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

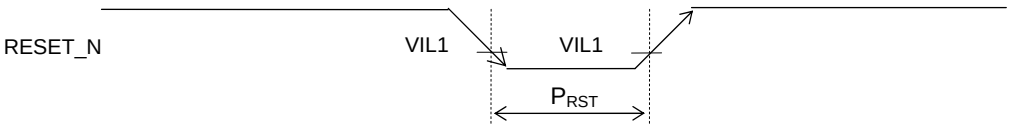
Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Common-mode input voltage	CMV_{IN}	—	0.2	—	V_{DD}-0.2	V	1
Analog Comparator Input offset voltage	V_{CMPOF}	Ta=25°C	-30	—	30	mV	
Analog Comparator Response time	T_{CMP}	Ta=25°C, Overdrive=100mV	—	—	1	µs	
Analog Comparator Wakeup time	T_{CMPW}	—	—	—	5	µs	
Analog Comparator supply current	I_{CMP}	Ta=25°C	—	33	45	µA	
Temperature sensor output voltage through x2	V_{TMP}	Ta=25°C	—	1355	—	mV	
Temperature sensor output voltage through x2 (Temperature property)	ΔV_{TMP}	Ta = -40 to +25°C	—	-3.585	—	mV/°C	
		Ta = 25 to 85°C	—	-3.718	—		
0.7V voltage source output voltage through x2	V_{REF}	Ta=25°C	1.386	1.400	1.414	V	
0.7V voltage source temperature deviation	ΔV_{REF}	—	—	0	—	%/°C	
0.7V voltage source supply current	I_{REF}	Ta=25°C	—	20	40	µA	
1/2 VDD voltage source	VDD2	—	VDD/2 x 0.96	VDD/2	VDD/2 x 1.04	V	
1/4 VDD voltage source	VDD4	—	VDD/4 x 0.96	VDD/4	VDD/4 x 1.04	V	

DC Characteristics (1/4)

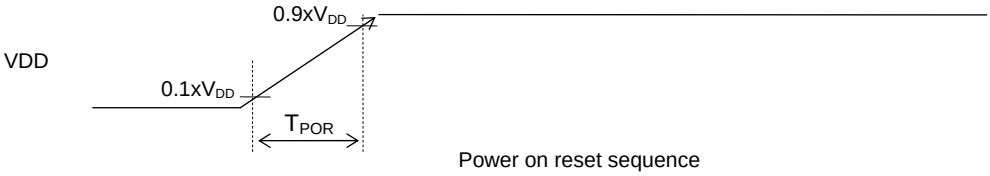
(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measurement circuit
500kHz/4MHz RC oscillation frequency	f_{RC}	V_{DD}=1.25 to 3.6V	Ta=25°C	Typ. -10%	500	Typ. +10%	kHz	1
			*2	Typ. -25%	500	Typ. +25%	kHz	
		V_{DD}=1.8 to 3.6V	Ta=25°C	Typ. -10%	4.0	Typ. +10%	MHz	
			*2	Typ. -25%	4.0	Typ. +25%	MHz	
Low-speed crystal oscillation start time*1	T_{XTL}	—		—	0.6	2	s	
500kHz/4MHz RC oscillation start time	T_{RC}	—		—	—	3	µs	
Reset pulse width	P_{RST}	—		200	—	—	µs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset generated power rise time	T_{POR}	—		—	—	10	ms	

*1: 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF).
*2: Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)



External reset sequence



Power on reset sequence

DC Characteristics (2/4)

(V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measurement circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/High-speed oscillation: stopped.	Ta=25°C	—	0.32	0.8	µA	1
			*4	—	—	8		
Supply current 2	IDD2	CPU: In HALT state. (LTBC, WDT: Operating)*2*3. High-speed 500kHz/4MHz oscillation: Stopped. Used halver	Ta=25°C	—	0.35	0.7	µA	
			*4	—	—	4		
Supply current 3-1	IDD3-1	CPU: In 32.768kHz operating state.*1*2 High-speed 500kHz/4MHz oscillation: Stopped, Not used halver	Ta=25°C	—	4.5	8	µA	
			*4	—	—	15		
Supply current 3-2	IDD3-2	CPU: In 32.768kHz operating state.*1*2 High-speed 500kHz/4MHz oscillation: Stopped, Used halver	Ta=25°C	—	2.5	4	µA	
			*4	—	—	7.5		
Supply current 4-1	IDD4-1	CPU: In 500kHz RC operating state. Not used halver	Ta=25°C	—	75	100	µA	
			*4	—	—	120		
Supply current 4-2	IDD4-2	CPU: In 4MHz RC operating state. Not used halver	Ta=25°C	—	600	750	µA	
			*4	—	—	800		

*1: When the CPU operating rate is 100% (no HALT state).
*2 : 32.768KHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF)
*3 : Significant bits of BLKCON0 to BLKCON3 registers are all "1".
*4 : Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)

DC Characteristics (3/4)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20, P21 (N-channel open drain output mode is not selected)) (P40 to P47) (P50 to P57) (P60 to P63)	VOH1	IOH1=-0.5mA, V_{DD}=1.8 to 3.6V	V_{DD} -0.5	—	—	V	2
		IOH1=-0.03mA, V_{DD}=1.25 to 3.6V	V_{DD} -0.3	—	—		
	VOL1	IOL1=+0.5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
		IOL1=+0.1mA, V_{DD}=1.25 to 3.6V	—	—	0.3		
Output voltage 2 (P20, P21 (N-channel open drain output mode is selected))	VOL2	IOL2=+5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
Output leakage (P20, P21) (P40 to P47) (P50 to P57) (P60 to P63)	IOOH	VOH=V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL=V_{SS} (in high-impedance state)	-1	—	—		
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1=V_{DD}	—	—	1	μA	4
	IIL1	VIL1=V_{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	2	300	600		
	IIL2	VIL2=V_{SS}	-1	—	—		
Input current 3 (P00 to P03) (P40 to P47) (P50 to P57)	IIH3	VIH3=V_{DD}, V_{DD}=1.8 to 3.6V (when pulled-down)	2	30	200		
		VIH3=V_{DD}, V_{DD}=1.25 to 3.6V (when pulled-down)	0.01	30	200		
	IIL3	VIL3=V_{SS}, V_{DD}=1.8 to 3.6V (when pulled-up)	-200	-30	-2		
		VIL3=V_{SS}, V_{DD}=1.25 to 3.6V (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3=V_{DD} (in high-impedance state)	—	—	1		
	IIL3Z	VIL3=V_{SS} (in high-impedance state)	-1	—	—		

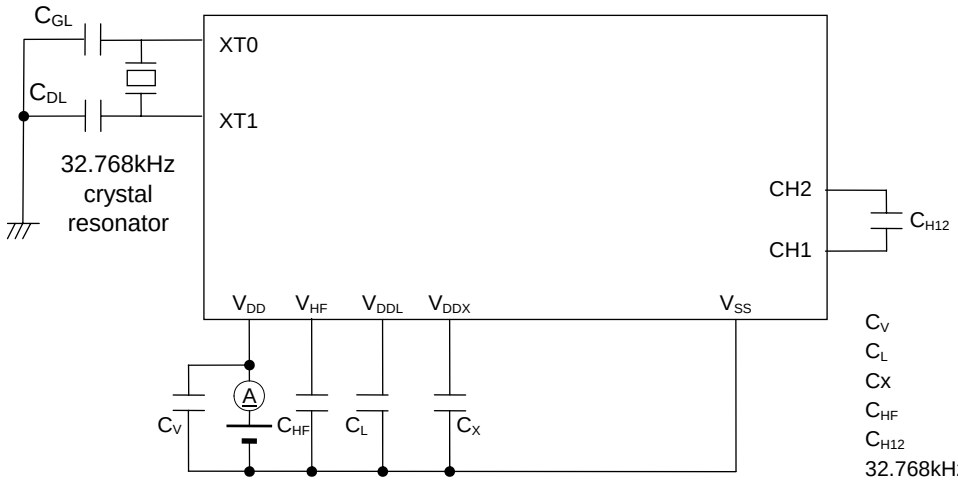
DC Characteristics (4/4)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST1_N) (TEST0) (P00 to P03) (P40 to P47) (P50 to P57)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	V_{DD}=1.25 to 3.6V	0	—	0.2 ×V_{DD}		
Input pin capacitance (P00 to P03) (P40 to P47) (P50 to P57)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	—	—	5	pF	—

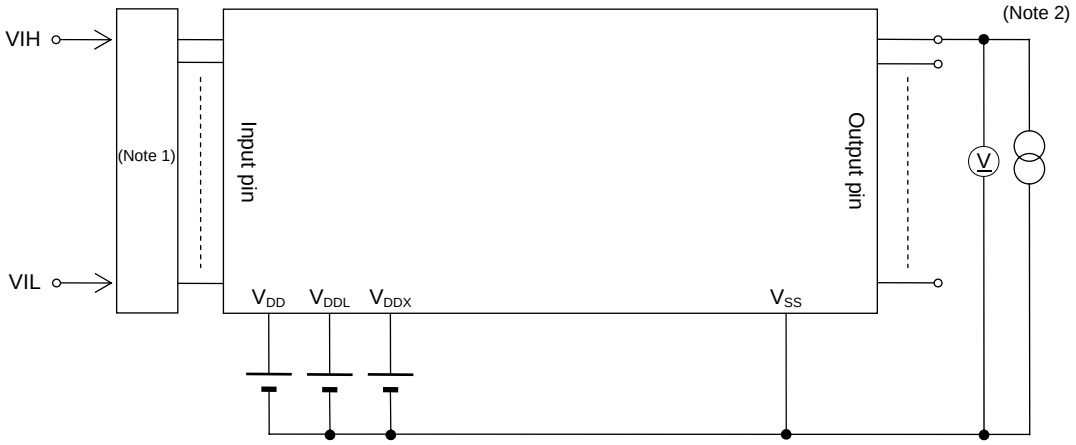
Measuring Circuits

Measuring Circuit 1



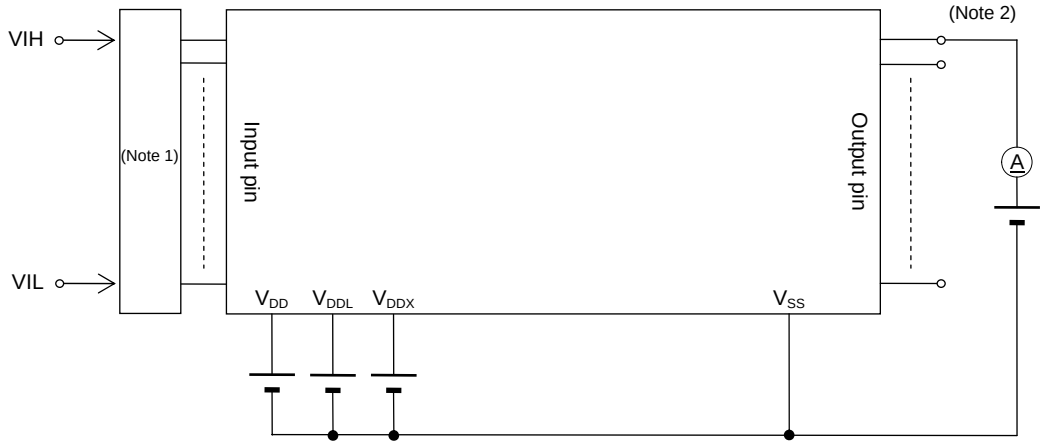
C_V : 2.2µF
C_L : 2.2uF
Cx : 0.1µF
C_{HF} : 0.1µF
C_{H12} : 0.1µF
32.768kHz crystal resonator
: DT-26 (Load capacitance 6pF)
(Made by KDS:DAISHINKU CORP.)
C_{GL}, C_{DL} : 6pF

Measuring Circuit 2



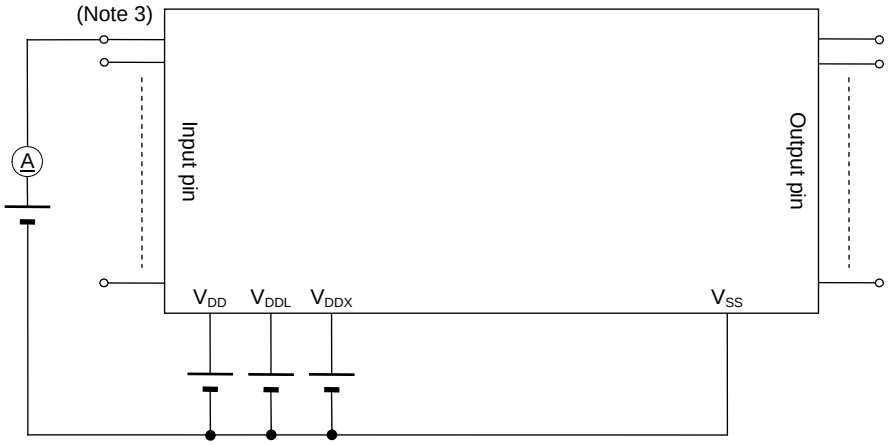
(Note 1): Input logic circuit to determine the specified measuring conditions.
(Note 2) Repeats for the specified output pin

Measuring Circuit 3



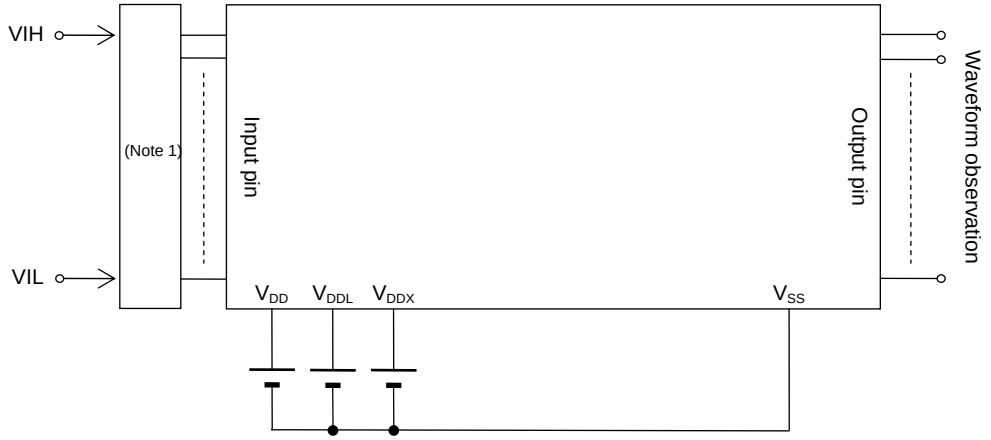
(Note 1): Input logic circuit to determine the specified measuring conditions.
(Note 2) Repeats for the specified output pin

Measuring Circuit 4



(Note 3) Repeats for the specified input pin

Measuring Circuit 5

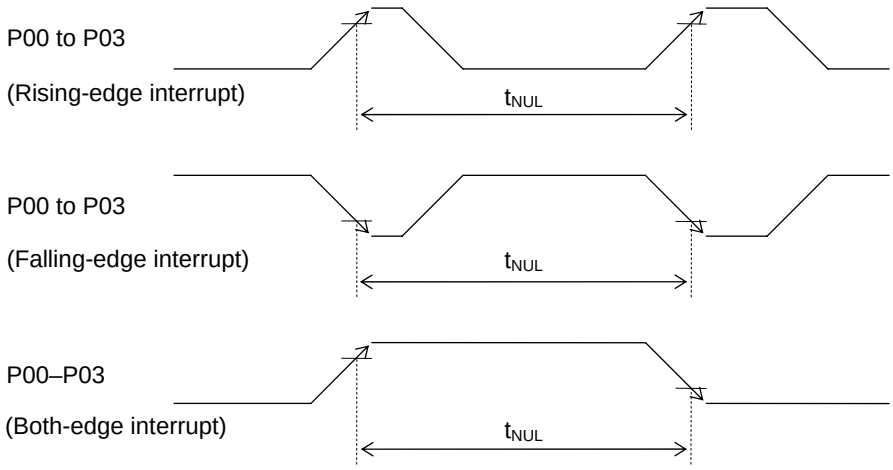


(Note 1): Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	µs

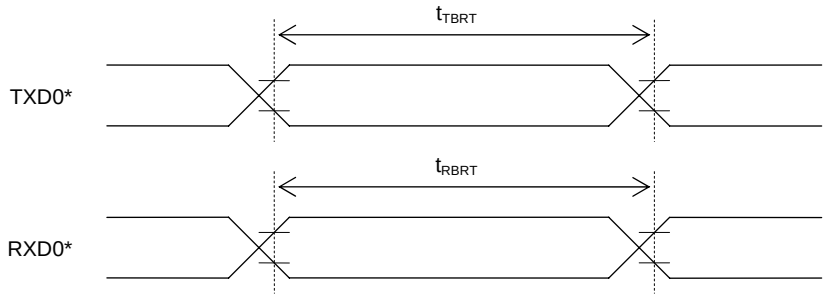


AC Characteristics (UART)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*[1]	—	s
Receive baud rate	t_{RBRT}	—	BRT*[1] -3%	BRT*[1]	BRT*[1] +3%	s

*[1]: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).



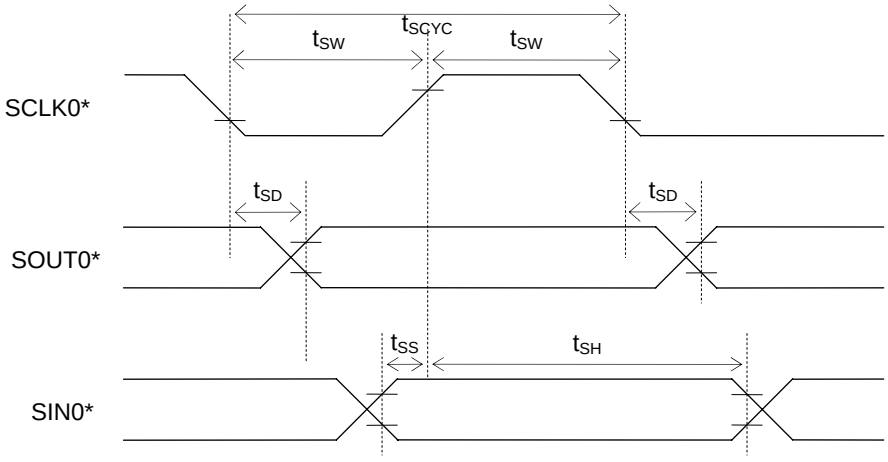
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK0 input cycle (slave mode)	t_{SCYC}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V)	10	—	—	µs
		When RC oscillation is 4MHz *3 (V_{DD} = 1.8 to 3.6V)	2	—	—	
SCLK0 output cycle (master mode)	t_{SCYC}	—	—	SCLK0*1	—	s
SCLK0 input pulse width (slave mode)	t_{SW}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V)	4	—	—	µs
		When RC oscillation is 4MHz *3 (V_{DD} = 1.8 to 3.6V)	04	—	—	
SCLK0 output pulse width (master mode)	t_{SW}	—	SCLK0*1 ×0.4	SCLK0*1 ×0.5	SCLK0*1 ×0.6	s
SOUT0 output delay time (slave mode)	t_{SD}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V) output load 10pF	—	—	500	ns
		When RC oscillation is 4MHz *3 (V_{DD} = 1.8 to 3.6V) output load 10pF	—	—	240	
SOUT0 output delay time (master mode)	t_{SD}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V) output load 10pF	—	—	500	ns
		When RC oscillation is 4MHz *3 (V_{DD} = 1.8 to 3.6V) output load 10pF	—	—	240	
SIN0 input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN0 input setup time (master mode)	t_{SS}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V)	500	—	—	ns
		When RC oscillation is 4MHz *3 (V_{DD} = 1.8 to 3.6V)	240	—	—	
SIN0 input hold time	t_{SH}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V)	300	—	—	ns
		When RC oscillation is 4MHz *3 (V_{DD} = 1.8 to 3.6V)	80	—	—	

*1: Clock period selected with S0CK3–0 of the serial port n mode register (SIO0MOD1)
*2: When 500kHz RC oscillation is selected by OSCM3 of the frequency control register (FCON0)
*3: When 4MHz RC oscillation is selected by OSCM3 of the frequency control register (FCON0)



*: Indicates the secondary function of the port

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q485-01	Aug.25,2014	–	–	Final edition 1

NOTES

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