Standard Products

UT28F64 Radiation-Hardened 8K x 8 PROM

Data Sheet

August 2001

FEATURES

- Programmable, read-only, asynchronous, radiation-hardened, 8K x 8 memory
  - Supported by industry standard programmer
- 35ns and 45ns maximum address access time (-55 °C to +125 °C)
- TTL compatible input and TTL/CMOS compatible output levels
- Three-state data bus
- Low operating and standby current
  - Operating: 100mA maximum @28.6MHz
    - Derating: 3mA/MHz
  - Standby: 500µA maximum (post-rad)
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
  - Total dose: 1E6 rad(Si)
  - $LET_{TH}(0.25) \sim 100$ MeV-cm^2/mg
  - SEL Immune $\geq$128 MeV-cm^2/mg
  - Saturated Cross Section cm^2 per bit, 1.0E-11
    - 1.2E-8 errors/device-day, Adams 90% geosynchronous heavy ion
  - Memory cell LET threshold: >128 MeV-cm^2/mg
- QML Q & V compliant part
  - AC and DC testing at factory
- Packaging options:
  - 28-pin 100-mil center DIP (0.600 x 1.4)
  - 28-lead 50-mil center flatpack (0.490 x 0.74)
- V_{DD}: 5.0 volts $\pm$ 10%
- Standard Microcircuit Drawing 5962-96873

PRODUCT DESCRIPTION

The UT28F64 amorphous silicon anti-fuse PROM is a high performance, asynchronous, radiation-hardened, 8K x 8 programmable memory device. The UT28F64 PROM features fully asychronous operation requiring no external clocks or timing strobes. An advanced radiation-hardened twin-well CMOS process technology is used to implement the UT28F64. The combination of radiation- hardness, fast access time, and low power consumption make the UT28F64 ideal for high speed systems designed for operation in radiation environments.

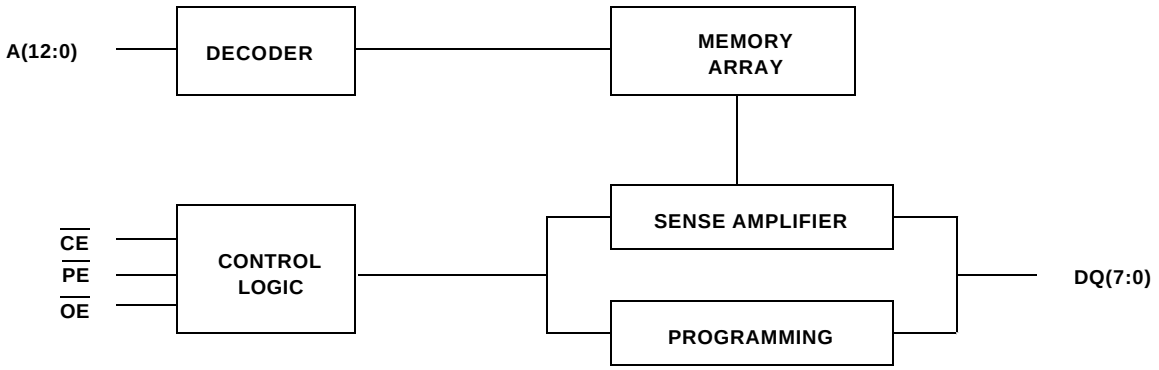


Figure 1. PROM Block Diagram

DEVICE OPERATION

The UT28F64 has three control inputs: Chip Enable ($\overline{CE}$), Program Enable ($\overline{PE}$), and Output Enable ($\overline{OE}$); thirteen address inputs, A(12:0); and eight bidirectional data lines, DQ(7:0). $\overline{CE}$ is the device enable input that controls chip selection, active, and standby modes. Asserting $\overline{CE}$ causes I_{DD} to rise to its active value and decodes the thirteen address inputs to select one of 8,192 words in the memory. $\overline{PE}$ controls program and read operations. During a read cycle, $\overline{OE}$ must be asserted to enable the outputs.

PIN NAMES

A(12:0)	Address
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PE}$	Program Enable
DQ(7:0)	Data Input/Data Output

PIN CONFIGURATION

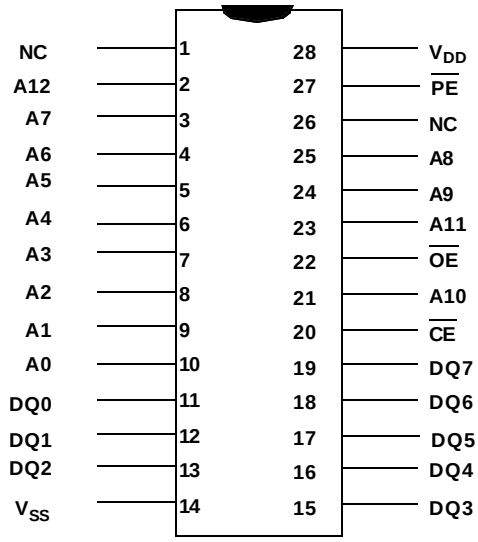


Table 1. Device Operation Truth Table [1]

$\overline{OE}$	$\overline{PE}$	$\overline{CE}$	I/O MODE	MODE
X	1	1	Three-state	Standby
0	1	0	Data Out	Read
1	0	0	Data In	Program
1	1	0	Three-state	Read [2]

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

ABSOLUTE MAXIMUM RATINGS [1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNITS
V_{DD}	DC supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage on any pin	-0.5 to (V_{DD} + 0.5)	V
T_{STG}	Storage temperature	-65 to +150	°C
P_D	Maximum power dissipation	1.5	W
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance, junction-to-case [2]	3.3	°C/W
I_I	DC input current	±10	mA

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012, infinite heat sink.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNITS
V_{DD}	Positive supply voltage	4.5 to 5.5	V
T_C	Case temperature range	-55 to +125	°C
V_{IN}	DC input voltage	0 to V_{DD}	V

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

(V_{DD} = 5.0V ±10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IH}	High-level input voltage	(TTL)	2.4		V
V_{IL}	Low-level input voltage	(TTL)		0.8	V
V_{OL1}	Low-level output voltage	I_{OL} = 4.8mA, V_{DD} = 4.5V (TTL)		0.4	V
V_{OL2}	Low-level output voltage	I_{OL} = 200µA, V_{DD} = 4.5V (CMOS)		V_{SS} + 0.05	V
V_{OH1}	High-level output voltage	I_{OH} = -400µA, V_{DD} = 4.5V (TTL) I_{OH} = -2.0mA	2.4 3.5		V
V_{OH2}	High-level output voltage	I_{OH} = -200µA V_{DD} = 4.5V (CMOS) I_{OH} = -100µA	4.45 V_{DD} - 0.3		V
C_{IN} [1]	Input capacitance	*f* = 1MHz, V_{DD} = 5.0V		15	pF
C_{IO} [1, 4]	Bidirectional I/O capacitance	*f* = 1MHz, V_{DD} = 5.0V V_{OUT} = 0V		15	pF
I_{IN}	Input leakage current	V_{IN} = 0V to V_{DD}	-1	1	µA
I_{OZ}	Three-state output leakage current	V_O = 0V to V_{DD} $\underline{V_{DD}}$ = 5.5V $\overline{OE}$ = 5.5V	-10	10	µA
I_{OS} [2,3]	Short-circuit output current	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	-90	90	mA mA
I_{DD}(OP)[5]	Supply current operating @28.6MHz (35ns product) @22.2MHz (45ns product)	TTL input levels (I_{OUT} = 0), V_{IL} = 0.2V V_{DD}, $\overline{PE}$ = 5.5V		100 85	mA
I_{DD}(SB) post-rad	Supply current standby	CMOS input levels , $\underline{V_{IL}}$ = V_{SS} to 0.25V $\overline{CE}$ = V_{DD} -025, V_{IH} = V_{DD} -0.25V		500	µA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Functional test.
5. Derates at 2.5mA/MHz.

READ CYCLE

A combination of $\overline{PE}$ greater than V_{IH}(min), and $\overline{CE}$ less than V_{IL}(max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

An address access read is initiated by a change in address inputs while the chip is enabled with $\overline{OE}$ asserted and $\overline{PE}$ deasserted. Valid data appears on data output, DQ(7:0), after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time.

The chip enable-controlled access is initiated by $\overline{CE}$ going active while $\overline{OE}$ remains asserted, $\overline{PE}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ELQV} is satisfied, the eight-bit word addressed by A(12:0) appears at the data outputs DQ(7:0).

Output enable-controlled access is initiated by $\overline{OE}$ going active while $\overline{CE}$ is asserted, $\overline{PE}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ELQV} have not been satisfied.

AC CHARACTERISTICS READ CYCLE (Post-Radiation)*

(V_{DD} = 5.0V ±10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	28F64-35		28F64-45		UNIT
		MIN	MAX	MIN	MAX	
t_{AVAV}[1]	Read cycle time	35		45		ns
t_{AVQV}	Read access time		35		45	ns
t_{AXQX}[2]	Output hold time	0		0		ns
t_{GLQX}[2]	$\overline{OE}$-controlled output enable time	0		0		ns
t_{GLQV}	$\overline{OE}$-controlled access time		15		15	ns
t_{GHQZ}	$\overline{OE}$-controlled output three-state time		15		15	ns
t_{ELQX}[2]	$\overline{CE}$-controlled output enable time	0		0		ns
t_{ELQV}	$\overline{CE}$-controlled access time		35		45	ns
t_{EHQZ}	$\overline{CE}$-controlled output three-state time		15		15	ns

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).
1. Functional test.
2. Three-state is defined as a 400mV change from steady-state output voltage.

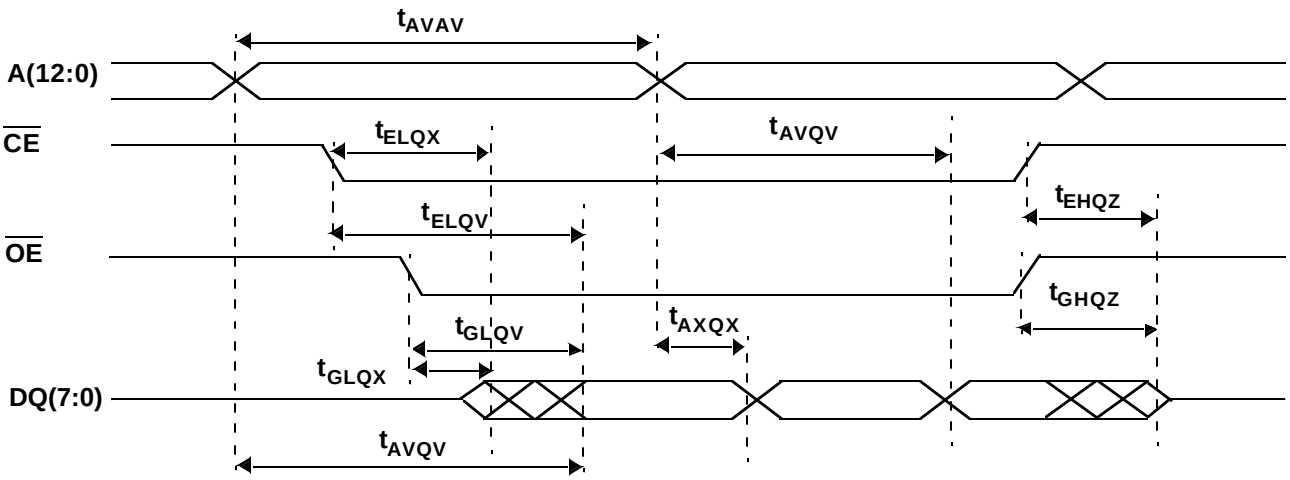


Figure 2. PROM Read Cycle

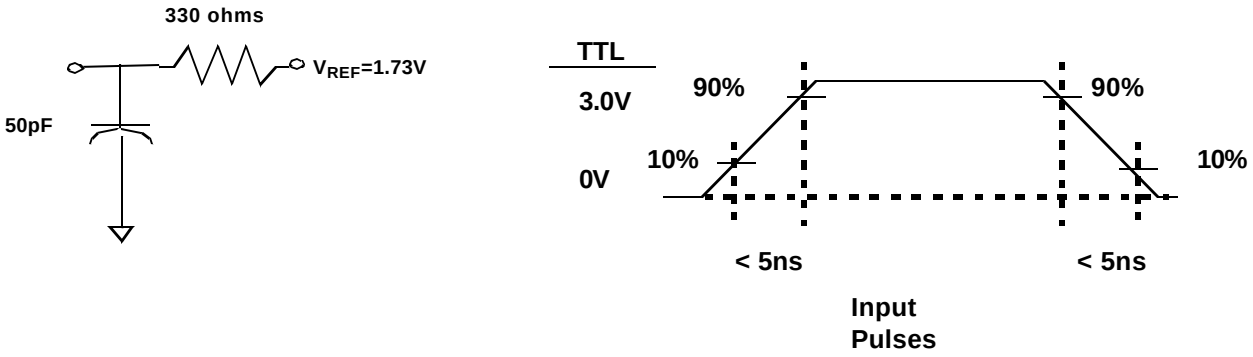
RADIATION HARDNESS

The UT28F64 PROM incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

RADIATION HARDNESS DESIGN SPECIFICATIONS [1]

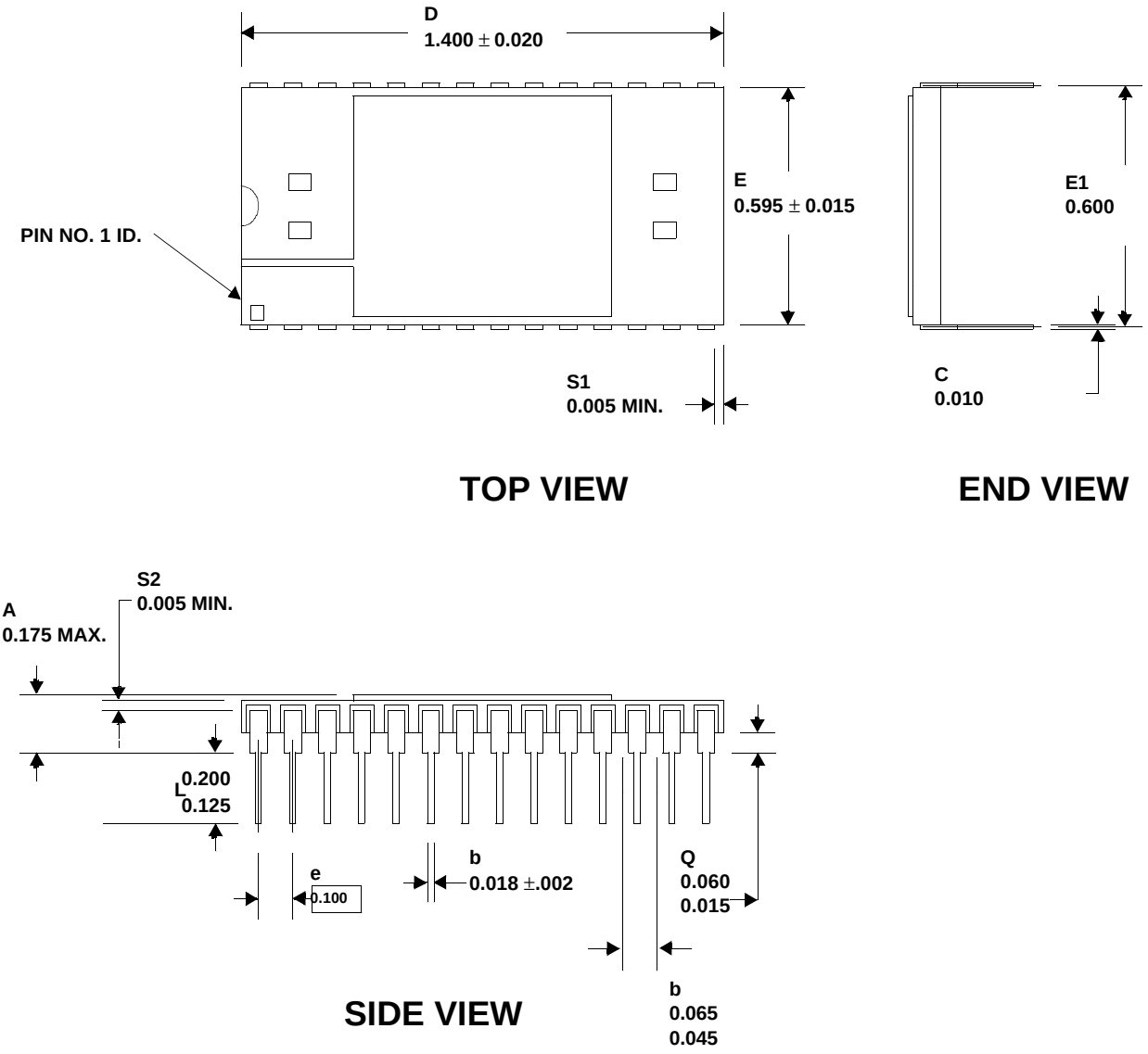
Total Dose	5.0E5	rad(Si)
Latchup LET Threshold	>128	MeV-cm^2/mg
Memory Cell LET Threshold	>128	MeV-cm^2/mg
Transient Upset LET Threshold	54	MeV-cm^2/mg
Transient Upset Device Cross Section @ LET=128 MeV-cm^2/mg	1E-6	cm^2

Note:
1. The PROM will not latchup during radiation exposure under recommended operating conditions.



Notes:
1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (TTL input = 1.5V).

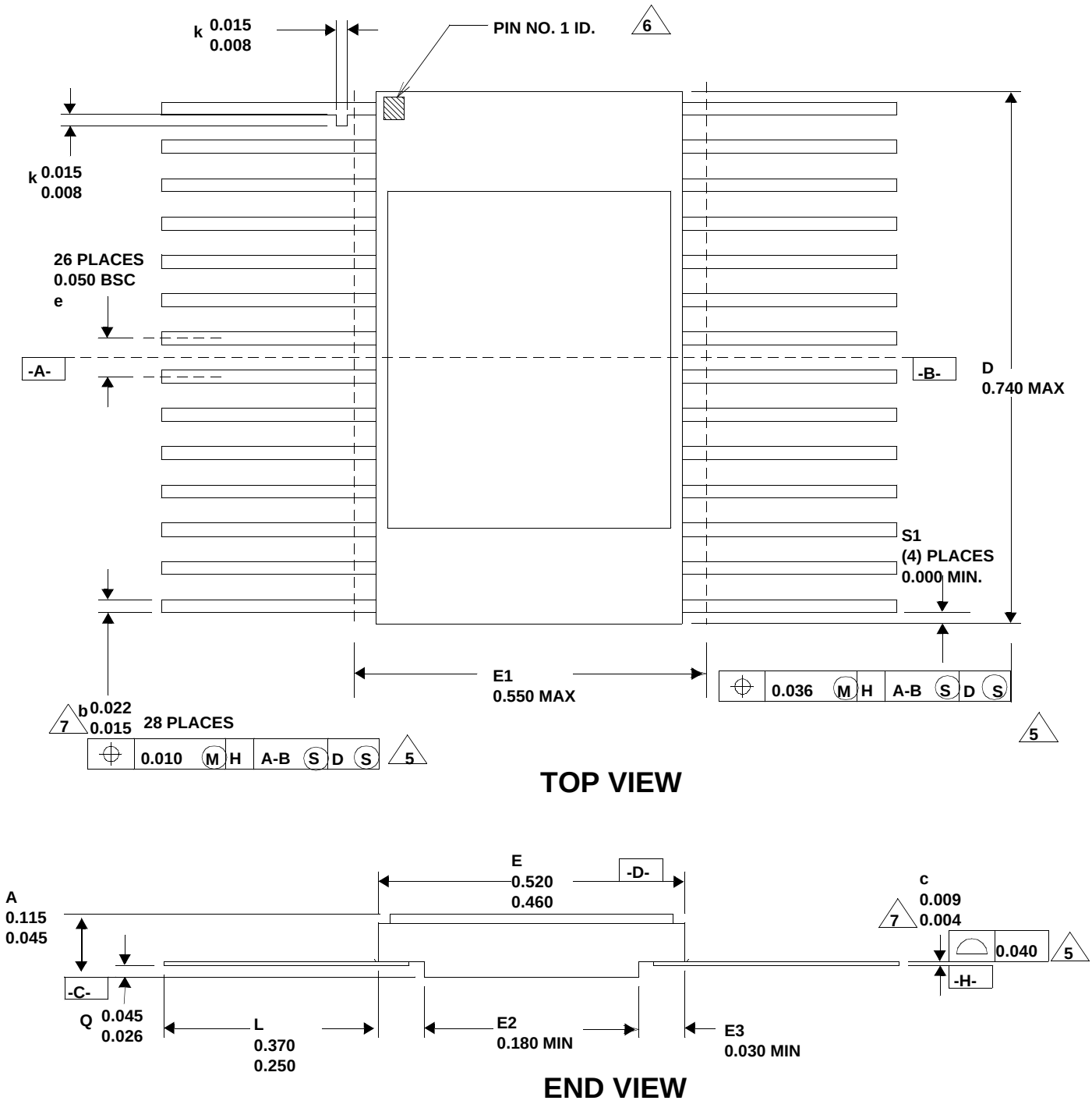
Figure 3. AC Test Loads and Input Waveforms



Notes:

1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-PRF-38535.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-STD-1835.

Figure 4. 28-Pin 100-mil Center DIP (0.600 x 1.4)



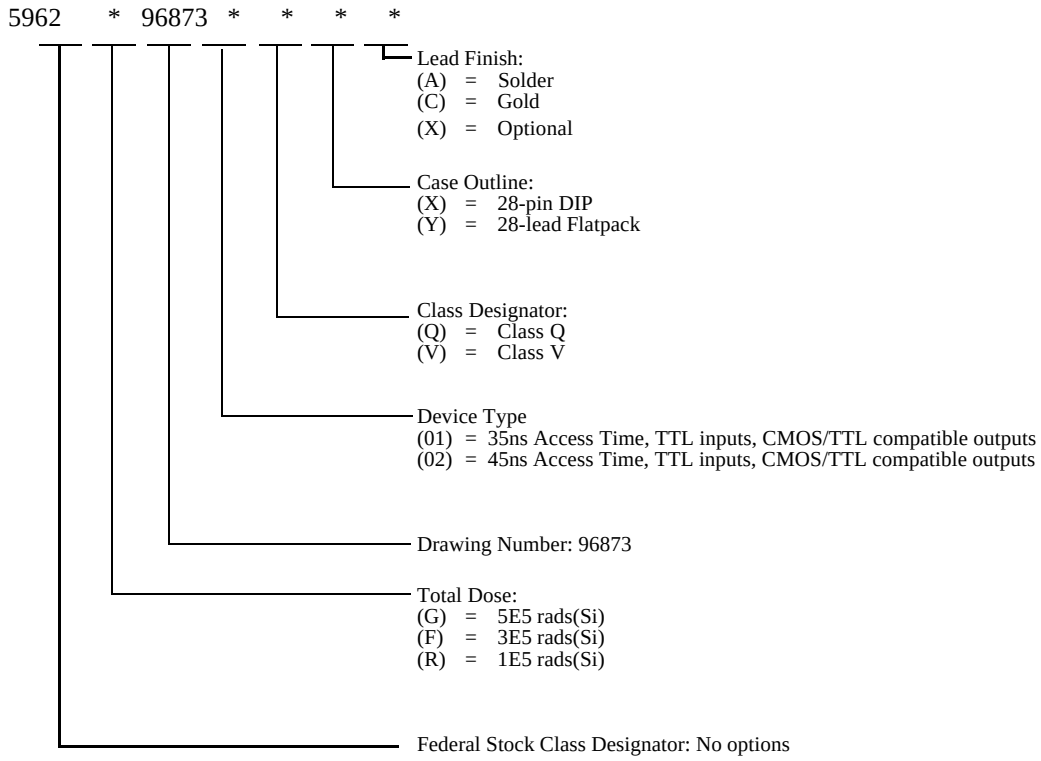
Notes:

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension letters refer to MIL-STD-1835.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option.
7. With solder, increase maximum by 0.003.

Figure 5. 28-Lead 50-mil Center Flatpack (0.490 x 0.74)

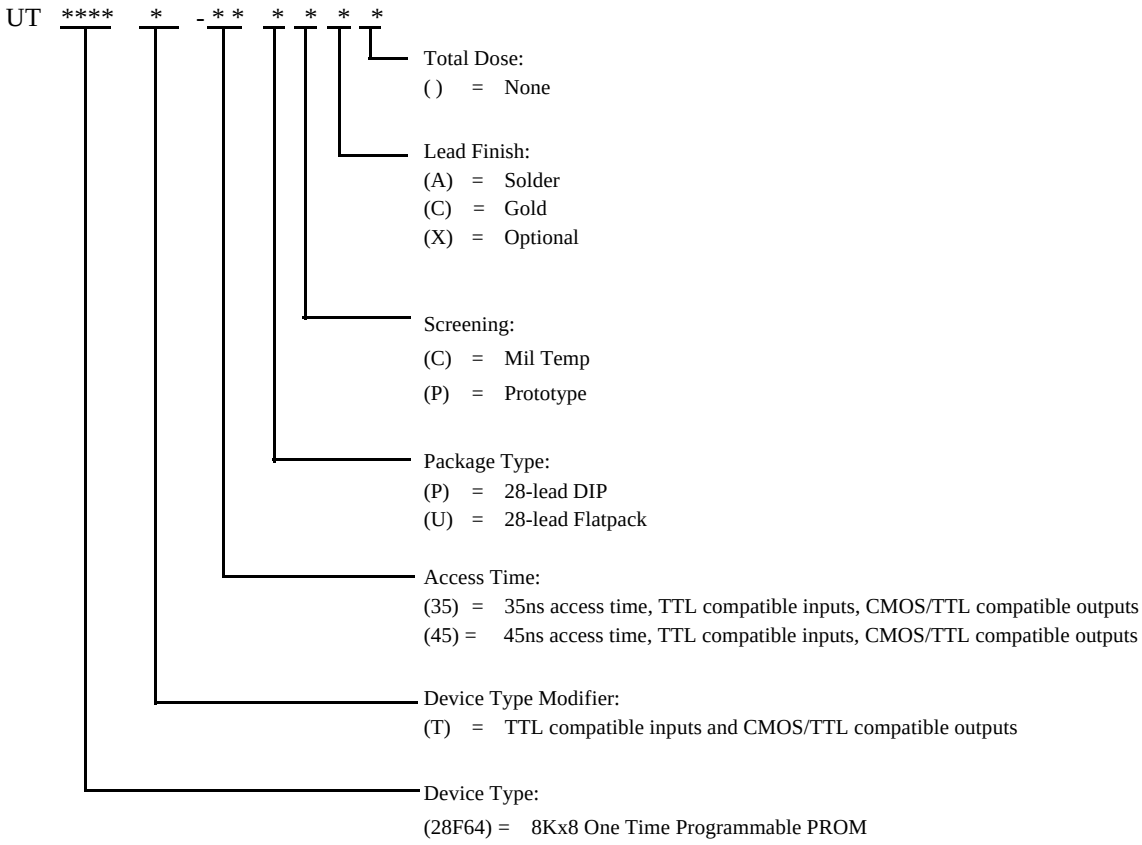
ORDERING INFORMATION

64K PROM: SMD



Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.
4. Lead finish: Factory programming either solder or gold. Field programming gold only.

64K PROM



Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Military Temperature Range flow per UTMC Manufacturing Flows Document. Radiation characteristics are neither tested nor guaranteed and may not be specified.
4. Prototype flow per UTMC Manufacturing Flows Document. Devices have prototype assembly and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed and may not be specified. Lead finish is gold only.
5. Lead finish: Factory programming either solder or gold. Field programming gold only.