TDC1035

Monolithic Peak Digitizer

8-Bit, 30ns Full Response Peak Width

Features

- 8-bit resolution
- Full DC linearity for pulses—30ns wide
- Does not require analog peak-hold circuit
- Continuous peak capture between resets
- Multiple read operations between resets
- 1/2 LSB linearity
- Narrow ambiguity region around reset
- Detects pulses as small as 12ns wide
- Guaranteed monotonic
- Selectable data format
- Available in 24-pin CERDIP and 28-lead PLCC packages
- 1.0W power consumption
- Three-state registered outputs

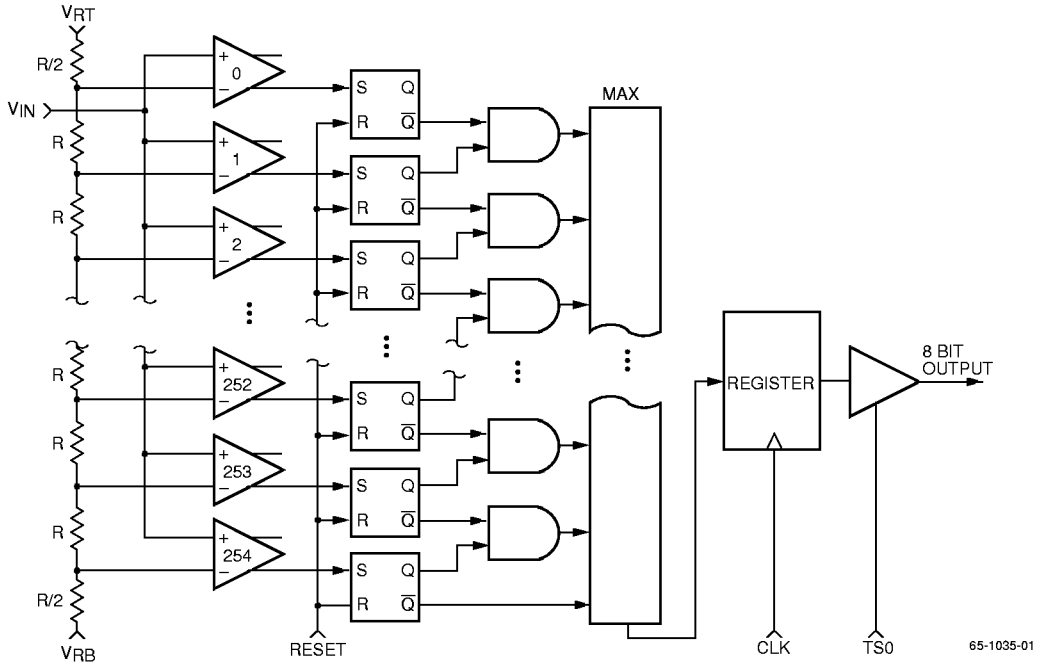
Description

The TDC1035 is a unique variant of the full-parallel ("flash") analog-to-digital converter, capable of capturing the maximum peak amplitude of one or more pulses applied to its input between asynchronous reset pulses. Multiple "peak read" operations can be performed between resets. Peaks are detected digitally, so operation is stable and predictable. Packaged in a 24-pin CERDIP, the TDC1035 features lower power consumption and smaller size than an analog peak detector/ADC combination. All digital inputs and outputs are TTL compatible, and all outputs are registered and three-state.

Applications

- Radar pulse classification
- Electronic countermeasures
- Radiation measurement
- Instrumentation

Block Diagram



Functional Description

General Information

The TDC1035 peak detector operates on ground-referenced negative-going signals. Within t_{RP} nanoseconds after the rising edge of the clock signal CLK, it outputs the most negative value reached since the previous RESET pulse. The active-HIGH RESET control is independent of CLK, but may be connected to CLK to provide a single-control peak detector. Multiple output cycles are permitted between reset operations.

The TDC1035 contains parallel array of comparators, an array of latches, and an encoder which outputs the location of the highest-valued latch which is set. The TDC1035's response characteristics are determined by its comparator array. A comparator's response time is determined by the degree of overdrive, since the output changes only when the area above threshold reaches a characteristic value. Therefore, the digitization accuracy of a pulse's peak value depends on the shape of the pulse.

To permit accurate, repeatable characterization, the TDC1035 is tested with a slew-rate limited "square" pulse. It will digitize (to its DC accuracy) the peak value of a square pulse having a minimum duration of 30ns. The accuracy degrades gracefully as the duration decreases from 30 down to 12ns, where it understates the applied amplitude by 15% (see Figure 5). Production characterization of the TDC1035 uses "square" pulses with controlled rise and fall times of 8ns.

Performance of the TDC1035 with other pulse shapes (such as Gaussian or bandwidth-limited square pulse) can be estimated by applying an energy above threshold model, with area of 120 picoVolt-seconds.

The operation of all asynchronous sequential logic circuits involves some temporal ambiguity. The most common form of this ambiguity, metastability, occurs in data synchronizers. In a peak digitizer such as the TDC1035, this ambiguity comes in the form of periods during which the accuracy of the measurement of a pulse may be affected, or the pulse may not even be detected. There is a 10ns (t_{RP}) ambiguity period after the falling edge of the RESET signal, during which detection or accuracy of detection of any pulse is not guaranteed. There is also a region of 40ns (t_{PC}) before the rising edge of the (output) clock (CLK) where a pulse may be missed or detected inaccurately. These regions are shown in the timing diagrams, Figure 1 and Figure 2. During the latter period, if the input signal increases to a new peak larger than the previously latched value, the value loaded into the output register may be incorrect (and will most likely be zero); nonetheless, the peak detection latches will hold the (correct) new peak value.

As shown in Figure 3, the TDC1035's comparator inputs have emitter-follower buffers, which limit the permissible input signal slew rate to 250V/µs. This corresponds to a full-scale transition time of 8ns.

Power

The TDC1035 operates from two supply voltages: +5.0V and -5.2V. The current return for the positive supply is D_{GND}, and the return for the negative (analog) supply is A_{GND}. All power and ground pins MUST be connected.

Reference

The reference for the TDC1035 is a negative voltage applied across a chain of 255 resistors. The top of this chain is connected to the R_T pin, and the voltage applied to the R_T pin (V_{RT}) should be within 0.1V of the analog ground. Note that the difference between the voltage applied to the pin and the voltage at the reference chain is the offset specification (E_{OT} and E_{OB}). The bottom of the reference resistor chain is connected to the R_B pin, and the voltage applied to the R_B pin (V_{RB}) should be between 1.8 and 2.2V negative with respect to the R_T pin for full-specification operation. Reduced reference voltage operation is possible at reduced accuracy (for example, for generating a nonlinear transfer function). The R_T–R_B reference source should be able to deliver at least 45mA.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be connected to circuit nodes with a low impedance to ground. For circuits in which the reference is not varied at a high rate, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (e.g., for AGC or nonlinear operation), a low-impedance reference source is required. The reference voltages may be varied dynamically; contact the factory for information on limitations when the device is used in this mode. The performance of the TDC1035 is specified with DC references of V_{RT} = 0.0V and V_{RB} = -2.0V.

Control

Two function control pins, $\overline{\text{MINV}}$ and $\overline{\text{LINV}}$, are provided. These names stand for active-LOW Most significant bit INVert and active-LOW Least significant bits INVert, respectively These controls are for DC (i.e., steadystate), not dynamic, use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the Output Coding Table. A single output state control pin, $\overline{\text{OE}}$, is provided. The three-state outputs may be placed in a high-impedance state by applying a logic HIGH to the $\overline{\text{OE}}$ control pin, and enabled by driving $\overline{\text{OE}}$ LOW.

The function control pins may be tied to V_{CC} for a logic HIGH, and D_{GND} for a logic LOW; however, a 2.2 kOhm pull-up resistor is preferred over direct connection to V_{CC}. If a pull-up resistor is not used, the absolute maximum voltage rating for the part becomes that of the TTL input, 5.5V, rather than the higher value for the V_{CC} terminal.

Command

Two pins, RESET and CLK, control the TDC1035. When brought HIGH, the level-sensitive RESET control resets the peak-storing latches. The edge-sensitive CLK control causes the peak value to be loaded into the output register when a rising-edge (LOW-to-HIGH) signal is applied. As noted above, there is a data ambiguity period associated with the operation of each of these inputs.

Analog Input

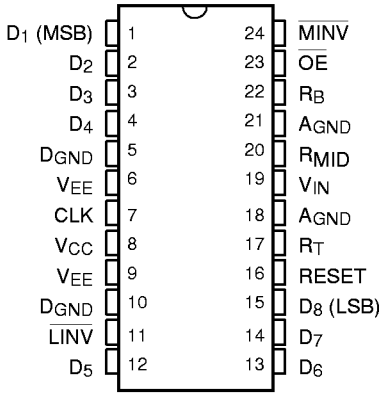
Although the TDC1035's 255 comparators have emitter-follower isolated inputs, the input impedance can vary up to 25 percent with the signal level, as comparator input transistors switch on or off. As a result, for optimal performance, the source impedance of the driving device must be less than 25 Ohms. The input signal will not damage the TDC1035 if it remains in the range V_{EE}–0.5V to V_{AGND}+0.5V. If the input signal stays between the V_{RT} and V_{RB} reference voltages, the 8-bit digital equivalent of the most negative voltage reached will be latched into the array of latches, subject to the dynamic effects mentioned above. A transient more negative than V_{RB} will cause a full-scale output t_{DO} after the CLK line rises.

Outputs

The outputs of the TDC1035 are TTL compatible, capable of driving four low-power Schottky TTL (54LS/74LS) unit loads or the equivalent. The outputs hold the previous data a minimum time t_{HO} after the rising edge of the CLK input, and are guaranteed to have the new output value after a maximum time t_{DO}. Under light DC load conditions (such as driving CMOS loads or base-input low-power Schottky such as the 74L5374) 2.2k pull-up resistors to +5.0V are recommended.

Pin Assignments

24 Lead Ceramic DIP



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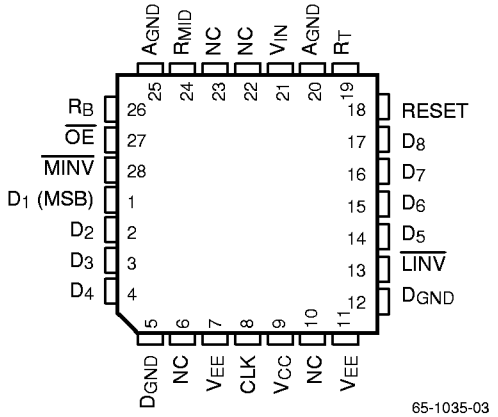
28 Lead PLCC



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Pin Definitions

Pin Name	Pin Number		Value	Pin Function Description
	Ceramic DIP	PLCC		
Power				
V_{CC}	8	9	+5.0V	Positive Supply Voltage
V_{EE}	6,9	7,11	-5.2v	Negative Supply Voltage
D_{GND}	5,10	5,12	0.0V	Digital Ground
A_{GND}	18, 21	20, 25	0.0V	Analog Ground
Reference				
R_T	17	19	0.0V	Reference Resistor, Top
R_{MID}	20	24	-1.0V	Reference Resistor, Middle
R_B	22	26	-2.0V	Reference Resistor, Bottom
Control				
$\overline{MINV}$	24	28	TTL (Active LOW)	MSB Invert
$\overline{LINV}$	11	13	TTL (Active LOW)	LSB Invert
$\overline{OE}$	23	27	TTL (Active LOW)	Output Enable
Command				
RESET	16	18	TTL (Active HIGH)	Resets Peak Value to Zero
CLK	7	8	TTL (Rising Edge)	Loads Output Register
Analog Input				
V_{IN}	19	21	0.0V to -2.0V	Analog Input Signal
Outputs				
D_1	1	1	TTL	MSB Output
D_2	2	2	TTL	
D_3	3	3	TTL	
D_4	4	4	TTL	
D_5	12	14	TTL	
D_6	13	15	TTL	
D_7	14	16	TTL	
D_8	15	17	TTL	LSB Output

Absolute Maximum Ratings[1]

(beyond which the device may be damaged)

Parameter	Min.	Max.	Unit
Supply Voltages			
V_{CC} (measured to D_{GND})	-0.5	+7.0	V
V_{EE} (measured to D_{GND})	-7.0	+0.5	V
A_{GND} (measured to D_{GND})	-0.5	+0.5	V
Input Voltages			
RESET, CLK, $\overline{OE}$, $\overline{MINV}$, $\overline{LINV}$ (measured to A_{GND})	-0.5	+5.5	V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	V_{EE} – 0.5	+0.5	V
V_{RT} (measured to V_{RB})	-2.2	+2.2	V

Absolute Maximum Ratings[1] (continued)

(beyond which the device may be damaged)

Parameter		Min.	Max.	Unit
Outputs				
Applied voltage (measured to D_{GND})[2]		-0.5	+0.5	V
Applied current (externally forced)[3,4]		-1.0	6.0	mA
Short-circuit duration (single output HIGH to shorted to ground)			1	Second
Temperature				
Operating	Ambient	-55	+125	°C
	Junction		+175	°C
Lead, soldering (10 seconds)			+300	°C
Storage		-65	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance is guaranteed only if specified operating conditions are met.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive current flowing into the device.

Operating Conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.5	V
V_{EE}	Negative Supply Voltage	-4.90	-5.2	-5.5	-4.90	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage	-0.1	0.0	0.1	-0.1	0.0	0.1	V
t_{PWHR}	Reset Minimum Pulse Width, HIGH	20			20			ns
t_{PWLC}	CLK Minimum Pulse Width, LOW	20			20			ns
t_{PWHC}	CLK Minimum Pulse Width, HIGH	20			20			ns
S_R	Input Signal Slew Rate			250			250	V/μS
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-400			-400	μA
V_{RT}	Reterence Voltage, Top	-0.1	0.0	0.1	-0.1	0.0	0.1	V
V_{RB}	Reference Voltage, Bottom	-1.8	-2.0	-2.2	-1.8	-2.0	-2.2	V
V_{RT-}	Reference Voltage Span	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage Range	V_{RT}		V_{RB}	V_{RT}		V_{RB}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		+125	°C

DC Electrical Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min.	Max.	Min.	Max.	
I_{CC}	Positive Supply Current	V_{CC} = Max, Static		35		35	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, Static		-160		-160	mA
I_{REF}	Reference Current	V_{RT}–V_{RB} = Nom		35		35	mA
R_{REF}	Reference Resistance	Total, R_T to R_B	57		57		Ohms
R_{IN}	Input Equivalent Resistance (DC)	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	50		50		kOhms
C_{IN}	Input Capacitance, Analog	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		50		50	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		250		350	µA
I_{IL}	Input Current Logic LOW	V_{CC} = Max, V_{IL} = 0.4V		-500		-500	µA
I_{IH}	Input Current Logic HIGH	V_{CC} = Max, V_{IH} = 2.4V		50		50	µA
I_{IM}	Input Current, V_{IN} = Max	V_{CC} = Max, V_{IH} = 5.5V		1		1	mA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = Max, V_O = 0V	-30	30	-30	30	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = Max, V_O = 5V	-30	30	-30	30	µA
I_{OS}	Short-Circuit Output[1]	V_{CC} = Max, Output HIGH, one output tied to D_{GND} for 1 second.		-50		-50	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Max, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
C_{IN}	Input Capacitance, Digital			10		10	pF

Note:

1. Worst case all digtal inputs and outputs LOW.

AC Electrical Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min.	Max.	Min.	Max.	
t_{PC}	CLK Setup Time	V_{CC} = Min, V_{EE} = Min, Load 1		30		30	ns
t_{RP}	RESET Delay	V_{CC} = Min, V_{EE} = Min, Load 1		5		5	ns
t_{DO}	Output Delay	V_{CC} = Min, V_{EE} = Min, Load 1		35		35	ns
t_{HO}	Output Hold Time	V_{CC} = Min, V_{EE} = Min, Load 1	5		5		ns
t_{DIS}	Output Disable Time	V_{CC} = Min, V_{EE} = Min, Load 1		20		20	ns
t_{ENA}	Output Enable Time	V_{CC} = Min, V_{EE} = Min, Load 1		70		90	ns

Note:

1. t_{RP} and t_{PC} are the guaranteed maximum lengths of the ambiguity periods.

Timing Diagrams

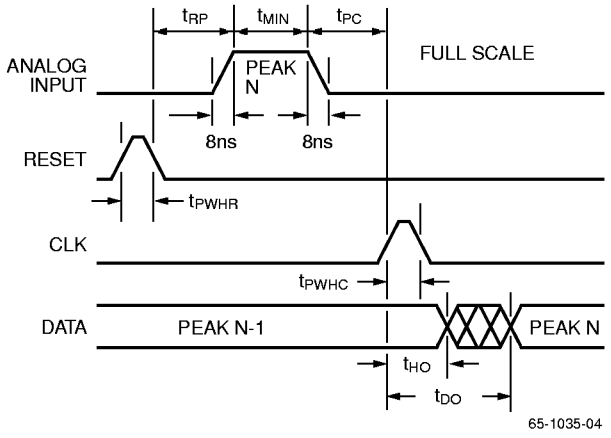


Figure 1. Timing with Separate RESET and CLK

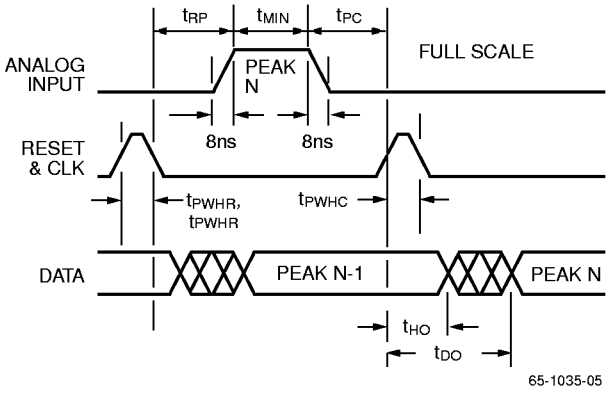


Figure 2. Timing with Common RESET and CLK

System Performance Characteristics

Parameter		Test Conditions		Temperature Range: Standard Min.	Standard Max.	Extended Min.	Extended Max.	Units
E_{LI}	Linearity Error, Integral, Independent	V_{RT}, V_{RB} = Nom			0.2		0.2	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB} = Nom			0.2		0.2	%FS
CS	Code Size	V_{RT}, V_{RB} = Nom		30	170	30	170	% Nominal
t_{MIN}	Analog Input Pulse Width	Square Pulse	15% Accuracy	12		12		ns
			DC Accuracy	30		30		ns
E_{OT}	Offset Error, Top	V_{IN} = V_{RT}			±8		±8	mV
E_{OB}	Offset Error, Bottom	V_{IN} = V_{RB}			±15		±15	mV
T_{CO}	Offset Error, Temperature Coefficent	V_{RT}, V_{RB}, V_{CC}, V_{EE} = Nom			±20		±20	µV/°C

Equivalent Circuits

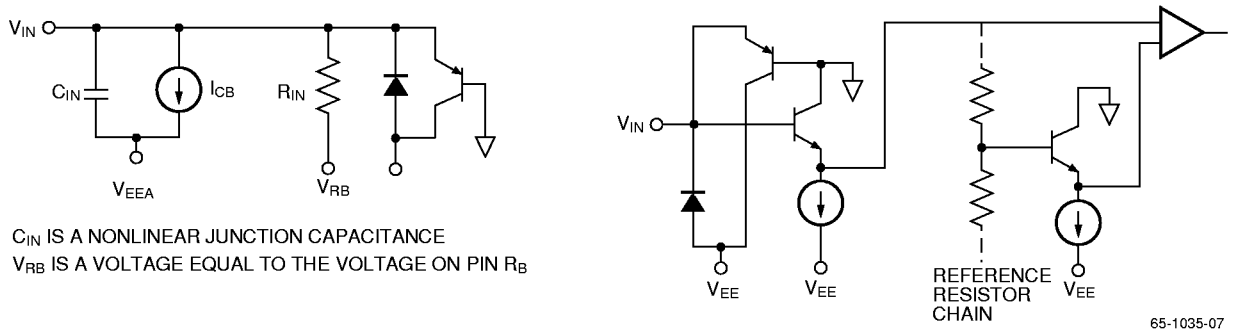


Figure 3. Simplified Analog Input Equivalent Circuits

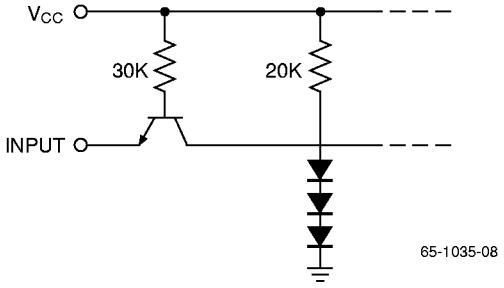


Figure 4. Digital Input Equivalent Circuit

Performance Curve

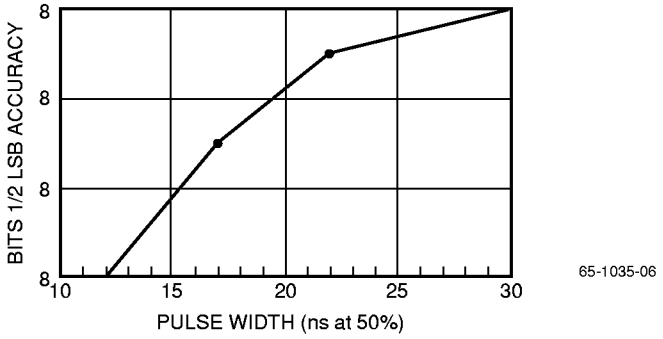


Figure 5. Variation of Accuracy as a Function of Width, "Square" Input Pulse

Output Coding

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	-2.0000V FS 7.8431mV Step	-2.0000V FS 8.000mV Step	MINV = 1 LINV = 1	0 0	0 1	1 0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	-0.0078V	-0.0080V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	-0.9922V	-1.0160V	01111111	10000000	11111111	00000000
128	-1.0000V	-1.0240V	10000000	01111111	00000000	11111111
129	-1.0078V	-1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	-1.9844V	-2.0240V	11111110	00000001	01111110	10000001
255	-1.9922V	-2.0320V	11111111	00000000	01111111	10000000

Applications Discussion

Under certain conditions, the real component of the input impedance may go negative at frequencies near 100MHz. To prevent oscillation at the input signal port, Fairchild recommends connecting the input signal to the TDC1035 via a series-connected resistor of at least 10 Ohms located close to the device. Further, if the signal bandwidth is not already limited so that the input slew rate limit is not exceeded, external circuitry is also recommended. The circuit shown in Figure 7 accomplishes both goals.

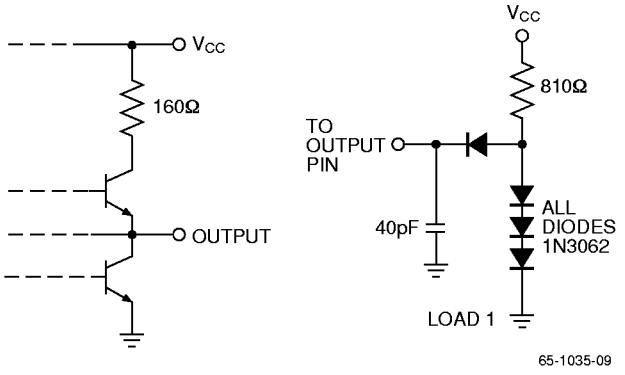


Figure 6. Output Circuits

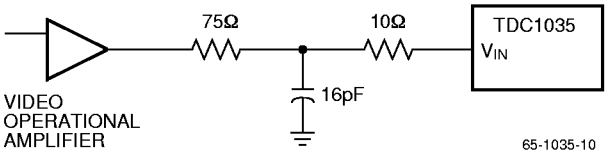


Figure 7. Recommended Input Circuit

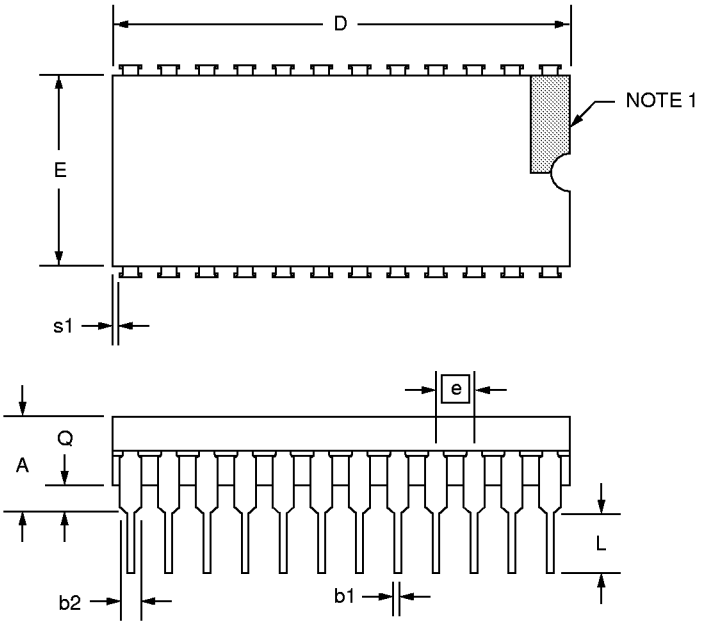
Mechanical Dimensions

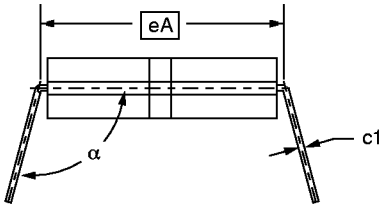
24 Lead Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.225	—	5.72	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.290	—	32.77	4
E	.500	.610	12.70	15.49	4
e	.100 BSC		2.54 BSC		5, 9
eA	.600 BSC		15.24 BSC		7
L	.120	.200	3.05	5.08	
Q	.015	.075	.38	1.91	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13 and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
6. Applies to all four corners (leads number 1, 12, 13, and 24).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twenty-two spaces.





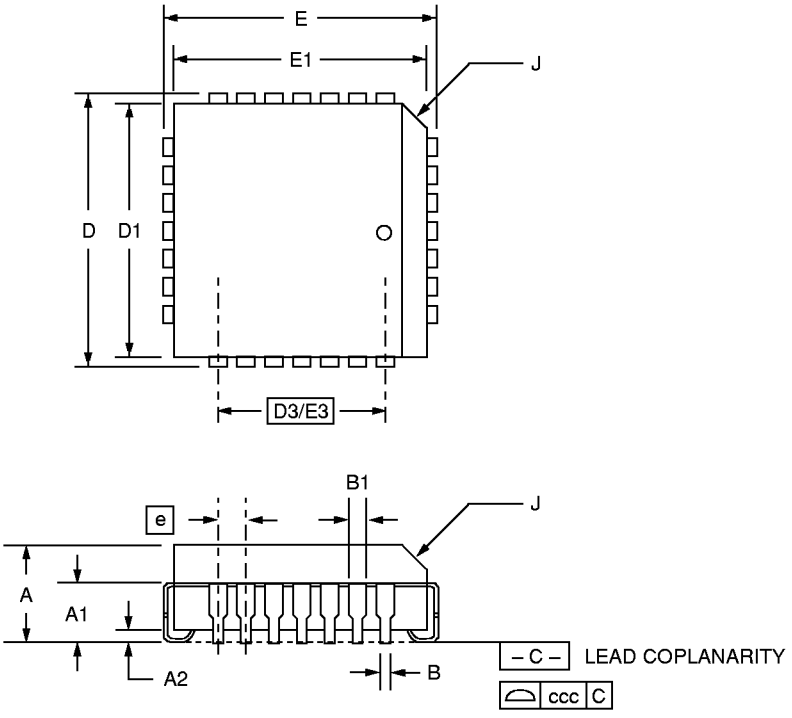
Mechanical Dimensions

28 Lead PLCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1035B7C	STD–T_A = 0°C to 70°C	Commercial	24 Lead Ceramic DIP	1035B7C
TDC1035B7V	EXT–T_C = -55°C to 125°C	MIL-STD-833	24 Lead Ceramic DIP	1035B7V
TDC1035R3C	T_A = 0°C to 70°C	Commercial	28 Lead PLCC	1035R3C

5/20/98 0.0m 001
Stock# DS90001035