

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14					
PMIC N/A	PREPARED BY Gary Zahn	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444																		
<b>STANDARDIZED MILITARY DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY Michael C. Jones	MICROCIRCUIT, LINEAR, DIGITAL TO SYNCHRO/RESOLVER CONVERTER, MICROPROCESSOR COMPATIBLE, 16-BIT, HYBRID																		
	APPROVED BY Kendall A. Cottongim																			
	DRAWING APPROVAL DATE 94-07-08	SIZE <b>A</b>	CAGE CODE <b>67268</b>	<b>5962-94646</b>																
	REVISION LEVEL	SHEET		1	OF		14													

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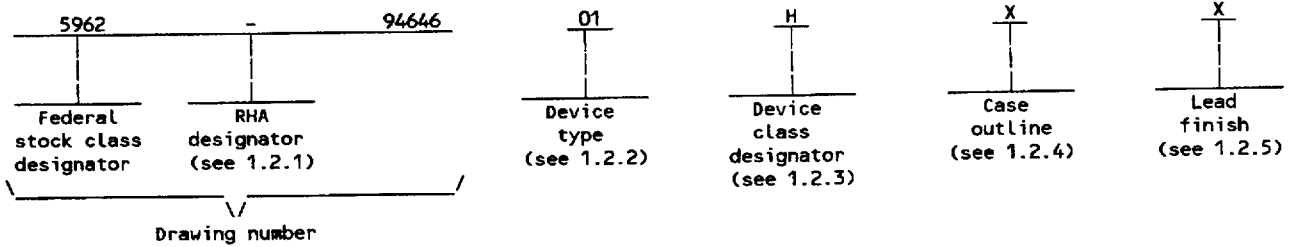
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1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). This drawing describes device requirements for hybrid microcircuits to be processed in accordance with MIL-H-38534. Two product assurance classes, military high reliability (device class H) and space application (device class K) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-H-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Accuracy</u>
01	HDSR2006-34V/S/2	Digital-to-synchro/resolver converter	± 1 arc min synchro mode ± 2 arc min resolver mode
02	HDSR2006-34V/R/2	Digital-to-synchro/resolver converter	± 1 arc min resolver mode ± 2 arc min synchro mode
03	HDSR2006-34H/2	Digital-to-synchro/resolver converter	± 2 arc min both modes
04	HDSR2006-34S/2	Digital-to-synchro/resolver converter	± 4 arc min both modes
05	HDSR2056-34V/S/2	Digital-to-synchro/resolver converter	± 1 arc min synchro mode ± 2 arc min resolver mode
06	HDSR2056-34V/R/2	Digital-to-synchro/resolver converter	± 1 arc min resolver mode ± 2 arc min synchro mode
07	HDSR2056-34H/2	Digital-to-synchro/resolver converter	± 2 arc min both modes
08	HDSR2056-34S/2	Digital-to-synchro/resolver converter	± 4 arc min both modes

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
H or K	Certification and qualification to MIL-H-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	36	Dual-in-Line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-H-38534 for classes H and K. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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1.3 Absolute maximum ratings. 1/

Power supplies:

+V <sub>S</sub> . . . . .	+18 V dc
-V <sub>S</sub> . . . . .	-18 V dc
Logic input voltage range . . . . .	-0.3 V dc to +6.5 V dc
Reference input voltage . . . . .	Twice the pin programmed voltage
Power dissipation (P <sub>D</sub> ) . . . . .	1 W
Storage temperature range . . . . .	-65°C to +150°C
Lead temperature (soldering, 10 seconds) . . . . .	+300°C
Junction temperature (T <sub>J</sub> ) . . . . .	+170°C

1.4 Recommended operating conditions.

Power supplies voltage range:

+V <sub>S</sub> . . . . .	+13.5 V dc to +16.5 V dc
-V <sub>S</sub> . . . . .	-13.5 V dc to -16.5 V dc
Ambient operating temperature range (T <sub>A</sub> ) . . . . .	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. Unless otherwise specified, the following specification, standards, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-H-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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### 3. REQUIREMENTS

- 3.1 Item requirements. The individual item requirements shall be in accordance with MIL-H-38534 and as specified herein.
- 3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-H-38534 and herein.
- 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.
- 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.
- 3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.
- 3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.
- 3.5 Marking. Marking shall be in accordance with MIL-H-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in QML-38534.
- 3.6 Manufacturer eligibility. In addition to the general requirements of MIL-H-38534, the manufacturer of the part described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DESC-EC) upon request.
- 3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DESC-EC shall affirm that the manufacturer's product meets the requirements of MIL-H-38534 and the requirements herein.
- 3.8 Certificate of conformance. A certificate of conformance as required in MIL-H-38534 shall be provided with each lot of microcircuits delivered to this drawing.

### 4. QUALITY ASSURANCE PROVISIONS

- 4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-H-38534.
- 4.2 Screening. Screening shall be in accordance with MIL-H-38534. The following additional criteria shall apply:
- a. Burn-in test, method 1015 of MIL-STD-883.
- (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EC or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- (2)  $T_A$  as specified in accordance with table I of method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES	MSB = 180° and LSB = .0055°	7, 8	ALL	16		Bits
Accuracy	A <sub>OUT</sub>	Measured at angles of 0°, 10°, 20°, 30°, 40°, 50°, 60°, 90°, 120°, 135°, 150°, 180°, 210°, 225°, 240°, 270°, 300°, 315°, and 330°	4, 5, 6	01,02, 05,06 03,07 04,08	-1 <u>2/</u>	+1 <u>2/</u>	Arc min
					-2 <u>3/</u>	+2 <u>3/</u>	
					-4 <u>3/</u>	+4 <u>3/</u>	

REFERENCE INPUTS

Reference voltage <sup>4/</sup> (pin programmable)	V <sub>IN</sub>	Input between RH' and RL', Input between RH and RL, Input between RH and RL with RH' and RL' grounded, see figure 3	4, 5, 6	ALL	1.17 23.47 103.5	1.43 28.6 126.5	V rms
Frequency <sup>4/</sup>		dc to 1000 Hz	4, 5, 6	ALL		1000	Hz
Input impedance <sup>4/</sup>	Z <sub>IN</sub>	RH and RL, differential	4, 5, 6	ALL	198	202	kΩ
		RH and RL, single ended			99	101	
		RH' and RL', differential			9.9	10.1	
		RH' and RL', single ended			4.95	5.05	

DIGITAL INPUT <sup>5/</sup>

Input low voltage	V <sub>IL</sub>	Logic "0"	1, 2, 3	ALL	-0.3	+0.8	V
Input high voltage	V <sub>IH</sub>	Logic "1"			2.4	5.5	

ANALOG OUTPUTS (resolver or synchro modes)

Output voltage (S <sub>in</sub> , C <sub>os</sub> )	V <sub>OUT</sub>		4, 5, 6	ALL	6.742	6.878	V rms
Output voltage (S <sub>1</sub> , S <sub>2</sub> , S <sub>3</sub> )	V <sub>OUT</sub>	Measured between any two of these pins			11.682	11.918	
Output current, each output	I <sub>OUT</sub>	+V <sub>S</sub> = +16.5 V dc	4, 5, 6	ALL		2	mA
		-V <sub>S</sub> = -16.5 V dc				2	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

**ANALOG OUTPUTS (resolver or synchro modes) - Continued.**

DC offset	V <sub>OS</sub>		1, 2, 3	ALL	-50	+50	mV
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**REGISTER CONTROLS (functional testing)**

Enables HI byte	HBE	Data inputs B1 through B8 enter the buffer register	7	ALL	logic "1"	
		Buffer register in the hold mode			logic "0"	
Enables LO byte	LBE	Data inputs B9 through B16 enter the buffer register	7	ALL	logic "1"	
		Buffer register in the hold mode			logic "0"	
Transfer data logic	LDC	Transfers contents of the buffer register to the holding register	7	ALL	logic "1"	
		Converter in the hold mode			logic "0"	
0° test angle	ST0	Normal operation	7	01,02, 03,04	logic "1"	
		Presets 0° angle to holding register			logic "0" <sup>6/</sup>	
90° test angle	ST90	Normal operation	7	01,02, 03,04	logic "1"	
		Presets 90° angle to holding register			logic "0" <sup>7/</sup>	

**POWER SUPPLIES**

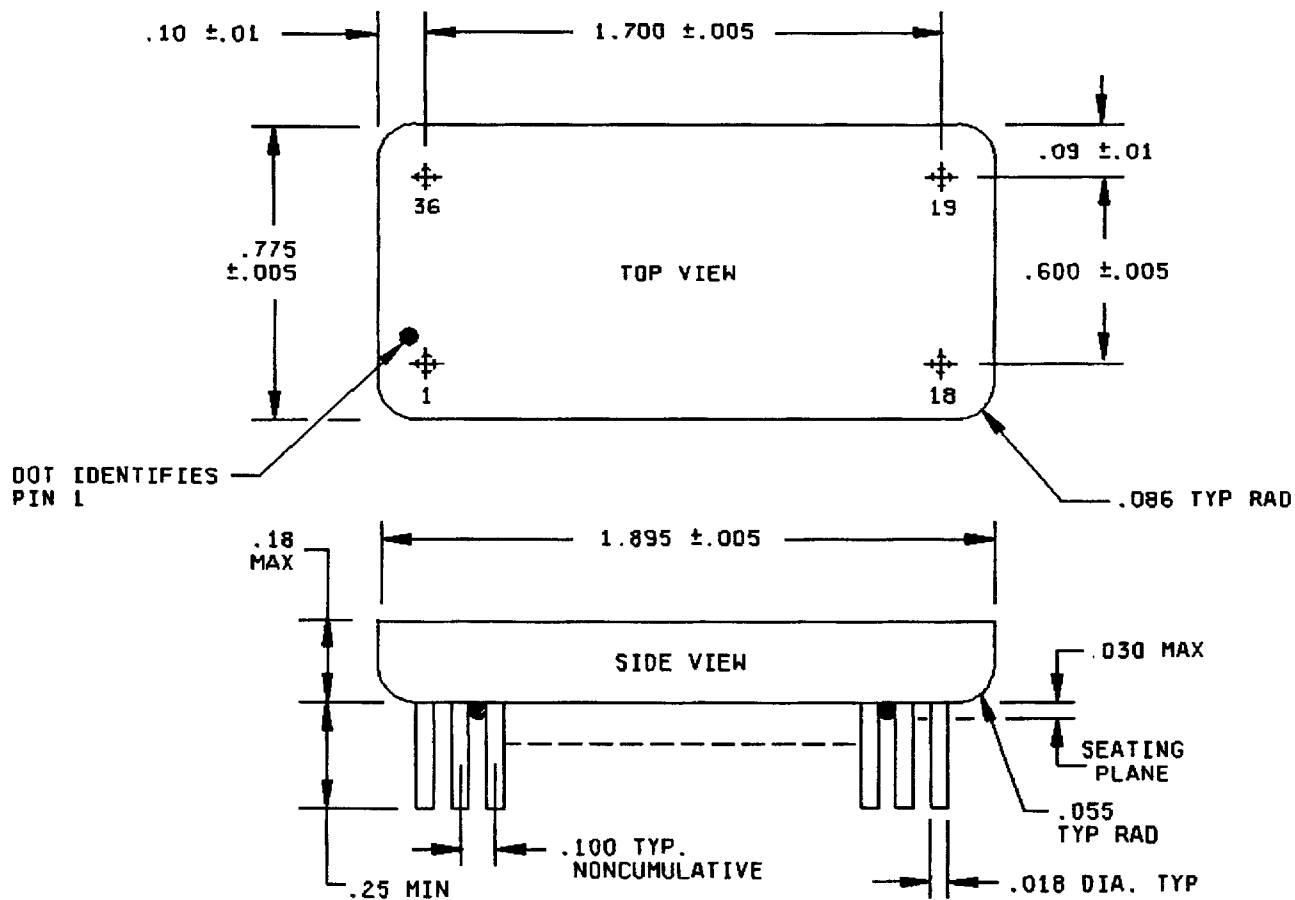
Supply currents	±I <sub>SQ</sub>	±V <sub>S</sub> = ±16.5 V dc, no load	1, 2, 3	ALL		±30	mA
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- 1/ Unless otherwise specified; +V<sub>S</sub> = +15 V dc and -V<sub>S</sub> = -15 V dc.
- 2/ Accuracy is measured and recorded in the highest accuracy mode at 400 Hz ±10% carrier frequency. The alternate mode is tested on a go-no-go basis at angles 90°, 180°, 225°, 270°, and 315°.
- 3/ Accuracy is measured and recorded at 400 Hz ±10% carrier frequency in the synchro mode; resolver mode is tested on a go-no-go basis.
- 4/ Parameters shall be tested as part of device initial characterization and after design and process changes. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.
- 5/ Logic "0" low limit of -0.3 V dc and logic "1" high of +V<sub>S</sub> are not tested and are guaranteed by design.
- 6/ Assumes ST90 = logic "1".
- 7/ Assumes ST0 = logic "1"

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Inches	mm	Inches	mm
.005	0.13	.100	2.54
.010	0.25	.180	4.57
.018	0.46	.250	6.35
.030	0.76	.600	15.24
.055	1.40	.775	19.69
.086	2.18	1.700	43.18
.090	2.29	1.895	48.13

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for information only.
3. Lead spacing dimensions apply only at seating plane.
4. Case is electrically floating.
5. Standoffs are ceramic or glass (3 each).

FIGURE 1. Case outline X.

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Device types	01-08
Case outline	X
Terminal number	Terminal connection
1	S1
2	S2 (Cos)
3	S3 (Sin)
4	S3'
5	S2'
6	R
7	RL'
8	RL
9	RH
10	RH'
11	STO
12	ST90
13	+V <sub>S</sub>
14	-V <sub>S</sub>
15	TP1
16	LDC
17	LBE
18	Ground
19	B16
20	B15
21	B14
22	B13
23	B12
24	B11
25	B10
26	B9
27	B8
28	B7
29	B6
30	B5
31	B4
32	B3
33	B2
34	B1
35	HBE
36	V <sub>L</sub>

NOTE: For device types 05, 06, 07, and 08, pins 11, 12, and 36 are NC (no connections).

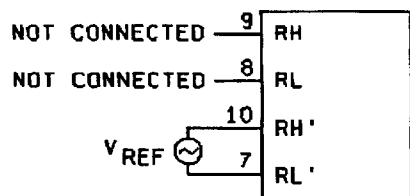
FIGURE 2. Terminal connections.

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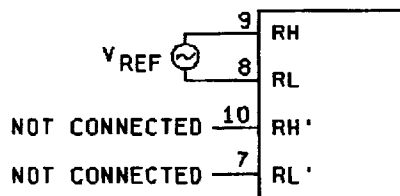
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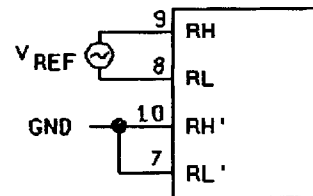




1.3 V rms REFERENCE

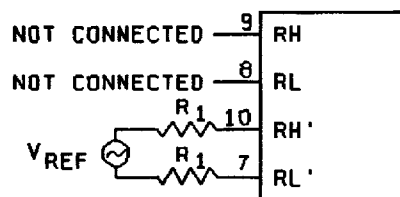


26 V rms REFERENCE



115 V REFERENCE

Circuit A



$$R_1 = \frac{5}{1.3} (V_{REF} - 1.3) \text{ k}\Omega$$

$V_{REF}$ (V rms)	2	3	5	7	10	13	16	20	25
$R_1$ (k $\Omega$ )	2.69	6.54	14.23	21.92	33.46	45.00	56.54	71.92	91.15

$$V_{REF} = 1.3 \text{ V rms to } 26 \text{ V rms}$$

Circuit B

FIGURE 3. Reference level adjustment circuits and tables.

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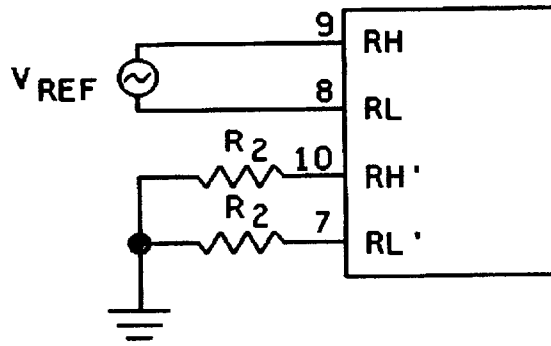
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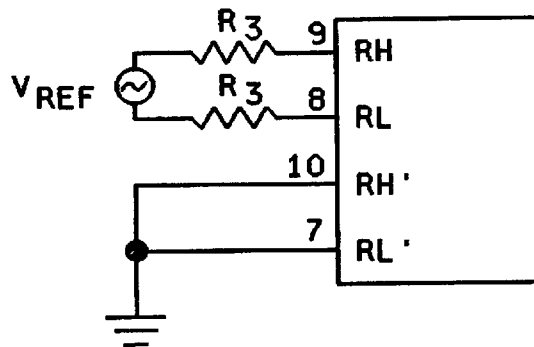


$$R_2 = \left( \frac{97.54}{V_{REF} - 26} - 1096 \right) \text{ k}\Omega$$

$V_{REF}$ (V <sub>rms</sub> )	30	40	50	60	70	80	90	100	110
$R_2$ (k $\Omega$ )	23.28	5.87	2.97	1.77	1.12	0.710	0.428	0.222	0.065

$V_{REF} = 26 \text{ V rms to } 115 \text{ V rms}$

Circuit C



$$R_3 = (0.8558 V_{REF} - 98.417) \text{ k}\Omega$$

$V_{REF}$ (V <sub>rms</sub> )	120	130	140	150	160	170	180	190	200
$R_3$ (k $\Omega$ )	4.28	12.84	21.40	29.95	38.51	47.07	55.63	64.19	72.74

$V_{REF}$  greater than 115 V rms

Circuit D

FIGURE 3. Reference Level adjustment circuits and tables - Continued.

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NOTES:

1. Internal resistors allow pin programming for three standard reference voltages with the normal analog output (6.81 V rms for resolvers and 11.8 V rms for synchros) as shown on circuit A. Proportionally higher or lower voltages will be obtained for analog outputs when higher or lower reference voltages are used.
2. To obtain nominal analog output with nonstandard reference voltages other than circuit A, two external resistors are required. The input resistance for RH and RL is 100 kΩ and RH' and RL' are 5 kΩ. The circuit configuration for reference voltages other than circuit A are shown on circuit B.
3. For high reference voltages (26 V rms to 115 V rms), the resistor values for R<sub>1</sub> in circuit B might become too large to be practical. In these situations, the external resistors should be connected as shown on circuit C.
4. For reference voltages greater than 115 V rms, the external resistors should be connected as shown on circuit D.

FIGURE 3. Reference level adjustment circuits and tables - Continued.

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TABLE II. Electrical test requirements.

MIL-H-38534 test requirements	Subgroups (in accordance with MIL-H-38534, group A test table)
Interim electrical parameters	1,4,7
Final electrical test parameters	1*,2,3,4,5,6,7,8
Group A test requirements	1,2,3,4,5,6,7,8
Group C end-point electrical parameters	1,2,3,4,7
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups ** (in accordance with method 5005, group A test table)

\* PDA applies to subgroup 1.

\*\* When applicable to this standardized military drawing,  
the subgroups shall be defined.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-H-38534 and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-H-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 9, 10, and 11 shall be omitted.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-H-38534.

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4.3.3 Group C inspection. Group C inspection shall be in accordance with MIL-H-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EC or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
  - (2)  $T_A$  as specified in accordance with table I of method 1005 of MIL-STD-883.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-H-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

- a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- b. End-point electrical parameters shall be as specified in table II herein.
- c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.
- d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-H-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5$  percent, after exposure.
- e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.
- f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.
- g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-H-38534.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5373.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document Listing</u>
New MIL-H-38534 Standardized Military Drawings	5962-XXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply for device classes H and K. Sources of supply for device classes H and K are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DESC-EC and have agreed to this drawing.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-94646</b>
		<b>REVISION LEVEL</b>	<b>SHEET 14</b>

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