

M28525/9 Data Sheet

Inverse Multiplexing for ATM (IMA) Family

The M2852x family of devices provides system designers with a complete integrated IMA solution for up to 32 ports. All devices include a Transmission Convergence block to perform cell delineation, 512 K internal RAM to meet ATM forum requirements for differential delay compensation and a dual mode (UTOPIA or Serial) PHY layer interface. Source code for all required software functions is available from Mindspeed. The M28529 supports 32 IMA groups with 1-32 links per group.

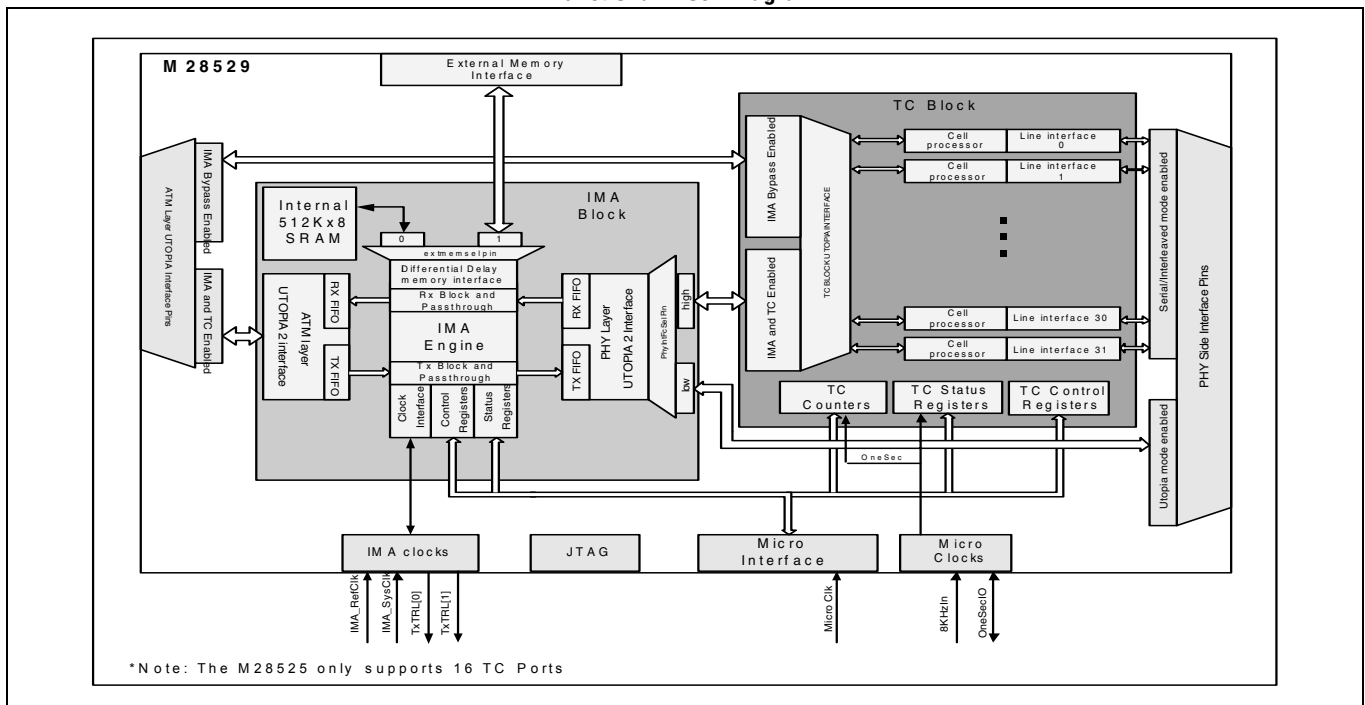
The TC block is capable of bit level cell delineation, which allows for direct connection DSL serial data streams without a frame sync pulse. Individual ports can be operated in a 'pass thru' mode without the IMA overhead.

The M28529 provides direct connection to 32 serial/interleaved highway links or a PHY side UTOPIA bus. In addition, an external memory bus allows the differential delay memory to access up to 2 Mbytes of external RAM. The M28529 supports both version 1.0 and 1.1 of IMA standard AF-PHY-0086.001

Distinguishing Features

- Complete IMA solution in a single package
 - 16 port, M28525
 - 32 port, M28529
- Field tested software available
- Up to 32 IMA groups with 1-32 links/group
- Supports 50 ms (beyond the IMA standard requirements for 25 ms) differential delay with 512K Internal memory
- Memory expandable to 2 M bytes via external bus
- UTOPIA level 2 interfaces
- Glueless serial and interleaved highway interfaces to Mindspeed Framers
- Octet or Bit level cell delineation
- Variable link data rates (64K–8.192 Mb/s)

Functional Block Diagram



Ordering Information

| Model Number | Manufacturing Part Number | Product Revision | Package | Operating Temperature |
|--------------|---------------------------|------------------|---------------------|-----------------------|
| M28525 | M28525-12 | B | 27mm PBGA, 484 pins | -40 °C to 85 °C |
| M28525G* | M28525G-12 | B | 27mm PBGA, 484 pins | -40 °C to 85 °C |
| M28529 | M28529-12 | B | 27mm PBGA, 484 pins | -40 °C to 85 °C |
| M28529G* | M28529G-12 | B | 27mm PBGA, 484 pins | -40 °C to 85 °C |

*The G in the part number indicates that this is an RoHS compliant package. Refer to www.mindspeed.com for additional information.

Revision History

| Revision | Level | Date | Description |
|----------|-------------|----------------|--|
| A | Advance | April 2003 | Advance A version |
| B | Advance | May 2003 | Advance B version |
| C | Advance | July 2003 | Advance C version |
| D | Advance | August 2003 | Advance D version |
| E | Advance | October 2003 | Advance E version |
| F | Preliminary | February 2004 | Preliminary F version |
| G | Preliminary | May 2004 | Preliminary G version |
| H | Released | July 2004 | Released H version |
| I | Released | September 2004 | Released I version. Added note to IMA_FE_TX_LNKn_GRP_ID, IMA_FE_TX_LNKn_CFG and ATM Cell Capture registers to indicate conditions under which these registers will be undefined. |
| J | Released | August 2006 | Changes made to explain limitations in Dual-Clav mode, like, only addresses 0 through 0xF are supported and that multiple M28529 devices cannot share the Utopia bus with an ATM-layer device. |
| K | Released | September 2007 | Clarified configuration of pass-through operation. Corrected minimum parameter for "disable from atmutxclk rise edge." Other misc. corrections. |



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1.0 Functional Description

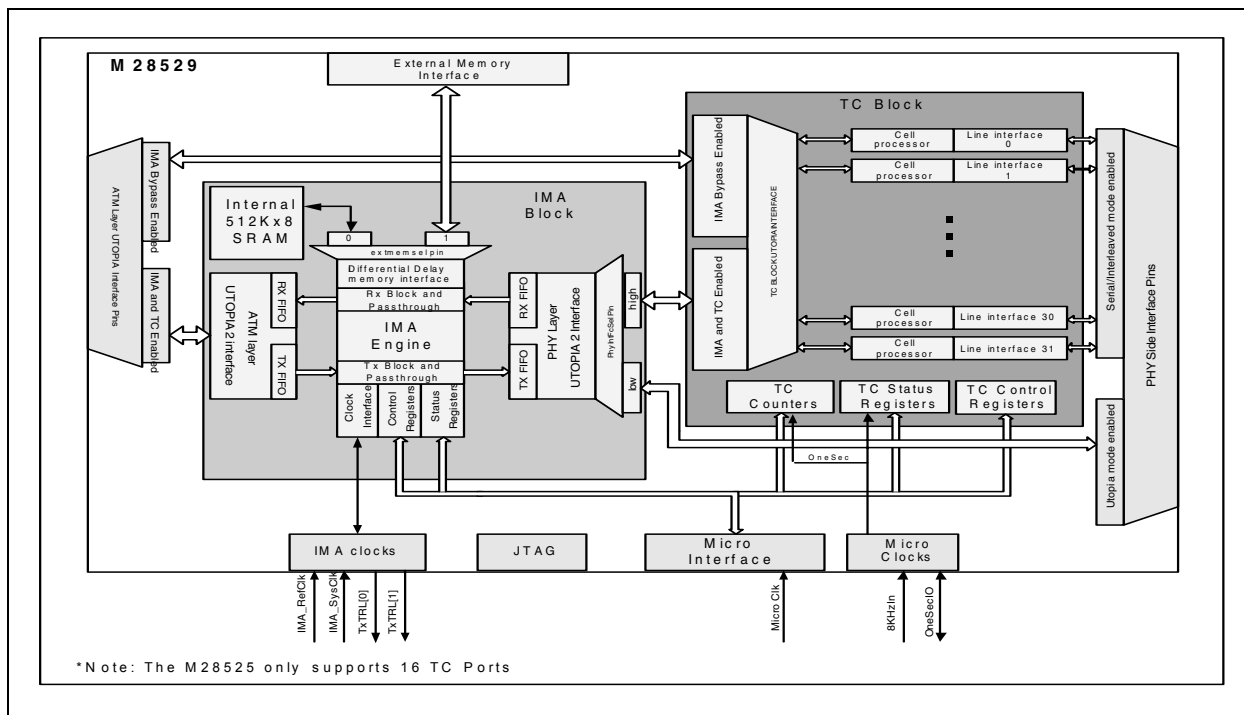
1.1 Overview

1.1.1 Introduction to IMA

This chapter provides a basic introduction to IMA. It will introduce common terminology, the IMA frame format and IMA Cell structure. It will also address one of the challenges of IMA: differential delay between links. For detailed coverage of these topics the reader should refer to the ATM forum's standard for IMA.

The M2852x is composed of the following major functional blocks as shown in [Figure 1-1](#).

Figure 1-1. M28525/9 Block Diagram Example



1.1.2 Introduction To Inverse Multiplexing for ATM

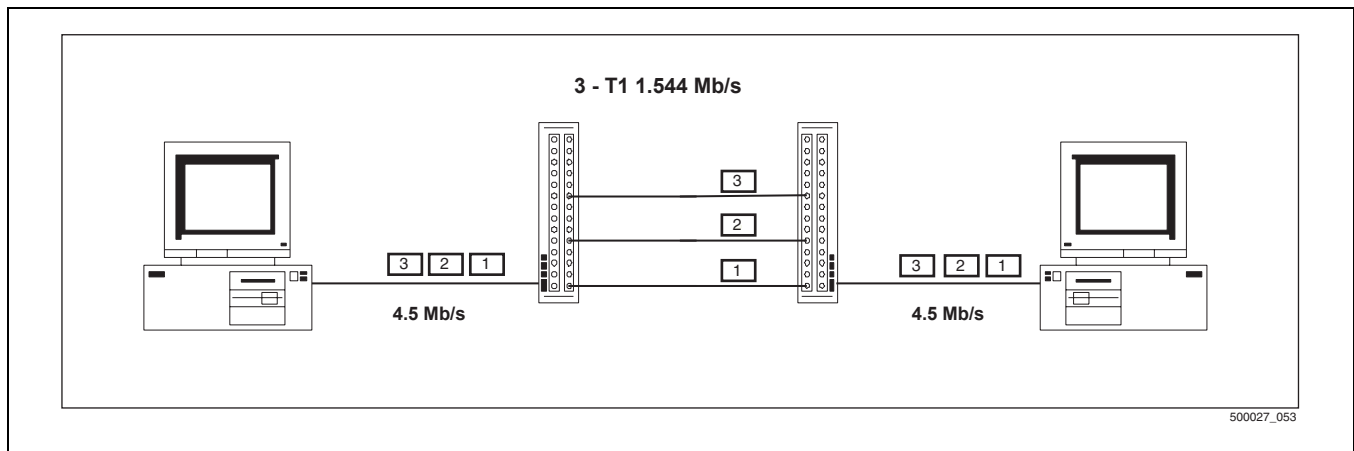
Bandwidth, or the lack thereof, has always been the main challenge of telecommunications. While numerous standards for high speed connections have been around for years, the cost of these higher speed connections often prohibit users from deploying them. For example, users who need a data rate higher than the standard T1, (1.544 Mbps) must pay for an entire DS3 (44 Mbps). Often the extra cost cannot be justified.

IMA solves this problem by allowing users to purchase bandwidth in smaller increments and combine these smaller 'pipes' into one high speed connection. An example is given in Figure 1-2 where 3 T1 lines are combined into one 4.6 Mbps data link.

At first glance, the concept of IMA is deceptively simple: spread the ATM cells out evenly over the available individual lines. However, many serious technical issues must be dealt with and a wide range of functions must be supported. These include IMA framing, differential delay accommodation, link/group state machines, IMA clocking, and maintenance. Several terms must be defined:

| | |
|---------------------|---|
| IMA Engine | The logic that performs the actual IMA function. This sits between the ATM layer and the individual links (see Figure 1-2). An IMA engine can control multiple independent groups. |
| Link | Refers to an individual physical connection such as a T1 or DSL line. Each link has an individual UTOPIA address or serial connection to the IMA engine. |
| Group | An IMA group is composed of links. A group appears as a single UTOPIA address to the ATM layer. Thus an IMA-4 group would have 4 individual links. |
| Group State Machine | The operation of the IMA group is governed by the Group State Machine (GSM), the Group Traffic State Machine (GTSM), and the Link Addition and Slow Recovery (LASR) procedure. These three processes ensure reliable transmission and reception of ATM layer cells across all links in the Active state. This includes the negotiation of group parameters (i.e., symmetry and M values), the bringing up of the IMA group, and the graceful addition/recovery and deletion of links to and from the group. For the M28529, this function is performed in the host software. The software itself is available from Mindspeed. |
| Link State Machine | A Link State Machine (LSM) is defined for the transmit and receive directions of each IMA link. The IMA protocol is defined to allow symmetric or asymmetric cell rate transfer over the IMA virtual link. It allows for smooth introduction of each link in the group. It also allows graceful handling of error conditions and removal of a link. This function is performed internally by the M28529. |

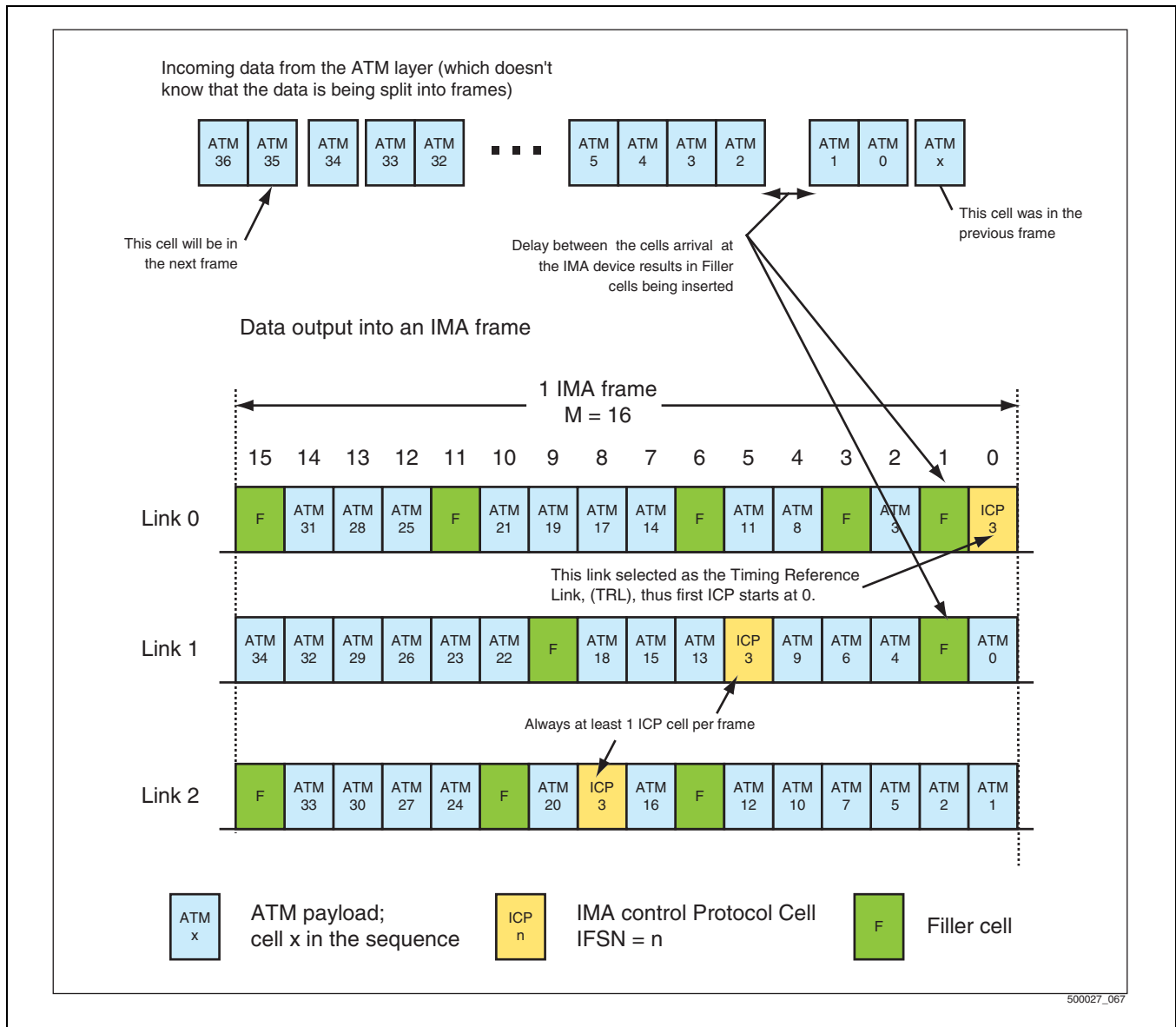
Figure 1-2. IMA Overview



1.1.2.1 IMA Framing

The IMA protocol employs a simple frame structure as shown in Figure 1-3. It consists of a single IMA overhead cell (ICP) and M – 1 ATM layer cells, where M is the IMA frame length. Valid frame lengths are 32, 64, 128 (default), or 256. This example shows a group composed of three links and an IMA frame length of 16. (An invalid frame length of 16 is used for brevity, the default frame length is 128.)

Figure 1-3. IMA Frame; Length = 16; Number of links = 3



Since the ATM layer data rate is often less than the bandwidth available across the links in the IMA group, the IMA engine generates IMA Filler cells when no ATM layer cells are available. (The IMA Filler cells perform the same basic function as Idle cells in a non-IMA ATM system and are discarded by the IMA receiver.)

The IMA frame rate is intentionally set slightly below the available payload bandwidth of the IMA link. To allow for timing differences between the links in a group, the IMA standard requires that the system insert an extra ICP cell every 2049 cells. This cell is called the SICP cell and is inserted immediately after the normal ICP cell for that link and results in the frame being M+1 cells long. Information in the ICP cell payload signals the insertion of these cells so that the receiver does not lose framing and can identify and discard these cells. For further details consult the IMA standard.

One link in each group is designated the Timing Reference Link (TRL). All timing issues for the group are relative to this link.

1.1.2.2 IMA Control Protocol Cells

The IMA Standard defines three types of IMA cells: IMA Control Protocol (ICP) cells, Filler cells, and ATM layer cells. ICP cells are the IMA overhead cells that carry the IMA control and status information between both ends of the link, assuring synchronization and configuration. The purpose of filler cells is rate decoupling; they are inserted into the IMA stream if no ATM layer cells are available.

NOTE: Standard ATM 'idle' cells are never transmitted over an IMA link.

ATM layer cells are the data “payload” carried by the IMA group. These are the standard ATM cells being sent from the ATM layer.

Table 1-1 describes the IMA Overhead Cell definition, and Table 1-2 lists format of the IMA Overhead Stuff Cell.

Table 1-1. IMA Overhead Cell Definition (1 of 3)

| Octet | Field | Description |
|-------|---|--|
| 1-5 | ATM Cell Header | OAM cell type: Octet 1 = 0000 0000 Octet 2 = 0000 0000 Octet 3 = 0000 0000 Octet 4 = 0000 1011 Octet 5 = 0110 0100 (valid HEC with Coset) |
| 6 | IMA Label | OAM type field: 0000 0001—IMA Version 1.0 0000 0011—IMA Version 1.1 |
| 7 | Cell ID Link ID | Bit 7 Set to 1 for ICP cell Bits 6–5 Unused and set to 0 Bits 4–0 Logical ID for physical link range (0... 31) |
| 8 | Frame Sequence Number | Cyclical counter: 0 to 255 |
| 9 | ICP Cell Offset | Indicates position of ICP cell within the IMA frame of size M cells. Range: (0... $M - 1$) |
| 10 | Link Stuff Indication (LSI) | Stuff Indication code for link on which ICP cell is being sent Bits 7–3 Unused and set to 0 Bits 2–0 111: no imminent stuff (default) 100: stuff event in 4 ICP cell locations (optional) 011: stuff event in 3 ICP cell locations (optional) 010: stuff event in 2 ICP cell locations (optional) 001: stuff event at the next ICP cell location (mandatory) 000: This is one out of the 2 ICP cells comprising the stuff event (mandatory) |
| 11 | Status / Control Change Indication (SCCI) | Status and Control Change Indication: 0 to 255 and cycling (count to be incremented every time there is a change to octets 12 to 49). |
| 12 | IMA ID | Logical IMA group ID |

Table 1-1. IMA Overhead Cell Definition (2 of 3)

| Octet | Field | Description |
|-------|-----------------------------|--|
| 13 | Group Status & Control | <p>Bits 7–4 Group Status</p> <ul style="list-style-type: none"> 0000: Start-up 0001: Start-up-Ack 0010: Config-Aborted: Unsupported M 0011: Config-Aborted: Incompatible Symmetry 0100: Config-Aborted: Unsupported IMA version 01xx: Available for other Config Abort reasons 1000: Insufficient-Links 1001: Blocked 1010: Operational <p>Bits 3–2 Others: Reserved</p> <p>Symmetry of Group</p> <ul style="list-style-type: none"> 00: Symmetrical configuration and operation 01: Symmetrical configuration and asymmetric operation 10: Asymmetrical configuration and operation <p>Bits 1–0 11: Reserved</p> <p>IMA Frame Length</p> <ul style="list-style-type: none"> 00: M=32 01: M=64 10: M=128 11: M=256 |
| 14 | Transmit Timing Information | <p>Transmit Clock Information</p> <ul style="list-style-type: none"> Bits 7–6 Unused, set to 00 Bit 5 Transmit Clock Mode (0: ITC mode, 1: CTC mode) Bits 4–0 Tx LID of the timing reference link (TRL)—Range: 0 to 31 |
| 15 | Tx Test Control | <p>Test Pattern Command</p> <ul style="list-style-type: none"> Bits 7–6 Unused, set to 00 Bit 5 Test Link Command (0: inactive, 1: active) Bits 4–0 Tx LID of test link—Range: 0 to 31 |
| 16 | Tx Test Pattern | Value from 0 to 255 |
| 17 | Rx Test Pattern | Value from 0 to 255 |

Table 1-1. IMA Overhead Cell Definition (3 of 3)

| Octet | Field | Description |
|-------|--------------------|--|
| 18 | Link 0 Information | Link State Machine and Defect Information for link with LID = 0 Bits 7–5 Transmit LSM state Bits 4–2 Receive LSM state Bits 1–0 Rx Link defect status 00: no errors 01: Physical Link defect (e.g., LOS, OOF/LOF, LCD) 10: LIF 11: LODS |
| 19–49 | Link 1–31 Info | Status and control of link with LID in the range 1–31 |
| 50 | Unused | Set to 0x6A (as defined in ITU-T I.432) |
| 51 | End-to-end channel | Proprietary channel (set to 0 if unused). The M2852x does not support this octet. |
| 52–53 | CRC Error Control | Bits 15-10 Reserved field for future use—default value is all zeros Bits 9-0 CRC-10 as defined in ITU-T Recommendation I.610 |

Table 1-2. IMA Overhead Filler Cell Format

| Octet | Field | Description |
|-------|--------------------|--|
| 1–5 | ATM Cell Header | OAM cell type: Octet 1 = 0000 0000 Octet 2 = 0000 0000 Octet 3 = 0000 0000 Octet 4 = 0000 1011 Octet 5 = 0110 0100 (valid HEC) |
| 6 | IMA Label | OAM type field: 0000 0001—IMA Version 1.0 0000 0011—IMA Version 1.1 |
| 7 | Cell ID Link ID | Bit 7 Set to 0 for IMA Filler cell Bits 6–0 Unused and set to 0 |
| 8–51 | Unused | Set to 0x6A (as defined in ITU-T I.432) |
| 52–53 | CRC Error Control | Bits 15-10 Reserved field for future use—default value is all zeros Bits 9-0 CRC-10 as defined in ITU-T Recommendation I.610 |

1.1.2.3 Link State Machine

Management of the individual links is performed by two state machines: the Transmit Link State Machine and the Receive Link State Machine. Four possible states are available for each link as shown in [Table 1-3](#).

Table 1-3. Link States

| State | Description |
|--------------|--|
| Not in Group | this link has not been added to an IMA group |
| Unusable | the link is in a group but cannot be used due to line fault etc. |
| Usable | assigned to a group and ready but is waiting for the other end |
| Active | fully configured and carrying traffic |

The Link State Machines are responsible for handling the transition from one state to another. All functions of the LSM's are performed internally by the M2852x. Further details are covered in [Section 1.12](#) and in the ATM standard on IMA.

1.1.2.4 Transmit Clocks

The IMA standard provides two options regarding the transmit clocks. The default mode, and most common IMA application, is Common Transmit Clock (CTC) mode, where all links in the IMA group are generated from the same source. Thus they are in phase and have the same rate of SICP insertion (1/2049) as the designated TRL link.

The Independent Transmit Clock (ITC) mode is available as an optional feature of the IMA protocol (of course, it is fully supported by the M2852x family). In this mode, each link runs off of an independent clock at the nominal line rate. To support these asynchronous links within an IMA group, the rate of SICP insertion is allowed to vary on the non-TRL links.

The IMA group frame rate for each IMA group must be re-created at the receive end. This regeneration is necessary to implement the IMA Data Cell Clock and smoothing buffer functionality of the IMA protocol. One method for generating the Receive IMA group frame rate is to use the line or payload clock recovered from the receive TRL physical port interface. This clock is a frequency locked reference of the far-end Transmit IMA group frame rate. Equivalently, the rate of cell transfers (i.e., payload bandwidth) from the TRL link can be used as the reference for generating the Receive IMA group frame rate. Both methods are available for use by the M2852x device, depending on the application and configuration.

1.1.2.5 Differential Delay

When dealing with multiple facilities, there is no guarantee that the individual links within a group will take the same physical path between the terminating equipment. This variation is referred to as Differential Delay. The ATM Forum specification requires an IMA implementation to absorb a minimum of 25 ms of differential delay between the links. Each link requires 8 K of memory for every 27.5 ms of delay (at E1; 8 K provides for 34.375 ms at T1 rates). The M28525/9 provides 512K bytes of on-board memory for the buffering necessary to re-align the links within an IMA group. This is sufficient to support the 50 ms of delay (at E1 rates) for 32 IMA ports. In addition, an external memory bus allows this to be expanded to 2 MB, which supports up to 200 ms of delay. [Table 1-4](#) shows the memory requirements for differential delay.

Table 1-4. Memory Requirements for Differential Delay (in bytes)

| Number of links | E1 | 27.5 ms | 55 ms | 110 ms | 220 ms |
|-----------------|----|-----------|----------|----------|--------|
| | T1 | 34.375 ms | 68.75 ms | 137.5 ms | 275 ms |
| 1 | | 8 K | 16 K | 32 K | 64 K |
| 2 | | 16 K | 32 K | 64 K | 128 K |
| 4 | | 32 K | 64 K | 128 K | 256 K |
| 8 | | 64 K | 128 K | 256 K | 512 K |
| 16 | | 128 K | 256 K | 512 K | 1024 K |
| 32 | | 256 K | 512 K | 1024 K | 2048 K |

General Note: Shaded areas can be supported by internal memory. Internal memory is disabled when the external bus is used.

The magnitude of the differential delay can be quite large when dealing with T1/E1 links; whereas DSL links generally follow the same path and have nearly identical delays.

1.1.3 Software Overview

NOTE: Mindspeed’s software supports both TC and IMA; however, this section only describes IMA software support.

All IMA devices require a software driver to interface to the system host. Since the GSM’s primary function only occurs during startup; the M2852x family relies on the IMA driver to perform these functions. This allows for maximum flexibility; simpler device design and requires very little overhead from the host.

Mindspeed provides a complete IMA and device driver in ANSI C to simplify system development. This software has been field tested and can be ported to virtually all systems. This is also covered in chapter 3, the IMA engine and the M28529TAP IMA Software Programming Guide.

Table 1-5 summarizes the API of the M28525/9 software. All functions require a pointer to the structure IMA_DEV. The additional parameters for each function are listed in the following sections. The functions named **IMA_xxxx()** are function calls to the M28525/9. The functions named **USER_xxxx()** are user defined functions called by the M28525/9. The pointers to the user defined functions are passed to M28525/9 during initialization as fields in the DRV initialization structure or after initialization using the **IMA_subsys_set()** function.

Table 1-5. Software Function Summary (1 of 2)

| Class | Function | Short Description |
|----------------|---------------------|--|
| Initialization | IMA_init_default () | Initializes the fields of the M28525/9 initialization structure to default values. |
| | IMA_init () | This function initializes the IMA software driver and the IMA device. |
| Interrupts | IMA_tick () | This function polls the error counters and failure monitoring registers of the IMA device and must be called at a regular periodic interval. |
| | IMA_intr () | This function should be called when the device interrupt line has been asserted. |

Table 1-5. Software Function Summary (2 of 2)

| Class | Function | Short Description |
|-----------------|---------------------------|---|
| IMA Subsystem | IMA_read () | This function provides a direct interface to read the registers within the IMA device. |
| | IMA_write () | This function provides a direct interface to write the registers within the IMA device. |
| | IMA_subsys_set () | This function provides a direct interface to set the M28525/9 Subsystem parameters. |
| | IMA_subsys_get () | This function provides a direct interface to retrieve the M28525/9 Subsystem parameters. |
| | IMA_test () | This function executes a specified IMA diagnostic test. |
| | IMA_facility_set() | This function provides a direct interface to set the M28525/9 Facility parameters. |
| | IMA_facility_get() | This function provides a direct interface to retrieve the M28525/9 Facility parameters. |
| Group Interface | IMA_group_set () | This function provides a direct interface to set the M28525/9 Group parameters. |
| | IMA_group_get () | This function provides a direct interface to retrieve the M28525/9 Group parameters. |
| | IMA_group_FM_status () | This function retrieves the current state of the parameters monitored by the Facility Monitoring subsystem for the IMA Group layer. |
| | IMA_group_PM_preset () | This function allows the user to initialize the IMA Group PM statistics to arbitrary values for the current interval of the 15 minute accumulation period. |
| | IMA_group_PM_status () | This function retrieves the states (from either the current or previous 15 minute accumulation interval) of the IMA Group Performance Monitoring parameters. |
| Link Interface | IMA_link_set () | This function provides a direct interface to set the M28525/9 Link parameters. |
| | IMA_link_get () | This function provides a direct interface to retrieve the M28525/9 Link parameters. |
| | IMA_link_FM_status () | This function retrieves the current state of the parameters monitored by the Facility Monitoring subsystem for the IMA Link layer. |
| | IMA_link_PM_preset () | This function allows the user to initialize the IMA Link PM statistics to arbitrary values for the current interval of the 15 minute accumulation period. |
| | IMA_link_PM_status () | This function retrieves the states (from either the current or previous 15 minute accumulation interval) of the IMA Link Performance Monitoring parameters. |
| PHY Interface | IMA_phy_link_set () | This function provides a direct interface to set the M28525/9 Link parameters, per facility. |
| | IMA_phy_link_get () | This function provides a direct interface to retrieve the M28525/9 Link parameters, per facility. |
| | IMA_phy_link_FM_status () | This function retrieves the current state of the parameters monitored by the Failure Monitoring subsystem for the IMA Link layer, per facility. |
| | IMA_phy_link_PM_preset () | This function allows the user to initialize the IMA Group PM statistics to arbitrary values for the current interval of the 15 minute accumulation period. |
| | IMA_phy_link_PM_status () | This function retrieves the states (from either the current or previous 15 minute accumulation interval) of the IMA Link Performance Monitoring parameters, per facility. |
| Monitor | IMA_mon() | This function is called to control the M28525/9 debugger. |
| User Defined | *USER_intr_disable() | This is an application defined function that disables interrupts from the IMA hardware device. |
| | *USER_intr_enable() | This is an application defined function that enables interrupts from the IMA hardware device. |
| | * USER_event () | This is an application defined function that accepts asynchronous event messages from the M28525/9 software. |

1.1.3.1 Software Subsystems

The internal architecture of the M28529TAP software is composed of five logical subsystems: Configuration (CF), Diagnostics (DG), IMA Group (GRP), Failure Monitoring (FM), and Performance Monitoring (PM).

The following sections summarize the interfaces of the M28525/9 IMA software device driver. It is important to point out that the M28525/9 products can be configured to run in different operating environments. As such, not all the interfaces described below are used in a given application.

1.1.3.2 Configuration (CF)

The CF subsystem is responsible for setting the operating parameters of the IMA device that are associated with the IMA Link and IMA Group termination entities. Additionally, some of the application specific configurations of the device are set by this subsystem. The default value for each parameter is used to initialize and set the operating mode of the device.

1.1.3.3 Diagnostics (DG)

The DG subsystem performs control and testing functions on the IMA device and its environment. One role of the DG subsystem is configuration, very similar to the CF subsystem but with different parameters. Similar in function to the Configuration subsystem, the default value for each DG parameter is used to initialize and set the operating mode of the device. The DG subsystem parameters are typically exercised only during test or maintenance conditions, and may affect ATM transmission through the device.

1.1.3.4 Failure Monitoring (FM)

The Failure Monitoring (FM) subroutine is responsible for monitoring the IMA links and groups for defects and anomalies and integrating the defects into failures. The primary role performed by this subsystem is alarm integration. The M28529TAP program is aware of changes in the state of the underlying defects and anomalies through periodic polling. The user has control over which Failure indicators are monitored and the length of both the activation and decay times.

Upon initializing the M28529TAP, the Failure indications required by the ATM MIB are enabled and the activation and decay times are set at 2.5 and 10 seconds, respectively.

1.1.3.5 Performance Monitoring (PM)

This is the set of functions and capabilities necessary for a Network Element (NE) to gather, store, and report performance data associated with its monitored digital transmission entities. In contrast with alarm/status indications, performance parameters are quantitative, not binary, in nature. These performance parameters are gathered over programmable, predetermined accumulation periods. The M28529TAP calculates these statistics over 15 minute intervals. The PM data is available to the application grouped in a structure encompassing one of the two accumulation sets: the current 15 minute interval or the previous 15 minute interval. The PM subsystem uses the raw anomaly and defect information obtained by the FM subsystem to calculate its performance statistics.

Upon initialization, the PM subsystem is basically disabled: none of the monitored statistics are calculated.

1.1.3.6 Group State Machine

Overall management of each Group is the responsibility of the Group State Machine. This actually involves three interrelated processes: the Group State Machine (GSM), the Group Traffic State Machine (GTSM), and the Link Addition and Slow Recovery (LASR) procedure. These three processes are used to ensure reliable transmission and reception of ATM layer cells across all links in the Active state. This includes the negotiation of group parameters (i.e., symmetry and M values), the bringing up of the IMA group, and the graceful addition/recovery and

deletion of links to and from the group. The seven possible states are shown in [Table 1-6](#). Again, this will be covered in more detail in [Chapter 1.12](#) and in the ATM standard on IMA.

Table 1-6. Group State Machine

| State | Description |
|--------------------|--|
| Not Configured | No groups configured |
| Start up | Waiting to establish communications with the other end |
| Start up Ack | Start Up acknowledge; has recognized the far end and waiting to enter the Insufficient links state |
| Config Aborted | Results when the Far End doesn't comply with the requested configuration parameters |
| Insufficient links | Both ends have accepted the group parameters and are waiting for the LSM to provide active links |
| Blocked | The host controller has inhibited the group (probably for maintenance reasons) |
| Operational | Fully operational and able to pass data |

1.2 Features

1.2.1 IMA Features

- Complete IMA solution in a single package
 - 16 port, M28525
 - 32 port, M28529
- Field proven design
- All software available
- Supports variable link data rates (64K–8.192 Mb/s)
- Supports fractional T1/E1 per AF-PHY-0130.00
- 512 K Internal memory
- Supports 50 ms (beyond the IMA standard requirements for 25 ms) differential delay with 512K Internal memory
- Connects directly to the Mindspeed SARs for inexpensive CPE solutions
- M28525 supports 16 facilities
 - Up to 16 independent groups:
Each group can have up to 16 links.
- M28529 supports 32 facilities
 - Up to 32 independent groups:
Each group can have up to 32 links.
- Memory expandable to 2 M bytes via external bus
- Supports IMA versions 1.0 and 1.1

1.2.2 Diagnostics/Loopbacks

- Source Loopback
- Far End Line Loopback
- IMA Line Loopback
- IMA System Loopback
- ICP Cell Access
- IEEE 1149.1 JTAG Interface

1.2.3 Cell Delineation Section

- Supports ATM cell interface for:
 - Circuit-based physical layer
 - Cell-based physical layer
- Performs single-bit HEC correction and single- or multiple-bit detection
- Inserts headers and generates HEC
- Direct connection to external Mindspeed components for:
 - T1/E1
 - xDSL
 - General purpose mode
- Byte-level or bit-level cell delineation

1.2.4 Control and Status

1.2.4.1 Microprocessor Interface

- Asynchronous SRAM-like interface mode
- 8-bit data bus
- Open-drain interrupt output
- Open-drain ready output
- Up to 66 MHz operation
- All control registers are read/write

1.2.4.2 ATM Interface

- ATM-side UTOPIA Interface:
 - 8/16-bit UTOPIA Level 2 Slave
 - Up to 50 MHz operation
 - Support for dual Clav and Enable signals
 - Supports 32 ATM addresses

1.2.4.3 PHY Interfaces

- PHY-side UTOPIA Interface:
 - 8/16-bit UTOPIA Level 2 Master
 - Supports 32 ports via dual CLAV and Enable lines
- Serial Interface
- Interleaved Highway
- Up to 33 MHz operation

1.2.4.4 Counters/Status Register Section

- Summary interrupt indications
- Configuration of interrupt enables
- One-second counter latching
- Counters for:
 - LOCD events
 - Corrected HEC errors
 - Uncorrected HEC errors
 - Transmitted cells
 - Matching received cells
 - Non-matching received cells
 - Idle cell receive

1.3 General Description

The M2852x family of devices provides system designers with a complete integrated IMA solution for up to 32 ports. All devices include a Transmission Convergence block to perform cell delineation, 512 K internal RAM to meet ATM forum requirements for differential delay compensation and a dual mode (UTOPIA or Serial) PHY layer interface. Source code for all required software functions is available from Mindspeed. The M28529 supports 32 IMA groups with 1-32 links per group.

The TC block is capable of bit level cell delineation, which allows for direct connection DSL serial data streams without a frame sync pulse. Individual ports can be operated in a 'pass thru' mode without the IMA overhead.

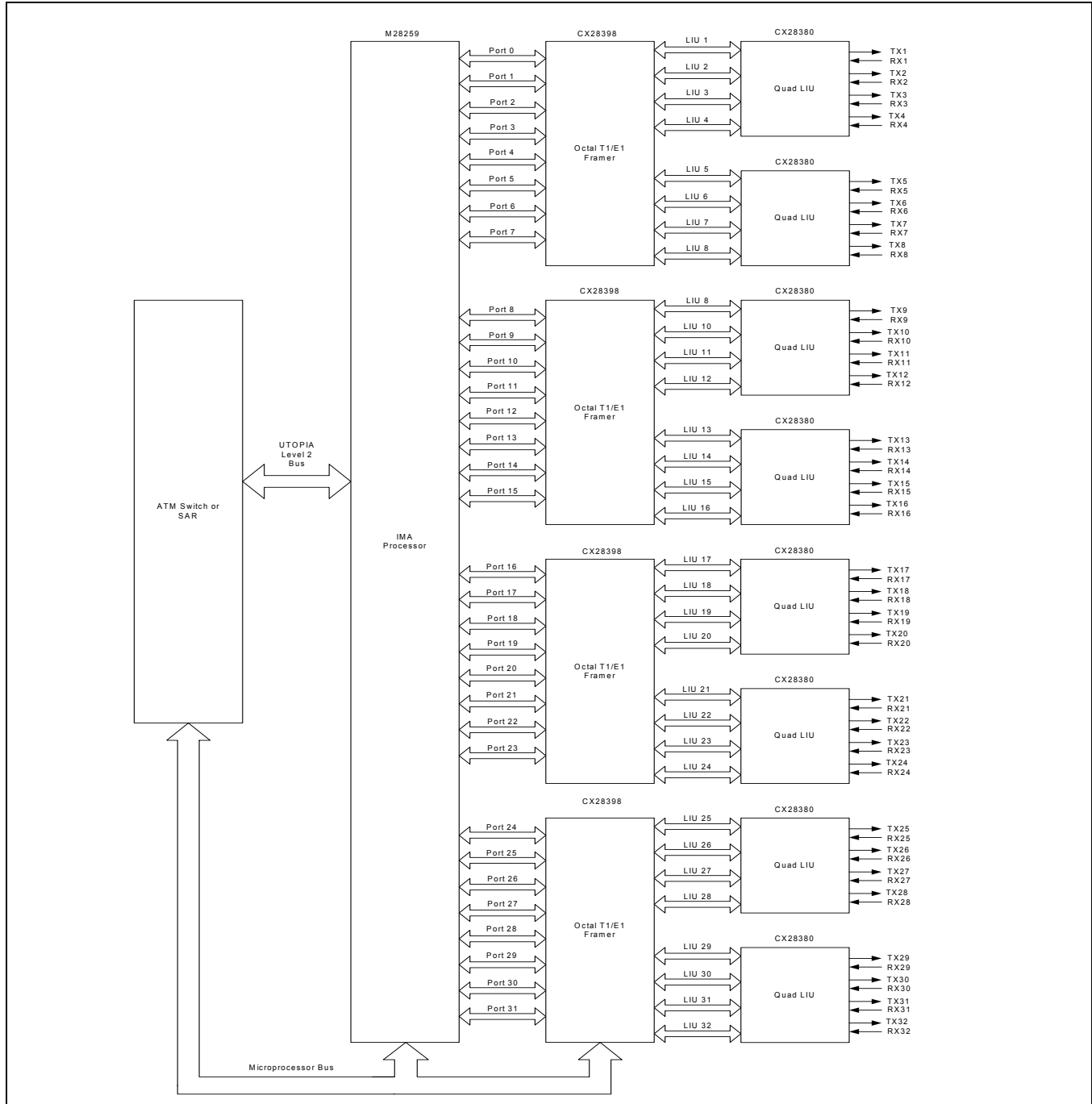
The M28529 provides direct connection to 32 serial/interleaved highway links or a PHY side UTOPIA bus. In addition, an external memory bus allows the differential delay memory to access up to 2 Mbytes of external RAM. The M28529 supports both version 1.0 and 1.1 of IMA standard AF-PHY-0086.001

1.4 Applications

1.4.1 Overview

The M2852x is typically used with line framer devices like the CX28398 T1/E1 octal framer or the M28985 ZipWireMulti™ Octal G.shdsl Transceiver with Embedded Microprocessor. Figure 1-4 illustrates a typical application.

Figure 1-4. M2852x Connected to a CX28398 Transceiver



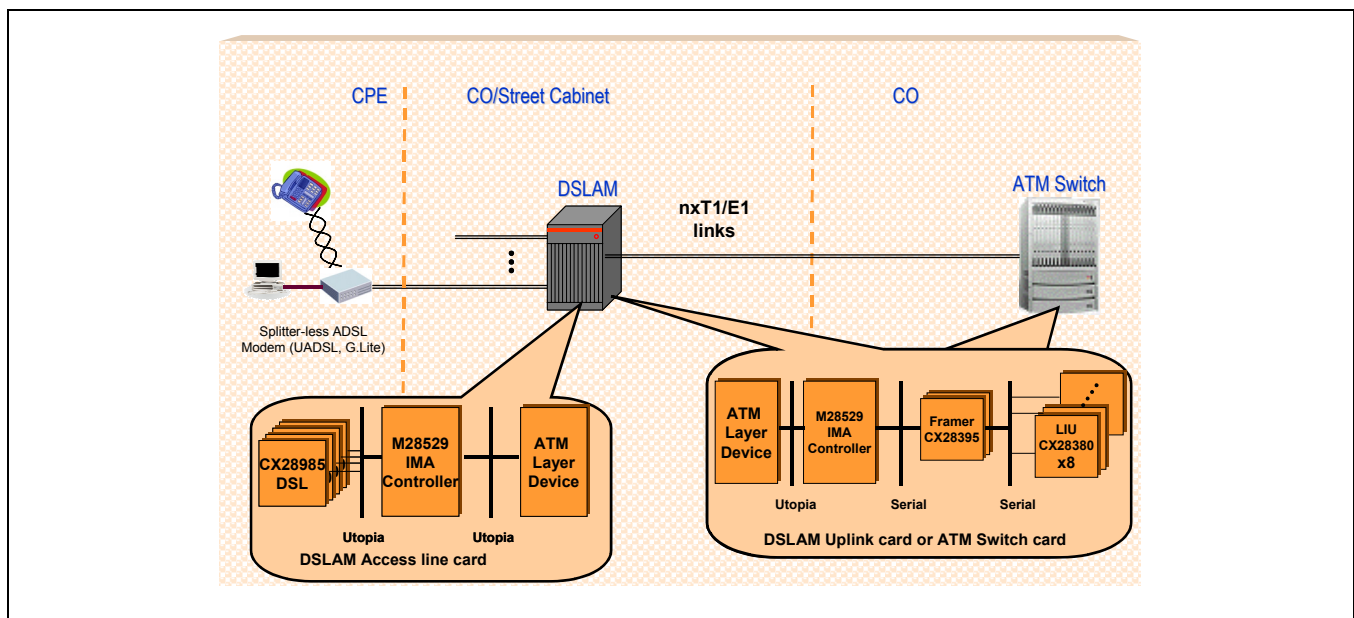
1.4.2 DSLAM

Digital Subscriber Line Access Multiplexers (DSLAM) and Broadband Loop Carriers (BLC) are being deployed to provide broadband services to business and residential customers. Although DSL and T1/E1 services delivers higher speeds than traditional dial-up connections, customers are increasingly finding the need for higher bandwidth than is available through a single DSL or T1/E1 line. The IMA protocol helps bridge the gap between lower cost xDSL solutions and higher cost lines such as T3. IMA allows customers to scale their bandwidth needs in T1/E1 or xDSL link increments, so they do not have to pay for more than they can use.

Figure 1-5 shows a typical example of how IMA can be used to meet the evolving needs of customers. The DSLAM can use the M28529 32-port IMA controller with the octal M28985 DSL modem chip for the customer access side. The CX28225 4-port IMA can be used in the DSL CPE equipment to complete the solution for providing flexible bandwidth scaling.

On the network side, DSLAMs generally need to backhaul customer traffic to the ATM backbone. This can be done by bonding multiple T1s together using IMA. This line card is also shown in Figure 1-4. The M28529 can be used once again with Mindspeed's CX28395 16-port framers and CX28380 quad LIUs. A similar line card is needed at the ATM/Multiservice Switch.

Figure 1-5. M28529 in DSLAM applications

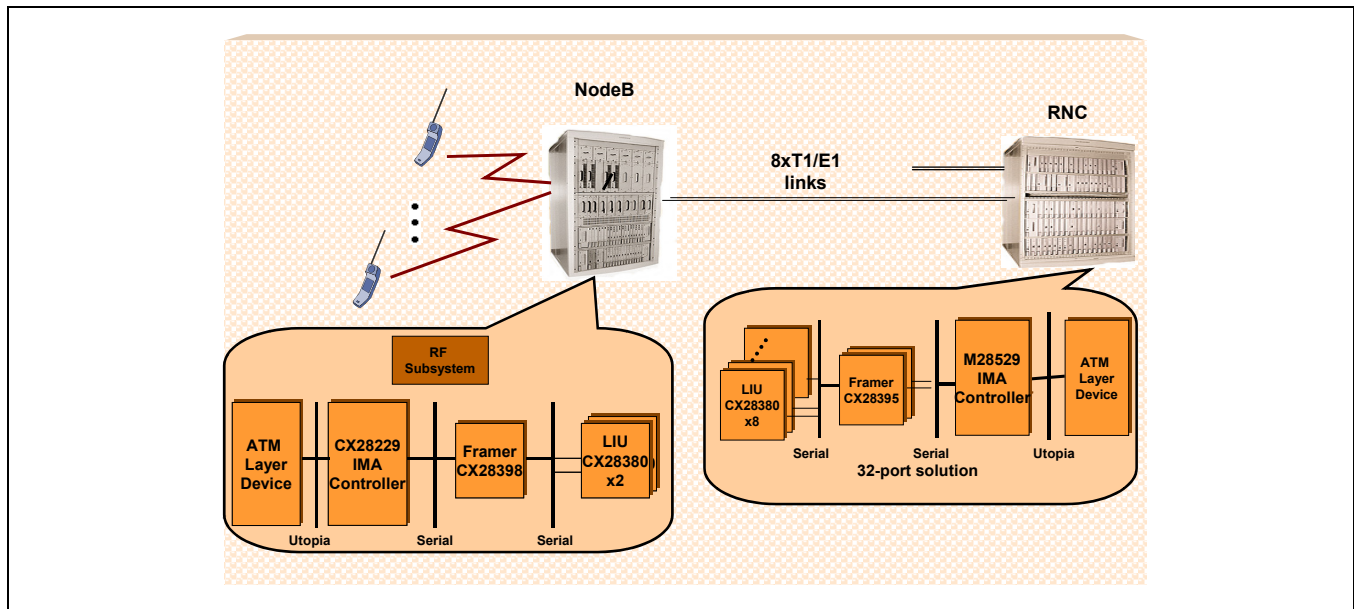


1.4.3 Wireless NodeB/RNC

Wireless Base Transceiver Stations (BTS) and NodeB equipment for 3G based networks have a need to send customer's compressed voice/data from the base station to the Radio Network Controller (RNC). Many times, high speed fiber links are not available where the equipment is deployed. By using IMA to bond multiple T1 or E1 links together, the traffic can be backhauled effectively and efficiently.

Figure 1-6 illustrates the NodeB/RNC example. The NodeB can either use a CX28229 for 8-ports or the M28529 for 16 to 32-port applications. The CX28398 framer and CX28380 complete the line card. The RNC can aggregate traffic from multiple base sites, so the M28529 can be used here. Again, the CX28395 16-port framer and CX8380 quad LIUs can be used to complete the line card solution.

Figure 1-6. M28529 in NodeB/RNC Application



1.5 Pin Definitions

Two versions of Mindspeed's IMA solution are available: M28525 and the M28529. All use the same software drivers and are basically pin compatible. Table 1-7 provides a quick comparison of the two devices.

Table 1-7. Available Parts

| Device | Internal memory | External memory interface | UTOPIA addresses (PHY side) | Serial ports |
|--------|-----------------|---------------------------|-----------------------------|--------------|
| M28525 | 512 Kbytes | 2 Mbyte ⁽¹⁾ | 0-15, 31 (NULL) | 16 |
| M28529 | 512 Kbytes | 2 Mbyte ⁽¹⁾ | 0-31 ⁽²⁾ | 32 |

Footnote:

(1) Internal memory is disabled when the external bus is used.

(2) Normally, 0x1F is the NULL address; however, the M28529 can be configured to treat it as a valid port address.

The following three configurations are available:

- UTOPIA-to-Serial*
- UTOPIA-to-UTOPIA
- UTOPIA-to-Interleaved Highway*

*Note: Interleaved Highway can be mixed with serial mode on a per group of four channel basis. Interleaved Highway mode is enabled by setting the EnIHx (x = 0 to 7) bit in the appropriate TCCTRLx (x = 0 to 7) register.

1.5.1 Pin Diagram and Definitions (UTOPIA-to-Serial Configuration)

Figure 1-7 illustrates a pinout diagram for the M28529 when operating in UTOPIA-to-Serial mode. It is a single CMOS integrated circuit packaged in a 484-pin PBGA. All unused input pins should be connected to ground or power. Unused outputs and bi-directional pins should be left unconnected.

NOTE: UTOPIA-to-Serial configuration is selected by tying the PhyIntFcSel pin high.

Figure 1-8 is a block diagram of an 32 link IMA solution using the device in the UTOPIA-to-serial mode to take advantage of the internal serial ports. Cell Delineation is performed internally and the M2852x interfaces directly to the framers. These framers could be T1/E1 or DSL. Further details can be found in the Mindspeed reference design available online. Configuration information is shown in Table 1-8.

Figure 1-7. M28529 Logic Diagram (UTOPIA-to-Serial)

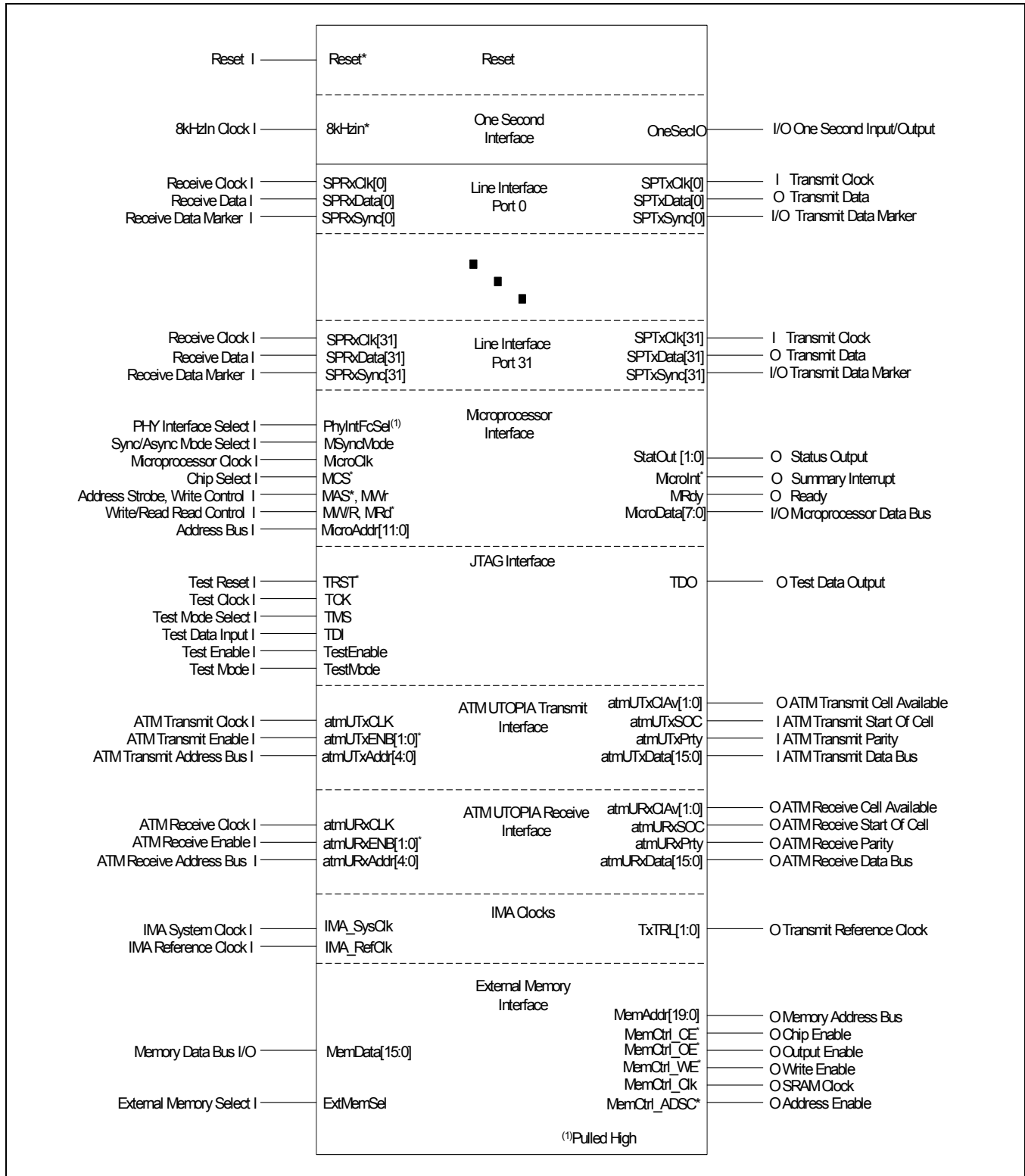


Figure 1-8. M28529 UTOPIA-to-Serial Mode

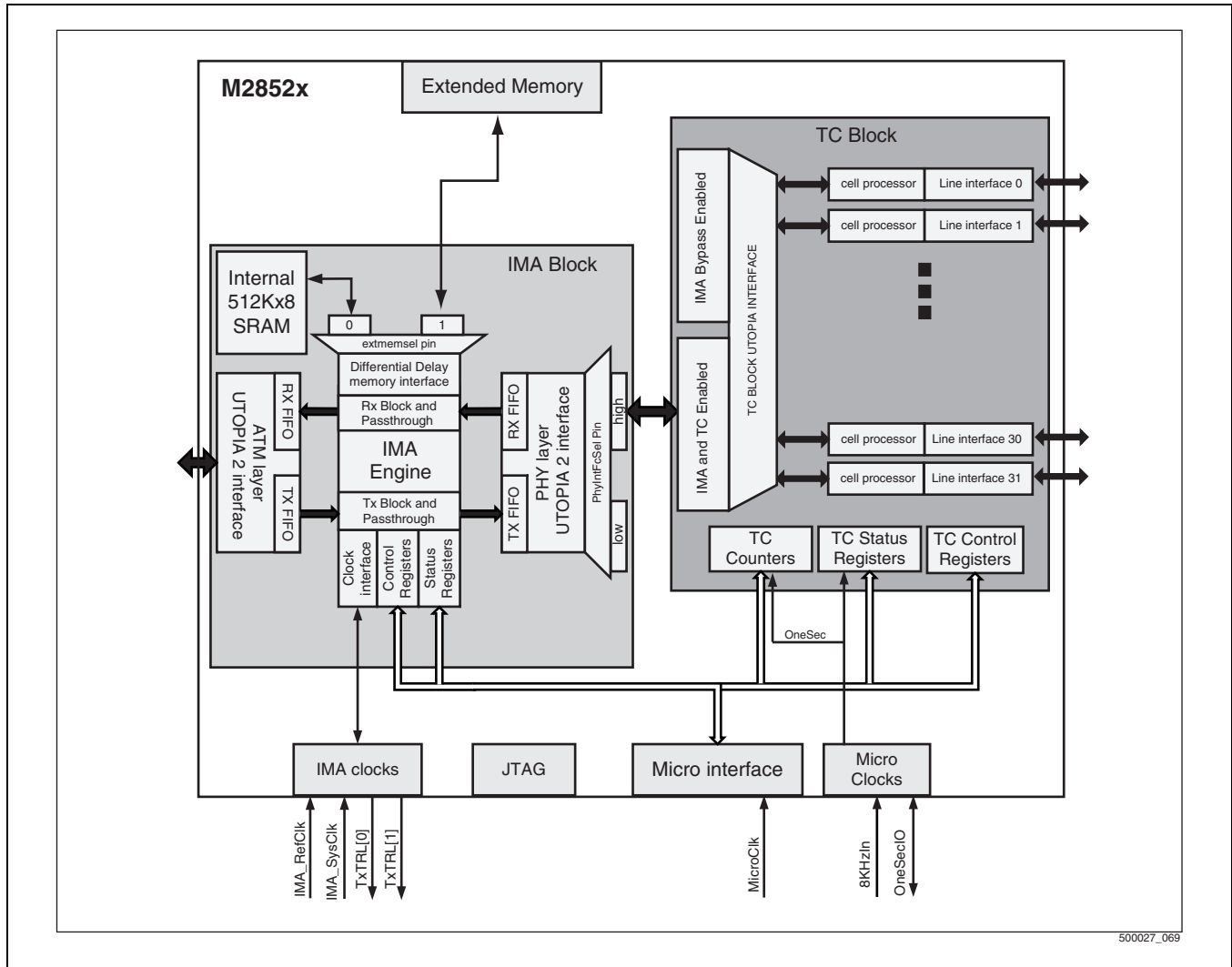


Table 1-8. M28529 UTOPIA-to-Serial Mode

| ATMMux [7,6] (ATMINTFC, 0xF03) | PhyIntFcSel (Pin AD24) | Description |
|--------------------------------|------------------------|---|
| 01 | High | IMA UTOPIA using Internal TC block; UTOPIA-to-Serial mode using 32 internal serial ports. |

General Note: External memory could be used if desired (M28525/9).

Table 1-9. M28529 Pin Descriptions (1 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|-----------------|------------|---|------|------|---|
| Micro Interface | StatOut[0] | Status Output | AB24 | 0 | General purpose output pins under software control. |
| | StatOut[1] | | AD26 | | |
| | MSyncMode | Microprocessor Synchronous/Asynchronous Bus Mode Select | AE24 | I/PD | Selects synchronous or asynchronous bus mode, which determines the functions of two pins, MW/R,MRd* (pin W4) and MAS*,MWr* (pin Y2). A logic 1 selects the synchronous bus mode. In this mode, these pins are defined as follows: MW/R (W4) and MAS* (Y2). A logic 0 selects the asynchronous SRAM-type bus mode. In this mode, the pins are defined as follows: MRd* (W4) and MWr* (Y2). |
| | Reset* | Device Reset | T4 | I/PU | When asserted low, resets the device. The microprocessor clock must be present before reset is released. If configuring the device for pass-through operation, a minimum delay of 25 uS for IMA_Sysclk of 66 MHz or 33us for IMA_Sysclk of 50 MHz is required from the release of reset to the first access of the IMA_RX_TRANS_TABLE register or the IMA_RX_ATM_TRANS_TABLE register (0x818/0x819). |
| | 8kHzIn | 8 kHz Input | AD25 | I | A clock input used to derive OneSecIO. Typically operates at a frequency of 8 kHz. |
| | OneSecIO | One-Second Input/Output | AE26 | I/O | Software can configure this pin as an output that equals the input from the 8kHzIn divided by 8000. When configured as an input, status registers and counters may be latched on the rising edge of this input. See Bit 0 of the Genctrl register (0xF00). |
| | MW/R, MRd* | Microprocessor Write/Read | W4 | I | When MSyncMode is asserted high, this pin is a read/write control pin. In this mode, when MW/R is asserted high, a write access is enabled and the MicroData[7:0] pin values will be written to the memory location indicated by the MicroAddr[11:0] pins. Also, when MW/R is asserted low in this mode, a read access is enabled and the memory location indicated by the MicroAddr[11:0] pins is read. Its value is placed on the MicroData[7:0] pins. Both read and write accesses assume the device is chip selected (MCS* = 0), the address is valid (MAS* = 0), and the device is not being reset (Reset* = 1). When MSyncMode is asserted low, this pin is a read control pin. In this mode, when MRd* is asserted low, a read access is enabled and the memory location indicated by the MicroAddr[11:0] pins is read. Its value is placed on the MicroData[7:0] pins. |
| | MCS* | Microprocessor Chip Select | V1 | I | When asserted low, the device is selected for read and write accesses. When asserted high, the device will not respond to input signal transitions on MicroClk, MW/R, MRd*, or MAS*, MWr*. Additionally, when MCS* is asserted high, the MicroData[7:0] pins are in a high-impedance state but the MicroInt* pin remains operational. |

Table 1-9. M28529 Pin Descriptions (2 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------|----------------------------------|-------------------------------|-----|---|--|
| Micro Interface | MAS*, MWr* | Microprocessor Address Strobe | Y2 | I | When MSyncMode is asserted high, this pin is an address strobe pin. When the MAS* pin is asserted low, it indicates a valid address, MicroAddr[11:0]. This signal is used to qualify read and write accesses. When MSyncMode is asserted low, this pin is a write control pin. When MWr* is asserted low, a write access is enabled and the MicroData[7:0] pin values will be written to the memory location indicated by the MicroAddr[11:0] pins. The write access assumes the device is chip selected (MCS* = 0), a read access is not being requested (MRd* = 1), and the device is not being reset (Reset* = 1). |
| | MicroAddr[0] | Microprocessor Address Bus | U2 | I | These 12 bits are an address input for identifying the register to access. |
| | MicroAddr[1] | | T3 | | |
| | MicroAddr[2] | | U1 | | |
| | MicroAddr[3] | | T2 | | |
| | MicroAddr[4] | | R4 | | |
| | MicroAddr[5] | | T1 | | |
| | MicroAddr[6] | | R3 | | |
| | MicroAddr[7] | | R2 | | |
| | MicroAddr[8] | | P4 | | |
| | MicroAddr[9] | | R1 | | |
| | MicroAddr[10] | | P3 | | |
| | MicroAddr[11] | | P2 | | |
| | MicroData[0] | Microprocessor Data Bus | W3 | I/O | A bi-directional data bus for reading and writing data to internal registers. |
| | MicroData[1] | | V4 | | |
| | MicroData[2] | | Y1 | | |
| | MicroData[3] | | W2 | | |
| | MicroData[4] | | V3 | | |
| | MicroData[5] | | U4 | | |
| | MicroData[6] | | W1 | | |
| MicroData[7] | V2 | | | | |
| MicroInt* | Microprocessor Interrupt Request | AA1 | 0 | When active low, the device needs servicing. It remains active until the pending interrupt is processed by the Interrupt Service Routine. This pin is an open drain output for an OR logic implementation. An external pull-up resistor is required for this pin. | |

Table 1-9. M28529 Pin Descriptions (3 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------|-------------|------------------------------------|------|--------|--|
| Micro Interface | MRdy | Microprocessor Ready | Y3 | 0 | When active high, the current read or write transaction has been completed. For a read transaction, the data is ready to be transferred to the microprocessor. For a write transaction, the data provided by the microprocessor has been written. This pin is an open drain output for an external wired OR logic implementation. An external pull-up resistor is required for this pin. |
| | MicroClk | Microprocessor Clock | R5 | I | In asynchronous mode the microprocessor clock signal input can be clocked up to 66 MHz. In synchronous mode this pin can be clocked up to 25 MHz. The device samples the microprocessor interface pins (MCS*, MW/R, MAS*, MicroAddr[11:0], and Microdata[7:0]) on the rising edge of this signal. The microprocessor interface output pins (Microdata[7:0], MicroInt*) are clocked on the rising edge of MicroClk. Note that this clock is required for both synchronous and asynchronous operations. See note in Section 1.15.1 . |
| External Memory | ExtMemSel | External Memory Enable | AC26 | I/PD | When this pin is pulled high, it enables the external differential delay SRAM bus. |
| | MemData[0] | Differential Delay Memory Data Bus | M26 | I/O/PD | Differential delay SRAM Data Bus. ATM cells extracted from the Receive data stream are stored in the SRAM for the purpose of differential delay compensation. This bus is enabled by pulling the ExtMemSel pin high. |
| | MemData[1] | | N24 | | |
| | MemData[2] | | N25 | | |
| | MemData[3] | | N26 | | |
| | MemData[4] | | P26 | | |
| | MemData[5] | | P25 | | |
| | MemData[6] | | P24 | | |
| | MemData[7] | | P23 | | |
| | MemData[8] | | R26 | | |
| | MemData[9] | | P22 | | |
| | MemData[10] | | R24 | | |
| | MemData[11] | | T26 | | |
| | MemData[12] | | R23 | | |
| | MemData[13] | | T25 | | |
| | MemData[14] | | T24 | | |
| | MemData[15] | | U26 | | |

Table 1-9. M28529 Pin Descriptions (4 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------|---------------|---------------------------------------|------|-----|---|
| External Memory | MemAddr[0] | Differential Delay Memory Address Bus | U25 | 0 | Receive SRAM Address Bus This signal is enabled by pulling the ExtMemSel pin high. |
| | MemAddr[1] | | T23 | | |
| | MemAddr[2] | | V26 | | |
| | MemAddr[3] | | U24 | | |
| | MemAddr[4] | | V25 | | |
| | MemAddr[5] | | W26 | | |
| | MemAddr[6] | | U23 | | |
| | MemAddr[7] | | V24 | | |
| | MemAddr[8] | | W25 | | |
| | MemAddr[9] | | Y26 | | |
| | MemAddr[10] | | V23 | | |
| | MemAddr[11] | | W24 | | |
| | MemAddr[12] | | Y25 | | |
| | MemAddr[13] | | AA26 | | |
| | MemAddr[14] | | W23 | | |
| | MemAddr[15] | | Y24 | | |
| | MemAddr[16] | | AA25 | | |
| | MemAddr[17] | | Y23 | | |
| | MemAddr[18] | | AB26 | | |
| | MemAddr[19] | | AA24 | | |
| | MemCtrl_CE* | Chip Enable | N23 | 0 | Receive SRAM Device Select (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high. |
| | MemCtrl_OE* | Output Enable | M25 | 0 | Receive SRAM Device Output (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high. |
| | MemCtrl_WE* | Write Enable | M24 | 0 | Receive SRAM write enable (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high. |
| External Memory | MemCtrl_CLK | SRAM Clock | AB25 | 0 | Receive SRAM clock signal. This signal is enabled by pulling the ExtMemSel pin high. |
| | MemCtrl_ADSC* | Address Enable | L26 | 0 | Receive SRAM address enable (active low) address strobe. This signal is enabled by pulling the ExtMemSel pin high. |

Table 1-9. M28529 Pin Descriptions (5 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|--------------------|---------------|--------------------------|------|------|--|
| JTAG | TRST* | Test Reset | C5 | I/PU | When asserted, the internal boundary-scan logic is reset. This pin has a pull-up resistor. |
| | TCK | Test Clock | A2 | I/PU | Samples the value of TMS and TDI on its rising edge to control the boundary scan operations. |
| | TMS | Test Mode Select | D5 | I/PU | Controls the boundary-scan Test Access Port (TAP) controller operation. This pin has a pull-up resistor. |
| | TDI | Test Data Input | C4 | I/PU | The serial test data input. This pin has a pull-up resistor. |
| | TDO | Test Data Output | C3 | O | The serial test data output. |
| Factory Test | TestEnable[0] | | AF26 | I/PD | Factory test use only, tie to VSS. |
| | TestEnable[1] | | AC22 | | |
| | ScanEnable | | AD23 | I/PD | Factory test use only, tie to VSS. |
| | Tristate | Tristate | AE25 | I/PD | When this pin is high, all outputs are tristate. |
| PHY Side Interface | PhyIntFcSel | PHY Interface Select | AD24 | I/PU | If this pin is tied low, the PHY UTOPIA Interface mode is selected. If this pin is tied high, the PHY Serial mode is selected (as shown in this table). |
| IMA Clocks | IMA_SysClk | IMA Subsystem Clock | E18 | I/PU | Most of the IMA logic circuits use this clock (or a derivative of it). It can also be used as a T1/E1 reference clock. Refer to Section 1.12 . |
| | IMA_RefClk | IMA Subsystem Clock | E16 | I/PU | If Ref_Xclk is to be used as a reference clock, set the frequency as shown in Section 1.12 . |
| | TxTRL[0] | Transmit Reference Clock | A19 | O | Transmit Reference Clocks. |
| | TxTRL[1] | | B19 | | |

Table 1-9. M28529 Pin Descriptions (6 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------------|--------------|------------------|------|------|--|
| Serial Line Interface | SPRxSync[0] | Frame Sync Input | B17 | I/PD | When the PHY serial interface is enabled, this is the frame sync input. Note that ports 16-31 are no connects in the M28525. ⁽¹⁾ |
| | SPRxSync[1] | | A17 | | |
| | SPRxSync[2] | | C16 | | |
| | SPRxSync[3] | | B16 | | |
| | SPRxSync[4] | | C11 | | |
| | SPRxSync[5] | | B10 | | |
| | SPRxSync[6] | | D11 | | |
| | SPRxSync[7] | | A9 | | |
| | SPRxSync[8] | | B4 | | |
| | SPRxSync[9] | | D6 | | |
| | SPRxSync[10] | | A3 | | |
| | SPRxSync[11] | | D3 | | |
| | SPRxSync[12] | | H1 | | |
| | SPRxSync[13] | | K4 | | |
| | SPRxSync[14] | | J3 | | |
| | SPRxSync[15] | | J2 | | |
| | SPRxSync[16] | | Y4 | | |
| | SPRxSync[17] | | AA3 | | |
| | SPRxSync[18] | | AD1 | | |
| | SPRxSync[19] | | AC2 | | |
| | SPRxSync[20] | | AE6 | | |
| | SPRxSync[21] | | AD7 | | |
| | SPRxSync[22] | | AC8 | | |
| | SPRxSync[23] | | AF6 | | |
| | SPRxSync[24] | | AF12 | | |
| | SPRxSync[25] | | AC13 | | |
| | SPRxSync[26] | | AD13 | | |
| | SPRxSync[27] | | AE13 | | |
| | SPRxSync[28] | | AD18 | | |
| | SPRxSync[29] | | AE19 | | |
| | SPRxSync[30] | | AF20 | | |
| | SPRxSync[31] | | AD19 | | |

Table 1-9. M28529 Pin Descriptions (7 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------------|-------------|--------------------------|------|------|--|
| Serial Line Interface | SPRxCiK[0] | Receive Line Clock Input | B18 | I/PD | When the PHY serial interface is enabled, this is the receive line clock input. Note that ports 16–31 are no-connects in the M28525. ⁽¹⁾ |
| | SPRxCiK[1] | | C17 | | |
| | SPRxCiK[2] | | A18 | | |
| | SPRxCiK[3] | | D16 | | |
| | SPRxCiK[4] | | A11 | | |
| | SPRxCiK[5] | | D12 | | |
| | SPRxCiK[6] | | B11 | | |
| | SPRxCiK[7] | | A10 | | |
| | SPRxCiK[8] | | B5 | | |
| | SPRxCiK[9] | | D7 | | |
| | SPRxCiK[10] | | C6 | | |
| | SPRxCiK[11] | | B3 | | |
| | SPRxCiK[12] | | G1 | | |
| | SPRxCiK[13] | | J4 | | |
| | SPRxCiK[14] | | H3 | | |
| | SPRxCiK[15] | | H2 | | |
| | SPRxCiK[16] | | AA2 | | |
| | SPRxCiK[17] | | AB1 | | |
| | SPRxCiK[18] | | AC1 | | |
| | SPRxCiK[19] | | AB2 | | |
| | SPRxCiK[20] | | AE5 | | |
| | SPRxCiK[21] | | AD6 | | |
| | SPRxCiK[22] | | AC7 | | |
| | SPRxCiK[23] | | AF5 | | |
| | SPRxCiK[24] | | AC12 | | |
| | SPRxCiK[25] | | AF11 | | |
| | SPRxCiK[26] | | AD12 | | |
| | SPRxCiK[27] | | AE12 | | |
| | SPRxCiK[28] | | AD17 | | |
| | SPRxCiK[29] | | AE18 | | |
| | SPRxCiK[30] | | AF18 | | |
| | SPRxCiK[31] | | AF19 | | |

Table 1-9. M28529 Pin Descriptions (8 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------------|--------------|-------------------------|------|------|---|
| Serial Line Interface | SPRxData[0] | Receive Line Data Input | D15 | I/PD | When the PHY serial interface is enabled, this is the receive line data input. Note that ports 16–31 are no-connects in the M28525. ⁽¹⁾ |
| | SPRxData[1] | | A16 | | |
| | SPRxData[2] | | C15 | | |
| | SPRxData[3] | | B15 | | |
| | SPRxData[4] | | C10 | | |
| | SPRxData[5] | | B9 | | |
| | SPRxData[6] | | A8 | | |
| | SPRxData[7] | | D10 | | |
| | SPRxData[8] | | C2 | | |
| | SPRxData[9] | | E4 | | |
| | SPRxData[10] | | C1 | | |
| | SPRxData[11] | | D2 | | |
| | SPRxData[12] | | J1 | | |
| | SPRxData[13] | | K3 | | |
| | SPRxData[14] | | L4 | | |
| | SPRxData[15] | | K2 | | |
| | SPRxData[16] | | AA4 | | |
| | SPRxData[17] | | AB3 | | |
| | SPRxData[18] | | AE1 | | |
| | SPRxData[19] | | AD2 | | |
| | SPRxData[20] | | AE7 | | |
| | SPRxData[21] | | AD8 | | |
| | SPRxData[22] | | AC9 | | |
| | SPRxData[23] | | AF7 | | |
| | SPRxData[24] | | AF13 | | |
| | SPRxData[25] | | AF14 | | |
| | SPRxData[26] | | AC14 | | |
| | SPRxData[27] | | AD14 | | |
| | SPRxData[28] | | AC18 | | |
| | SPRxData[29] | | AE20 | | |
| | SPRxData[30] | | AF21 | | |
| | SPRxData[31] | | AD20 | | |

Table 1-9. M28529 Pin Descriptions (9 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------------|--------------|--------------------------|------|-----|--|
| Serial Line Interface | SPTxSync[0] | Frame Sync Input/ Output | A14 | I/O | When the PHY serial interface is enabled, this is the frame sync. SPTxSync is input only for all port modes except DSL mode. In DSL Mode, SPTxSync is output only. Note that ports 16–31 are no-connects in the M28525. ⁽¹⁾ Caution: Some of the SPTxSync pins become outputs when the device is configured for UTOPIA-UTOPIA mode. The designer is cautioned to ensure that PhyIntFcSel never gets configured low. |
| | SPTxSync[1] | | A13 | | |
| | SPTxSync[2] | | B13 | | |
| | SPTxSync[3] | | C13 | | |
| | SPTxSync[4] | | C8 | | |
| | SPTxSync[5] | | B7 | | |
| | SPTxSync[6] | | A6 | | |
| | SPTxSync[7] | | C7 | | |
| | SPTxSync[8] | | G4 | | |
| | SPTxSync[9] | | F3 | | |
| | SPTxSync[10] | | E1 | | |
| | SPTxSync[11] | | F2 | | |
| | SPTxSync[12] | | L1 | | |
| | SPTxSync[13] | | M3 | | |
| | SPTxSync[14] | | N5 | | |
| | SPTxSync[15] | | M1 | | |
| | SPTxSync[16] | | AC4 | | |
| | SPTxSync[17] | | AD4 | | |
| | SPTxSync[18] | | AF2 | | |
| | SPTxSync[19] | | AF3 | | |
| | SPTxSync[20] | | AE9 | | |
| | SPTxSync[21] | | AD10 | | |
| | SPTxSync[22] | | AF9 | | |
| | SPTxSync[23] | | AC11 | | |
| | SPTxSync[24] | | AD15 | | |
| | SPTxSync[25] | | AF16 | | |
| | SPTxSync[26] | | AE16 | | |
| | SPTxSync[27] | | AC16 | | |
| | SPTxSync[28] | | AE22 | | |
| | SPTxSync[29] | | AC20 | | |
| | SPTxSync[30] | | AD21 | | |
| | SPTxSync[31] | | AF24 | | |

Table 1-9. M28529 Pin Descriptions (10 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------------|--------------|---------------------------|------|-----|---|
| Serial Line Interface | SPTxData[0] | Transmit Line Data Output | D13 | 0 | When the PHY serial interface is enabled, this is the transmit line data output. Note that ports 16–31 are no-connects in the M28525. ⁽¹⁾ |
| | SPTxData[1] | | A12 | | |
| | SPTxData[2] | | E13 | | |
| | SPTxData[3] | | C12 | | |
| | SPTxData[4] | | D8 | | |
| | SPTxData[5] | | B6 | | |
| | SPTxData[6] | | A5 | | |
| | SPTxData[7] | | A4 | | |
| | SPTxData[8] | | H4 | | |
| | SPTxData[9] | | G3 | | |
| | SPTxData[10] | | F1 | | |
| | SPTxData[11] | | G2 | | |
| | SPTxData[12] | | N4 | | |
| | SPTxData[13] | | N3 | | |
| | SPTxData[14] | | N1 | | |
| | SPTxData[15] | | P1 | | |
| | SPTxData[16] | | AD5 | | |
| | SPTxData[17] | | AC6 | | |
| | SPTxData[18] | | AE4 | | |
| | SPTxData[19] | | AF4 | | |
| | SPTxData[20] | | AE10 | | |
| | SPTxData[21] | | AF10 | | |
| | SPTxData[22] | | AD11 | | |
| | SPTxData[23] | | AE11 | | |
| | SPTxData[24] | | AD16 | | |
| | SPTxData[25] | | AE17 | | |
| | SPTxData[26] | | AF17 | | |
| | SPTxData[27] | | AC17 | | |
| | SPTxData[28] | | AE23 | | |
| | SPTxData[29] | | AC21 | | |
| | SPTxData[30] | | AD22 | | |
| | SPTxData[31] | | AF25 | | |

Table 1-9. M28529 Pin Descriptions (11 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------------|-------------|---------------------------|------|------|---|
| Serial Line Interface | SPTxCIk[0] | Transmit Line Clock Input | A15 | I/PD | When the PHY serial interface is enabled, this is the transmit line clock input. Note that ports 16–31 are no-connects in the M28525. ⁽¹⁾ |
| | SPTxCIk[1] | | D14 | | |
| | SPTxCIk[2] | | C14 | | |
| | SPTxCIk[3] | | B14 | | |
| | SPTxCIk[4] | | C9 | | |
| | SPTxCIk[5] | | B8 | | |
| | SPTxCIk[6] | | A7 | | |
| | SPTxCIk[7] | | D9 | | |
| | SPTxCIk[8] | | F4 | | |
| | SPTxCIk[9] | | E3 | | |
| | SPTxCIk[10] | | D1 | | |
| | SPTxCIk[11] | | E2 | | |
| | SPTxCIk[12] | | K1 | | |
| | SPTxCIk[13] | | L3 | | |
| | SPTxCIk[14] | | L2 | | |
| | SPTxCIk[15] | | M4 | | |
| | SPTxCIk[16] | | AC3 | | |
| | SPTxCIk[17] | | AB4 | | |
| | SPTxCIk[18] | | AF1 | | |
| | SPTxCIk[19] | | AE2 | | |
| | SPTxCIk[20] | | AE8 | | |
| | SPTxCIk[21] | | AD9 | | |
| | SPTxCIk[22] | | AC10 | | |
| | SPTxCIk[23] | | AF8 | | |
| | SPTxCIk[24] | | AF15 | | |
| | SPTxCIk[25] | | AE14 | | |
| | SPTxCIk[26] | | AC15 | | |
| | SPTxCIk[27] | | AB14 | | |
| | SPTxCIk[28] | | AC19 | | |
| | SPTxCIk[29] | | AE21 | | |
| | SPTxCIk[30] | | AF22 | | |
| | SPTxCIk[31] | | AF23 | | |

Table 1-9. M28529 Pin Descriptions (12 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|-----------------------------------|----------------------------|-----------------------------|------|---|--|
| ATM Layer UTOPIA Interface | atmUTxAddr[0] | ATM UTOPIA Transmit Address | L23 | I | Transmit ATM Cell Bus address. |
| | atmUTxAddr[1] | | K25 | | |
| | atmUTxAddr[2] | | L24 | | |
| | atmUTxAddr[3] | | K26 | | |
| | atmUTxAddr[4] | | L25 | | |
| | atmUTxData[0] | ATM UTOPIA Transmit Data | E26 | I | Transmit direction ATM side cell data. |
| | atmUTxData[1] | | F25 | I | |
| | atmUTxData[2] | | H23 | I | |
| | atmUTxData[3] | | G24 | I | |
| | atmUTxData[4] | | F26 | I | |
| | atmUTxData[5] | | G25 | I | |
| | atmUTxData[6] | | H24 | I | |
| | atmUTxData[7] | | J23 | I | |
| | atmUTxData[8] | | G26 | I/PD | |
| | atmUTxData[9] | | H25 | I/PD | |
| | atmUTxData[10] | | J24 | I/PD | |
| | atmUTxData[11] | | K23 | I/PD | |
| | atmUTxData[12] | | H26 | I/PD | |
| | atmUTxData[13] | | J25 | I/PD | |
| | atmUTxData[14] | | K24 | I/PD | |
| atmUTxData[15] | J26 | | I/PD | | |
| atmUTxPrty | ATM UTOPIA Transmit Parity | D26 | I | Parity status signal. In 8 bit UTOPIA mode, a parity calculation is performed over atmUTxData[7:0] for each clock cycle of atmUTxCk. Odd parity is used. In 16 bit UTOPIA mode, this signal is the parity of atmUTxData[15:0]. This signal is optional. | |

Table 1-9. M28529 Pin Descriptions (13 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|----------------------------|---------------|------------------------------------|-----|------|---|
| ATM Layer UTOPIA Interface | atmUTxClAv[0] | ATM UTOPIA Transmit Cell Available | G23 | O/TS | Cell Available signals for transmit ATM cells (active high). When atmUTxClAv[1] or atmUTxClAv[0] is active one or more complete cells can be transferred from the ATM layer. Only atmUTxClAv[0] is used (atmUTxClAv[1] is ignored) when the DualClavEnb (bit 4) is low (default) in the ATMINTFC register 0xF03. This is the most common configuration. |
| | atmUTxClAv[1] | | E25 | | |
| | atmUTxSOC | ATM UTOPIA Transmit Start of Cell | F24 | I | Start of Cell synchronization signal for transmit ATM cells (active high). Indicates that the first byte/word of the 53 byte cell is being placed on the atmUTxData bus. |
| | atmUTxEnb[0]* | ATM UTOPIA Transmit Enable | D25 | I/PU | Data transfer enable(s) for transmit ATM cells (active low). Indicates that the first byte/word of the 53 byte cell is being placed on the atmUTxData bus. Only atmUTxEnb[0] is used (atmUTxEnb[1] will be ignored) when the DualClavEnb (bit 4) is low (default) in the ATMINTFC register 0xF03. This is most common configuration. When using single clav mode (DualClavEnb bit is set to 0), atmUTxEnb[1] must be pulled up. |
| | atmUTxEnb[1]* | | C26 | | |
| | atmUTxCIk | ATM UTOPIA Transmit Clock | M23 | I | Clock signal used for transfer of transmit ATM cells from the ATM Layer. The maximum clock rate is 50 MHz (Note: 33 MHz in TC Only mode). |
| | atmURxSOC | ATM UTOPIA Receive Start of Cell | C19 | O/TS | Start of Cell synchronization signal for receive ATM cells (active high). Indicates that the first byte/word of the 53 byte cell is being placed on the atmURxData bus. |
| | atmURxCIk | ATM UTOPIA Receive Clock | F23 | I | Clock signal used for transfer of receive ATM cells from the ATM Layer. The maximum clock rate is 50 MHz. (Note: 33 MHz in TC Only mode). |
| | atmURxClav[0] | ATM UTOPIA Receive Cell Available | B20 | O/TS | Cell Available signals for receive ATM cells (active high). When atmURxClav[1] or atmURxClav[0] is active, one or more complete cells can be transferred to the ATM Layer. Only atmURxClav[0] is used (atmURxClav[1] is ignored) when the DualClavEnb (bit 4) is low (default) in the ATMINTFC register 0xF03. This is the most common configuration. |
| | atmURxClav[1] | | A21 | | |
| | atmURxEnb[0]* | ATM UTOPIA Receive Enable | A20 | I/PU | Enable Data transfer and output enable for receive ATM cells (active low). When using single Clav mode (DualClavEnb, bit4 in ATMINTFC register 0xF03, is set low), only atmURxEnb[0] is used and atmURxEnb[1] is not used but must be pulled up. This is most common configuration. |
| | atmURxEnb[1]* | | D18 | | |

Table 1-9. M28529 Pin Descriptions (14 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|-----------------------------------|----------------|----------------------------|-----|------|--|
| ATM Layer UTOPIA Interface | atmURxData[0] | ATM UTOPIA Receive Data | C20 | O/TS | Receive direction ATM side cell data. |
| | atmURxData[1] | | B21 | | |
| | atmURxData[2] | | A22 | | |
| | atmURxData[3] | | D20 | | |
| | atmURxData[4] | | C21 | | |
| | atmURxData[5] | | B22 | | |
| | atmURxData[6] | | A23 | | |
| | atmURxData[7] | | A24 | | |
| | atmURxData[8] | | D21 | | |
| | atmURxData[9] | | C22 | | |
| | atmURxData[10] | | B23 | | |
| | atmURxData[11] | | B24 | | |
| | atmURxData[12] | | C23 | | |
| | atmURxData[13] | | D22 | | |
| | atmURxData[14] | | B25 | | |
| | atmURxData[15] | | A26 | | |
| | atmURxPrtly | ATM UTOPIA Receive Parity | D19 | O/TS | Parity status signal. In 8 bit UTOPIA mode, a parity calculation is performed over atmURxData[7:0] for each clock cycle of atmURxCik. Odd parity is used. In 16 bit UTOPIA mode, this signal is the parity of atmURxData[15:0]. This signal is optional. |
| | atmURxAddr[0] | ATM UTOPIA Receive Address | E23 | I | Receive ATM Cell Bus address. This address determines the source channel of the Receive ATM cells output from the IMA subsystem and also selects the channel sourcing the atmURxCIAv signal. All 5 bits are not required in every application. |
| | atmURxAddr[1] | | D24 | | |
| | atmURxAddr[2] | | C25 | | |
| | atmURxAddr[3] | | B26 | | |
| | atmURxAddr[4] | | E24 | | |

Table 1-9. M28529 Pin Descriptions (15 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|--------------|-----------|------------------------|-----|-----|-----------------------------------|
| Power Supply | VDD18 | Supply Voltage (1.8 V) | E9 | | Power supply connections. (1.8 V) |
| | | | E10 | | |
| | | | E17 | | |
| | | | J5 | | |
| | | | J22 | | |
| | | | K5 | | |
| | | | K10 | | |
| | | | K11 | | |
| | | | K16 | | |
| | | | K17 | | |
| | | | K22 | | |
| | | | L10 | | |
| | | | L17 | | |
| | | | T10 | | |
| | | | T17 | | |
| | | | U5 | | |
| | | | U10 | | |
| | | | U11 | | |
| | | | U16 | | |
| | | | U17 | | |
| U22 | | | | | |
| V5 | | | | | |
| V22 | | | | | |
| AB9 | | | | | |
| AB10 | | | | | |
| AB17 | | | | | |
| AB18 | | | | | |

Table 1-9. M28529 Pin Descriptions (16 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|--------------|-------------------|---------------------------------------|--|-----|-----------------------------------|
| Power Supply | VDD33 | Supply Voltage (3.3 V) | C18 C24 E7 E8 E11 E12 E15 E19 E20 G5 G22 H5 H22 K12 K15 L5 L22 M2 M5 M10 M17 M22 R10 R17 R22 T5 | | Power supply connections. (3.3 V) |
| Power Supply | VDD33 (Continued) | Supply Voltage (3.3 V) (Continued) | T22 U3 U12 U15 W5 W22 Y5 Y22 AB7 AB8 AB11 AB12 AB15 AB16 AB19 AB20 AE3 | | Power supply connections. (3.3 V) |

Table 1-9. M28529 Pin Descriptions (17 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|--------------|-----------|-------------|-----|-----|---------------------|
| Power Supply | VSS | Ground | A1 | | Ground connections. |
| | | | B2 | | |
| | | | B12 | | |
| | | | D17 | | |
| | | | D23 | | |
| | | | E5 | | |
| | | | E6 | | |
| | | | E14 | | |
| | | | E21 | | |
| | | | E22 | | |
| | | | F5 | | |
| | | | F22 | | |
| | | | K13 | | |
| | | | K14 | | |
| | | | L11 | | |
| | | | L12 | | |
| | | | L13 | | |
| L14 | | | | | |
| L15 | | | | | |
| L16 | | | | | |
| M11 | | | | | |
| M12 | | | | | |
| M13 | | | | | |
| M14 | | | | | |
| M15 | | | | | |
| M16 | | | | | |

Table 1-9. M28529 Pin Descriptions (18 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|---------------------|--------------------|-----------------------|--|------------|---------------------|
| Power Supply | VSS (Continued) | Ground (Continued) | N2 N10 N11 N12 N13 N14 N15 N16 N17 N22 P5 P10 P11 P12 P13 P14 P15 P16 P17 R11 R12 R13 R14 R15 R16 R25 T11 T12 | | Ground connections. |

Table 1-9. M28529 Pin Descriptions (19 of 19)

| | Pin Label | Signal Name | No. | I/O | Description |
|---|--------------------|--|--|-----|---|
| Power Supply | VSS (Continued) | Ground (Continued) | T13 T14 T15 T16 U13 U14 AA5 AA22 AB5 AB6 AB13 AB21 AB22 AC24 AD3 AE15 | | Ground connections. |
| | VGG | Electrostatic Discharge (ESD) Supply Voltage | AC23 D4 | | Provides ESD protection when interfacing with 5 V systems. If using this device in a system with 5 V logic, this pin must be connected to 5 V. If using 3.3 V system, connect to 3.3 V. |
| Spare | | Spare Pins | A25 B1 AA23 AB23 AC05 AC25 | | Spare (unused) pins on the package. Reserved for future use and should be left unconnected. |
| Footnote: (1) All unused inputs should be tied to ground or left unconnected. All unused outputs or bidirectional pins should be left unconnected. | | | | | |

1.5.2 Pin Diagram and Definitions (UTOPIA-to-UTOPIA Configuration)

Figures 1-9 and 1-10 illustrate the logic and block diagrams of the M2852x’s functional modules. Pin descriptions are listed in Table 1-11.

Figure 3-33 is the pinout diagram for the M28529 when operating in the UTOPIA-to-UTOPIA mode. It is a single CMOS integrated circuit packaged in a 484-pin PBGA. All unused input pins should be connected to ground or power. Unused output and bidirectional pins should be left unconnected.

NOTE:

UTOPIA-to-UTOPIA configuration is selected by tying the PhyIntFcSel pin low.

When using the M28525/9 in Utopia to Utopia configuration, in addition to the standard Utopia Level 2 specification definitions, the device uses the PHY side RX and TX CLAV signals for the following purpose:

- The PHY TX CLAV signals are used to determine the stuffing rate for SICP cells. The M28525/9 will monitor the CLAV signal to determine the fullness of the downstream device's Utopia FIFO.
- For applications where timing is not available from the RX_TRLs (such as DSL), the M28525/9 can be configured to use the PHY RX CLAV signals to generate a clock that approximates the payload timing. As such, the expectation is the RX CLAV signals from the TC/PHY layer approximates an ideal PHY layer device in the sense that cell boundary times present on the receive physical bus are reproduced with a fixed offset in time to the cells available on the PHY Utopia bus.

Contact Mindspeed applications engineering for more details.

Figure 1-9. M28529 Logic Diagram (UTOPIA-to-UTOPIA)

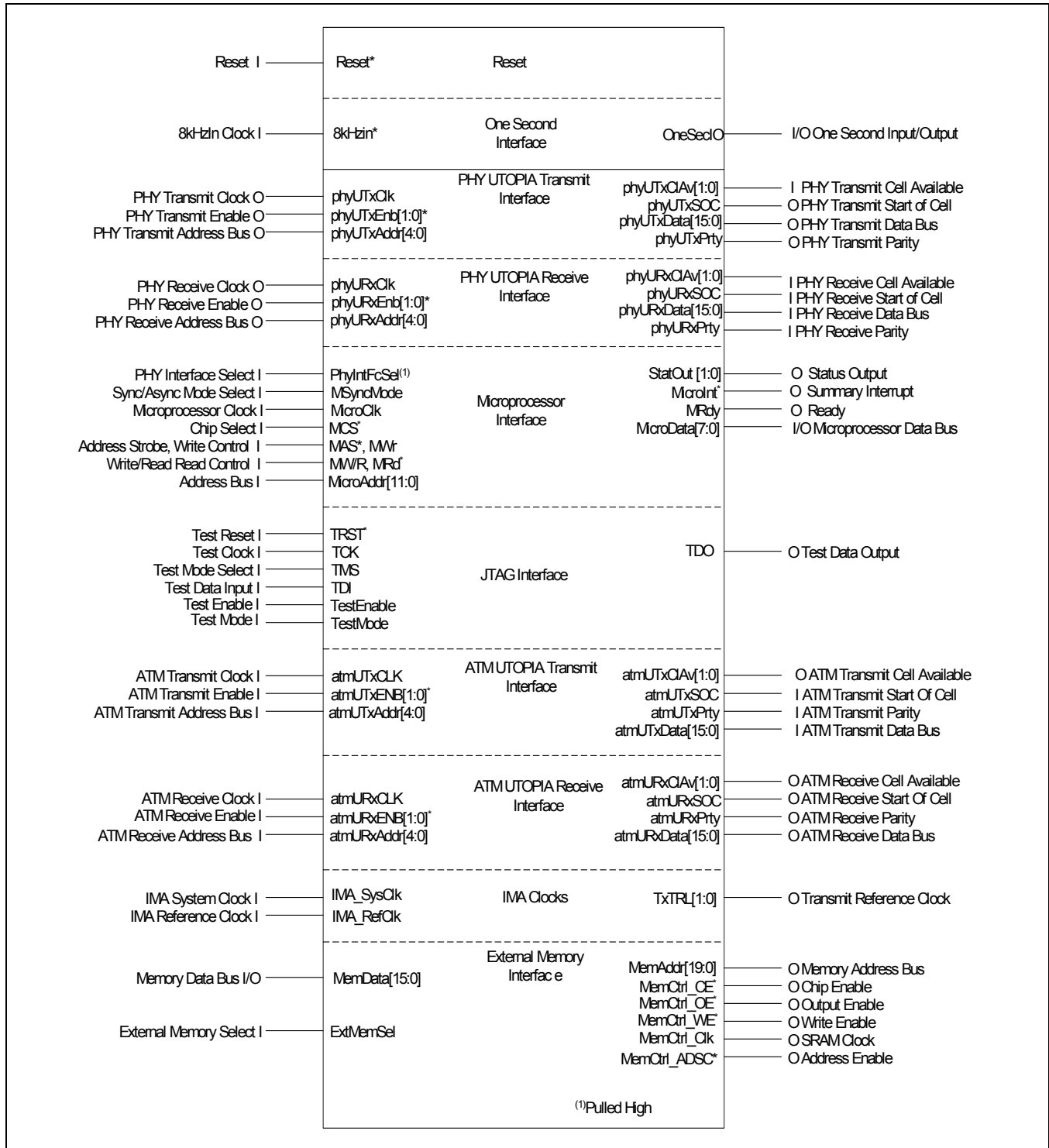


Figure 1-10. IMA Block Diagram

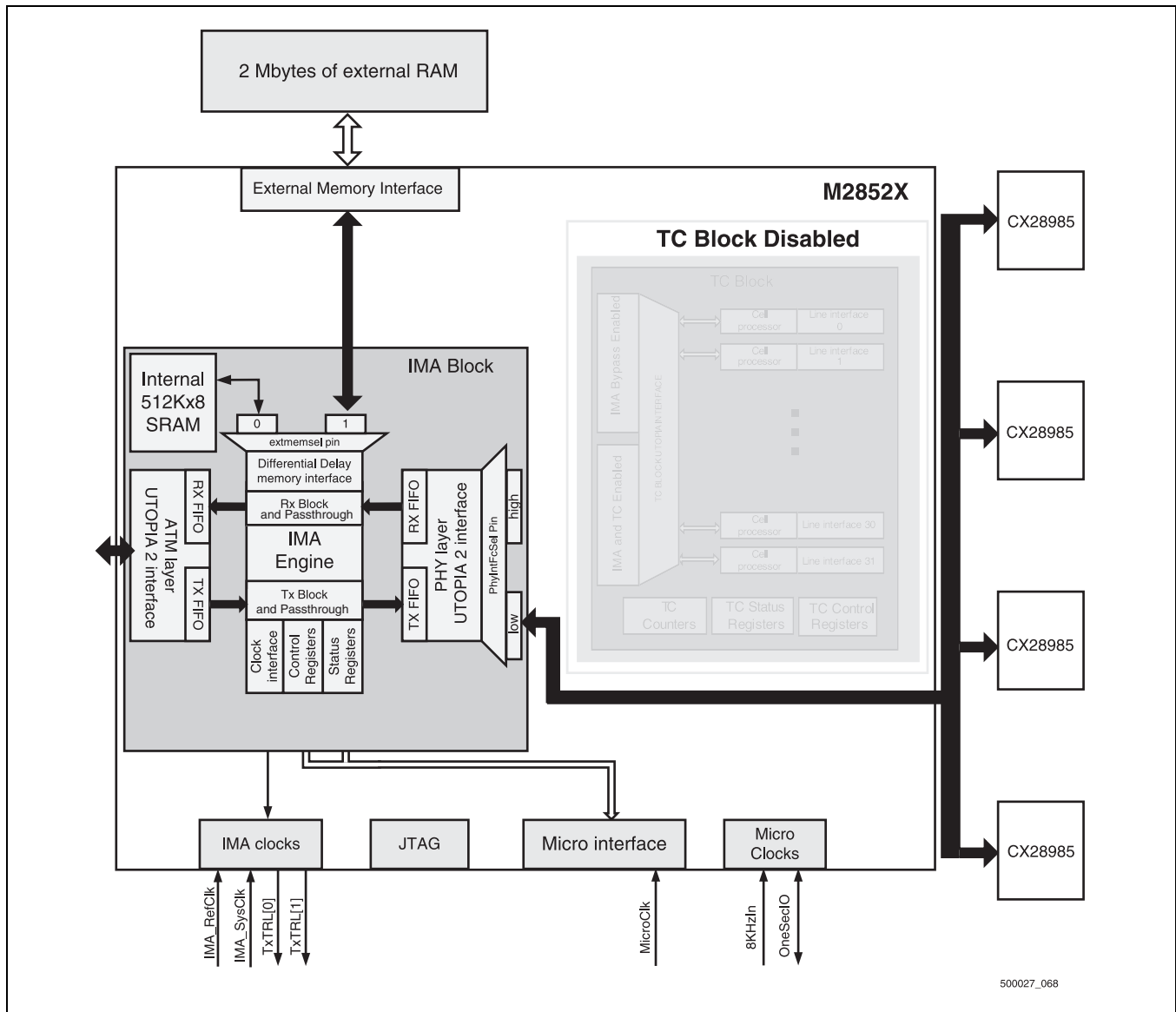


Table 1-10. UTOPIA-to-UTOPIA Configuration Information

| ATMMux [7,6] (ATMINTFC, 0xF03) | PhyIntFcSel (Pin AD24) | Description |
|--------------------------------|------------------------|--|
| 01 | Low | IMA UTOPIA using the PHY Side UTOPIA; Internal TC block and serial ports not used. |

General Note: Use of external memory is optional.

Table 1-11. M2852x Pin Descriptions (1 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|-----------------|------------|---|------|------|---|
| Micro Interface | StatOut[0] | Status Output | AB24 | 0 | General purpose output pins under software control. |
| | StatOut[1] | | AD26 | | |
| | MSyncMode | Microprocessor Synchronous/Asynchronous Bus Mode Select | AE24 | I/PD | Selects synchronous or asynchronous bus mode, which determines the functions of two pins, MW/R, MRd* (pin W4) and MAS*,MWr* (pin Y2). A logic 1 selects the synchronous bus mode. In this mode, these pins are defined as follows: MW/R (W4) and MAS* (Y2). A logic 0 selects the asynchronous SRAM-type bus mode. In this mode, the pins are defined as follows: MRd* (W4) and MWr* (Y2). |
| | Reset* | Device Reset | T4 | I/PU | When asserted low, resets the device. The microprocessor clock must be present before reset is released. If configuring the device for pass-through operation, a minimum delay of 25 uS for IMA_Sysclk of 66 MHz or 33 uS for IMA_Sysclk of 50 MHz is required from the release of reset to the first access of the IMA_RX_TRANS_TABLE register or the IMA_RX_ATM_TRANS_TABLE register (0x818/0x819). |
| | 8kHzIn | 8 kHz Input | AD25 | I | A clock input used to derive OneSecIO. Typically operates at a frequency of 8 kHz. |
| | OneSecIO | One-Second Input/Output | AE26 | I/O | Software can configure this pin as an output that equals the input from the 8kHzIn divided by 8000. When configured as an input, status registers and counters may be latched on the rising edge of this input. See Bit 0 of the Genctrl register (0xF00). |
| | MW/R, MRd* | Microprocessor Write/Read | W4 | I | When MSyncMode is asserted high, this pin is a read/write control pin. In this mode, when MW/R is asserted high, a write access is enabled and the MicroData[7:0] pin values will be written to the memory location indicated by the MicroAddr[11:0] pins. Also, when MW/R is asserted low in this mode, a read access is enabled and the memory location indicated by the MicroAddr[11:0] pins is read. Its value is placed on the MicroData[7:0] pins. Both read and write accesses assume the device is chip selected (MCS* = 0), the address is valid (MAS* = 0), and the device is not being reset (Reset* = 1). When MSyncMode is asserted low, this pin is a read control pin. In this mode, when MRd* is asserted low, a read access is enabled and the memory location indicated by the MicroAddr[11:0] pins is read. Its value is placed on the MicroData[7:0] pins. |
| | MCS* | Microprocessor Chip Select | V1 | I | When asserted low, the device is selected for read and write accesses. When asserted high, the device will not respond to input signal transitions on MicroCik, MW/R, MRd*, or MAS*, MWr*. Additionally, when MCS* is asserted high, the MicroData[7:0] pins are in a high-impedance state but the MicroInt* pin remains operational. |

Table 1-11. M2852x Pin Descriptions (2 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|-----------------|----------------------------------|-------------------------------|-----|--|--|
| Micro Interface | MAS*, MWr* | Microprocessor Address Strobe | Y2 | I | When MSyncMode is asserted high, this pin is an address strobe pin. When the MAS* pin is asserted low, it indicates a valid address, MicroAddr[11:0]. This signal is used to qualify read and write accesses. When MSyncMode is asserted low, this pin is a write control pin. When MWr* is asserted low, a write access is enabled and the MicroData[7:0] pin values will be written to the memory location indicated by the MicroAddr[11:0] pins. The write access assumes the device is chip selected (MCS* = 0), a read access is not being requested (MRd* = 1), and the device is not being reset (Reset* = 1). |
| | MicroAddr[0] | Microprocessor Address Bus | U2 | I | These 12 bits are an address input for identifying the register to access. |
| | MicroAddr[1] | | T3 | | |
| | MicroAddr[2] | | U1 | | |
| | MicroAddr[3] | | T2 | | |
| | MicroAddr[4] | | R4 | | |
| | MicroAddr[5] | | T1 | | |
| | MicroAddr[6] | | R3 | | |
| | MicroAddr[7] | | R2 | | |
| | MicroAddr[8] | | P4 | | |
| | MicroAddr[9] | | R1 | | |
| | MicroAddr[10] | | P3 | | |
| | MicroAddr[11] | | P2 | | |
| | MicroData[0] | Microprocessor Data Bus | W3 | I/O | A bi-directional data bus for reading and writing data to internal registers. |
| | MicroData[1] | | V4 | | |
| | MicroData[2] | | Y1 | | |
| | MicroData[3] | | W2 | | |
| | MicroData[4] | | V3 | | |
| | MicroData[5] | | U4 | | |
| | MicroData[6] | | W1 | | |
| MicroData[7] | V2 | | | | |
| MicroInt* | Microprocessor Interrupt Request | AA1 | O | When active low, the device needs servicing. It remains active until the pending interrupt is processed by the Interrupt Service Routine. This pin is an open drain output for an external wired OR logic implementation. An external pull-up resistor is required for this pin. | |

Table 1-11. M2852x Pin Descriptions (3 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|-----------------|-------------|------------------------------------|------|--------|--|
| Micro Interface | MRdy | Microprocessor Ready | Y3 | 0 | When active high, the current read or write transaction has been completed. For a read transaction, the data is ready to be transferred to the microprocessor. For a write transaction, the data provided by the microprocessor has been written. This pin is an open drain output for an external wired OR logic implementation. An external pull-up resistor is required for this pin. |
| | MicroClk | Microprocessor Clock | R5 | I | In asynchronous mode the microprocessor clock signal input can be clocked up to 66 MHz. In synchronous mode this pin can be clocked up to 25 MHz. The device samples the microprocessor interface pins (MCS*, MW/R, MRd*, MAS*, MicroAddr[11:0], and MicroData[7:0]) on the rising edge of this signal. The microprocessor interface output pins (MicroData[7:0], MicroInt*) are clocked on the rising edge of MicroClk. Note that this clock is required for both synchronous and asynchronous operations. See note in Section 1.15.1 . |
| External Memory | ExtMemSel | External Memory Enable | AC26 | I/PD | When this pin is pulled high, it enables the external differential delay SRAM bus. |
| | MemData[0] | Differential Delay Memory Data Bus | M26 | I/O/PD | Differential delay SRAM Data Bus. ATM cells extracted from the Receive data stream are stored in the SRAM for the purpose of differential delay compensation. |
| | MemData[1] | | N24 | | |
| | MemData[2] | | N25 | | |
| | MemData[3] | | N26 | | |
| | MemData[4] | | P26 | | |
| | MemData[5] | | P25 | | |
| | MemData[6] | | P24 | | |
| | MemData[7] | | P23 | | |
| | MemData[8] | | R26 | | |
| | MemData[9] | | P22 | | |
| | MemData[10] | | R24 | | |
| | MemData[11] | | T26 | | |
| | MemData[12] | | R23 | | |
| | MemData[13] | | T25 | | |
| | MemData[14] | | T24 | | |
| | MemData[15] | | U26 | | |

Table 1-11. M2852x Pin Descriptions (4 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|------------------------|---------------|--|------|------|--|
| External Memory | MemAddr[0] | Differential Delay Memory Address Bus | U25 | 0 | Receive SRAM Address Bus. These signals are enabled by tying the ExtMemSel pin high. |
| | MemAddr[1] | | T23 | | |
| | MemAddr[2] | | V26 | | |
| | MemAddr[3] | | U24 | | |
| | MemAddr[4] | | V25 | | |
| | MemAddr[5] | | W26 | | |
| | MemAddr[6] | | U23 | | |
| | MemAddr[7] | | V24 | | |
| | MemAddr[8] | | W25 | | |
| | MemAddr[9] | | Y26 | | |
| | MemAddr[10] | | V23 | | |
| | MemAddr[11] | | W24 | | |
| | MemAddr[12] | | Y25 | | |
| | MemAddr[13] | | AA26 | | |
| | MemAddr[14] | | W23 | | |
| | MemAddr[15] | | Y24 | | |
| | MemAddr[16] | | AA25 | | |
| | MemAddr[17] | | Y23 | | |
| | MemAddr[18] | | AB26 | | |
| | MemAddr[19] | | AA24 | | |
| | MemCtrl_CE* | Chip Enable | N23 | 0 | Receive SRAM Device Select (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high. |
| | MemCtrl_OE* | Output Enable | M25 | 0 | Receive SRAM Device Output (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high. |
| | MemCtrl_WE* | Write Enable | M24 | 0 | Receive SRAM write enable (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high. |
| | MemCtrl_CLK | SRAM Clock | AB25 | 0 | Receive SRAM clock signal. This signal is enabled by pulling the ExtMemSel pin high. |
| | MemCtrl_ADSC* | Address Enable | L26 | 0 | Receive SRAM address enable (active low) address strobe. This signal is enabled by pulling the ExtMemSel pin high. |
| JTAG | TRST* | Test Reset | C5 | I/PU | When asserted, the internal boundary-scan logic is reset. This pin has a pull-up resistor. |
| | TCK | Test Clock | A2 | I/PU | Samples the value of TMS and TDI on its rising edge to control the boundary scan operations. |
| | TMS | Test Mode Select | D5 | I/PU | Controls the boundary-scan Test Access Port (TAP) controller operation. This pin has a pull-up resistor. |
| | TDI | Test Data Input | C4 | I/PU | The serial test data input. This pin has a pull-up resistor. |
| | TDO | Test Data Output | C3 | 0 | The serial test data output. |

Table 1-11. M2852x Pin Descriptions (5 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|---------------------------|---------------|-----------------------------------|------|------|--|
| Test | TestEnable[0] | | AF26 | I/PD | Factory test use only, tie to VSS. |
| | TestEnable[1] | | AC22 | | |
| | ScanEnable | | AD23 | I/PD | Factory test use only, tie to VSS |
| | Tristate | Tristate | AE25 | I/PD | When this pin is high, all outputs are tristate. |
| PHY Side Interface | PhyIntFcSel | PHY Interface Select | AD24 | I/PU | If this pin is tied low, the PHY UTOPIA Interface mode is selected. This table shows pin configurations with this pin tied low. If this pin is tied high, the PHY Serial mode is selected. |
| | phyURxCIk | UTOPIA Receive Clock | AF9 | 0 | IMA_SysClk/2 |
| | phyURxEnb[0]* | PHY UTOPIA Receive Enable | AF16 | 0 | Data transfer and output enable for Receive PHY cells (active low). To support multiple PHY devices, separate enable signals are provided. Depending on the software configuration, some of the enable signals may not be available and will be replaced by additional PHY cell bus address bits. When the PHY Size (bits 4 and 5) of register 0x804 are set to 2 (single clav), phyURxEnb[1] must be pulled up. |
| | phyURxEnb[1]* | | AD15 | | |
| | phyURxAddr[0] | PHY UTOPIA Receive Address | AE11 | 0 | Receive PHY Cell Bus address. The following limitations apply: |
| | phyURxAddr[1] | | AD11 | | |
| | phyURxAddr[2] | | AF10 | | |
| | phyURxAddr[3] | | AE10 | | |
| | phyURxAddr[4] | | AC11 | | |
| | phyURxClAv[0] | PHY UTOPIA Receive Cell Available | AF19 | I/PD | Cell Available signals for Receive PHY interfaces. phyURxClAv[n] is active when one or more complete cells can be transferred. To support different PHY devices, separate cell available signals are provided. This allows expansion to 32 points. |
| phyURxClAv[1] | AF18 | | I/PD | | |

| Device | Addresses |
|--------|-----------|
| M28525 | 0–15, 31 |
| M28529 | 0–31 |

Table 1-11. M2852x Pin Descriptions (6 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|---------------------------------------|------------------------------------|-------------------------|------|---|---|
| PHY Side Interface (Continued) | phyURxData[0] | PHY UTOPIA Receive Data | AB14 | I/PD | Received 16 bit PHY Cell Data. All received cells are passed to the internal IMA processor. |
| | phyURxData[1] | | AC15 | | |
| | phyURxData[2] | | AE14 | | |
| | phyURxData[3] | | AF15 | | |
| | phyURxData[4] | | AD14 | | |
| | phyURxData[5] | | AC14 | | |
| | phyURxData[6] | | AF14 | | |
| | phyURxData[7] | | AF13 | | |
| | phyURxData[8] | | AE13 | | |
| | phyURxData[9] | | AD13 | | |
| | phyURxData[10] | | AC13 | | |
| | phyURxData[11] | | AF12 | | |
| | phyURxData[12] | | AE12 | | |
| | phyURxData[13] | | AD12 | | |
| | phyURxData[14] | | AF11 | | |
| | phyURxData[15] | | AC12 | | |
| phyURxSOC | PHY UTOPIA Start of Cell | AD17 | I/PD | Start of Cell synchronization signal for Receive PHY cells (active high). Indicates that the first byte of the cell is being placed on the PhyURxData[7:0] bus. | |
| phyURxPrty | PHY UTOPIA Receive Parity | AE18 | I/PD | Odd parity calculated over phyURxData[15:0] pins in 16-bit mode and over phyURxData[7:0] pins in 8-bit mode. | |
| phyUTxAddr[0] | PHY UTOPIA Transmit Address | G2 | 0 | Transmit PHY Cell Bus address. The following limitations apply: | |
| phyUTxAddr[1] | | F1 | | | |
| phyUTxAddr[2] | | G3 | | | |
| phyUTxAddr[3] | | H4 | | | |
| phyUTxAddr[4] | | F2 | | | |
| phyUTxCIaV[0] | PHY UTOPIA Transmit Cell Available | E2 | I/PD | Cell Available signals for Transmit ATM cells. When phyUTxCIaV[n] is active high, the PHY has space available for one or more complete cells. To support different PHY devices, separate cell available signals are provided. | |
| phyUTxCIaV[1] | | D1 | | | |
| phyUTxCIk | PHY UTOPIA Transmit Clock | G4 | 0 | IMA_SysCIk divided by two. | |

| Device | Addresses |
|--------|-----------|
| M28525 | 0–15, 31 |
| M28529 | 0–31 |

Table 1-11. M2852x Pin Descriptions (7 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|--------------------------------|----------------|-----------------------------------|------|------|---|
| PHY Side Interface (Continued) | phyUTxData[0] | PHY UTOPIA Transmit Data | AF4 | 0 | 8 bit PHY Cell Data to be sent out the PHY facility. 8 bit UTOPIA interface used to transmit data to the external TC devices. |
| | phyUTxData[1] | | AE4 | | |
| | phyUTxData[2] | | AC6 | | |
| | phyUTxData[3] | | AD5 | | |
| | phyUTxData[4] | | AF3 | | |
| | phyUTxData[5] | | AF2 | | |
| | phyUTxData[6] | | AD4 | | |
| | phyUTxData[7] | | AC4 | | |
| | phyUTxData[8] | | P1 | | |
| | phyUTxData[9] | | N1 | | |
| | phyUTxData[10] | | N3 | | |
| | phyUTxData[11] | | N4 | | |
| | phyUTxData[12] | | M1 | | |
| | phyUTxData[13] | | N5 | | |
| | phyUTxData[14] | | M3 | | |
| | phyUTxData[15] | | L1 | | |
| | phyUTxEnb[0]* | PHY UTOPIA Transmit Enable | E1 | 0 | Data transfer enable for Transmit PHY cells (active low signal). To support different PHY devices, separate enable signals are provided. When the PHY Size (bits 4 and 5) of register 0x804 are set to 2 (single clav), phyUTxEnb[1] must be pulled up. |
| | phyUTxEnb[1]* | | F3 | | |
| | phyUTxSOC | PHY UTOPIA Transmit Start of Cell | AE9 | 0 | Start of Cell synchronization signal for Transmit PHY cells (active high). Indicates that the first byte of a cell is being placed on the phyUTxData[7:0] bus. |
| | phyUTxPrty | PHY UTOPIA Transmit Parity | AD10 | 0 | Odd parity calculated over phyUTxData[15:0] pins in 16-bit mode and over phyUTxData[7:0] pins in 8-bit mode. |
| IMA Clocks | IMA_SysClk | IMA Subsystem Clock | E18 | I/PU | Most of the IMA logic circuits use this clock (or a derivative of it). It can also be used as a T1/E1 reference clock. Refer to Section 1.12 . |
| | IMA_RefClk | IMA Reference Clock | E16 | I/PU | If this is to be used as a reference clock, set the frequency as shown in Section 1.12 . |
| | TxTRL[0] | Transmit Reference Clocks | A19 | 0 | Transmit Reference Clocks. |
| | TxTRL[1] | | B19 | | |

Table 1-11. M2852x Pin Descriptions (8 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|-----------------------------------|----------------------------|-----------------------------|-----|---|--|
| ATM Layer UTOPIA Interface | atmUTxAddr[0] | ATM UTOPIA Transmit Address | L23 | I | Transmit ATM Cell Bus address. |
| | atmUTxAddr[1] | | K25 | | |
| | atmUTxAddr[2] | | L24 | | |
| | atmUTxAddr[3] | | K26 | | |
| | atmUTxAddr[4] | | L25 | | |
| | atmUTxData[0] | ATM UTOPIA Transmit Data | E26 | I | Transmit direction ATM side cell data. |
| | atmUTxData[1] | | F25 | I | |
| | atmUTxData[2] | | H23 | I | |
| | atmUTxData[3] | | G24 | I | |
| | atmUTxData[4] | | F26 | I | |
| | atmUTxData[5] | | G25 | I | |
| | atmUTxData[6] | | H24 | I | |
| | atmUTxData[7] | | J23 | I | |
| | atmUTxData[8] | | G26 | I/PD | |
| | atmUTxData[9] | | H25 | I/PD | |
| | atmUTxData[10] | | J24 | I/PD | |
| | atmUTxData[11] | | K23 | I/PD | |
| | atmUTxData[12] | | H26 | I/PD | |
| | atmUTxData[13] | | J25 | I/PD | |
| | atmUTxData[14] | | K24 | I/PD | |
| atmUTxData[15] | J26 | I/PD | | | |
| atmUTxPrty | ATM UTOPIA Transmit Parity | D26 | I | Parity status signal. In 8 bit UTOPIA mode, a parity calculation is performed over atmUTxData[7:0] for each clock cycle of atmUTxCk. Odd parity is used. In 16 bit UTOPIA mode, this signal is the parity of atmUTxData[15:0]. This signal is optional. | |

Table 1-11. M2852x Pin Descriptions (9 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|----------------------------|---------------|------------------------------------|-----|------|--|
| ATM Layer UTOPIA Interface | atmUTxClAv[0] | ATM UTOPIA Transmit Cell Available | G23 | O/TS | Cell Available signals for transmit ATM cells (active high). When atmUTxClAv[1] or atmUTxClAv[0] is active one or more complete cells can be transferred from the ATM layer. Only atmUTxClAv[0] is used (atmUTxClAv[1] is ignored) when the DualClavEnb (bit 4) is low (default) in the ATMINTFC register 0xF03. This is the most common configuration. |
| | atmUTxClav[1] | | E25 | | |
| | atmUTxSOC | ATM UTOPIA Transmit Start of Cell | F24 | I | Start of Cell synchronization signal for transmit ATM cells (active high). Indicates that the first byte/word of the 53 byte cell is being placed on the atmUTxData bus. |
| | atmUTxEnb[0]* | ATM UTOPIA Transmit Enable | D25 | I/PU | Enable Data transfer enable(s) for transmit ATM cells (active low). Indicates that the first byte/word of the 53 byte cell is being placed on the atmUTxData bus. When using single Clav mode (DualClavEnb, bit4 in ATMINTFC register 0xF03, is set low), only atmUTxEnb[0] is used and atmUTxEnb[1] is not used but must be pulled up. This is most common configuration. |
| | atmUTxEnb[1]* | | C26 | I/PU | |
| | atmUTxCIk | ATM UTOPIA Transmit Clock | M23 | I | Clock signal used for transfer of transmit ATM cells from the ATM Layer. The maximum clock rate is 50 MHz. (Note: 33 MHz for TC Only mode.) |
| | atmURxSOC | ATM UTOPIA Receive Start of Cell | C19 | O/TS | Start of Cell synchronization signal for receive ATM cells (active high). Indicates that the first byte/word of the 53 byte cell is being placed on the atmURxData bus. |
| | atmURxCIk | ATM UTOPIA Receive Clock | F23 | I | Clock signal used for transfer of receive ATM cells from the ATM Layer. The maximum clock rate 50 MHz. (Note: 33 MHz for TC Only mode.) |
| | atmURxClAv[0] | ATM UTOPIA Receive Cell Available | B20 | O/TS | Cell Available signals for receive ATM cells (active high). When atmURxClAv[1] or atmURxClAv[0] is active, one or more complete cells can be transferred to the ATM Layer. Only atmURxClAv[0] is used (atmURxClAv[1] is ignored) when the DualClavEnb (bit 4) is low (default) in the ATMINTFC register 0xF03. This is the most common configuration. |
| | atmURxClAv[1] | | A21 | | |
| | atmURxEnb[0]* | ATM UTOPIA Receive Enable | A20 | I/PU | Data transfer and output enable for receive ATM cells (active low). Only atmURxEnb[0] is used (atmURxEnb[1] will be ignored) when the DualClavEnb (bit 4) is low (default) in the ATMINTFC register 0xF03. This is most common configuration. When using single clav mode (DualClavEnb bit is set to 0), atmURxEnb[1] must be pulled up. |
| | atmURxEnb[1]* | | D18 | I/PU | |

Table 1-11. M2852x Pin Descriptions (10 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|-----------------------------------|------------------|----------------------------|------------|------------|---|
| ATM Layer UTOPIA Interface | atmURxData[0] | ATM UTOPIA Receive Data | C20 | 0/TS | Receive direction ATM side cell data. |
| | atmURxData[1] | | B21 | | |
| | atmURxData[2] | | A22 | | |
| | atmURxData[3] | | D20 | | |
| | atmURxData[4] | | C21 | | |
| | atmURxData[5] | | B22 | | |
| | atmURxData[6] | | A23 | | |
| | atmURxData[7] | | A24 | | |
| | atmURxData[8] | | D21 | | |
| | atmURxData[9] | | C22 | | |
| | atmURxData[10] | | B23 | | |
| | atmURxData[11] | | B24 | | |
| | atmURxData[12] | | C23 | | |
| | atmURxData[13] | | D22 | | |
| | atmURxData[14] | | B25 | | |
| | atmURxData[15] | | A26 | | |
| | atmURxPrty | ATM UTOPIA Receive Parity | D19 | 0/TS | Parity status signal. In 8 bit UTOPIA mode, a parity calculation is performed over atmURxData[7:0] for each clock cycle of atmUTxCk. Odd parity is used. In 16 bit UTOPIA mode, this signal is the parity of atmURxData[15:0]. This signal is optional. |
| | atmURxAddr[0] | ATM UTOPIA Receive Address | E23 | I | Receive ATM Cell Bus address. This address determines the source channel of the Receive ATM cells output from the IMA subsystem and also selects the channel sourcing the atmURxCIAv signal. |
| | atmURxAddr[1] | | D24 | | |
| | atmURxAddr[2] | | C25 | | |
| | atmURxAddr[3] | | B26 | | |
| | atmURxAddr[4] | | E24 | | |

Table 1-11. M2852x Pin Descriptions (11 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|--------------|-----------|---------------------------|-----|-----|-----------------------------------|
| Power Supply | VDD18 | Supply Voltage (1.8 V) | E9 | | Power supply connections. (1.8 V) |
| | | | E10 | | |
| | | | E17 | | |
| | | | J5 | | |
| | | | J22 | | |
| | | | K5 | | |
| | | | K10 | | |
| | | | K11 | | |
| | | | K16 | | |
| | | | K17 | | |
| | | | K22 | | |
| | | | L10 | | |
| | | | L17 | | |
| | | | T10 | | |
| | | | T17 | | |
| | | | U5 | | |
| | | | U10 | | |
| | | | U11 | | |
| | | | U16 | | |
| | | | U17 | | |
| U22 | | | | | |
| V5 | | | | | |
| V22 | | | | | |
| AB9 | | | | | |
| AB10 | | | | | |
| AB17 | | | | | |
| AB18 | | | | | |

Table 1-11. M2852x Pin Descriptions (12 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|--------------|----------------------|--|--|-----|--|
| Power Supply | VDD33 | Supply Voltage (3.3 V) | C18 C24 E7 E8 E11 E12 E15 E19 E20 G5 G22 H5 H22 K12 K15 L5 L22 M2 M5 M10 M17 M22 R17 R10 R22 T5 | | Power supply connections. (3.3 V) |
| Power Supply | VDD33 (Continued) | Supply Voltage (3.3 V) (Continued) | T22 U12 U15 W5 W22 Y5 Y22 AB7 AB8 AB11 AB12 AB15 AB16 AB19 AB20 AE3 U3 | | Power supply connections. (3.3 V) (Continued) |

Table 1-11. M2852x Pin Descriptions (13 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|---------------------|-----------|-------------|---|-----|---------------------|
| Power Supply | VSS | Ground | A1 B2 B12 D17 D23 E5 E6 E14 E21 E22 F5 F22 K13 K14 L11 L12 L13 L14 L15 L16 M11 M12 M13 M14 M15 M16 | | Ground connections. |

Table 1-11. M2852x Pin Descriptions (14 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|--------------|--------------------|---|--|-----|---|
| Power Supply | VSS | Ground | N2 N10 N11 N12 N13 N14 N15 N16 N17 N22 P5 P10 P11 P12 P13 P14 P15 P16 P17 R11 R12 R13 R14 R15 R16 R25 T11 T12 | | Ground connections. |
| | VSS (Continued) | Ground (Continued) | T13 T14 T15 T16 U13 U14 AA5 AA22 AB5 AB6 AB13 AB21 AB22 AC24 AD3 AE15 | | Ground connections. (Continued) |
| | VGG | Electrostatic Discharge (ESD) Supply Voltage | AC23 D4 | | Provides ESD protection when interfacing with 5 V systems. If using this device in a system with 5 V logic, this pin must be connected to 5 V. If using 3.3 V system, connect to 3.3 V. |

Table 1-11. M2852x Pin Descriptions (15 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|---------------------|-----------|---------------|---|-----|--------------------------------------|
| Power Supply | | Unused Inputs | A3 A7 A8 A9 A10 A11 A15 A16 A17 A18 B3 B4 B5 B8 B9 B10 B11 B14 B15 B16 B17 B18 C1 C2 C6 C9 C10 C11 C14 C15 C16 C17 D2 D3 D6 D7 D9 D10 D11 D12 D14 D15 D16 E3 E4 F4 G1 H1 H2 H3 J1 J2 | | Unused Inputs with internal pulldown |

Table 1-11. M2852x Pin Descriptions (16 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|---------------------|-----------|--------------|---|-----|--------------------------------------|
| Power Supply | | Unused Input | J3 J4 K1 K2 K3 K4 L2 L3 L4 M4 Y4 AA2 AA3 AA4 AB1 AB2 AB3 AB4 AC1 AC2 AC3 AC7 AC8 AC9 AC10 AC18 AC19 | | Unused Inputs with Internal Pulldown |

Table 1-11. M2852x Pin Descriptions (17 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|---------------------|-----------|--------------|------|-----|--------------------------------------|
| Power Supply | | Unused Input | AD1 | | Unused Inputs with Internal Pulldown |
| | | | AD2 | | |
| | | | AD6 | | |
| | | | AD7 | | |
| | | | AD8 | | |
| | | | AD9 | | |
| | | | AD18 | | |
| | | | AD19 | | |
| | | | AD20 | | |
| | | | AE1 | | |
| | | | AE2 | | |
| | | | AE5 | | |
| | | | AE6 | | |
| | | | AE7 | | |
| | | | AE8 | | |
| | | | AE19 | | |
| | | | AE20 | | |
| | | | AE21 | | |
| | | | AF1 | | |
| | | | AF5 | | |
| | | | AF6 | | |
| | | | AF7 | | |
| | | | AF8 | | |
| | | AF20 | | | |
| | | AF21 | | | |
| | | AF22 | | | |
| | | AF23 | | | |

Table 1-11. M2852x Pin Descriptions (18 of 18)

| | Pin Label | Signal Name | No. | I/O | Description |
|--------------|-----------|----------------|--|-----|---|
| Power Supply | | Unused I/O | A6 A13 A14 AC16 AC20 AD21 AE16 AE22 AF24 B7 B13 C7 C8 C13 | | Unused I/O with pulldown (outputs in tristate) Note: Leave unconnected. |
| Power Supply | | Unused Outputs | A12 AC17 AC21 AD16 AD22 AE17 AE23 AF17 AF25 B6 C12 D13 D8 E13 | | Unused Outputs (tristate) Note: Leave unconnected. |
| Spare | | Spare | A25 B1 AA23 AB23 AC5 AC25 | | Spare (unused) pins on the package. Reserved for future use and should be left unconnected. |

1.5.3 Interleaved Highway Configuration

Four serial data streams can be combined together into one serial data stream using an Interleaved Highway Interface. For more information on the operation of the Interleaved Highway, refer to [Section 1.14.2.5.5](#). The Interleaved Highway interface can be enabled on a per highway basis. When an Interleaved Highway is enabled the pinout of the group of four muxed serial streams, see [Table 1-12](#) for the grouping, changes to the pinout described in [Table 1-14](#), [Table 1-15](#) and [Table 1-16](#). [Table 1-13](#) describes the functionality of each of the interleaved highway interface pins.

Table 1-12. Serial Stream Muxing into Interleaved Highway

| Interleaved Highway | Serial Stream | Interleaved Highway | Serial Stream |
|---------------------|---------------|---------------------|---------------|
| 0 | 0 | 4 | 16 |
| | 1 | | 17 |
| | 2 | | 18 |
| | 3 | | 19 |
| 1 | 4 | 5 | 20 |
| | 5 | | 21 |
| | 6 | | 22 |
| | 7 | | 23 |
| 2 | 8 | 6 | 24 |
| | 9 | | 25 |
| | 10 | | 26 |
| | 11 | | 27 |
| 3 | 12 | 7 | 28 |
| | 13 | | 29 |
| | 14 | | 30 |
| | 15 | | 31 |

Table 1-13. M28529 Interleaved Highway Pin Descriptions

| | Pin Label | Signal Name | I/O | Description |
|----------------------------------|-------------|---|------|---|
| Interleaved Hwy Interface | IHRxSync[x] | Interleaved Highway Receive Frame Sync Input | I/PD | When the Interleaved Highway interface is enabled, this is the frame sync input. |
| | IHRxCIk[x] | Interleaved Highway Transmit Clock Input | I/PD | When the Interleaved Highway interface is enabled, this is the receive line clock input. |
| | IHRxInDo[x] | Interleaved Highway Receive Timeslot Indicator Input | I/PD | When the Interleaved Highway interface is enabled, this is the receive timeslot indicator input. |
| | IHRxData[x] | Interleaved Highway Receive Data Input | I/PD | When the Interleaved Highway interface is enabled, this is the receive line data input. |
| | IHTxSync[x] | Interleaved Highway Transmit Frame Sync Input/Output | I/PD | When the Interleaved Highway interface is enabled, this is the frame sync. |
| | IHTxCIk[x] | Interleaved Highway Transmit Clock Input | I/PD | When the Interleaved Highway interface is enabled, this is the transmit line clock input. |
| | IHTxInDo[x] | Interleaved Highway Transmit Timeslot Indicator Input | I/PD | When the Interleaved Highway interface is enabled, this is the transmit timeslot indicator input. |
| | IHTxData[x] | Interleaved Highway Transmit Data Output | O | When the Interleaved Highway interface is enabled, this is the transmit line data output |

Table 1-14. Interleaved Highway Port 0 - 3 Pinouts

| Interleaved Highway 0 | | Interleaved Highway 1 | | Interleaved Highway 2 | | Interleaved Highway 3 | |
|-----------------------|-----|-----------------------|-----|-----------------------|-----|-----------------------|-----|
| Pin Label | No. | Pin Label | No. | Pin Label | No. | Pin Label | No. |
| IHRxSync[0] | B17 | IHRxSync[1] | C11 | IHRxSync[2] | B4 | IHRxSync[3] | H1 |
| IHRxCIk[0] | B18 | IHRxCIk[1] | A11 | IHRxCIk[2] | B5 | IHRxCIk[3] | G1 |
| IHRxInDo[0] | A17 | IHRxInDo[1] | B10 | IHRxInDo[2] | D6 | IHRxInDo[3] | K4 |
| IHRxData[0] | D15 | IHRxData[1] | C10 | IHRxData[2] | C2 | IHRxData[3] | J1 |
| IHTxSync[0] | A14 | IHTxSync[1] | C8 | IHTxSync[2] | G4 | IHTxSync[3] | L1 |
| IHTxData[0] | D13 | IHTxData[1] | D8 | IHTxData[2] | H4 | IHTxData[3] | N4 |
| IHTxInDo[0] | A13 | IHTxInDo[1] | B7 | IHTxInDo[2] | F3 | IHTxInDo[3] | M3 |
| IHTxCIk[0] | A15 | IHTxCIk[1] | C9 | IHTxCIk[2] | F4 | IHTxCIk[3] | K1 |

Table 1-15. Interleaved Highway Port 4 - 7 Pinouts

| Interleaved Highway 4 | | Interleaved Highway 5 | | Interleaved Highway 6 | | Interleaved Highway 7 | |
|-----------------------|-----|-----------------------|------|-----------------------|------|-----------------------|------|
| Pin Label | No. | Pin Label | No. | Pin Label | No. | Pin Label | No. |
| IHRxSync[4] | Y4 | IHRxSync[5] | AE6 | IHRxSync[6] | AF12 | IHRxSync[7] | AD18 |
| IHRxCIk[4] | AA2 | IHRxCIk[5] | AE5 | IHRxCIk[6] | AC12 | IHRxCIk[7] | AD17 |
| IHRxInDo[4] | AA3 | IHRxInDo[5] | AD7 | IHRxInDo[6] | AC13 | IHRxInDo[7] | AE19 |
| IHRxData[4] | AA4 | IHRxData[5] | AE7 | IHRxData[6] | AF13 | IHRxData[7] | AC18 |
| IHTxSync[4] | AC4 | IHTxSync[5] | AE9 | IHTxSync[6] | AD15 | IHTxSync[7] | AE22 |
| IHTxData[4] | AD5 | IHTxData[5] | AE10 | IHTxData[6] | AD16 | IHTxData[7] | AE23 |
| IHTxInDo[4] | AD4 | IHTxInDo[5] | AD10 | IHTxInDo[6] | AF16 | IHTxInDo[7] | AC20 |
| IHTxCIk[4] | AC3 | IHTxCIk[5] | AE8 | IHTxCIk[6] | AF15 | IHTxCIk[7] | AC19 |

General Note:

1. Interleaved Highway serial port 4-7 pins are no connects on the M28525.

The interleaved highway can be selected on a per group of 4 channel basis. When interleaved highway mode is selected, the following serial mode pins, as identified in [Table 1-16](#) become unused.

Table 1-16. No Connects Per Interleaved Highway Group (1 of 4)

| Highway | Pin | Description |
|-----------|---|---|
| Highway 0 | A16 A18 B14 B15 B16 C14 C15 C16 C17 D14 D16 | Input No Connects With Pulldown |
| | B13 C13 | Unused I/O (Pulled Down/Outputs tristate) Note: Leave unconnected. |
| | A12 C12 E13 | Unused Outputs (tristate) Note: Leave unconnected. |

Table 1-16. No Connects Per Interleaved Highway Group (2 of 4)

| Highway 1 | A7 A8 A9 A10 B8 B9 B11 D9 D10 D11 D12 | Unused Input (Pulled Down) |
|-----------|---|---|
| | A6 C7 | Unused I/O (Pulled down/Outputs tristate) Note: Leave unconnected. |
| | A4 A5 B6 | Unused Output (tristate) Note: Leave unconnected. |
| Highway 2 | A3 B3 C1 C6 D1 D2 D3 D7 E2 E3 E4 | Unused Input (Pulled Down) |
| | E1 F2 | Unused I/O (Pulled down/Outputs tristate) Note: Leave unconnected. |
| | F1 G2 G3 | Unused Output (tristate) Note: Leave unconnected. |
| Highway 3 | H2 H3 J2 J3 J4 K2 K3 L2 L3 L4 M4 | Unused Input (Pulled Down) |
| | M1 N5 | Unused I/O (Pulled down/Outputs tristate) Note: Leave unconnected. |
| | N1 N3 P1 | Unused Output (tristate) Note: Leave unconnected. |

Table 1-16. No Connects Per Interleaved Highway Group (3 of 4)

| Highway 4 | AB1 AB2 AB3 AB4 AC1 AC2 AD1 AD2 AE1 AE2 AF1 | Unused Input (Pulled Down) |
|-----------|--|---|
| | AF2 AF3 | Unused I/O (Pulled down/Outputs tristate) Note: Leave unconnected. |
| | AC6 AE4 AF4 | Unused Output (tristate) Note: Leave unconnected. |
| Highway 5 | AC7 AC8 AC9 AC10 AD6 AD8 AD9 AF5 AF6 AF7 AF8 | Unused Input (Pulled Down) |
| | AC11 AF9 | Unused I/O (Pulled down/Outputs tristate) Note: Leave unconnected. |
| | AD11 AE11 AF10 | Unused Output (tristate) Note: Leave unconnected. |
| Highway 6 | AB14 AC14 AC15 AD12 AD13 AD14 AE12 AE13 AE14 AF11 AF14 | Unused Input (Pulled Down) |
| | AC16 AE16 | Unused I/O (Pulled down/Outputs tristate) Note: Leave unconnected. |
| | AC17 AE17 AF17 | Unused Output (tristate) Note: Leave unconnected. |

Table 1-16. No Connects Per Interleaved Highway Group (4 of 4)

| Highway 7 | AD19 AD20 AE18 AE20 AE21 AF18 AF19 AF20 AF21 AF22 AF23 | Unused Input (Pulled Down) |
|-----------|--|---|
| | AD21 AF24 | Unused I/O (Pulled down/Outputs tristate) Note: Leave unconnected. |
| | AC21 AD22 AF25 | Unused Output (tristate) Note: Leave unconnected. |

1.6 Stand Alone Cell Delineation

Figure 1-11 is an example of a non-IMA application. The M28529 is being used as a stand alone Cell Delineator. Cell Delineation is performed internally and the M2852x interfaces directly to the framers. These framers could be T1/E1 or DSL.

NOTE: There may be applications that require the flexibility of the M28529 in a non-IMA mode. This mode is also useful for troubleshoot during development since the IMA block is bypassed. Configuration information is shown in Table 1-17.

Figure 1-11. Non-IMA Application

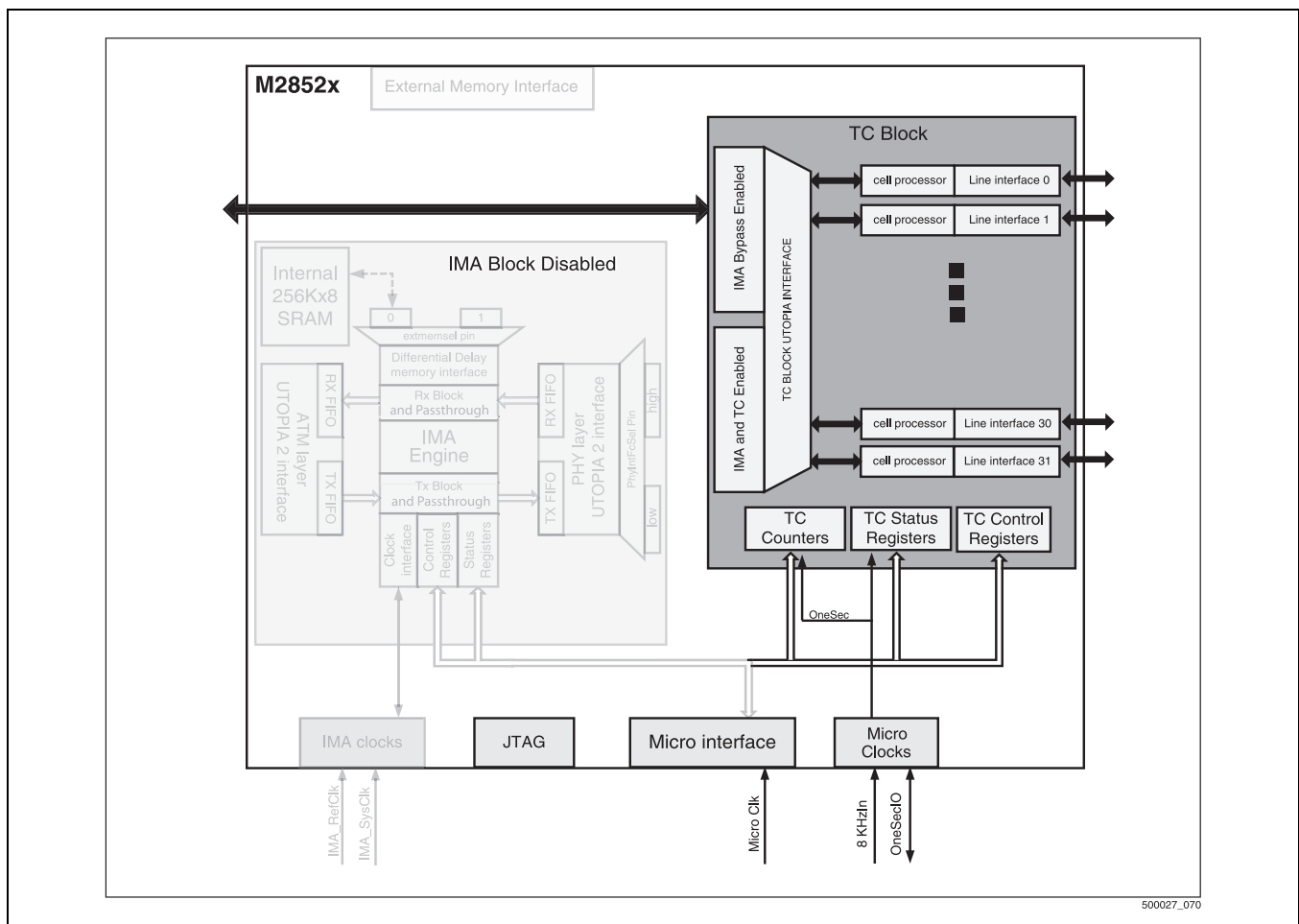


Table 1-17. Cell Delineation Configuration Information

| ATMMux [7,6] (ATMINTFC, 0xF03) | PhyIntFcSel (Pin AD24) | Description |
|--------------------------------|------------------------|---|
| 10 | High | TC Block Direct; Device used as Stand-alone cell delineator with 32 serial ports; IMA block not used. |

1.7 Source Loopbacks (UTOPIA-to-Serial Configuration Only)

Source loopback checks that the host (the ATM layer) is communicating with the PHY. It is enabled and disabled in bit 5 of the PMODE register (0x04). When source loopback is enabled for a given port, all data transmitted by the M2852x on that port is also looped back through the Receive Line Interface. Data from the framer interface is ignored.

There are two different modes of source loopback, source loopback mode 0 and source loopback mode 1. The loopbacks work in TC enabled modes.

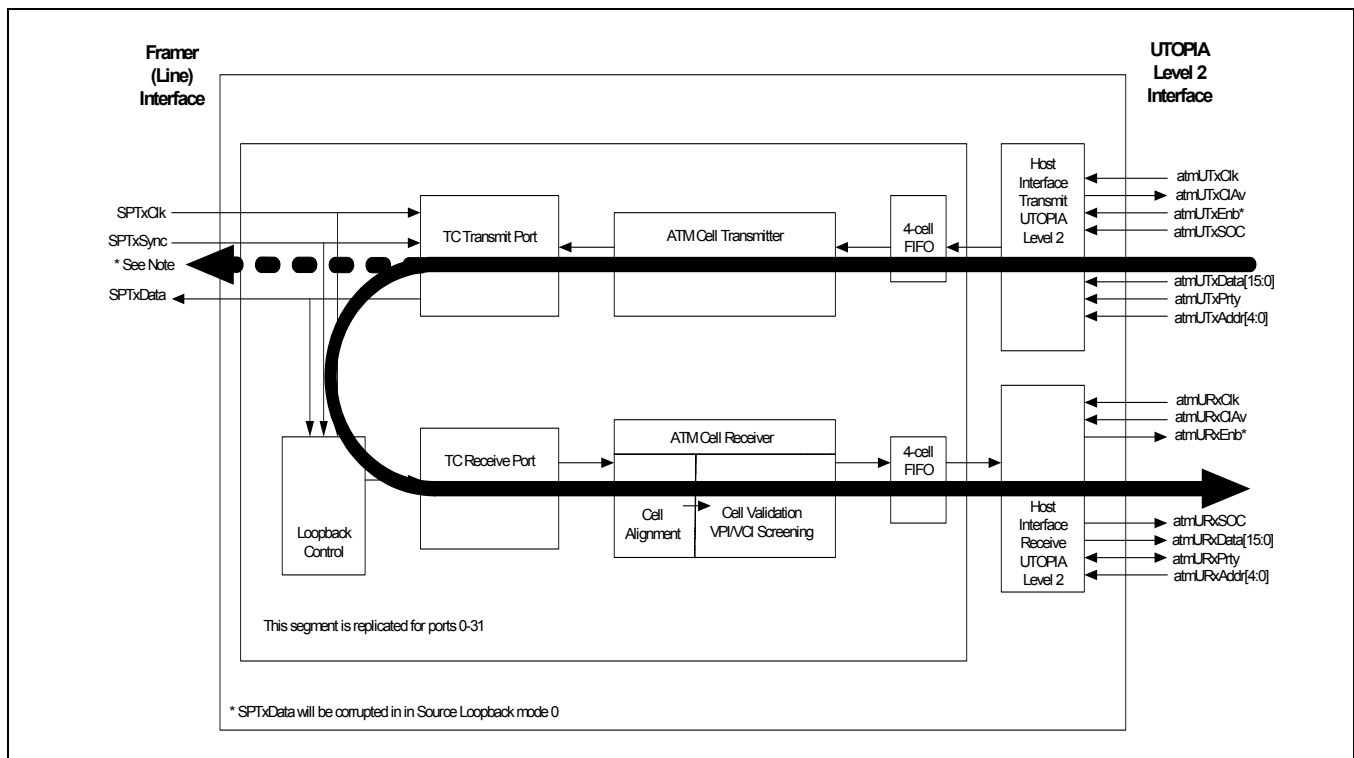
1.7.1 Source Loopback Mode 0

During source loopback mode 0, the port is automatically placed in General Purpose mode and an internal clock (IMA_SysClk/2 for IMA mode, atmUTxClk for TC Only mode) is used as the clock to loop back cells. As a result of the automatic mode switch and clock used, the data on the Tx serial lines will be corrupted.

1.7.2 Source Loopback Mode 1

During source loopback mode 1, the port is not placed in General Purpose mode (the serial framing remains as configured) and the SPTxCLK and SPTxSync device input signals are routed along with the SPTxDATA to the TC receive port circuit.

Figure 1-12. Source Loopback Diagram (For simplicity the diagram shows the TC Block Only.)

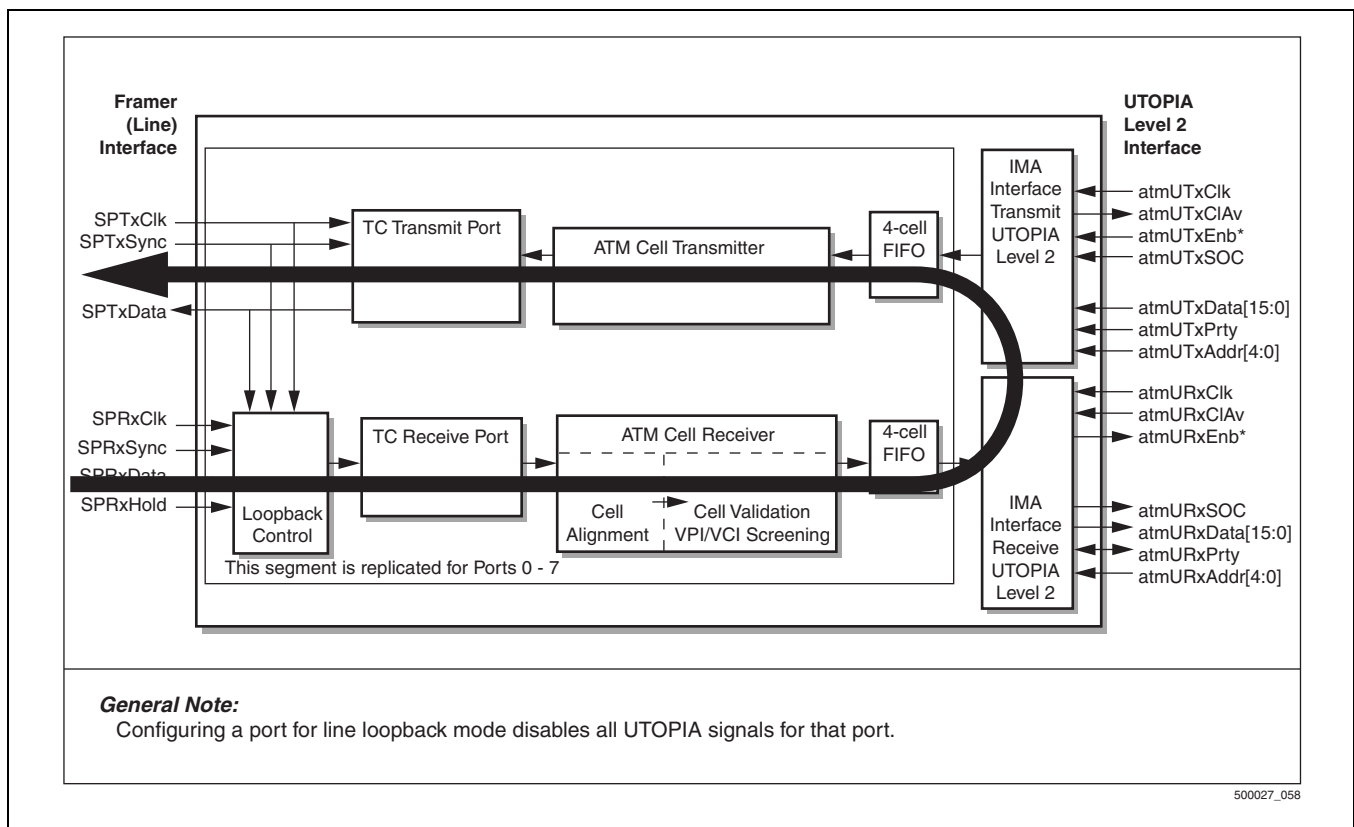


1.8 Far-End Line Loopback (Serial Configuration Only)

Far-End Line loopback verifies Line interface is communicating with the PHY. It is enabled by bit 4 of the PMODE register (0x04). When line loopback is enabled for a given port, all data received by the M2852x on that port is processed by the Receive Line Interface and transmitted out the line interface. Data from the Transmit UTOPIA bus is ignored.

NOTE: SPTxCk, SPRxCk, SPTxSync, and SPRxSync must be present for the loopback mode to function properly for a given port.

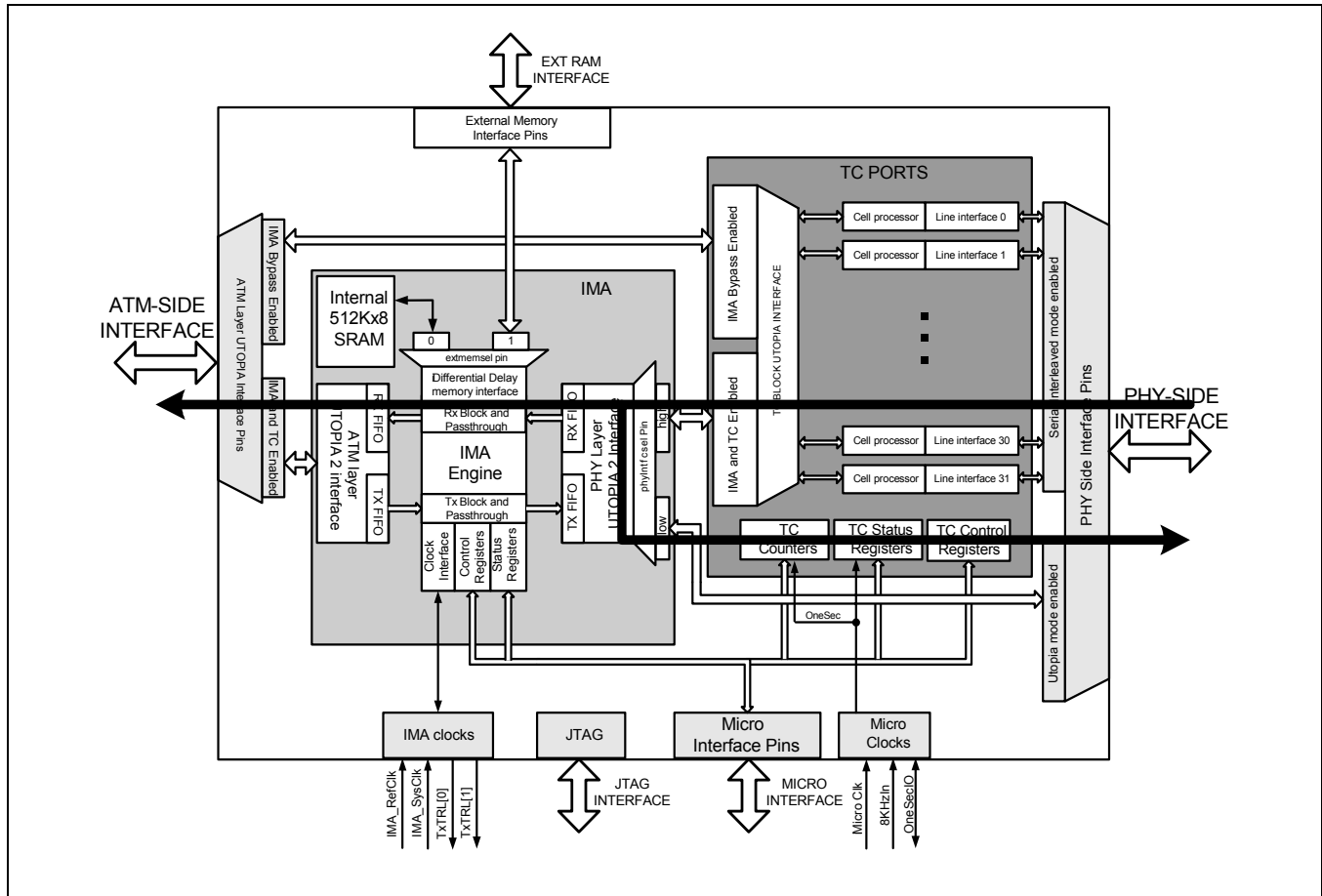
Figure 1-13. Far-End Line Loopback (This only shows the TC Block.)



1.9 IMA Line Loopback

IMA line loopback is provided as shown in Figure 1-14. This loopback occurs in the PHY layer UTOPIA interface of the IMA block. The loopback is functional both when the serial/interleaved (TC enabled) and when the PHY side UTOPIA interface (TC bypass) is selected. When this loopback is selected, incoming receive data continues through the IMA processor and is looped back out of the transmit interface.

Figure 1-14. IMA Line Loopback



1.10 IMA System Loopbacks

IMA system loopback is provided as shown in Figure 1-15. This loopback occurs in the PHY layer UTOPIA interface in the IMA block. When this loopback is selected, incoming transmit system data is looped back after IMA processing and continues out the PHY side interface. The loopback is functional regardless of which PHY side interface mode is selected. There are two different modes of system loopback, IMA System Loopback 0 and IMA System loopback 1.

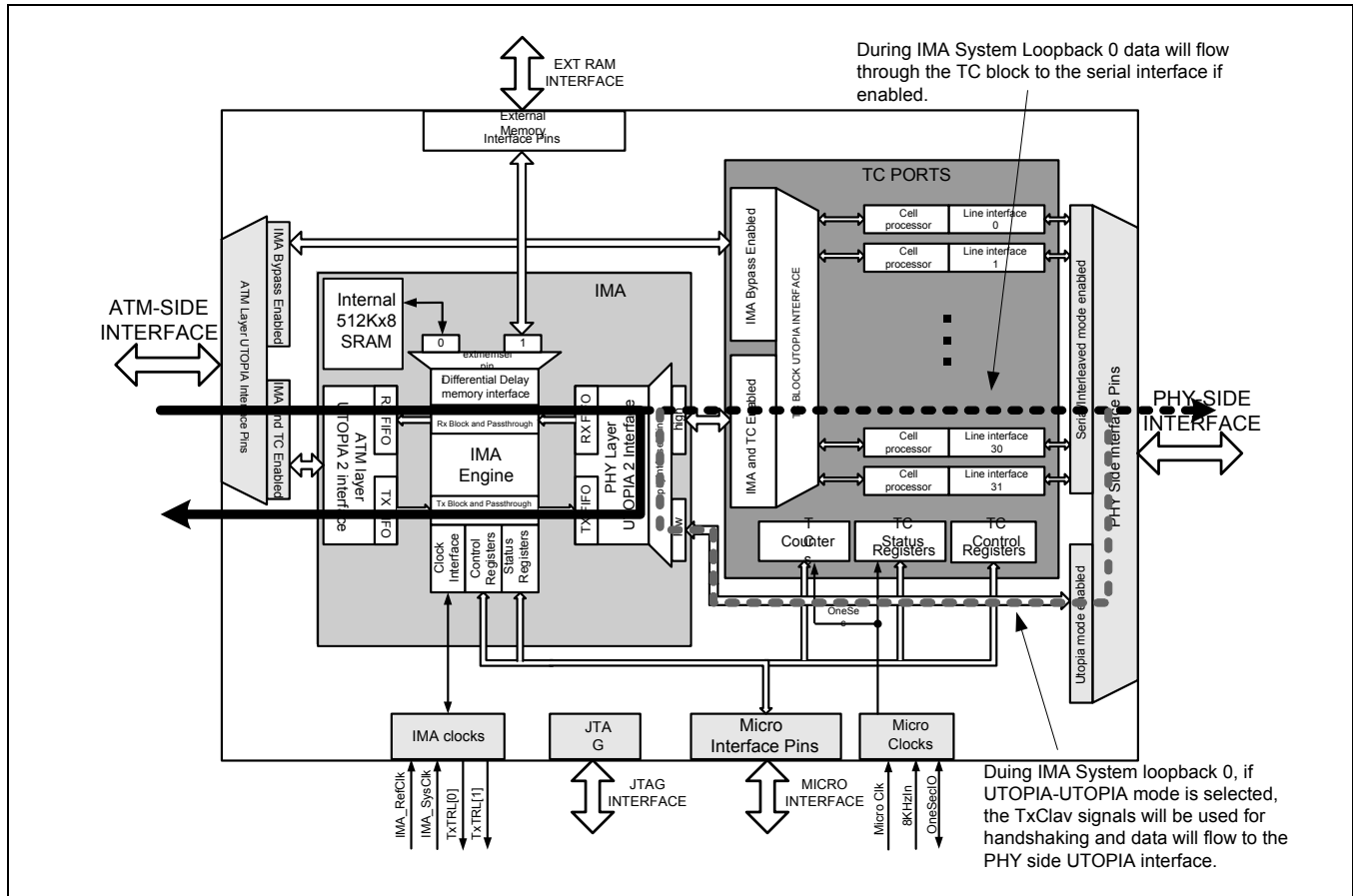
1.10.1 IMA System Loopback 0

During IMA System Loopback 0, data is looped back at the PHY Layer UL2 Interface. The TxClav signals from the PHY (TC or External) are used for handshaking and data is passed through the TC Block to the serial interface (if the TC block is enabled) or is routed to the PHY side UTOPIA Interface (if the TC block is disabled).

1.10.2 IMA System Loopback 1

During IMA System loopback 1, data is looped back at the PHY Layer UL2 Interface, but the TxCLAV signals are ignored from the PHY layer. Data is not passed through the TC Block during this mode.

Figure 1-15. IMA System Loopback



1.11 Reference Designs

Please contact Mindspeed for information on reference designs and schematic examples.

1.12 IMA Clocks

IMA frame rates must be locked to the PHY payload rates (the bandwidth reserved for ATM cells) used by those PHY ports designated as IMA timing reference links. This applies to both the Transmit and Receive directions. IMA frame rates can be derived from a number of sources:

- IMA_SysClk
 - Fixed Divide-By-24 or
 - Programmable divider
- IMA_RefClk

- Line rate clock input or
- Programmable divider
- SPRxCk or IHRxCk
 - PHY Line/Payload rate clock
- Rx PHY side cell stream
 - PHY payload rate derived (synthesized) from cell transfer rate across PHY side UTOPIA interface

It should be noted that the IMA frame rates can not be directly derived from the SPTxCk[31:0] inputs.

In a typical application (see Case 1 in [Table 1-18](#)), the Tx direction is referenced from local clock sources whereas the Rx direction is slaved to the FE Tx. It is also quite common (Case 2 in [Table 1-18](#)) for the Tx direction to be slaved to the FE Tx, often using the same source as the Rx direction. In some rarer applications, (Case 3 in [Table 1-18](#)) both the Tx and Rx directions are referenced from local clock sources.

Table 1-18. Reference Clock Configurations / Sources

| Case | Tx Direction | | Rx Direction | |
|------------------|-------------------|--|-------------------|---|
| | Configuration | Possible Sources | Configuration | Sources |
| 1 | Master / Internal | IMA_SysCk IMA_RefCk | Slave / External | SPRxCk or IHRxCk Rx Cell stream IMA_SysCk or IMA_RefCk ⁽¹⁾ |
| 2 | Slave / External | SPRxCk or IHRxCk Rx Cell stream IMA_SysCk or IMA_RefCk | Slave / External | SPRxCk or IHRxCk Rx Cell stream IMA_SysCk or IMA_RefCk |
| 3 ⁽²⁾ | Master / Internal | IMA_SysCk IMA_RefCk | Master / Internal | IMA_SysCk IMA_RefCk |

Footnotes:

(1) These sources provide a “last resort” clock in case no valid timing can be derived from Rx side sources.

(2) This case assumes the FE Tx is loop timed to the NE Tx; this will limit applications. It is also applicable in loopback testing.

Internally the IMA engine generates a Transmit Data Cell Rate clock (Tx IDCR) to match the exact cell rate of each group in the transmit side of the IMA device. The IMA engine also generates a Receive Data Cell Rate clock (Rx IDCR) to match receive cell rate for each group and operates the Receive Cell Smoothing buffer. There is a Tx IDCR and Rx IDCR for each of the 32 groups that the M28529 supports.

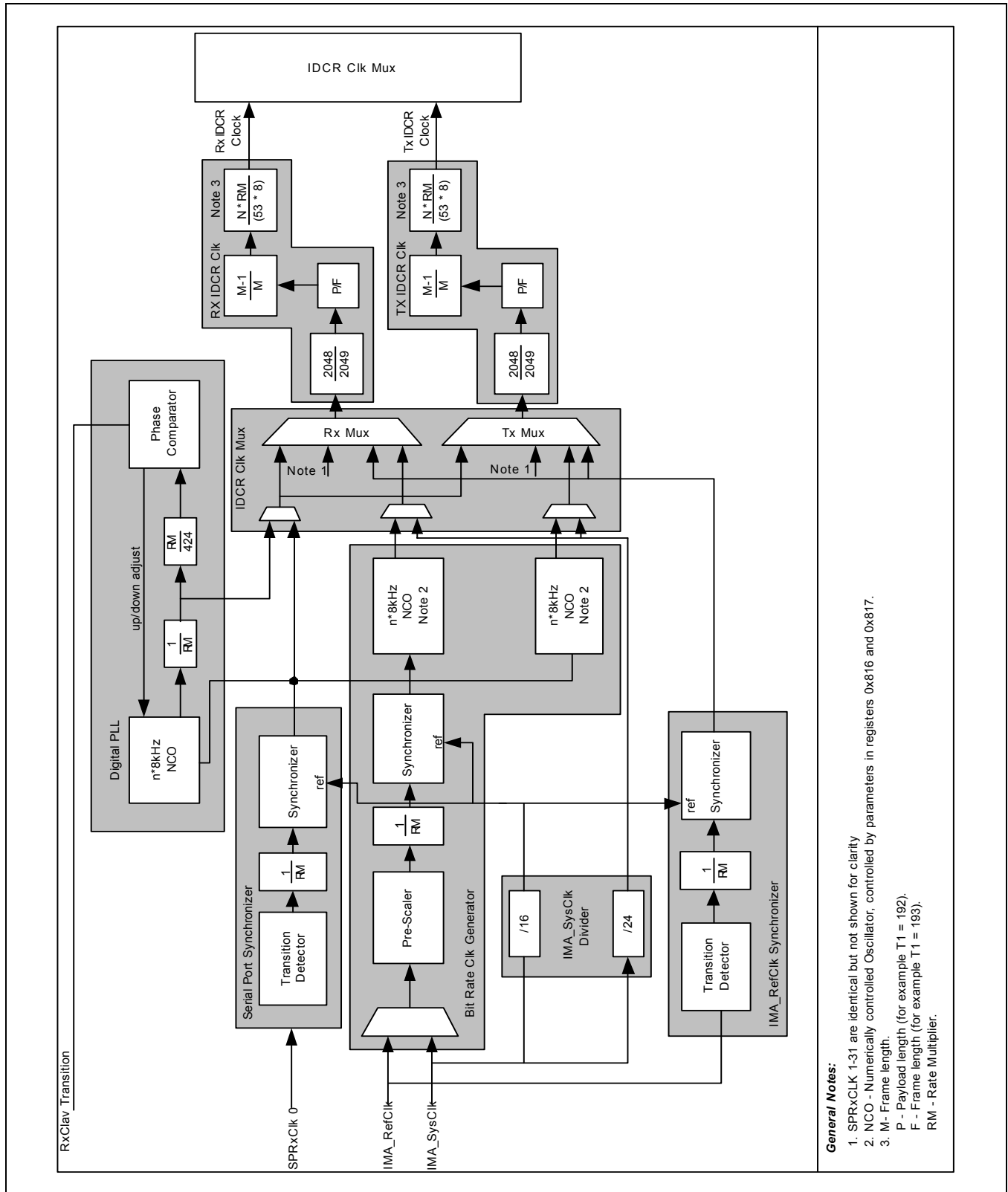
The M28529 also provides two clock outputs: Tx_TRL[1] and Tx_TRL[0]. These can be used to output one of the reference clock inputs or generate an 8 KHz reference that is phase locked to IMA_SysCk or IMA_RefCk (whichever is used as a timing reference).

[Figure 1-16](#) shows the details of the M28529's IMA clock block from [Figure 1-1](#). This block is responsible for generating all clocks required by the IMA engine. It can be further divided into 8 sections, as shown in [Table 1-19](#):

Table 1-19. IMA Block Clock Sections

| Clock Section | Description |
|---------------------------|--|
| Serial Port Synchronizer | This block contains a transition detector and a synchronizer. It synchronizes the clocks from the TC block Serial ports to the IMA_SysClk divided by 16 and the rate multiplier (RM). It handles all 32 internal serial ports independently. The rate multiplier is configured to values 1, 2, or 4 based on the range of the link rate. |
| IMA_SysClk Dividers | This block contains two dividers: a divide by 16, a divide by 24, and divide by rate multiplier (RM). The divide_16 is used to synchronize external clocks to internal logic. The divide_24 allows the IMA_SysClk to be used to generate both the Rx IDCR and the Tx IDCR clocks (provided that IMA_SysClk is 24 times the bit rate). |
| IMA_RefClk Synchronizer | This block contains a transition detector and a synchronizer. It synchronizes the IMA_RefClk to the IMA_SysClk divided by 16 and the RM factor. |
| IDCR Source Mux | This software controlled mux selects which clock sources are feed to the appropriate IDCR clock dividers. |
| Rx IDCR Clock | This block divides the bit rate clock down to a link cell data rate clock based on the values of frame length (M), number of links in the group (N), frame payload (P) and frame bit (F), then adjusts based on the rate multiplier (RM). (The 2048/2049 factor results from the IMA standards requirement of inserting a stuff event every 2048 cells.) This block can generate 16 independent Rx IDCR clock outputs (one per group). |
| Tx IDCR Clock | This block divides the bit rate clock down to a Link cell data rate clock based on the values of frame length (M), number of links in the group (N), frame payload (P) and frame bit (F), then adjusts based on the rate multiplier (RM). (The 2048/2049 factor results from the IMA standards requirement of inserting a stuff event every 2048 cells.) This block can generate 16 independent Rx IDCR clock outputs (one per group). |
| Bit Rate Clock Generator | <p>This block generates a clock that represents the link data rate. It can generate 16 independent Tx and 16 independent Rx clocks. In normal operation, all parameters are configured automatically by the software driver. It contains the following blocks:</p> <ul style="list-style-type: none"> • Pre-scaler—This block divides the selected input (either IMA_RefClk or IMA_SysClk) by the factor of Pnum divided by Pden. • Synchronizer—Synchronizes the Pre-Scaler output to the internal logic using the IMA_SysClk divided by 16 and the RM factor. • Numerically Controlled Oscillator—This clock circuit generates the link bit rate. |
| Digital Phase Locked Loop | This block generates a bit rate clock that is phase locked to the PHY side RxClAv signal. It can monitor all 32 ports on the bus. Any port can be selected as the group timing reference. |

Figure 1-16. M28529 Clock Diagram



General Notes:

- 1. SPRxCLK 1-31 are identical but not shown for clarity
- 2. NCO - Numerically controlled Oscillator, controlled by parameters in registers 0x816 and 0x817.
- 3. M- Frame length.
P - Payload length (for example T1 = 192).
F - Frame length (for example T1 = 193).
RM - Rate Multiplier.

1.12.1 IMA Link Rates

In addition to supporting standard T1/E1 bit rates, the M2852x devices support fractional T1/E1 and DSL rates from 64 kbps to more than 8.192 Mbps. The actual nominal link rate must be configured through software parameters. Section 1.12.2.2 discusses the input clock requirements. When operating the device with only a single link rate used for all IMA groups, any link rate within the specified range is possible. A reference clock synchronous with that link rate must be provided to the device.

For multi-rate applications, internal timing generators (includes the synthesizers) within the device must be supplied a reference clock with sufficient accuracy and resolution to generate the required bit rates. The following relationship between link rate and IMA_SysClk frequency exists:

Table 1-20. Link Rate Resolution for Variable Rate Applications (direct serial clock)

| | Link Rate < IMA_SysClk/16 | IMA_SysClk/16 < Link Rate < IMA_SysClk/8 | Link Rate > IMA_SysClk/8 |
|-----------|---------------------------|--|--------------------------|
| Link Rate | n x 8 kbps | n x 16 kbps | n x 32 kbps |

As an example, if IMA_SysClk is 49.152 MHz, the link rate boundaries occur at 3.072 Mbps and 6.144 Mbps. The maximum IMA link rate is given by IMA_SysClk/4, or 12.288 Mbps.

When using the internal bit rate clock generator, the resolution boundaries and maximum link rate are a function of the “intermediate” frequency (output of the Prescaler) selected. The “intermediate” frequency is a function of the frequency of the input reference clock (IMA_SysClk or IMA_RefClk) and the resolution of the prescaler (8 bits). This “intermediate” frequency (INT_FREQ) is limited to IMA_SysClk/16 due to internal synchronization. At this limit, the values of Table 1-21 apply. But it is also likely that the “intermediate” frequency will be lower than IMA_SysClk/16 and the following applies:

Table 1-21. Link Rate Resolution for Variable Rate Applications (internal bit rate generator)

| | Link Rate < INT_FREQ | INT_FREQ < Link Rate < INT_FREQ/2 | Link Rate > INT_FREQ/2 |
|-----------|----------------------|-----------------------------------|------------------------|
| Link Rate | n x 8 kbps | n x 16 kbps | n x 32 kbps |

Returning to the example of IMA_SysClk = 49.152 MHz, if INT_FREQ = 2.56 MHz, then the rate boundaries occur at 2.56 Mbps and 5.12 Mbps, with a maximum link rate of 10.24 Mbps.

1.12.2 Clock Input Requirements

The system designer must select the frequencies of IMA_SysClk and IMA_RefClk such that the IMA core can process the aggregate cell bandwidth (BW), sample the serial clocks, and the IMA frame rates can be derived.

1.12.2.1 Aggregate Cell Bandwidth

The maximum aggregate cell bandwidth requirement (rule of thumb) is a function of the frequency of IMA_SysClk and the number of active IMA groups. The following are empirically determined limits when operating with 1 or more IMA groups:

- 32 IMA groups:
 - Maximum Aggregate BW (Mbps) < Frequency of IMA_SysClk (MHz) * (20 / 9).
- 16 IMA groups
 - Maximum Aggregate BW (Mbps) < Frequency of IMA_SysClk (MHz) * (24 / 9).

- 1 IMA group
 - Maximum Aggregate BW (Mbps) < Frequency of IMA_SysClk (MHz) * (28 / 9).
- If only pass-throughs are enabled, then the aggregate cell bandwidth limitation is:
 - Maximum Aggregate BW (Mbps) < Frequency of IMA_SysClk (MHz) * (16 / 5)

Table 1-22 list some examples.

Table 1-22. Maximum Aggregate Bandwidth Examples

| IMA_SysClk | # ports | # groups | Maximum BW (Mbps) |
|------------|---------|----------|-------------------|
| 49.152 MHz | 1-32 | 0 | 157.3 |
| | 1-32 | 1 | 152.9 |
| | 1-32 | ≤ 16 | 131.1 |
| | 1-32 | ≤ 32 | 109.2 |
| 66 MHz | 1-32 | 0 | 211.2 |
| | 1-32 | 1 | 205.3 |
| | 1-32 | ≤ 16 | 176.0 |
| | 1-32 | ≤ 32 | 146.7 |

As an example, setting IMA_SysClk = 49.152 MHz constrains the Maximum Aggregate BW to be less than 152.9 Mbps for configurations with at least 1 IMA group. For a 32 port application, depending on the number of active IMA groups, this implies a maximum aggregate BW in the range of 109.2 - 152.9 Mbps with an average link BW in the range of 3.41 - 4.78 Mbps.

As another example, for a 16 port application, with 16 IMA groups, the average link BW would be limited to 8.192 Mbps (131.1 Mbps / 16). This average link rate would increase if less than 16 IMA groups were active.

1.12.2.2 Serial Clock Sampling

IMA_SysClk is also used to sample the serial receive clocks (SPRxClk) and IMA_RefClk. These sampled signals are used for IMA frame rate generation. When operating with the Interleaved Highway interface enabled, the 4x input clock (IHRxClk) is first divided by 4 before being distributed to the IMA block where it is sampled. If the serial interface is operating in fractional T1/E1 mode, either directly or using the Interleaved Highway interface, the resulting “gated” clock being routed over to the IMA core is not used.

The requirements of the SPRxClk, IHRxClk, and IMA_RefClk inputs are summarized below:

Table 1-23. IMA Serial Clock Requirements

| Interface | | Clock Period ⁽¹⁾ | | IMA Link Rate |
|--------------------------|-----------|-----------------------------|----------------|-----------------------------------|
| Signal | Mode | Maximum | Minimum | Maximum ⁽²⁾ |
| SPRxCk | T1/E1/DSL | 256 / IMA_SysCk | 4 / IMA_SysCk | Min (4 / IMA_SysCk, INT_FREQ / 4) |
| | FT1/FE1 | N/A | N/A | INT_FREQ / 4 |
| IHRxCk | T1/E1 | N/A, f = 8.192 MHz | | 1.920 Mbps |
| | FT1/FE1 | N/A | N/A | 2.048 Mbps |
| IMA_RefCk ⁽³⁾ | All | 256 / IMA_SysCk | 16 / IMA_SysCk | IMA_SysCk / 16 |

Footnotes:

- (1) Clock period is shown since the sampling circuit is sensitive to the interval between rising edges of the clock signal.
- (2) Limit is a function of whether bit rate generator is used. If not used, then IMA_SysCk caps the link rate. If used, the intermediate frequency (INT_FREQ) determines the maximum link rate with the requirement that $INT_FREQ \leq IMA_SysCk / 16$.
- (3) IMA_RefCk used as a line rate reference; In this case, IMA_RefCk is not used as a reference for the internal bit rate generator.

1.12.2.3 Clock Generator Reference

The internal clock generators and synthesizers operate in the IMA_SysCk domain but are referenced from either the IMA_SysCk or IMA_RefCk input. Due to internal synchronization circuitry, the following restriction applies to the IMA_RefCk input when it is used as a reference for these generators:

$$\text{Frequency of IMA_RefCk} > \text{Frequency of IMA_SysCk} / 16$$

1.12.3 Summary Examples

The preceding sections listed many constraints on the IMA_SysCk and IMA_RefCk inputs. [Table 1-24](#) provides some simplified (and conservative) examples for these two clock signals.

Table 1-24. IMA Reference Clock Summary Examples

| PHY Interface | | | IMA_SysClk | | IMA_RefClk | |
|---------------|--------|---------|---------------------|---|------------|---|
| Type | Mode | # Ports | Ref? ⁽¹⁾ | Requirements | Ref? | Requirements |
| T1/E1 | Serial | ≤ 32 | Yes | T1: 37.056 MHz E1: 49.152 MHz | Opt. | T1: 1.544 MHz E1: 2.048 MHz |
| | | | No | T1: ≥ 36.23 MHz (typical LIU) ⁽²⁾ E1: ≥ 48.06 MHz (typical LIU) | Yes | T1: 1.544 or 1.536 MHz ⁽³⁾ E1: 2.048 or 1.920 MHz |
| DSL | Serial | ≤ 24 | Yes | n x 8 kHz, ≥ 40.96 MHz ⁽⁴⁾ | N/A | |
| | | > 24 | | n x 8 kHz, ≥ 49.152 MHz | | |
| | | ≤ 24 | No | ≥ 40.96 MHz | Yes | n x 8 kHz, ≥ 4.64 MHz |
| | | > 24 | | ≥ 49.152 MHz | | |
| T1/E1/ DSL | UTOPIA | ≤ 24 | Yes | n x 8 kHz, ≥ 40.96 MHz | N/A | |
| | | > 24 | | n x 8 kHz, ≥ 49.152 MHz | | |
| | | ≤ 24 | No | ≥ 40.96 MHz | Yes | n x 8 kHz, ≥ 4.64 MHz |
| | | > 24 | | ≥ 49.152 MHz | | |

Footnotes:
 (1) Indicates whether the clock signal is used as a timing reference.
 (2) Frequency determined based on sampling SPRxCLK as described in [Section 1.12.2.2](#).
 (3) A line or payload rate clock signal may be used. A payload rate can only be used if all possible references (e.g., SPRxClk) are also payload rate clocks.
 (4) 40.96 MHz is selected as a minimum frequency for G.shdsl applications.

1.12.4 Typical Clock Configurations

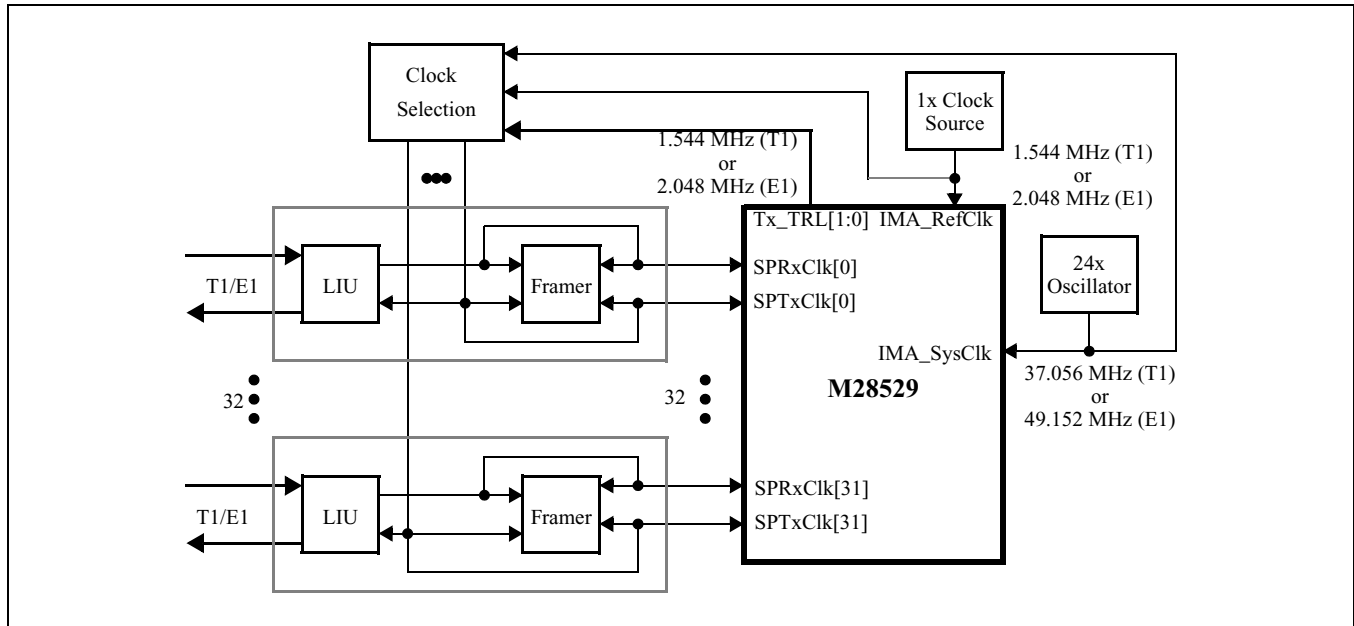
1.12.4.1 Serial Mode (using internal TC)

Figure 1-17 and Figure 1-18 show simplified applications that utilize the serial interfaces and internal TC block of the M28529 device. The block labeled “clock selection” in each figure may take on many forms depending on the clock configuration / sources and specific capabilities of the LIU and Framers devices used in a given system application.

1.12.4.1.1 T1/E1 Configurations

In the most common T1/E1 application (shown in Figure 1-17), T1/E1 line rate clocks and IMA_SysClk are used to provide timing references. The M28529 device has internal dividers that generate the proper PHY payload rates (1.536 Mbps / 1.920 Mbps) necessary for IMA frame generation. Since the line rate clocks are accessible within the M28529 device and all facilities operate at the same nominal rate, although they may be asynchronous, no programmable clock dividers or synthesizers tend to be used in these applications. Asynchronous facilities are allowed in Independent Transmit Clock (ITC) mode and are accommodated using the IMA stuffing mechanism.

Figure 1-17. Typical T1/E1 Configurations



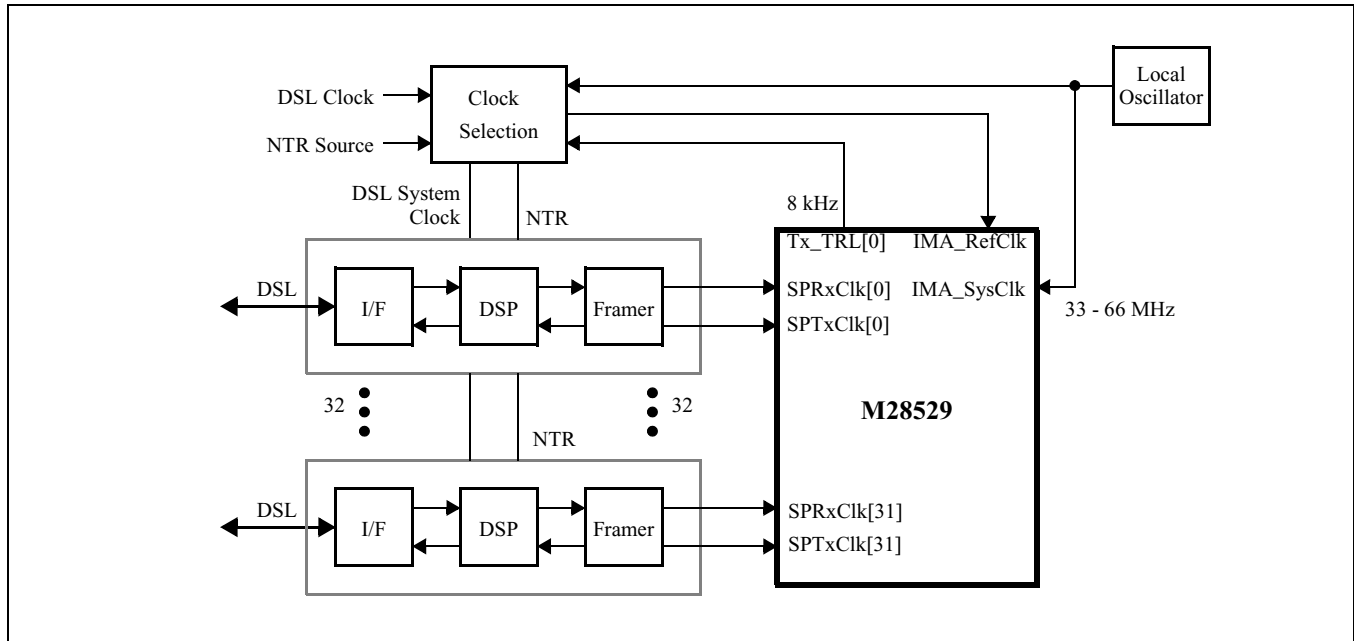
In the fractional T1/E1 application, the $n \times 64$ kbps link rates are usually supported by relying on the programmable dividers and clock synthesizers within the M28529 device rather than reliance on the serial clocks themselves. The clock reference for these dividers and synthesizers is either IMA_SysClk or IMA_RefClk. Whichever input is being used, it must be an integer multiple of 8 kHz. For IMA_SysClk, the same 24x frequency as shown in [Figure 1-17](#) can be used but any frequency in the range of 33 - 66 MHz is permissible, subject to the restrictions discussed in [Section 1.12.2](#).

1.12.4.1.2 DSL Configurations

The DSL application is similar to the fractional T1/E1 in the sense that the serial clocks are not often used directly as timing references. The link rates are usually set within the DSL transceiver as a programmable derivative of the “system clock” provided to that device. In some cases, an 8 kHz Network Timing Reference (NTR) signal affects the generated rate.

For the IMA frame rates to be locked when operating in the “Master / Internal” configuration, the M28529 and the DSL transceivers must have clocks that are derived from the same source. Often, this is a simple matter of connecting the DSL System Clock to the IMA_RefClk pin or using the IMA_SysClk signal as the source of the DSL System Clock. The “Slave / External” configuration usually relies on the clock synthesizers.

Figure 1-18. Serial DSL Configurations



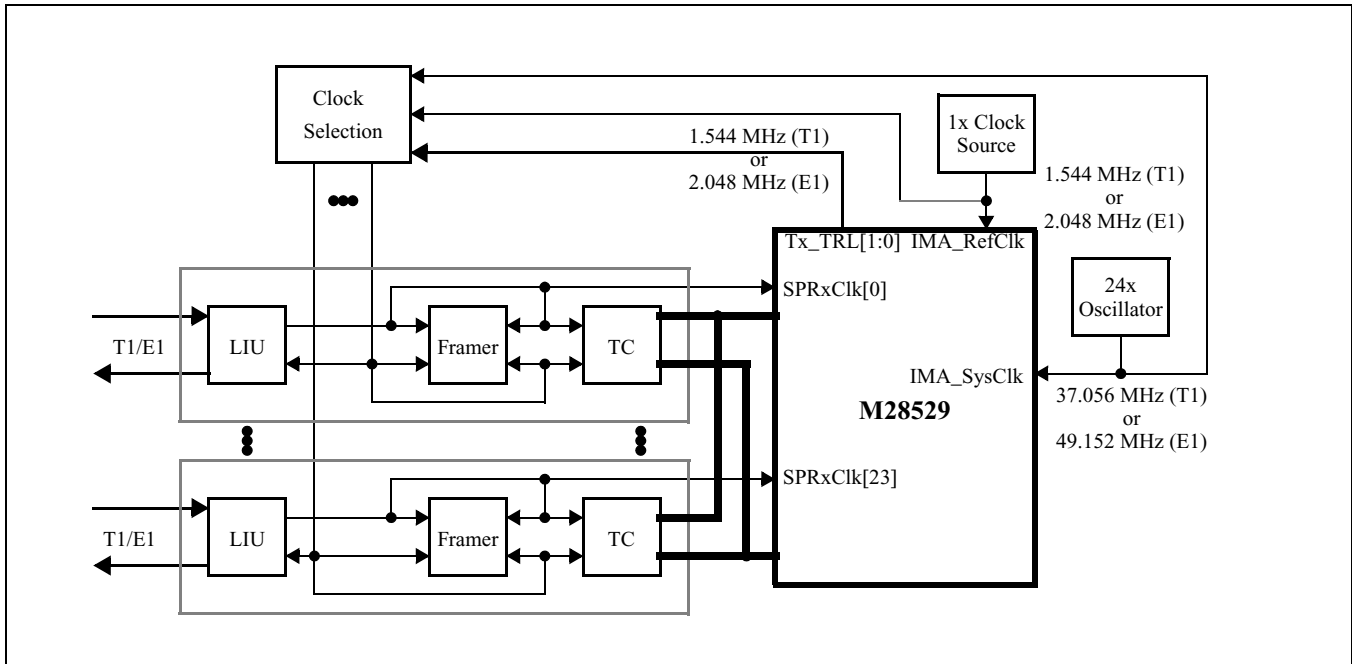
1.12.4.2 UTOPIA Mode

The UTOPIA mode applications are similar to the serial mode but the serial clocks are not typically used (or always available). In UTOPIA mode, the M28529 device only has the SPRxCIk[23:0] inputs available for those applications that can take advantage of them. As noted, these aren't typically used.

1.12.4.2.1 T1/E1 Configurations

The T1/E1 UTOPIA application is shown in Figure 1-19. It is similar to Figure 1-17 with the TC blocks external to the M28529 device. Since the device does not provide 32 serial clocks, the IMA function most often is configured to use its internal clock synthesizers when operating in the "Slave / External" configuration. This approach is used when operating in fractional T1/E1 applications.

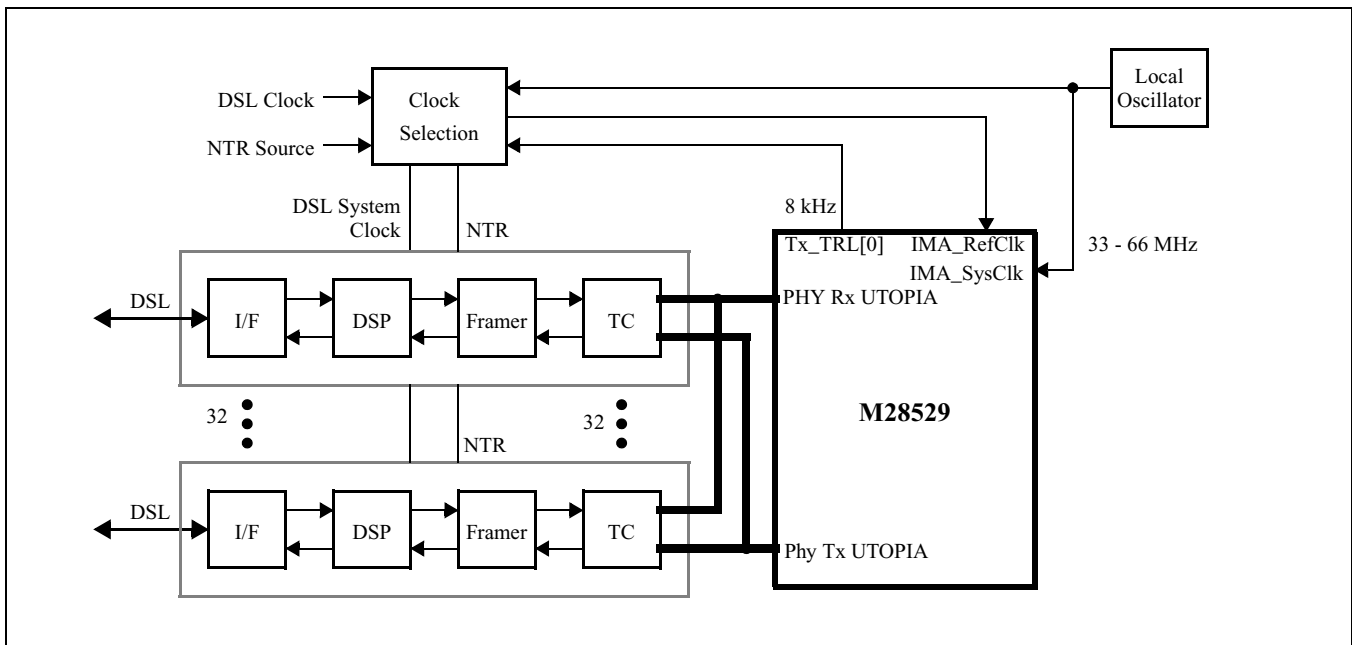
Figure 1-19. T1/E1 Configurations (UTOPIA Mode)



1.12.4.2.2 DSL Configurations

Since the serial clocks are not typically used as timing references when operating in DSL applications, the UTOPIA mode configurations are similar to the Serial mode configurations. Figure 1-20 shows the DSL UTOPIA application.

Figure 1-20. DSL Configurations (UTOPIA Mode)



The solution for high port count and variable rate DSL applications is to use internal counters and frequency synthesizers referenced from a common (n x y kHz) clock input with feedback from the cell available signal from the PHY side UTOPIA bus.

For low port count, single rate applications that take advantage of the embedded ATM Cell Processor, the use of receive bit clock inputs is the most straight-forward solution.

1.12.5 IMA Internal Timing Examples

1.12.5.1 T1/E1 Using Internal Serial Ports

1.12.5.1.1 Using IMA_SysClk as the Transmit Clock

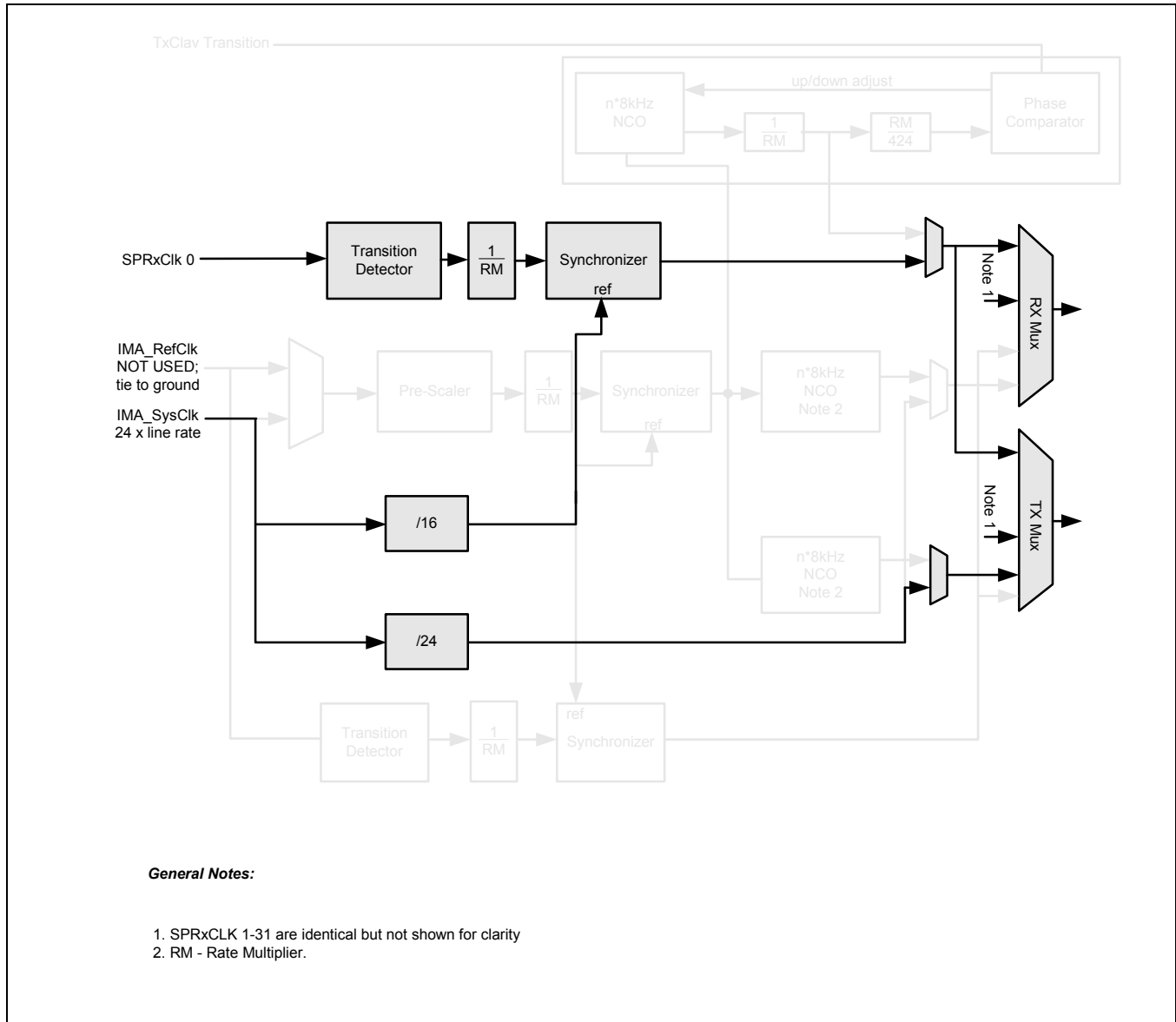
Figure 1-21 illustrates T1/E1 with internal serial ports, using IMA_SysClk equal to 24 times the line rate. This is one of the simplest implementations of IMA when a clock equal to 24 times the line rate is available. Several issues are worth noting:

- The IMA_RefClk input is unused and should be tied to ground. The M28529 is deriving all required clocks from the Serial port clocks and the IMA_SysClk.
- The IMA_SysClk is used to synchronize the SPRxClk inputs to internal logic (via the divide by 16 block).
- The SPRxClk is being used to generate the Rx IDCR clock. Also note that the receive clock from any link within a group could be used to generate the Rx IDCR for that group.
- The IMA_SysClk is being used to derive the TX IDCR clock.

The device is configured using a software driver. The following code is an example of calls to the driver:

```
IMA_LINK_TYPE = IMA_DS1
IMA_DSL_USE_REF_CLK2 = IMA_INACTIVE
IMA_DSL_REF_GENERATOR = IMA_INACTIVE
IMA_ALT_RX_TRL = IMA_INACTIVE
IMA_GRP_TX_TRL_SRC = IMA_REF_XCLK (grp#)
IMA_GRP_RX_TRL_SRC = IMA_RX_TRL_(x) (grp#)
```

Figure 1-21. T1/E1 using Internal Serial ports; IMA_SysClk equals 24x line rate



1.12.5.1.2 Using IMA_RefClk as the Transmit Clock

Figure 1-22 illustrates T1/E1 with internal serial ports, using IMA_RefClk. There are several important differences from the first example:

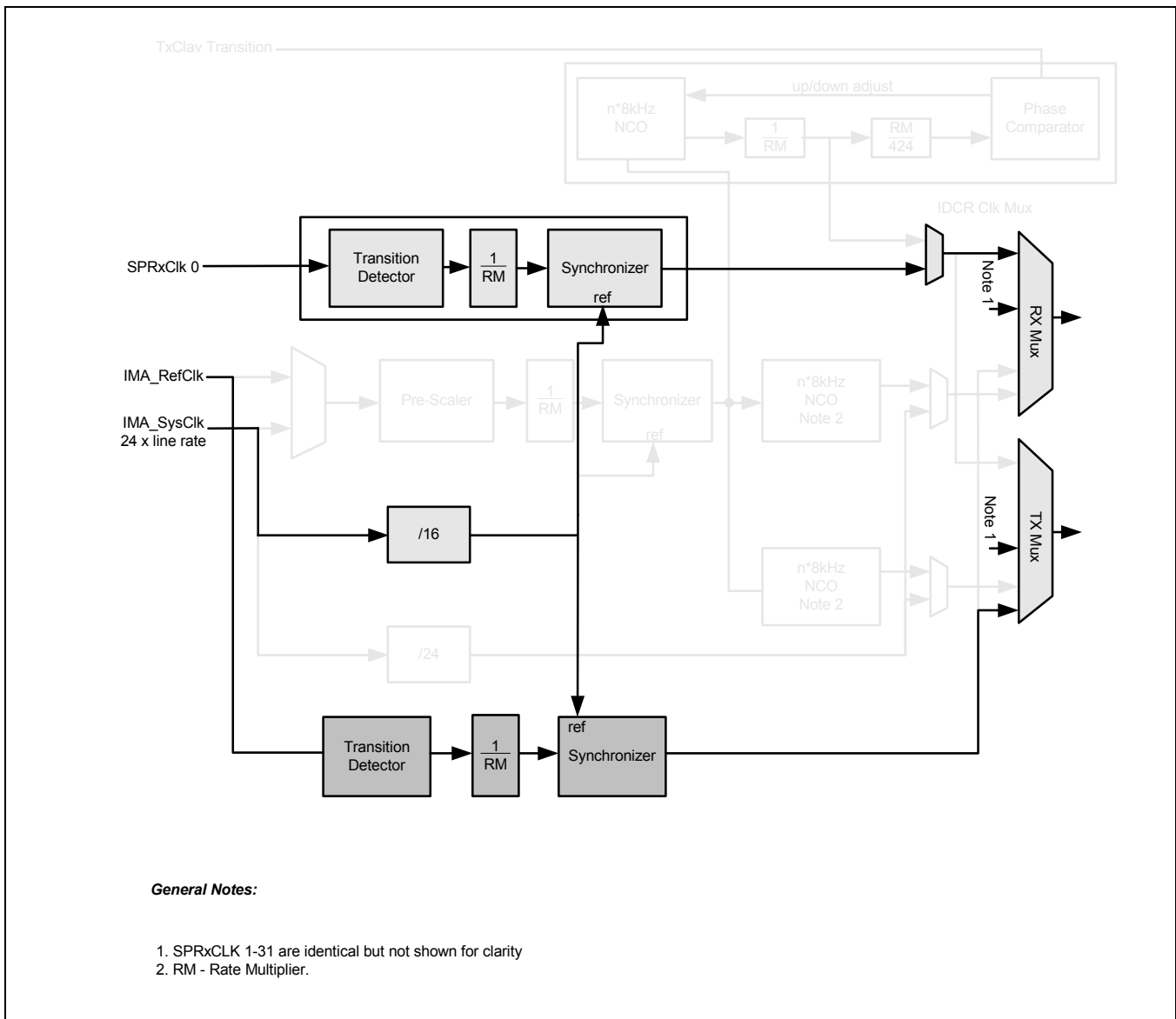
- In this case, IMA_SysClk is only used by internal logic. It must be greater than or equal to 22 times the line rate to ensure that internal logic can keep up with the data.
- Again, the SPRxClk is used to generate the RxIDCR clock.
- The TX IDCR clocks are generated from the IMA_RefClk. Thus IMA_RefClk must equal 1.544, 1.536, 2.028, or 1.920 MHz depending of the frame format used.

The device is configured using a software driver. The following code is an example of calls to the driver:


```

IMA_LINK_TYPE = IMA_DS1
IMA_DSL_USE_REF_CLK2 = IMA_INACTIVE
IMA_DSL_REF_GENERATOR = IMA_INACTIVE
IMA_ALT_RX_TRL = IMA_INACTIVE
IMA_GRP_TX_TRL_SRC = IMA_REF_CLK1 (grp#)
IMA_GRP_RX_TRL_SRC = IMA_RX_TRL_(x) (grp#)
    
```

Figure 1-22. T1/E1 using Internal Serial ports; IMA_RefClk equals line rate



1.12.5.2 DSL/T1/E1 Using UTOPIA-to-UTOPIA Interfaces

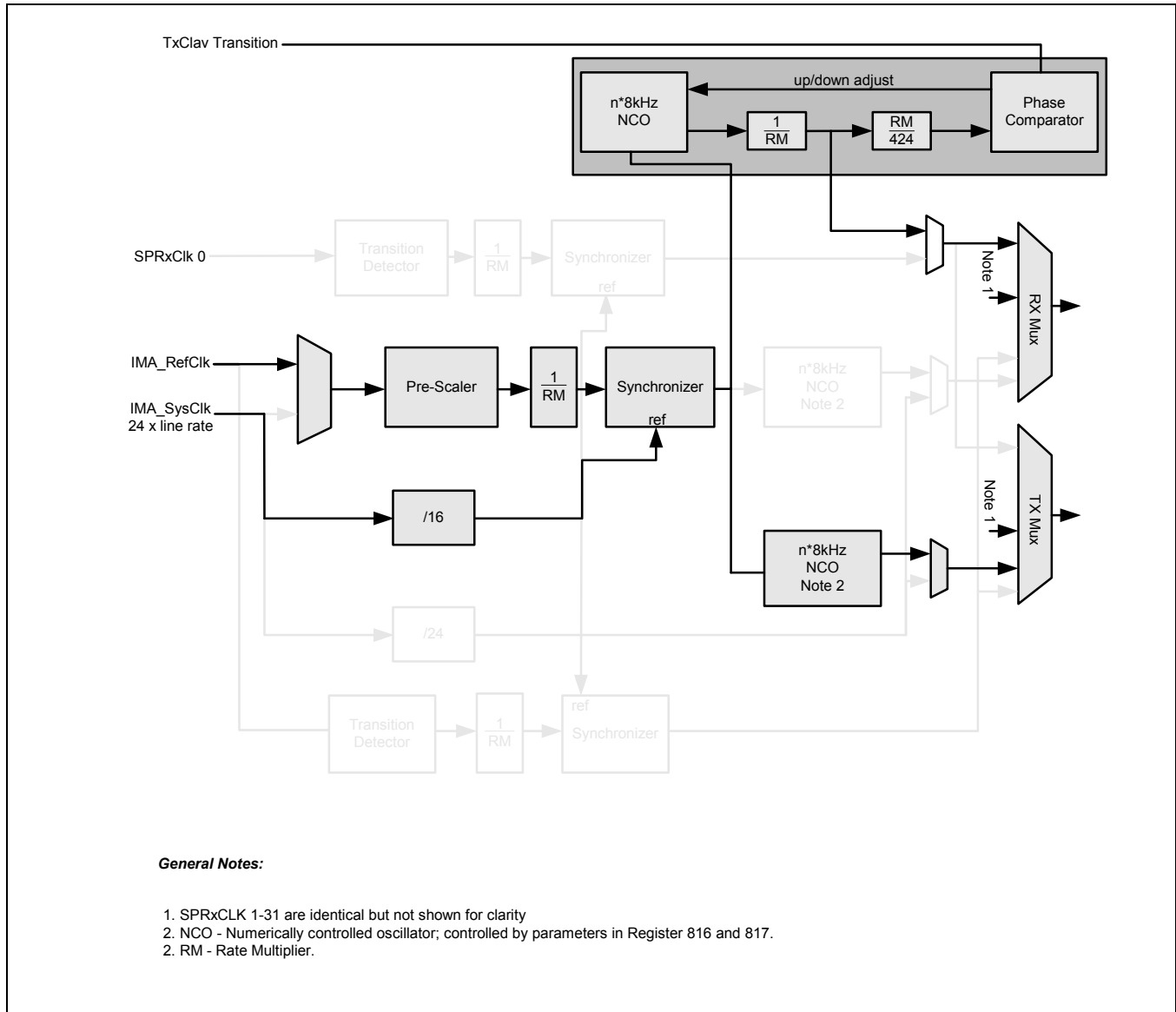
Figure 1-23 illustrates the configuration most commonly used with applications that require more the TC block to be external. Up to 32 links and 32 groups can be supported using external Cell Delineators. For the discussion below, assume the link rates are less than 3.072 Mbps.

- The Rx IDCR clock is synthesized using the RxClAv input from the PHY side UTPOIA bus. This is performed on a per group basis; that is, one link in each group is selected (via software) to provide the Rx IDCR for that group.
- IMA_SysClk must be greater than or equal to 40.96 MHz (less than 24 ports) and be greater than or equal to 49.152 MHz if there are more than 24 ports.
- Either IMA_SysClk or IMA_RefClk can be used as the Tx IDCR clock:
 - IMA_SysClk may be used if it is an 8 kHz multiple of the bit rate.
 - IMA_RefClk may be used if it is an 8 kHz multiple of the bit rate and greater than or equal to 4.64 MHz.

The device is configured using a software driver. The following code is an example of calls to the driver:

```
IMA_LINK_TYPE = IMA_VAR_RATE
IMA_DSL_REF_CLK_FREQUENCY = 40960000
IMA_DSL_USE_REF_CLK2 = IMA_INACTIVE
IMA_DSL_REF_GENERATOR = IMA_ACTIVE
IMA_ALT_RX_TRL = IMA_ACTIVE
IMA_GRP_LINK_BANDWIDTH = 2304 (grp#)
IMA_GRP_CLK_REF_FACTOR = IMA_NO_DIV (grp#)
IMA_GRP_TX_TRL_SRC = IMA_REF_XCLK (grp#)
IMA_GRP_RX_TRL_SRC = IMA_RX_TRL_(x) (grp#)
```

Figure 1-23. DSL—UTOPIA-to-UTOPIA



1.13 UTOPIA Interfaces

The M2852x supports multi-PHY operation as described in the UTOPIA Level specification (AF-PHY-0039.000, see www.atmforum.com). This standard allows up to 31 ports to be interfaced to both the ATM and PHY side interfaces. The interfaces use either 8-bit or 16-bit wide data buses, and cell-level handshaking.

Each of the M2852x's UTOPIA blocks have two sections, transmit and receive. For the ATM interface, on the transmit side, ATM cell data is placed in the transmit FIFOs where it can then be passed to the ATM cell processing block. On the receive side of the UTOPIA interface, incoming cells are placed in the receive FIFO until sent. Both FIFOs on the ATM side are 4 cells deep.

With regard to IMA, each IMA group is considered one logical port and will only take up one UTOPIA address. For example, a group with 8 T1 links could be assigned to address 0; the IMA engine handles the translation between the ATM layer and the physical links. In addition, each pass-through connection also requires one address.

NOTE: By convention, data being transferred from the PHY to the ATM layer is considered received data, while data from the ATM layer to the PHY is called transmitted data.

To provide maximum flexibility for system design the M28529 has 3 UTOPIA Level 2 interface modes. This allows the M28529 to be used in either UTOPIA-to-UTOPIA or UTOPIA-to-Serial IMA applications or it can function as a stand-alone cell delineator block. These interfaces are shown in [Figure 1-26](#) and described below.

1. IMA direct—This interface allows the ATM layer to interface directly to the IMA engine. This would be the normal mode for all IMA applications. It is controlled by registers in the IMA section.
2. TC block direct—This interface is selected when the IMA engine is disabled and the device is being used as a stand-alone cell delineator. It may also be invoked during troubleshooting to verify serial port operation without having to run the IMA drivers. It is configured by registers in the TC section.
3. PHY side UTOPIA—This interface is selected when the TC block is disabled and the designer wishes to interface to a device via an UTOPIA interface. This allows the M28529 IMA engine to address up to 32 ports on the line side.

1.13.1 General UTOPIA Operation

Three primary functions are performed by the UTOPIA controller: polling, selection, and data transfer. These functions are basically the same for both the transmit and receive sides of the UTOPIA bus. The following example describes the transmit functions. Refer to [Figure 1-24](#).

The ATM layer UTOPIA controller polls the connected PHY ports by transmitting the port addresses on the UTxAddr lines. If a port is ready to transfer data, it asserts UTxCIAv. Note that the process of polling a port does NOT result in that port being selected to transfer data! Polling allows the controller to determine which port is ready for data; it must then select that port before sending data. It does so by reasserting the desired address and then asserting UtxEnb*. The PHY will then be ready to transfer data on the UTxData lines. UtxEnb* is deasserted when the transfer is completed. Polling can continue during the data transfer process but not during port selection. It operates independently of the state of UtxEnb*.

To pause the data transfer, UtxEnb* can be deasserted. To continue the transfer, the controller must reselect the port by transmitting its address one clock cycle before asserting UtxEnb*. The controller must ensure that the cell transfer from this port has been completed, to avoid a start-of-cell error.

On the ATM side, the UTOPIA interface is a slave. On the PHY side, the UTOPIA interface is a master.

1.13.2 UTOPIA 8-bit and 16-bit Bus Widths (PHY and ATM)

The ATM side UTOPIA interface on the M2852x devices have two bus width options, 8-bit or 16-bit, depending on the selection of AtmBusWidth, bit 5, of the ATMINTFC register (0xF03). The PHY side UTOPIA interface also has two bus width options 8-bit or 16-bit, depending on the selection of PHYBusWidth, bit 5, of the PHYINTFC register (0xF02).

The protocols and timing are the same in both modes, except that 8-bit mode uses only the lower half of the data bus (TxData[7:0] and RxData[7:0]) and odd parity is only generated or checked over those bits. The ATM-Side UTOPIA Level 2 interface operates up to 50 MHz in 16 bit mode (Note: 33 MHz for TC Mode Only) and 33 MHz in 8 bit mode. The PHY-Side UTOPIA interface operates at half the IMA_Sysclk rate (IMA_SysClk/2)

In 8-bit mode, each ATM cell consists of 53 bytes. The first five bytes are used for header information. The remaining bytes are used for payload.

In 16-bit mode, the cell consists of 54 bytes. The first five bytes contain header information. The sixth byte, UDF2, is required to maintain alignment but is not read by the M2852x. The remaining bytes are used for payload.

1.13.3 UTOPIA Interface Blocks

1.13.3.1 IMA UTOPIA

This is the normal interface for IMA applications and is selected as shown in [Table 1-25](#).

It is intended to interface to a single ATM Layer device and appear as a multi-port PHY device. [Figure 1-24](#) illustrates the connections to/from the ATM Layer device. The number of “ports” or channels on the IMA Subsystem is the sum of the number of configured IMA groups plus the number of pass-through facilities. The IMA M28529 requires a unique UTOPIA address for each channel (IMA group or pass-through). There are no restrictions placed on the address assignment and not all 32 locations are normally used.

In IMA UTOPIA mode, the UTOPIA interface can operate with single Clav/Enb or Dual Clav/Enb handshaking. The default configuration is for single Clav/Enb handshaking (See register 0xF03 ATMINTFC for more information). When operated in single Clav/Enb mode, the UTOPIA bus address 0x1F can be configured as a valid port address and not a null address, note this is nonstandard from the UTOPIA specification and must be supported by connective devices.

When using dual Clav/Enb mode, Clav0/Enb0 are assigned to addresses 0x0 - 0xF while Clav1/Enb1 are assigned to addresses 0x10 - 0x1F. Note that only the first 4 bits[3:0] of the 5 bit address bus are used internally, bit 4 is ignored. For example, if Clav is supposed to be active for addresses 0x1 and 0x11, polling with address 0x1 on the address bus will cause Clav0 to be asserted and Clav1 to be asserted.

NOTE:

Dual Clav/Enb does not allow multiple M28529 devices to interface with a single ATM Layer device on the ATM-side UTOPIA Interface. Multiple M28529 devices cannot share one Utopia bus with an ATM-layer device.

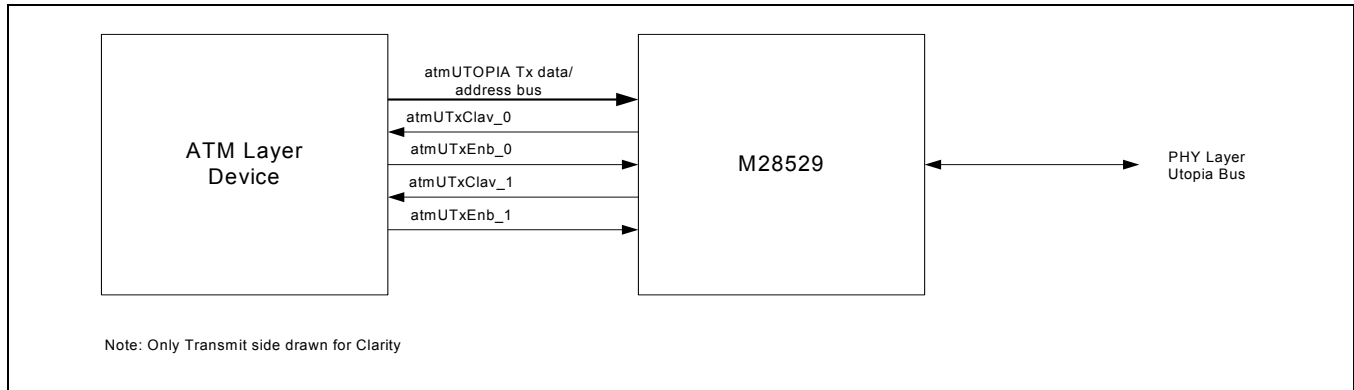
If only one channel is programmed, (a single IMA group and no pass-through facilities), then the M28529 can be compatible with UTOPIA Level 1 by fixing the address lines to a specific value and setting the IMA group's ATM address (through the software driver) to that value.

The M28529 provides numerous options to match non-standard UTOPIA controllers. See the IMA_ATM_UTOPIA_BUS_CTL register, 0x813, for more information.

NOTE:

In single Clav mode, address 0x1F can be assigned as a valid port address to enable 32 unique addresses.
The behavior of Clav when a port is not selected can be set to either driven low or tri-state. See the IMA_ATM_UTOPIA_BUS_CTL register, 0x813, bit 1.

Figure 1-24. ATM Layer UTOPIA Interface Connections



1.13.3.2 TC Block UTOPIA

This interface is selected when using the device as a stand-alone cell delineator. See Table 1-25 and Section 1.6. It interfaces to the ATM layer as a normal UTOPIA Level 2 interface with the following enhancements.

UDF2 Programmability

The user can program the contents of the UDF2 byte when operating in 16-bit UTOPIA mode. By default, the contents of the UDF2 byte on the receive interface will match the default value of the UTOPIA port address. This can be changed by writing the desired value to the corresponding UDF2 control register, 0x0F. Bus width is controlled by bit 5 of the ATMINTFC register.

Port Number Assignment

The UTOPIA address for each port is stored in bits 0–4 of the UTOP2 register (0x0E). The default for this value is the port number. For example, the UTOP2 register for port 4 (0x10E [with the offset]) defaults to 04 hex. However, the value can be changed to any value from 00–1E hex by programming the register to accommodate multiple devices on the same UTOPIA bus. The value 1F hex is reserved for the null address. The UTOPIA address should be changed only when the device or port is in the reset state.

HEC Override

In normal operation, the HEC is calculated by the TC layer and put in byte 5, UDF1. This may be overridden by setting bit 7 of the CGEN register (0x08) to a 1. In this case, data inserted by the ATM layer into byte 5 is transmitted unchanged by the device.

Table 1-25. Device Configuration Options

| ATMMux [7,6] (ATMINTFC, 0xF03) | PhyIntFcSel (Pin AD24) | Description |
|-----------------------------------|---------------------------|---|
| 01 | Low | IMA UTOPIA using the PHY Side UTOPIA; UTOPIA-to-UTOPIA; TC block/serial ports not used. |
| 01 | High | IMA UTOPIA using Internal TC block; UTOPIA-to-Serial mode; 32 internal serial ports |
| 10 | High | TC only; Device used as Stand-alone cell delineator with 32 serial ports; IMA block not used. |

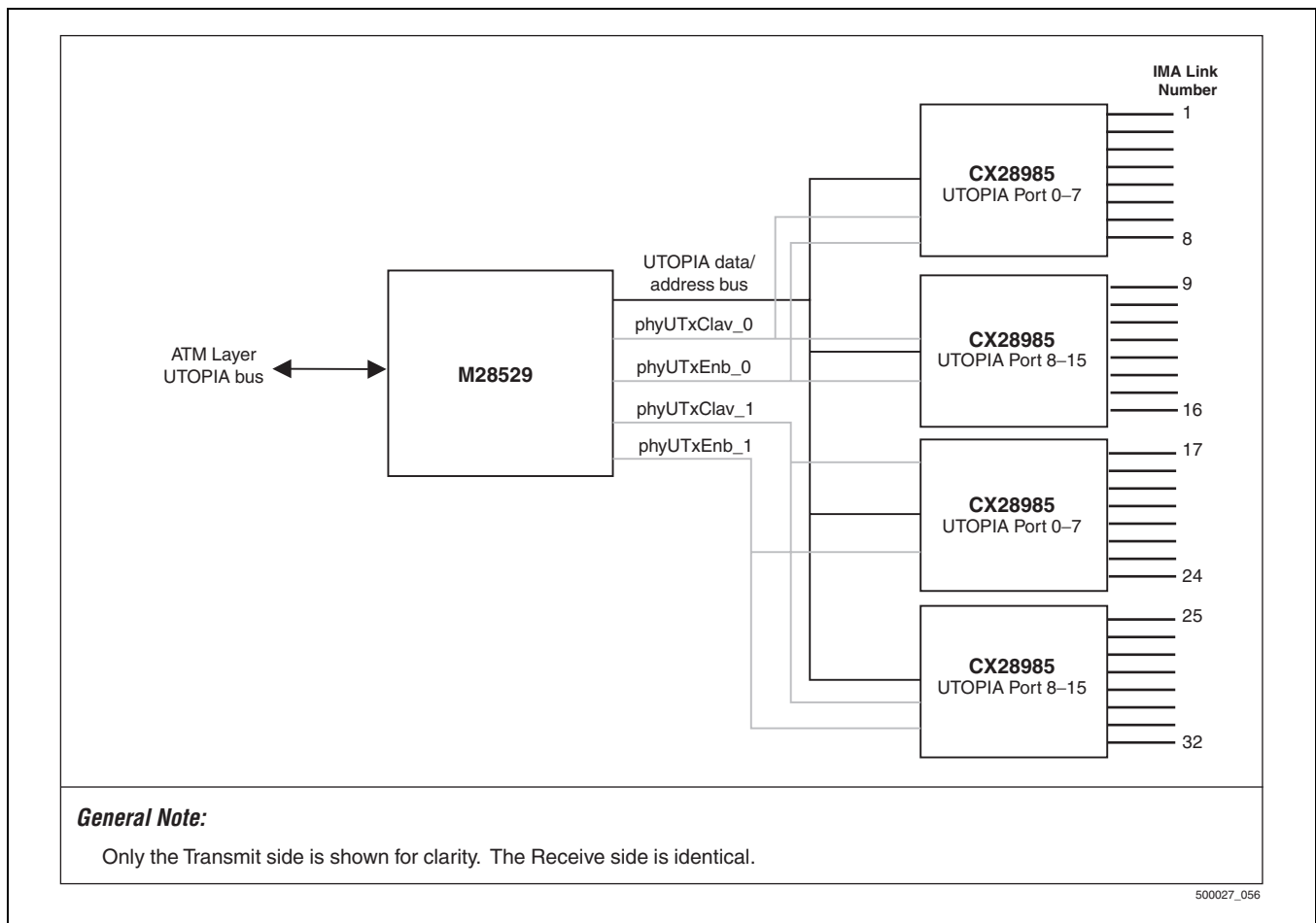
In TC Block UTOPIA mode, both Single and Dual Clav/Enb modes are supported, however the Single Clav/Enb mode only supports 31 addresses. UTOPIA address 0x1F is a null address. In dual Clav/Enb mode, the device can respond as 32 unique phy devices (by sharing the same address but using different Clav/Enb's), however address 0x1F is still a null address.

1.13.3.3 PHY-Side UTOPIA

An ATM forum compliant UTOPIA interface is provided for interfacing to PHY layer devices. Several unique features should be noted:

1. It is only UTOPIA level 2.
2. This bus supports 8-bit and 16-bit wide data paths.
3. The UTOPIA interface has a second set of control lines (Dual Clav/Enb), which allow up to 32 ATM devices to be connected to the bus. These can be connected as shown in [Figure 1-25](#). This effectively provides two buses with up to 16 devices each, all sharing common address and data lines but with separate control lines. (Remember, UTOPIA uses address 0x1F as the null address thus limiting the bus to 31 ports. However, the standard also allows for multiple Clav and Enable lines.)
4. When using only a single Clav/Enb the device can be programmed to recognize null address 0x1F as a valid address. Note that the TC block does not support 0x1F as an address. Thus when using the Utopia-Serial configuration, dual Clav/Enb must be used if 32 ports are desired.

Figure 1-25. M28529 Multiple UTOPIA Control Lines



1.13.4 Dual Clav/Enb Operation

The UTOPIA level 2 specification allows for 31 unique addresses 0-30 to be assigned to devices on the UTOPIA bus. UTOPIA address 31 is a Null address. While both the ATM and PHY side Utopia support the null address assigned as a valid address, many connecting devices may not support this. To alleviate this, the dual Clav/Enb mode is available to support all 32 ports. When using Dual Clav/Enb, the UTOPIA port will respond to either Clav0/Enb0 or Clav1/Enb1 depending on the port. For the ATM side, Clav0/Enb0 is assigned to port 0 - 15 and Clav1/Enb1 is assigned to port 16-32. Enabling of dual Clav/Enb mode for the ATM side is set in the ATMMINTFC 0xF03 register. For the PHY side, assignment of ports to Clav/Enb is configurable in the IMA_MISC_CONFIG register 0x804.

1.14 Transmission Convergence Block

The M2852x's ATM Transmission Convergence (TC) block is responsible for recovering cell alignment using the HEC octet, performing detection/correction, and descrambling the payload octets. The resulting ATM cells are then passed to the ATM layer via the UTOPIA interface. Simultaneously, the ATM transmitter block is receiving data from the ATM layer, optionally inserting header fields, optionally calculating the HEC, and sending the cells to the framers. If no data is being received from the ATM layer, the cell processor generates idle cells based on the data programmed into the associated registers.

NOTE: When operating in the UTOPIA-to-UTOPIA mode, the ATM Cell processor block is disabled.

1.14.1 ATM Cell Transmitter

The ATM cell transmitter controls the generation and formatting of 53-octet ATM cells that are sent to the Framer (Line) Transmit Ports. This block formats an octet stream containing ATM data cells from the ATM layer device when those cells are available. All 53 octets of the data cells may be obtained from the external data source and formatted into the outgoing octet stream.

This block calculates the HEC octet in the outgoing cell from the header field. The calculated HEC octet can be inserted in place of the incoming data octet by writing DisHEC (bit 7) in the CGEN register (0x08) to a logic 0. For testing purposes, this HEC octet can be corrupted by XORing the calculated value with a specific error pattern input set in the ERRPAT register (0x0B). This HEC error is achieved by writing ErrHEC (bit 4) in the CGEN register (0x08) to a logic 1. The remaining 48-octet payload field of the outgoing cell is obtained from the external data source. The payload can be scrambled.

When there is no data from the ATM layer device, the TC Block inserts idle cells automatically in the outgoing octet stream. The 4-octet header field for these idle cells comes from the TXIDL1–4 registers (0x14–17). The HEC octet is calculated and inserted automatically. The payload field is filled with the octet contained in the IDLPAY register (0x0A).

In normal operation, the 4-octet header field in the outgoing cell is passed on from the ATM layer device. Header patterns can be modified in the TXHDR1–4 registers (0x10–13) and inserted into outgoing cells in place of header bytes received from the ATM layer. Whether the original header cells or replacement cells are sent is controlled by bits 0–4 in the HDRFIELD (0x09) register.

1.14.1.1 HEC Generation

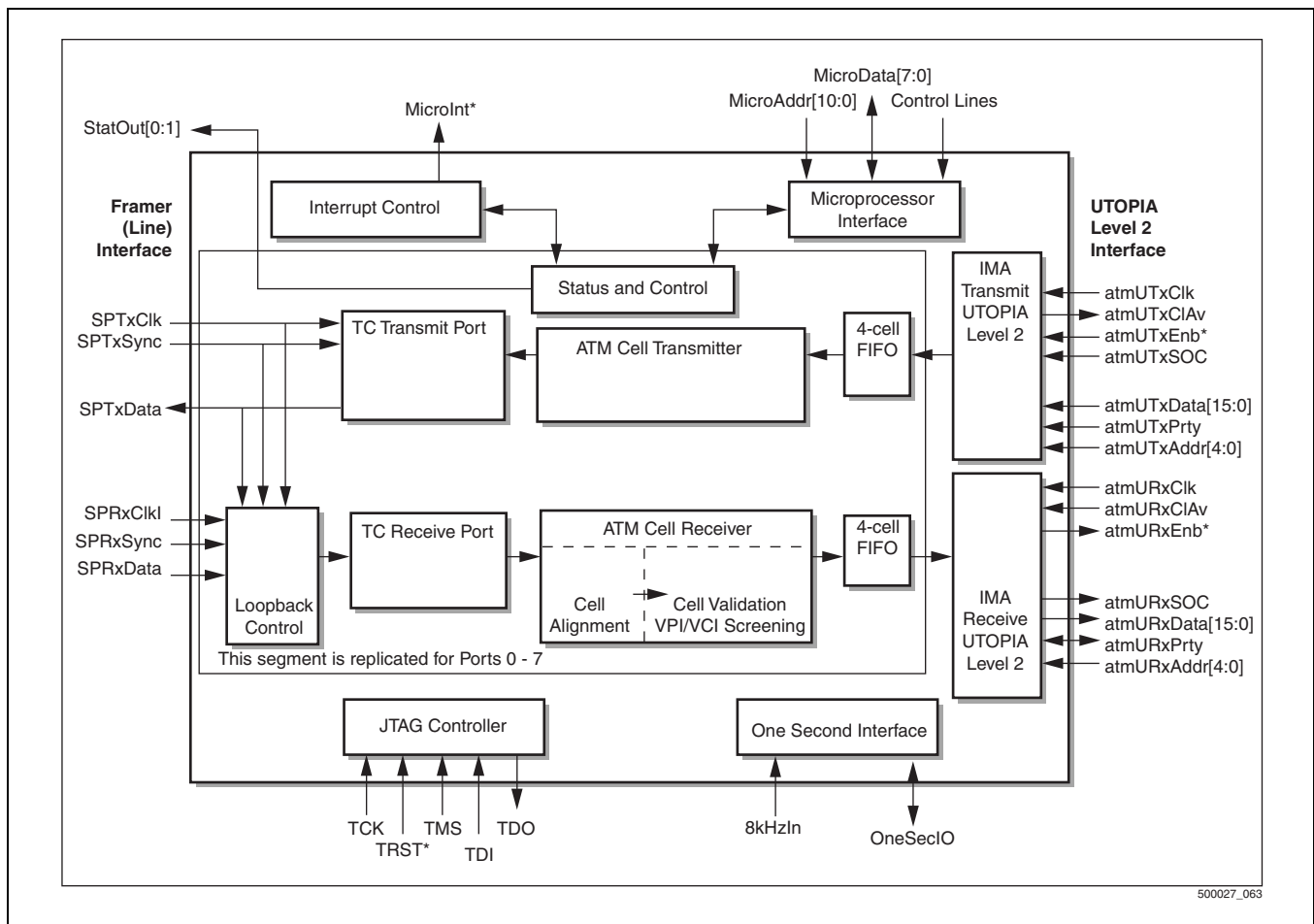
In normal operation, the M2852x calculates the HEC for the four header bytes of each cell coming from the ATM layer. It then adds the HEC coset (55 hex, by ATM standards) and inserts the result in octet 5 of the outgoing cell. HEC calculation can be disabled by setting bit 7 of CGEN (0x08) to a 1. When HEC is disabled, the M2852x leaves the contents of the HEC field unchanged and transmits whatever data is placed in that field by the ATM layer.

The HEC coset is used to maintain a value other than zero in the HEC field. If the first four bytes in the header are zero, the HEC derived from these bytes is also zero. When this occurs and there are strings of zeros in the data, the receiver cannot determine cell boundaries. Therefore, it is recommended that the value 55 hex be added to the HEC before transmission. To enable the HEC coset on the transmit side, set bit 6 in register CGEN (0x08) to one. To enable the receive HEC coset, set bit 5 in register CVAL (0x0C) to one.

1.14.2 ATM Cell Receiver

The ATM cell receiver performs cell delineation on incoming data cells by searching for the position of a valid HEC field within the cell. The HEC coset can be either active or inactive; this is determined in bit 5 in the CVAL (0x0C) register.

Figure 1-26. Details of the TC Block

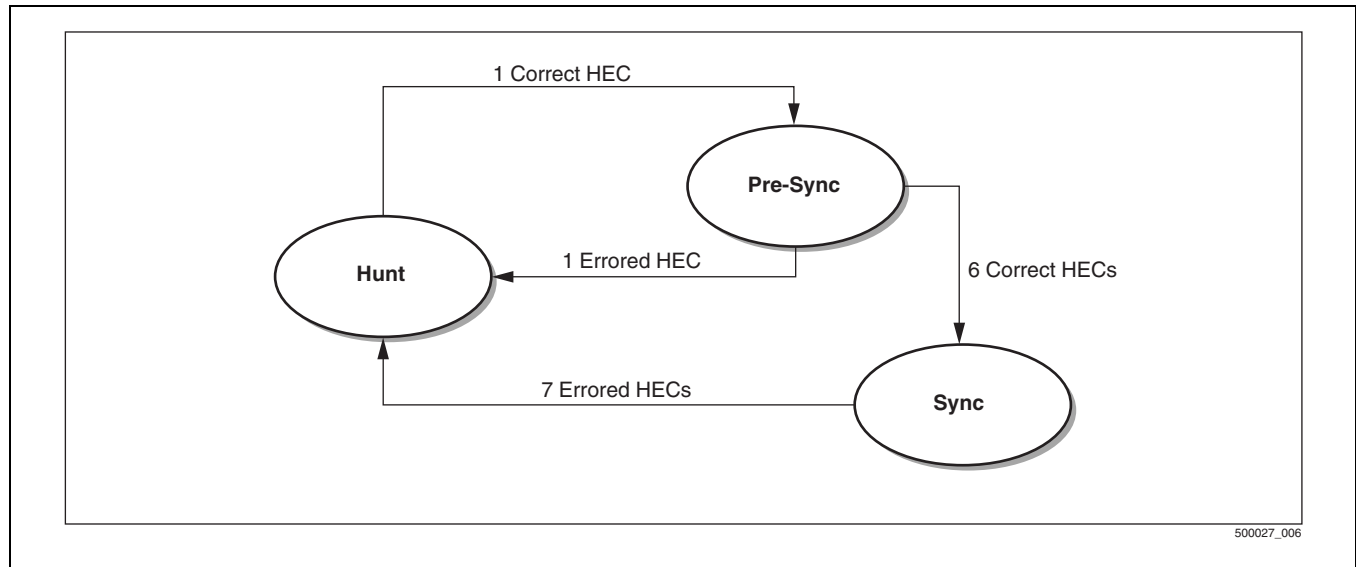


1.14.2.1 Cell Delineation

The ATM block receives octets from the framers and recovers ATM cells by means of cell delineation. Cell delineation is achieved by aligning ATM cell boundaries using the HEC algorithm. Four consecutive bytes are chosen and the HEC value is calculated. The result is compared with the value of the following byte. This "hunt" is continued by shifting this four-byte window, one byte at a time, until the calculated HEC value equals the received HEC value. When this occurs, a pre-sync state is declared and the next 48 bytes are assumed to be payload. The ATM block calculates HEC on the four bytes following this payload, assuming that a new cell has begun. If seven

consecutive header blocks are found, synchronization is declared. If any HEC calculation fails in the pre-sync state, the process begins again (see [Figure 1-27](#)). Synchronization will be held until seven consecutive incorrect HECs are received. At this time, the “hunt” state is reinitiated.

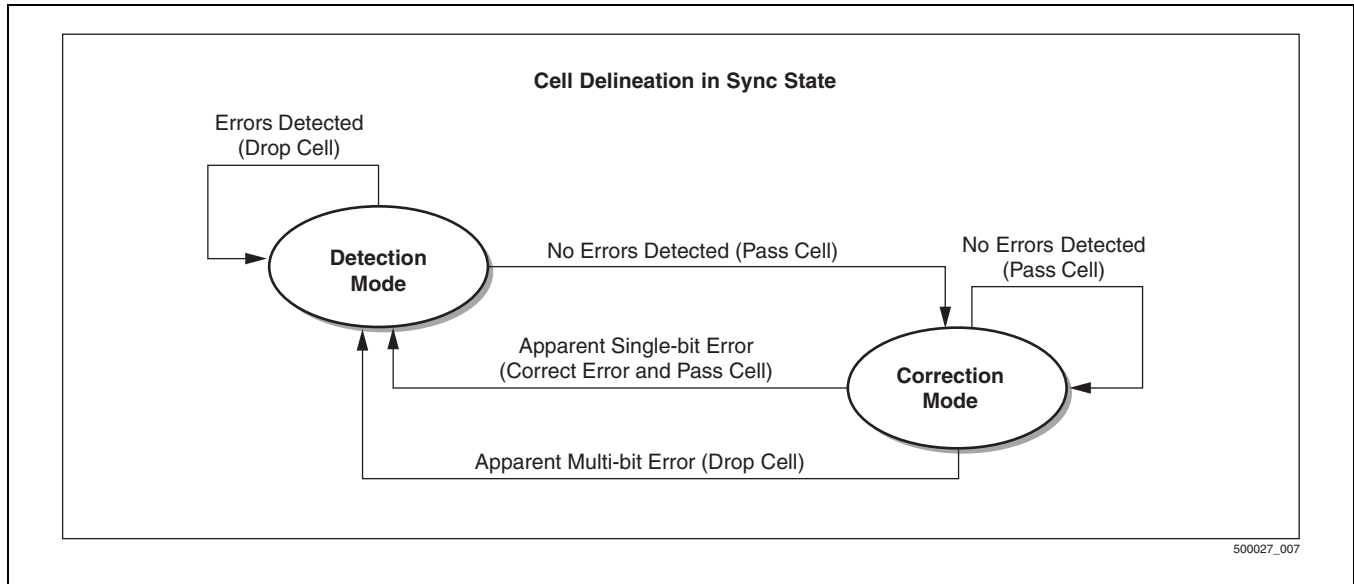
Figure 1-27. Cell Delineation Process



During the sync state of cell delineation, cells are passed to the UTOPIA interface if the HEC is valid. If a single-bit error in the header is detected, the error is corrected (optionally), and the cell is passed to the UTOPIA interface. If HEC checking is enabled and HEC correcting is disabled (bit 3 in the CVAL register [0x0C]), cells with single-bit HEC errors are discarded. If a multi-bit error is detected, the cell is dropped. Once either type of error is noted, all subsequent errored cells are dropped until a valid cell is received. This rule applies even for single-bit errors that could be corrected. Once a valid cell is detected, the process begins again. (See [Figure 1-28](#).)

When loss-of-cell delineation (LOCD) occurs, an interrupt is generated and the M2852x automatically enters the “hunt” mode. However, the cell is still being scrambled by the far-end transmitter, leaving only the headers (or just the HEC byte in Distributed Sample Scrambler [DSS]) unscrambled. This means that the only repetitive byte patterns in the data stream that meet the cell delineation criteria are valid headers (or just the HEC bytes in DSS).

Figure 1-28. Header Error Check Process



When the M2852x is in general purpose mode, a synchronization pulse from the framer interface is not always available. In this mode, the M2852x performs a bit serial search to find byte and cell alignment. The M2852x selects a starting window of 32 sequential bits and calculates the HEC over this window. This HEC is then compared to the next eight incoming bits. If they do not match, the M2852x shifts the 32-bit window by 1 bit and recalculates the HEC until a valid HEC position is found. Once byte-alignment is achieved, cell delineation is performed.

1.14.2.2 Cell Delineation Control Modes

The M28529 contains two independent “HEC Check” state machines. The Cell Delineator (CD) State Machine is used to find Cell Delineation and, conversely, to declare loss of cell delineation (LOCD). The other is the Cell Valid (CV) State Machine, which is used to validate the cells to pass to the UTOPIA FIFOs.

These state machines are controlled by two register bits, (CVAL register, 0x0C), that allow the M28529 to be programmed for special applications. [Table 1-26](#) shows the control bits function.

Table 1-26. Control Bit Functions

| DisLOCD | DisHECChk | Description |
|--|-----------|---|
| 0 | 0 | Normal operation; used for standard ATM traffic. Cells are output to the UTOPIA FIFO only after cell delineation is found. Only cells with valid HECs are passed (this includes cells with single bit errors that have been corrected). |
| 0 | 1 | Ignore HEC Errors Mode; used for IMA applications. The Cell Delineator state machine is active and looking for valid ATM cells. It will follow the ATM Forum's Cell Delineation process. However, since the Cell Valid State machine is turned off, the M28529 will pass all cells, including those with HEC errors, to the UTOPIA FIFOs. The M28529 will not transfer cells during LOCD. |
| 1 | 0 | The cell delineation function is disabled and every 53 bytes of incoming data is treated as a 'cell'. However, since the CV machine is still active, only cells with valid HECs will be output. As a result, almost all data will be dropped. Occasionally, random data will have what appears to be a valid HEC and will be output. Mindspeed is not aware of any use for this mode. |
| 1 | 1 | Raw Data mode; allows the M28529 to be used as a generic 'serial to parallel' convertor. All data received will be passed across the UTOPIA bus in blocks of 53 bytes. No attempt is made to find ATM cells. |
| General Note: 1. The HEC Error Correction circuit is independent of the DisHECChk control bit. The M28529 will correct single bit errors even when the DisHECChk is enabled (assuming that the EnHECCor bit is set to 1). | | |

1.14.2.3 Cell Screening

The M2852x provides two optional types of cell screening. The first type, idle cell rejection, prevents idle cells from being passed on. The second type, user traffic screening, compares incoming bits to the values in the receive cell header registers. Cells are rejected or accepted based on the bit patterns of their headers.

Idle cell rejection is enabled in bit 6 of the CVAL register (0x0C). If this bit is set to 1, all incoming cells that match the contents of the Receive Idle Cell Header Control Registers, RXIDL1–4 (0x20–23), are rejected. Individual bits in the Receive Idle Cell Mask Control Registers, IDLMSK1–4 (0x24–27), can be set to 1 or Don't Care, causing the corresponding bits of the incoming cell to be treated as matching, regardless of their value. If idle cell rejection is disabled, cells pass directly to user traffic screening.

User traffic cell screening is similar to idle cell screening in that the incoming cells are compared to the Receive Cell Header Control Registers, RXHDR1–4 (0x18–1B). Individual bits in the Receive Cell Mask Control Registers, RXMSK1–4 (0x1C–1F), can be set to 1 or Don't Care, causing the corresponding bits of the incoming cell to be treated as matching, regardless of their values. The RejHdr bit (bit 7) in the CVAL register (0x0C) determines whether matching cells are rejected or accepted. If it is set to 0, matching cells are accepted. If it is set to 1, matching cells are rejected. See [Table 1-27](#) and [Table 1-28](#).

Table 1-27. Cell Screening—Matching

| Receive Cell Mask Bit | Receive Cell Header Bit | Incoming Bit | Result |
|-----------------------|-------------------------|--------------|--------|
| 0 | 0 | 0 | Match |
| 0 | 0 | 1 | Fail |
| 0 | 1 | 0 | Fail |
| 0 | 1 | 1 | Match |
| 1 | x | x | Match |

Table 1-28. Cell Screening—Accept/Reject Cell

| Cell | Reject Header | Result |
|-------|---------------|-------------|
| Match | 0 | Accept Cell |
| Match | 1 | Reject Cell |
| Fail | 0 | Reject Cell |
| Fail | 1 | Accept Cell |

1.14.2.4 Cell Scrambler

The ATM standard requires cell scrambling to ensure that only valid headers are found in the cell delineation process. Scrambling randomizes any repeated patterns or other data strings that could be mistaken for valid headers. The M2852x supports two types of scrambling as defined by ITU-T I.432:

1. Self Synchronizing Scrambler (SSS)
2. Distributed Sample Scrambler (DSS). Typically, SSS is used and is, therefore, the M2852x’s default method. However, xDSL in asynchronous format generally use DSS.

NOTE: If both SSS and DSS are enabled, SSS overrides DSS.

1.14.2.4.1 SSS Scrambling

SSS scrambling uses the polynomial $x^{43} + 1$ to scramble the payload, leaving the five header bytes untouched. It can be enabled in EnTxCellScr, bit 5, of the CGEN register (0x08).

Descrambling uses the same polynomial to recover the 48-byte cell payload. It can be enabled in EnRxCellScr, bit 4, of the CVAL register (0x0C).

1.14.2.4.2 DSS Scrambling

DSS scrambling uses the $x^{31} + x^{28} + 1$ polynomial to scramble the entire cell, except the HEC byte. HEC is calculated after the first four bytes of the header have been scrambled. DSS scrambling is enabled in EnTxDSSScr, bit 1, of the CGEN register (0x08).

Descrambling uses the first six bits of the HEC for alignment. Once alignment is found, all eight bits of the HEC are sampled. Descrambling uses the same polynomial to recover the 48-byte cell payload. It is enabled in EnRxDSSScr, bit 0, of the CGEN register (0x08). If DSS descrambling fails, the M2852x defaults to unscrambled mode.

NOTE: DSS Scrambling is only supported in General Purpose Mode.

1.14.2.5 Framing Modes (UTOPIA-to-Serial Configuration)

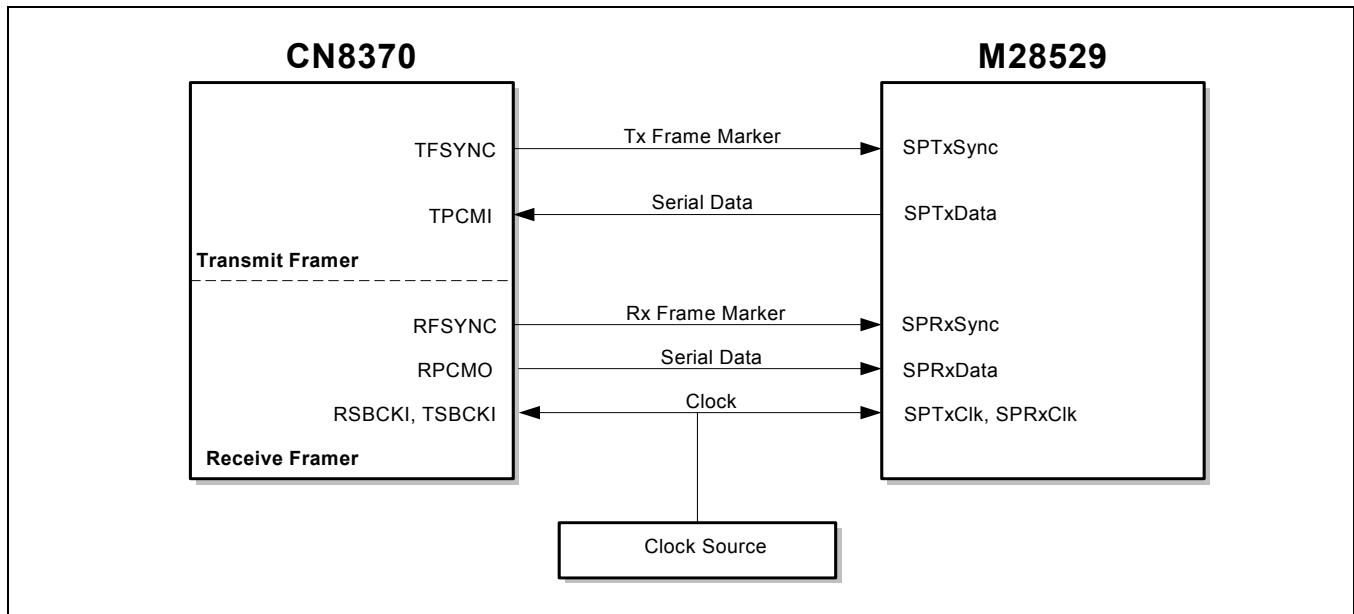
The M2852x’s 32 serial ports can be individually configured for the major framing modes: T1/E1, fractional T1/E1 and DSL. A general purpose framing mode provides an interface to customized framers and each of the 32 ports can be configured for a different mode. The M2852x also supports an Interleaved Highway mode where a combination of four T1, E1, Fractional T1 or Fractional E1’s can be transported over a higher bandwidth 8.192 MHz Interface.

1.14.2.5.1 T1/E1 Interface

This describes the timing requirements of the M28529 when operating in T1 or E1 mode. Connection to a CN8370 T1/E1 framer is used as an example, as illustrated in Figure 1-29. The M28529 receives a T1/E1 data stream from the external framer, ignores the T1/E1 overhead, extracts the ATM cells, and passes the ATM cells to the ATM layer device. In the transmit direction, the M28529 inserts 0’s in the overhead bit locations and fills the rest of the frame with ATM cells from the UTOPIA bus.

For the E1 mode, the ATM cells are mapped into time slots 1–15 and 17–31 as described in Recommendation G.804. For the T1 mode, the ATM cells are mapped into time slots 1–24.

Figure 1-29. CN8370 Interface Diagram



NOTE: The 8370 is a single port transceiver which is shown here for simplicity.

Figure 1-30. CN8370 Interface - T1 Timing Diagram

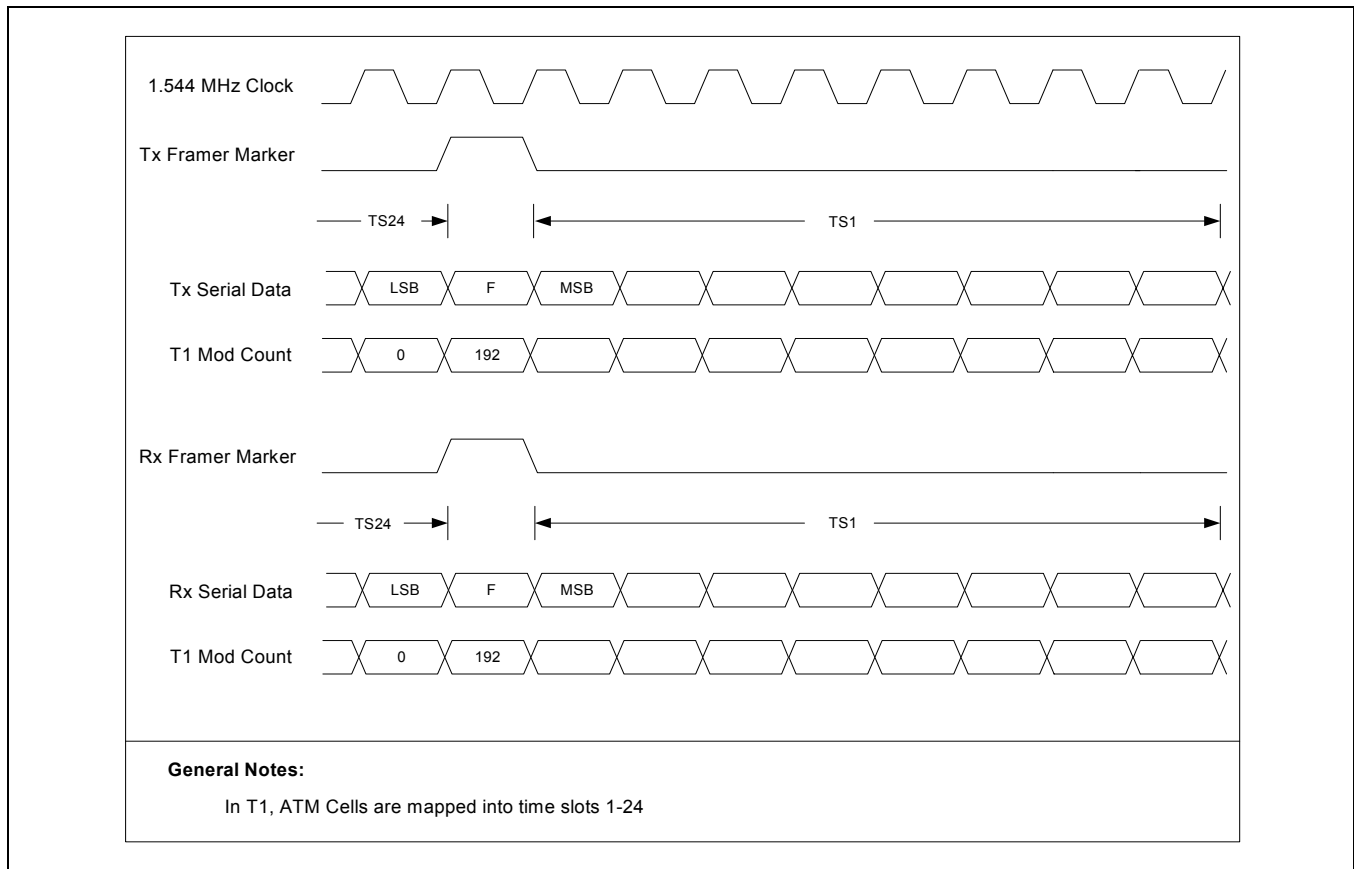
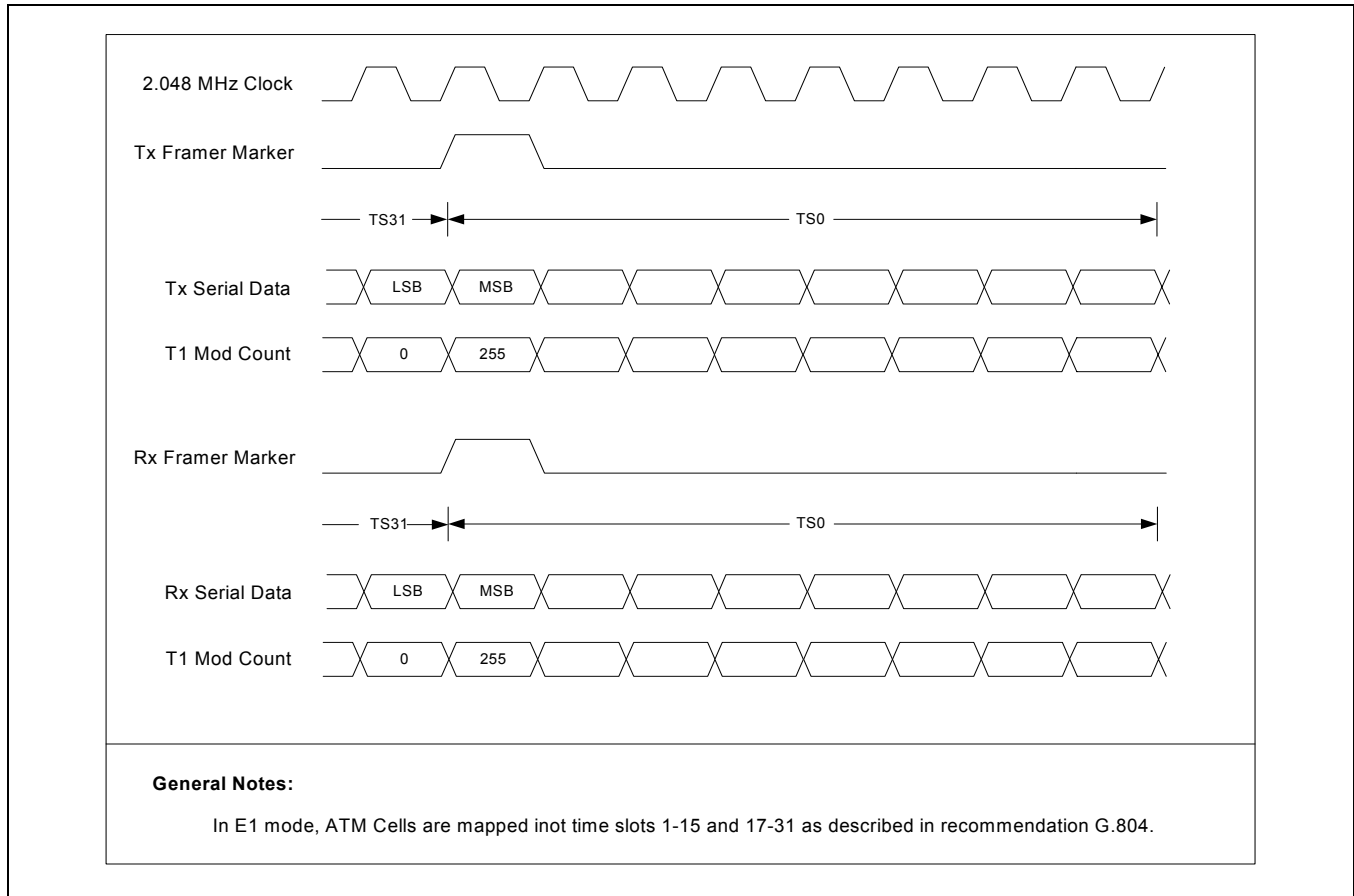


Figure 1-31. CN8370 Interface - E1 Timing Diagram



1.14.2.5.2 Fractional T1/E1 Interface

The purpose of the fractional T1/E1 logic is to gate off the serial clocks during inactive timeslots. The fractional T1/E1 logic is enabled on a link-by-link basis when in serial mode or on all four links when the interleaved highway mode is enabled.

Figure 1-32 shows an example of fractional T1 timing. In this mode, the clock frequency is 1.544 MHz and the sync input is used to indicate active data timeslots. The clocks are gapped internally in the M28525/9 during inactive timeslots. ATM cell bytes are continuously mapped into active timeslots.

Figure 1-32. Fractional T1 Timing.

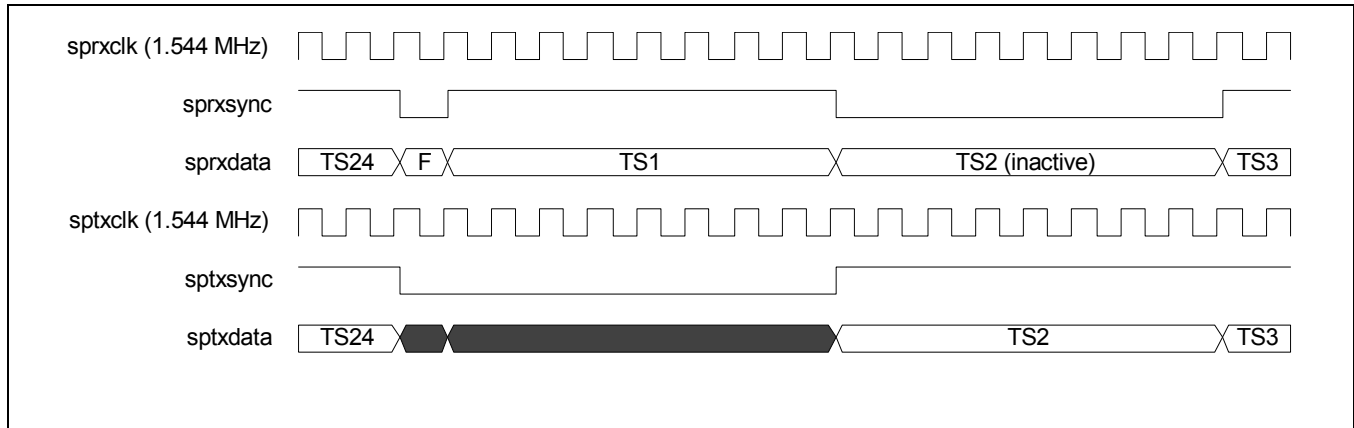
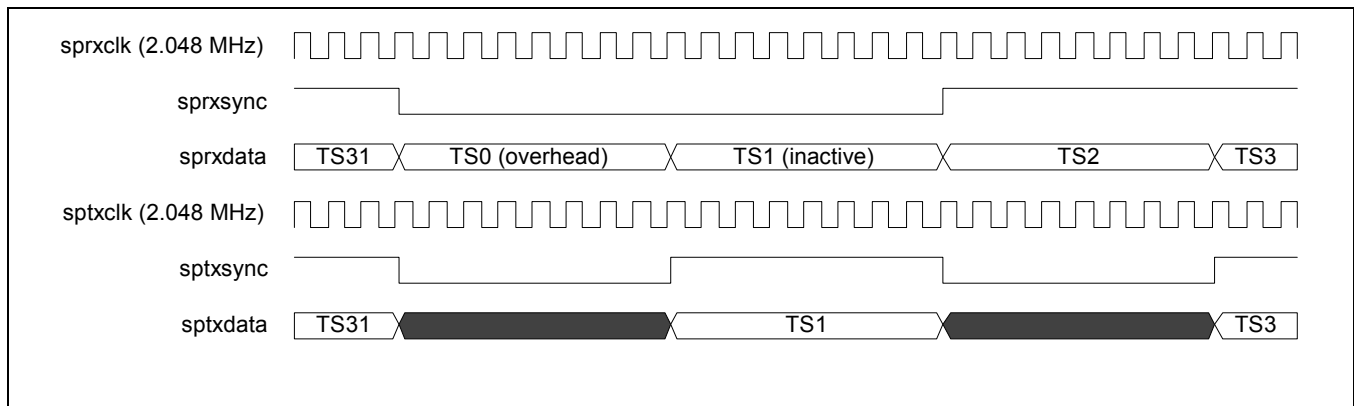


Figure 1-33 shows an example of fractional E1 timing. In Fractional E1 mode, the clock frequency is 2.048 MHz, and the sync inputs are used to indicate active data timeslots. The clocks are gapped internally in the M28525/9 during inactive timeslots. ATM cell bytes are continuously mapped into active timeslots.

Figure 1-33. Fractional E1 Timing.



NOTE: To enable fractional T1/E1 on a link, the appropriate EnFrac bits must be set in the TC Control Registers, (TCCTRL0-TCCTRL7). The PhyType[2:0] bits in the Port Mode Control register for the link should also be configured to be in xDSL framing mode (PMODE[2:0] = 110). CGEN[3] (DSL Sync Pol) must also be set to 1.

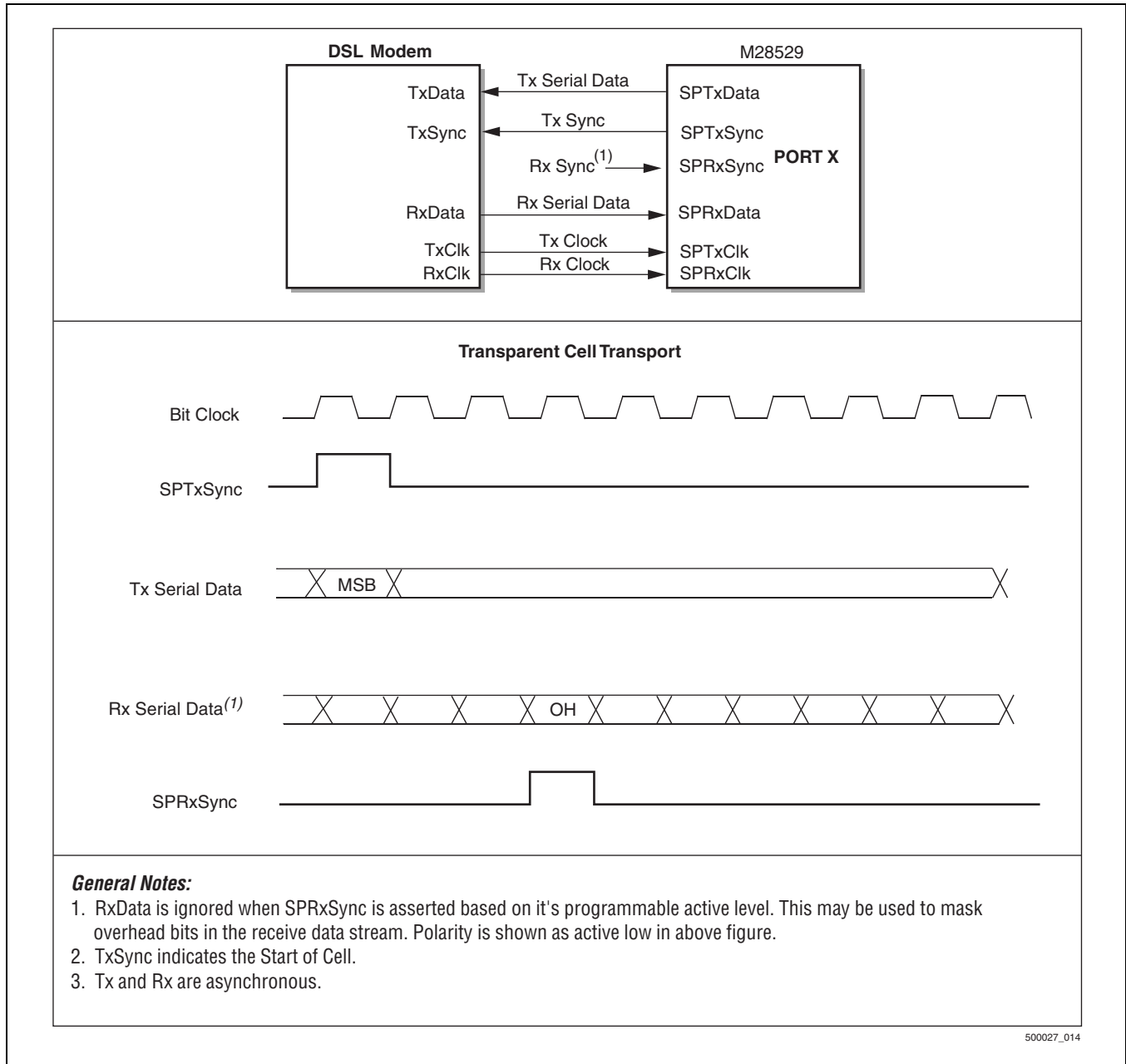
1.14.2.5.3 DSL Mode Interface

In DSL mode, the clock frequency can be up to 8.192 MHz. On the receive side, the sync input signals tell the TC Port receiver to ignore the corresponding bits on the data bus. This can be used to mask out overhead bits. Other than such overhead bits, the receive data stream should contain only serialized ATM cells. On the transmit side, sync is an output and is used to indicate the start of cell – the MSB of the first byte of the cell. Only serialized ATM data cells are present in the transmit data stream

The M2852x has a DSL mode interface as illustrated in Figure 1-34. This mode allows connection with framers that require frame synchronization. The M2852x receives a data stream from the external framer, performs bit level cell

delineation, and passes the ATM cells to the ATM layer device. In this mode, the framer must ensure that only ATM cells are present in the receive data stream. The M2852x performs the inverse process on transmitted data.

Figure 1-34. DSL Mode

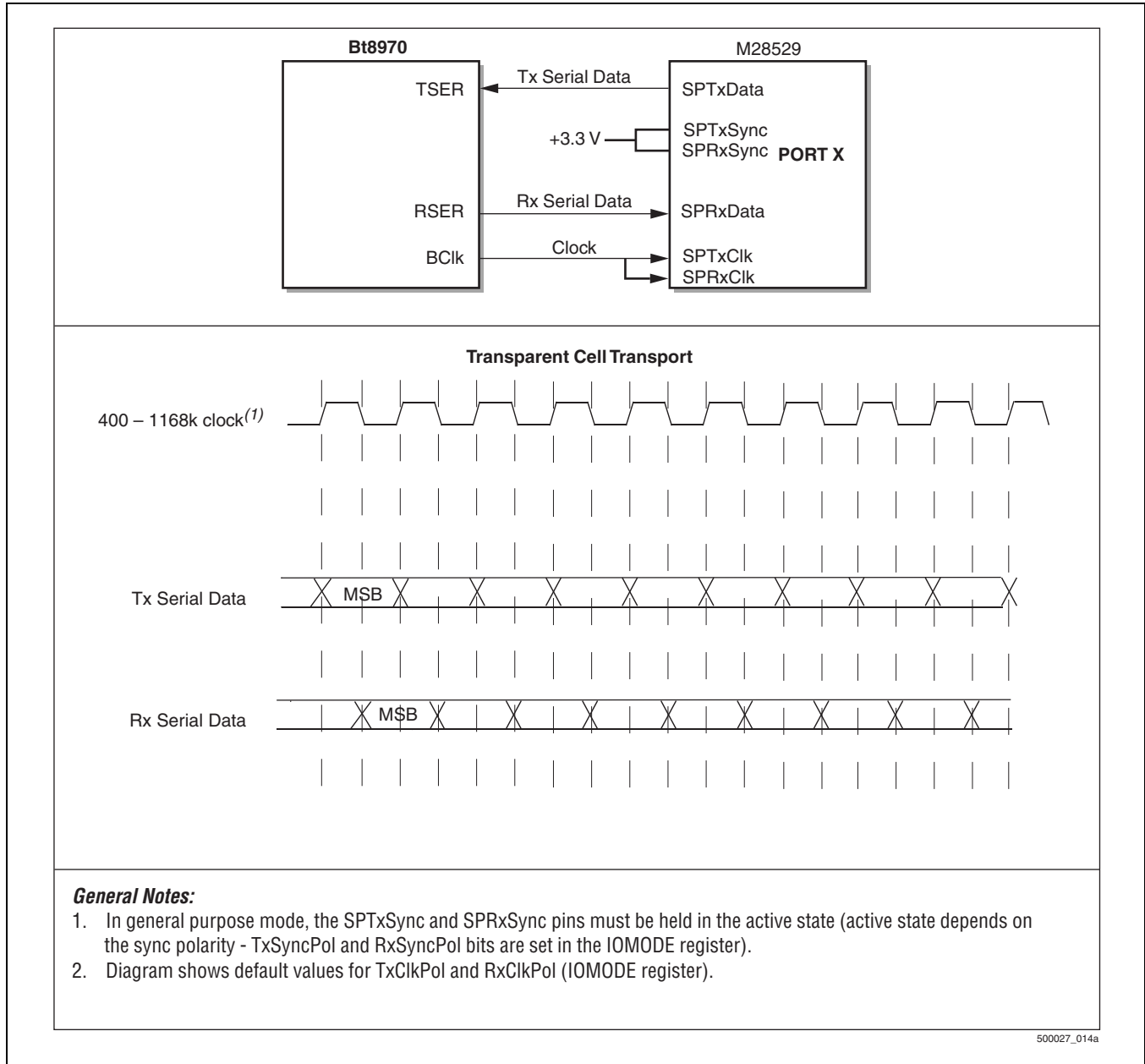


1.14.2.5.4 General Purpose Mode Interface

The M2852x has a general purpose mode interface as illustrated in Figure 1-35. This mode allows connection with framers that do not provide frame synchronization. The M2852x receives a data stream from the external framer, performs bit level cell delineation, and passes the ATM cells to the ATM layer device. In this mode, the framer must ensure that only ATM cells are present in the receive data stream. The M2852x performs the inverse process on transmitted data.

In general purpose framing mode, there is no frame synchronization or overhead bit indicators – the sync inputs should be held high. The receive data streams should contain only serialized ATM cells. The transmit data will only contained serialized ATM cells.

Figure 1-35. General Purpose Mode



1.14.2.5.5 Interleaved Highway Interface

The M2852x has interleaved highway interfaces (8-M28529, 4-M28525) as illustrated in [Figure 1-36](#) and [Figure 1-37](#). Four serial data streams can be combined together into one serial data stream using an Interleaved Highway interface. This interface is designed to communicate with Mindspeed's CX2839x framer devices, running in internally multiplexed mode.

Figure 1-36. Interfacing Interleaved Highway to CX2839x (Frame Sync Provided by CX2389x)

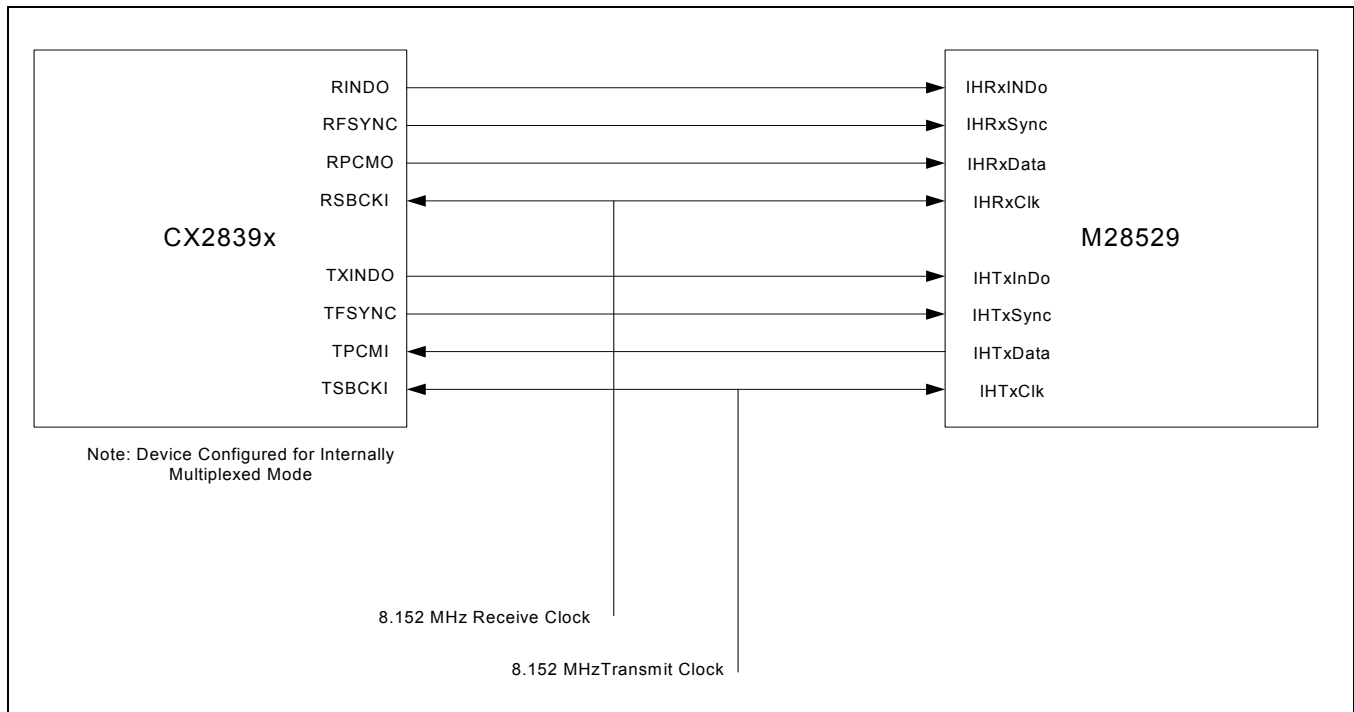
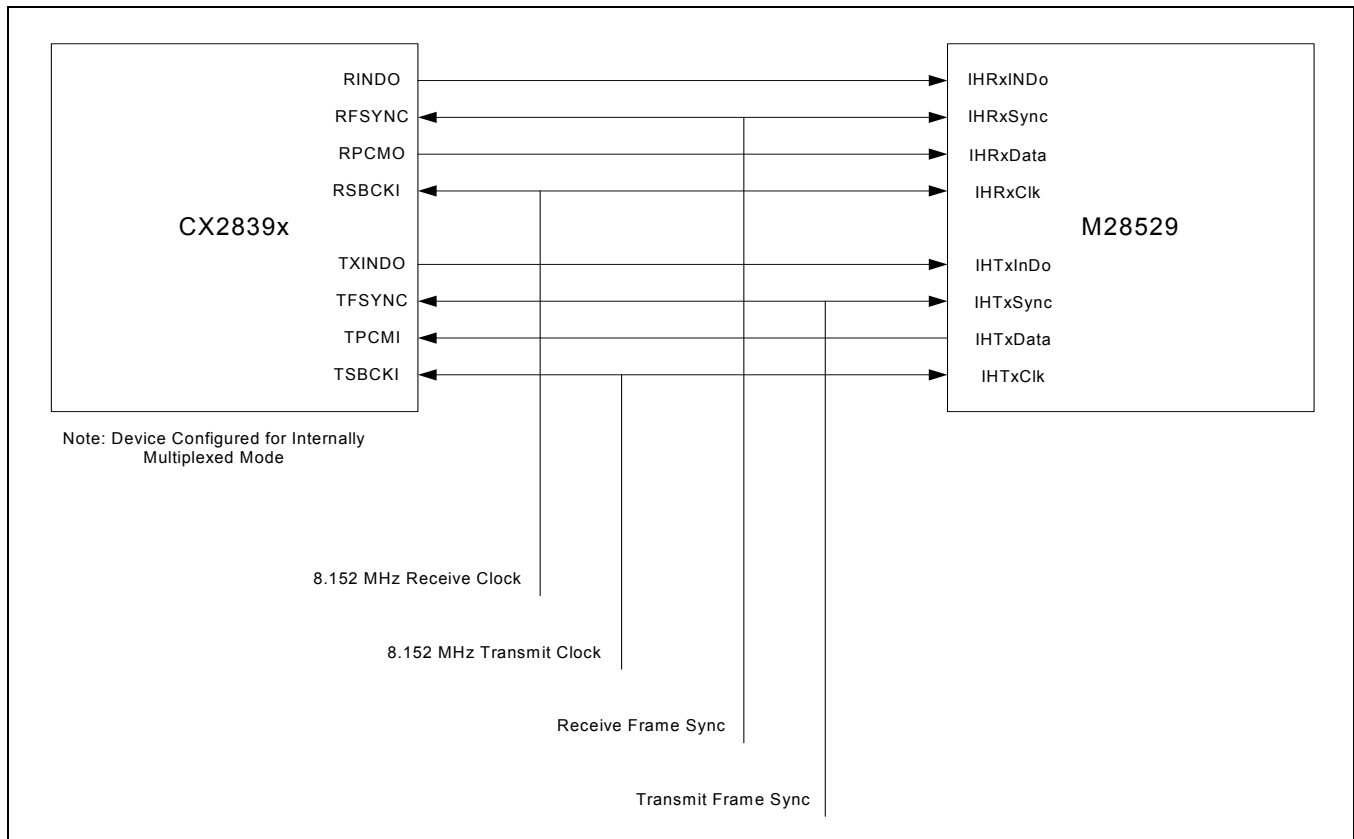


Figure 1-37. Interfacing Interleaved Highway to CX2839x (Frame Sync Externally Provided)



Each Interleaved highway interface carries four separate T1, E1, Fractional T1, or Fractional E1 style data streams (32 8-bit timeslots per frame). The data streams are interleaved one timeslot at a time. T1 links are supported over the Interleaved Highway interface, by mapping the 24 T1 timeslots (numbered 1-24) into the corresponding E1 timeslots. The remaining E1 timeslots, 0 and 25-31 are unused.

The interleaved highway mode can be selected on a per group of four link basis where the groups are as follows:

- Interleaved highway 0: Serial streams 0-3
- Interleaved highway 1: Serial streams 4-7
- Interleaved highway 2: Serial streams 8-11
- Interleaved highway 3: Serial streams 12-15
- Interleaved highway 4: Serial streams 16-19
- Interleaved highway 5: Serial streams 20-23
- Interleaved highway 6: Serial streams 24-27
- Interleaved highway 7: Serial streams 28-31

Input pins IHRxSync and IHTxSync are provided to indicate the first bit (MSB) of the first timeslot of the first data stream, in the receive and transmit directions respectively. The streams are multiplexed in order of the lowest numbered stream to highest number.

Fractional T1/E1 is also supported over the Interleaved Highway interface. Two extra signals, IHRxInDo and IHTxInDo, are used to indicate which timeslots are active on each of the data streams. These signals should be high for active timeslots.

Active timeslots in each case are as follows (timeslot 0 is always inactive as it is used for overhead in E1 frames, and has no corresponding timeslot in T1 frames):

- Full T1: timeslots 1-24 are used.
- Full E1: timeslots 1-15 and 17-31 are used.
- Fractional T1: subset of timeslots 1-24 is used.
- Fractional E1: subset of timeslots 1-15 and 17-31 are used.

The Fractional T1/E1 logic is automatically enabled when using the Interleaved Highway interface, to provide the necessary internal clock gating. Figure 1-38 shows how the datastreams are combined on the interleave highway. In this example time slots 31A and TS0B are inactive as indicated by IHRxInDo being low. If for example Figure 1-38 represented Interleaved highway 5, the streams would be grouped as follows: A = Stream 20, B = Stream 21, C = Stream 22, D = Stream 23.

Figure 1-38. Combined Datastreams on the Interleaved Highway

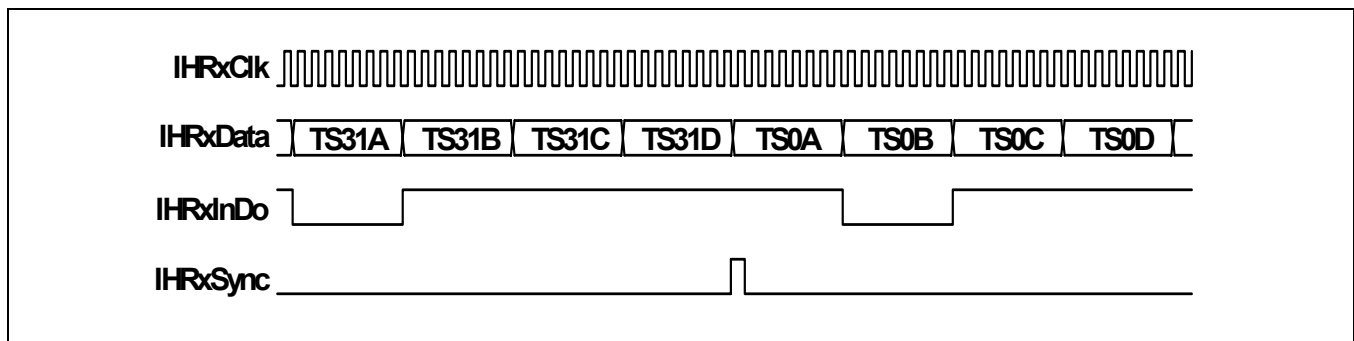


Figure 1-39. Full T1 Interleaved Highway Frame

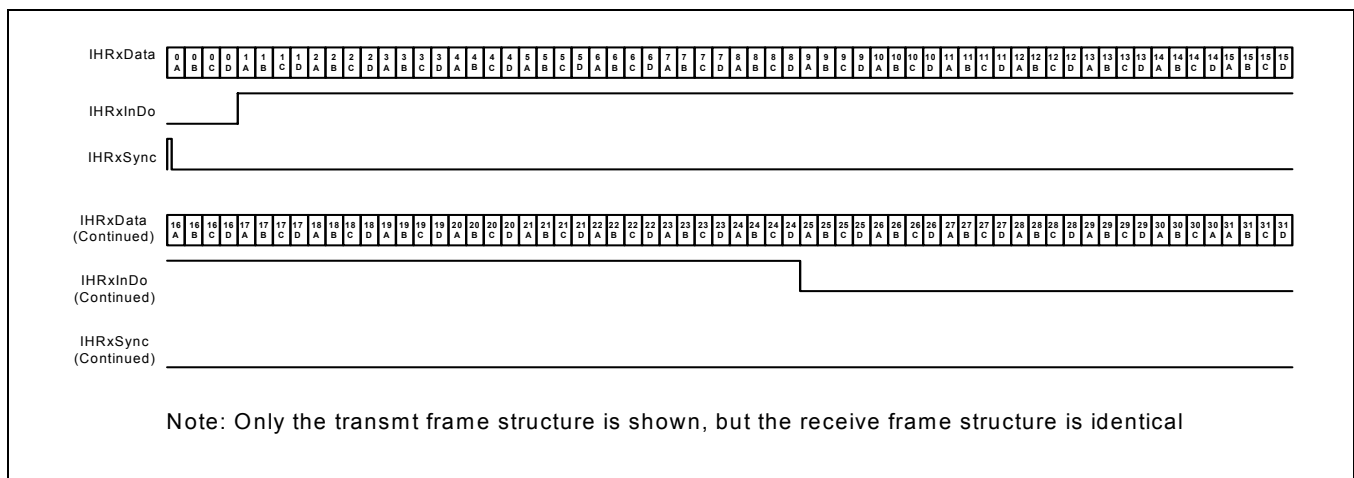
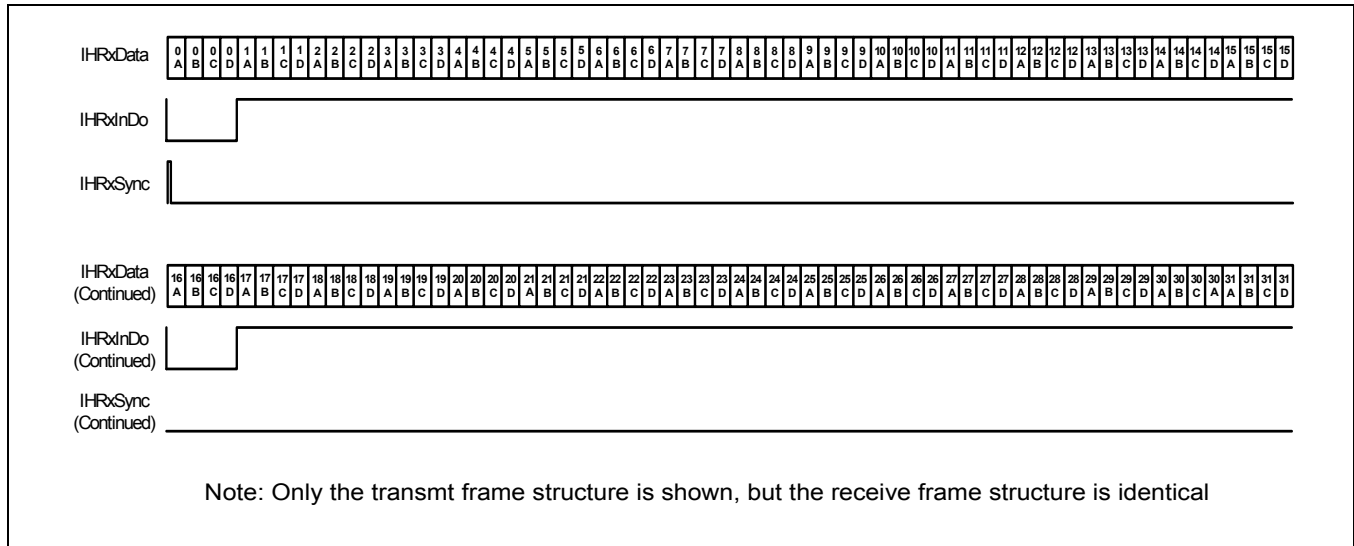


Figure 1-40. Full E1 Interleaved Highway Frame

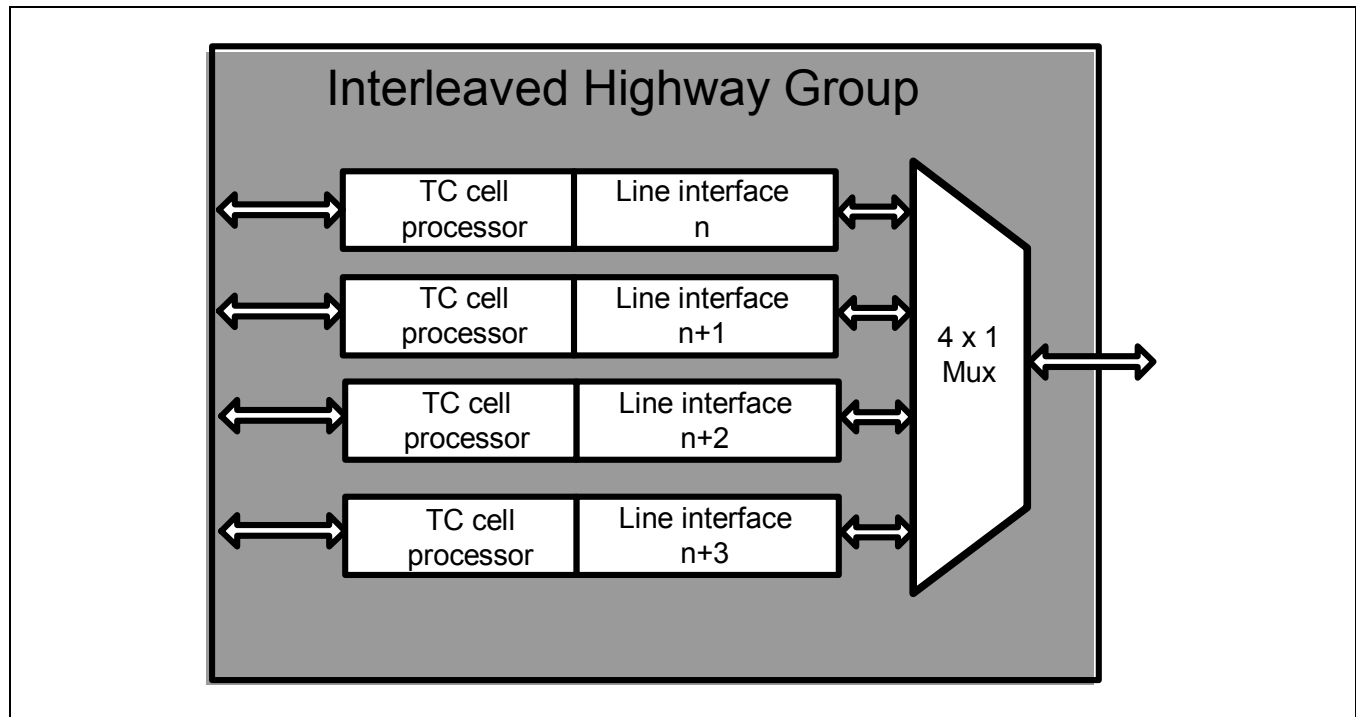


NOTE: The TC Processors belonging to the Interleaved Highway group should be configured in xDSL mode, by setting PhyType to 110 in the Port Mode Control Registers (PMODE[2:0]) 0x04, as this is required when using the Fractional T1/E1 logic. Also, the IOMODE registers 0x05 should be set to their default values. This is because the clock polarities in Interleaved Highway mode are controlled via the TCCTRL registers. Also the Internal sync inputs to the TC processor are tied low (inactive state when IOMODE[6] and IOMODE[4] are set to default values in xDSL mode) so that they have no effect

NOTE: The T1/E1 streams must be locked to the 8.192 MHz clock rate.

Figure 1-41 is a block diagram showing how four serial links are combined.

Figure 1-41. Interleaved Highway Mux



1.15 General Issues

1.15.1 Micro Interface

The microprocessor interface transfers control and status information in 8-bit data transfers between the external microprocessor and M2852x by means of write and/or read access to internal registers. This interface allows the microprocessor to configure the M2852x by writing various control registers. These control registers can also be read for configuration confirmation. This interface also provides the ability to read the device's current condition via its status registers and counters. Summary status is available for rapid interrupt identification.

The microprocessor interface can operate in either an asynchronous mode or a synchronous mode. The MSyncMode (pin AE24) determines which mode is active.

In the synchronous mode, the timing of these signals is synchronized to MicroClk, which is intended to be directly driven by the external microprocessor.

NOTE:

The MicroClk is required for both modes. In asynchronous mode, a MicroClk frequency of up to 66MHz, must be present but can be asynchronous to the other microprocessor signals. In synchronous mode, MicroClk is limited to 25MHz.

1.15.1.1 Resets

There are four software controlled reset functions, two at the device level and two at the port level. The two levels allow a user to reset either the entire M2852x with one command or only a port within the device. The two logic resets allow the user to keep the device or port in a reset state while the control registers are being programmed. When the reset bit is deasserted, all changes to the registers take place simultaneously.

At the device level, the software-controlled DevMstRst, bit 7, in the GENCTRL register (0x0F00), restarts all device functions and sets the control and status registers, including IMA, to their default values except this bit (DevMstRst). The DevLgcRst, bit 6, in the GENCTRL register (0x0F00) restarts all device functions in the TC block but leaves all control registers unaffected. During a device logic reset the IMA core is held in a complete reset state.

NOTE:

If configuring the device for pass-through operation, a minimum delay of 25 uS for IMA_Sysclk of 66 MHz or 33 uS for IMA_Sysclk of 50 MHz is required from the release of device reset (DevMstRst) to the first access of the IMA_RX_TRANS_TABLE register or IMA_RX_ATM_TRANS_TABLE register (0x818/0x819).

At the port level, the PrtMstRst, bit 7, in the PMODE register (0x04), restarts all port functions and sets the registers for the associated port to their default values except this bit (PrtMstRst). The PrtLgcRst, bit 6, in the PMODE register (0x04) restarts all functions but leaves the port control registers unaffected.

1.15.1.2 Counters (TC Block Only)

The M2852x counters record events within the TC block. Two types of events are recorded: error events, such as Section BIP errors, and transmission events, such as transmitted ATM cells.

Counters comprised of more than one register must be accessed by reading the least significant byte (LSB) first. This guarantees that the value contained in each component register accurately reflects the composite counter value at the time the LSB was read, because the counter may be updated while the component registers are being read.

Each counter is large enough to accommodate the maximum number of events that may occur within a one-second interval. The counters are cleared after being read. Therefore, if the counters are read every second, the application will receive an accurate recording of all events.

1.15.1.2.1 One-second Latching

The M2852x's implementation of one-second latching ensures the integrity of the statistics being gathered by the network management software. Internal statistics counters can be latched at one-second intervals, which are synchronized to the OneSecIO pin (pin AE26). Therefore, the data read from the statistic counters represents the same one second of real-time data, independent of network management software timing.

The M2852x implements one-second latching for both status signals and counter values. When the EnStatLat (bit 5) in the GENCTRL register (0xF00) is written to a logical 1, a read from any of the status registers returns the state of the device at the time of the previous OneSecIO (pin AE26) assertion. When the EnCntrLat (bit 4) in the GENCTRL register (0xF00) is written to a logical 1, a read from any of the counters returns the state of the device at the time of the previous OneSecIO (pin AE26) assertion. Every second, the counter is read, moved to the latch, and the counter is cleared. The latch is cleared when read.

Software can configure the OneSecIO pin as an output that equals the input from the 8kHzIn divided by 8000. When configured as an input, status registers and counters may be latched on the rising edge of this input. See Bit 0 of the GENCTRL register (0xF00).

NOTE:

When latching is disabled and a counter is wider than one byte, the LSB should be read first to retain the values of the other bytes for a subsequent read.

1.15.1.2.2 Interrupts

The M2852x's interrupt indications can be classified as either single- or dual-event; a single-event interrupt is triggered by a status assertion; a dual-event interrupt is triggered by either a status assertion or deassertion. Both types of interrupts are further described in the following examples.

Single-event interrupt: When a parity error occurs on the UTOPIA transmit data bus, an interrupt is generated on ParErrInt, bit 7, in the TXCELLINT register (0x2C). This bit is cleared when read.

Dual-event interrupt: When LOCD occurs, bit 7 of the corresponding RXCELLINT register (0x0D) is set to 1. This bit is cleared when the register is read. Once cell delineation is recovered, bit 7 is set to 1 again, generating another interrupt.

All interrupt bits have a corresponding enable bit. This allows software to disable or mask interrupts as required.

NOTE: The IMA block does not generate interrupts.

The M2852x uses three levels of interrupt indications. The first level consists of receive or transmit interrupt indications, which correspond to specific events on a specific port. The second level summarizes first level interrupts and indicates framer and one-second interrupts for each port. The third level indicates which port generated an interrupt.

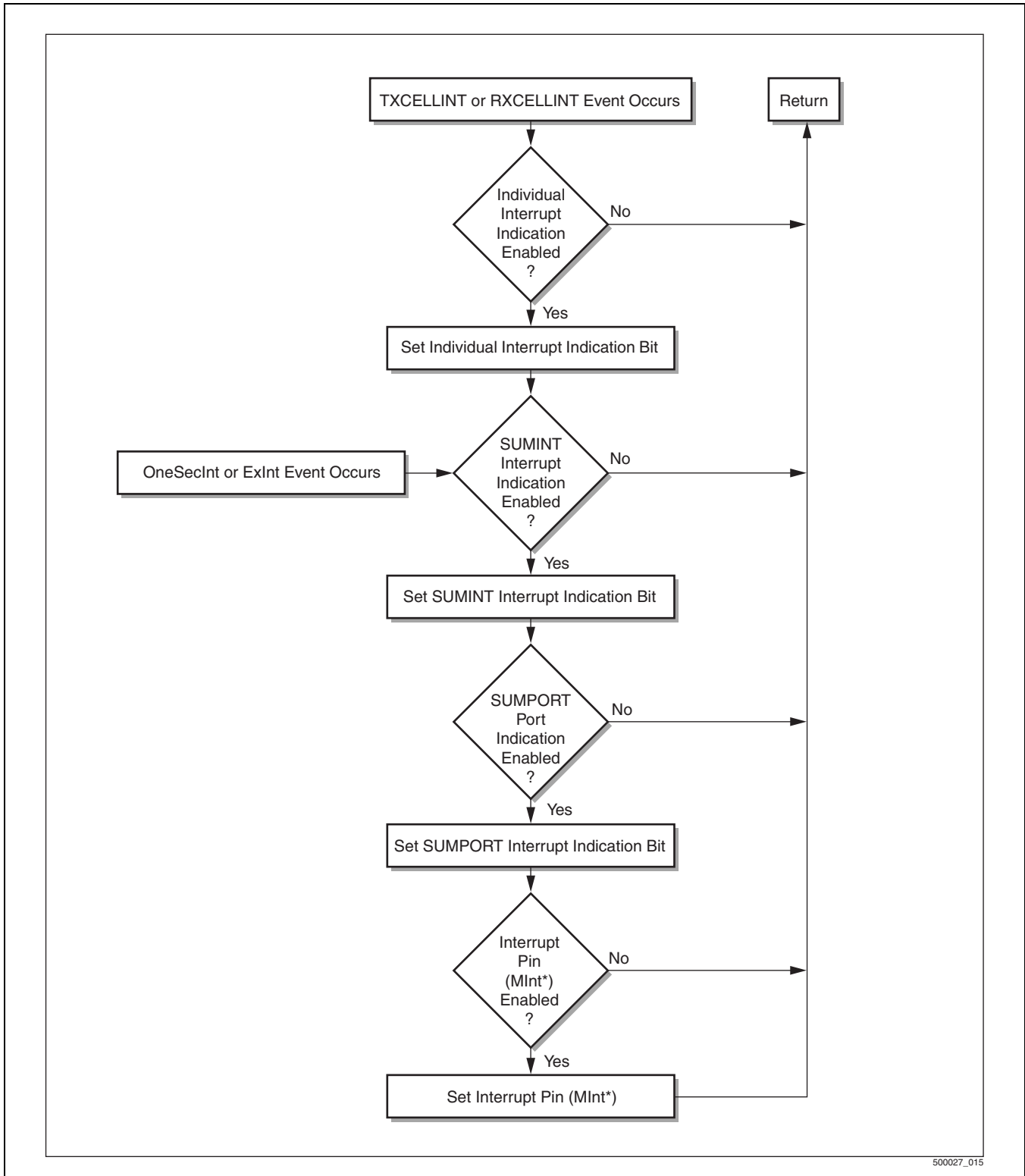
The first level interrupt indications are located in registers TXCELLINT and RXCELLINT for each port. Each interrupt bit in these registers can be disabled in the corresponding ENCELLR or ENCELLT register, respectively. The result is then ORed into the appropriate bit in the port's SUMINT register.

The second level consists of summary interrupt indications, located in the SUMINT register. It also includes the OneSecInt and the ExInt indications. Each interrupt bit in these registers can be disabled in the corresponding ENSUMINT register. The result is then ORed into the appropriate bit in the SUMPORT register.

The third level contains the overall interrupt indications for each port in the SUMPORT register. These bits can be disabled in the ENSUMPORT register. The result is ORed to the MicroInt* pin. The MicroInt* pin can be enabled or disabled by setting the EnIntPin (bit 3) in the GENCTRL register (0x0F00).

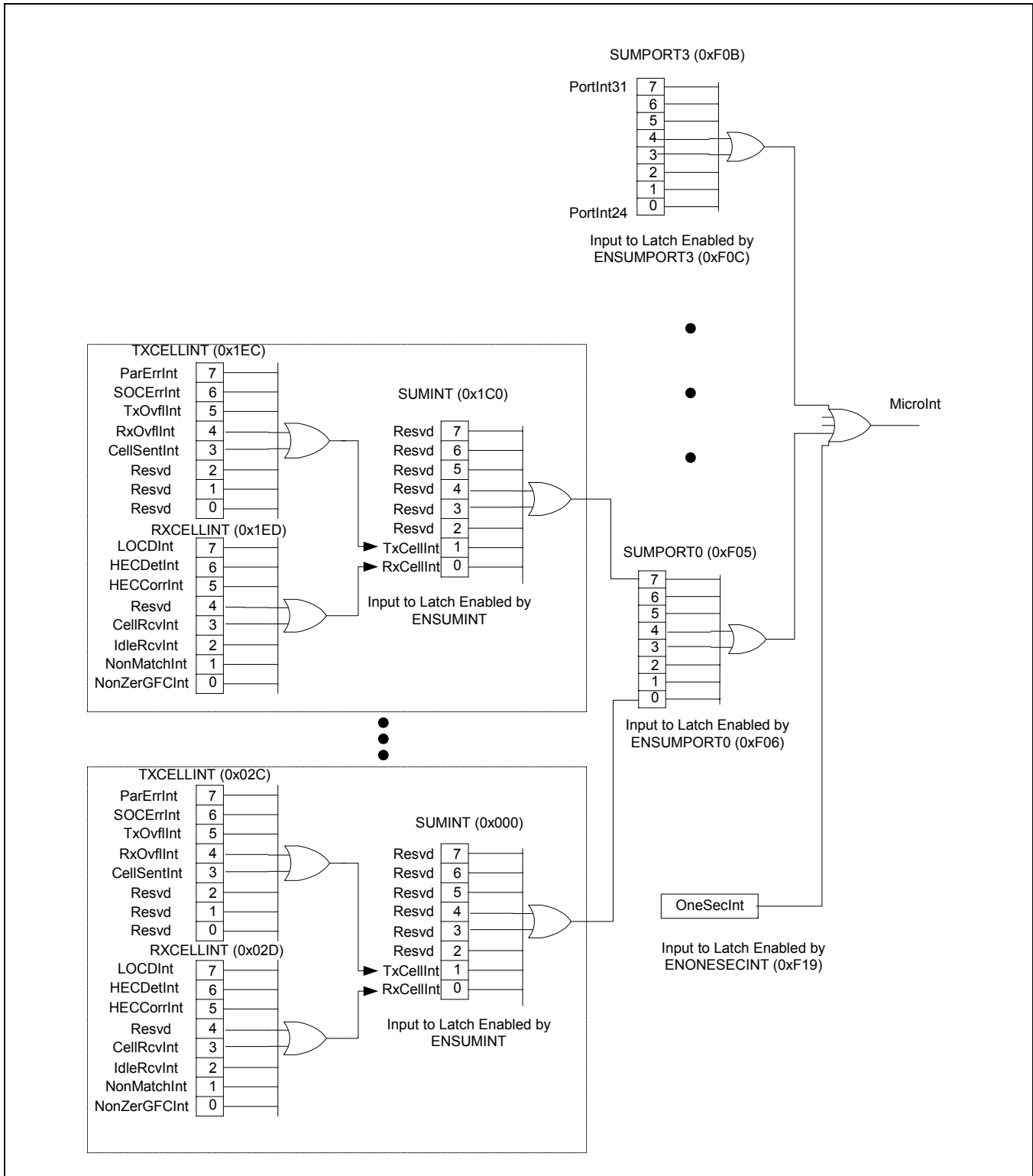
[Figure 1-42](#) illustrates the flow chart of the interrupt generation process and [Figure 1-43](#) illustrates the registers involved in the interrupt generation process.

Figure 1-42. Interrupt Indication Flow Chart



500027_015

Figure 1-43. Interrupt Indication Diagram (TC Block)



1.15.1.2.3 Interrupt Servicing

When an interrupt occurs on the MicroInt* pin (pin AA1), it could have been generated by any of 385 events. The M2852x's interrupt indication structure ensures that no more than a maximum of seven register reads are needed to determine the source of an interrupt. The interrupt is traced back to its source using the following steps:

1. Read the SUMPOR0-3 registers and the ONESECINT register to see which port(s) shows an interrupt and/or whether there was a one second interrupt.
2. Read the appropriate SUMINT register to see which bit(s) shows an interrupt.
 - Bit 0, RxCellInt, reflects activity in the RXCELLINT register.
 - Bit 1, TxCellInt, reflects activity in the TXCELLINT register.
 - Bits 2–7 are reserved.
3. If necessary, read the appropriate TXCELLINT or RXCELLINT register.

All Level 1 bits are cleared when the register is read. Once the register is read, ALL bits in that register are reset to their default values. Therefore, interrupt service routines must be designed to handle multiple interrupts in the same registers. In Level 2, OneSecInt and ExInt are cleared when the register is read. However, the TxCellInt and RxCellInt bits are cleared only when the corresponding Level 1 register is read and cleared. Level 3 bits are cleared when the entire corresponding Level 2 register has been read and cleared.



2.0 Registers

2.1 Address Map

The M2852x registers control and observe the device's operations. [Table 2-1](#) lists the address ranges that represent a device control and status range. The registers in each port range are replicated for the other ports. [Table 2-2](#) lists the device-level control and status registers. [Table 2-3](#) lists the port-level control and status registers. All registers are 8 bits wide. All control registers can be read to verify contents.

NOTE: Control bits that do not have a documented function are reserved and must be written to a logical 0.

Table 2-1. Address Ranges (1 of 2)

| Port Offset Address Range (Hex) | Description | Port Base Address (Hex) |
|------------------------------------|--------------------------------------|----------------------------|
| 0000–003F | Port 0 Control and Status Registers | 0000 |
| 0040–007F | Port 1 Control and Status Registers | 0040 |
| 0080–00BF | Port 2 Control and Status Registers | 0080 |
| 00C0–00FF | Port 3 Control and Status Registers | 00C0 |
| 0100–013F | Port 4 Control and Status Registers | 0100 |
| 0140–017F | Port 5 Control and Status Registers | 0140 |
| 0180–01BF | Port 6 Control and Status Registers | 0180 |
| 01C0–01FF | Port 7 Control and Status Registers | 01C0 |
| 0200–023F | Port 8 Control and Status Registers | 0200 |
| 0240–027F | Port 9 Control and Status Registers | 0240 |
| 0280–02BF | Port 10 Control and Status Registers | 0280 |
| 02C0–02FF | Port 11 Control and Status Registers | 02C0 |
| 0300–033F | Port 12 Control and Status Registers | 0300 |
| 0340–037F | Port 13 Control and Status Registers | 0340 |
| 0380–03BF | Port 14 Control and Status Registers | 0380 |
| 03C0–03FF | Port 15 Control and Status Registers | 03C0 |
| 0400–043F | Port 16 Control and Status Registers | 0400 |
| 0440–047F | Port 17 Control and Status Registers | 0440 |
| 0480–04BF | Port 18 Control and Status Registers | 0480 |

Table 2-1. Address Ranges (2 of 2)

| Port Offset Address Range (Hex) | Description | Port Base Address (Hex) |
|------------------------------------|--------------------------------------|----------------------------|
| 04C0-04FF | Port 19 Control and Status Registers | 04C0 |
| 0500-053F | Port 20 Control and Status Registers | 0500 |
| 0540-057F | Port 21 Control and Status Registers | 0540 |
| 0580-05BF | Port 22 Control and Status Registers | 0580 |
| 05C0-05FF | Port 23 Control and Status Registers | 05C0 |
| 0600-063F | Port 24 Control and Status Registers | 0600 |
| 0640-067F | Port 25 Control and Status Registers | 0640 |
| 0680-06BF | Port 26 Control and Status Registers | 0680 |
| 06C0-06FF | Port 27 Control and Status Registers | 06C0 |
| 0700-073F | Port 28 Control and Status Registers | 0700 |
| 0740-077F | Port 29 Control and Status Registers | 0740 |
| 0780-07BF | Port 30 Control and Status Registers | 0780 |
| 07C0-07FF | Port 31 Control and Status Registers | 07C0 |
| 0800-0EFF | IMA Control and Status Registers | — |
| 0F00-0FFF | Device Control and Status Registers | — |

The device level registers in [Table 2-2](#) provide control for the device’s major operating modes, as well as status and control for summary interrupts.

Table 2-2. Device Control and Status Registers (1 of 2)

| Address | Name | Type | OneSec Latching | Description | Page Number |
|---------|------------|------|--------------------|---|--------------------------|
| 0x0F00 | GENCTRL | R/W | — | General Device Control Register | page 179 |
| 0x0F01 | PARTNUM | R/W | — | Part and Version Number | page 179 |
| 0x0F02 | PHYINTFC | R/W | — | PHY-side Interface Control Register | page 180 |
| 0x0F03 | ATMINTFC | R/W | — | ATM-side Interface Control Register | page 180 |
| 0x0F04 | STATOUT | R | — | Output Status Control Register | page 180 |
| 0x0F05 | SUMPORT0 | R/W | — | Summary Interrupt Status Register (TC Ports 0-7) | page 181 |
| 0x0F06 | ENSUMPORT0 | R | — | Summary Interrupt Control Register (TC Ports 0-7) | page 181 |
| 0x0F07 | SUMPORT1 | R/W | — | Summary Interrupt Status Register (TC Ports 8-15) | page 182 |
| 0x0F08 | ENSUMPORT1 | R | — | Summary Interrupt Control Register (TC Ports 8-15) | page 182 |
| 0x0F09 | SUMPORT2 | R/W | — | Summary Interrupt Status Register (TC Ports 16-23) | page 183 |
| 0x0FOA | ENSUMPORT2 | R | — | Summary Interrupt Control Register (TC Ports 16-23) | page 183 |
| 0x0FOB | SUMPORT3 | R/W | — | Summary Interrupt Status Register (TC Ports 24-31) | page 184 |
| 0x0FOC | ENSUMPORT3 | R | — | Summary Interrupt Control Register (TC Ports 24-31) | page 184 |
| 0x0F0D | — | | — | Reserved, set register to all 0’s | |

Table 2-2. Device Control and Status Registers (2 of 2)

| Address | Name | Type | OneSec Latching | Description | Page Number |
|---------|-------------|------|-----------------|--|--------------------------|
| 0x0F0E | — | | — | Reserved, set register to all 0's | |
| 0x0F0F | SCRATCH | | — | Scratch Pad Register | page 184 |
| 0x0F10 | TCCTRL0 | | — | TC Control Register for TC Ports 0-3 | page 185 |
| 0x0F11 | TCCTRL1 | | — | TC Control Register for TC Ports 4-7 | page 185 |
| 0x0F12 | TCCTRL2 | | — | TC Control Register for TC Ports 8-11 | page 186 |
| 0x0F13 | TCCTRL3 | | — | TC Control Register for TC Ports 12-15 | page 186 |
| 0x0F14 | TCCTRL4 | | — | TC Control Register for TC Ports 16-19 | page 187 |
| 0x0F15 | TCCTRL5 | | — | TC Control Register for TC Ports 20-23 | page 187 |
| 0x0F16 | TCCTRL6 | | — | TC Control Register for TC Ports 24-27 | page 188 |
| 0x0F17 | TCCTRL7 | | — | TC Control Register for TC Ports 28-31 | page 188 |
| 0x0F18 | ONESECINT | | — | One Second Interrupt Status Register | page 188 |
| 0x0F19 | ENONESECINT | | — | One Second Interrupt Control Register | page 189 |

The registers listed in [Table 2-3](#) are replicated for each port. Two methods can be used to determine the exact address of a specific register in a specific port. All numbers are in hexadecimal.

1. Add the port offset address to the port base address as shown in [Table 2-1](#). For example:
For Port 3, IOMODE register 0xC0 (Port 3 base address) + 0x05 (port offset address) = 0xC5
2. Use the following formula:
 $0x40 \text{ (port register map size)} \times n \text{ (port number)} + \text{port offset address} = \text{exact register address}$

Table 2-3. Port Control and Status Registers (1 of 3)

| Port Offset Address | Name | Type | One-second Latching | Description | Page Number |
|---------------------|----------|------|---------------------|--|--------------------------|
| 0x00 | SUMINT | R | — | Summary Interrupt Indication Status Register | page 150 |
| 0x01 | ENSUMINT | R/W | — | Summary Interrupt Control Register | page 151 |
| 0x02 | — | — | — | Reserved, set to a logical 0 | — |
| 0x03 | — | — | — | Reserved, set to a logical 0 | — |
| 0x04 | PMODE | R/W | — | Port Mode Control Register | page 152 |
| 0x05 | IOMODE | R/W | — | Input/Output Mode Control Register | page 153 |
| 0x08 | CGEN | R/W | — | Cell Generation Control Register | page 154 |
| 0x09 | HDRFIELD | R/W | — | Header Field Control Register | page 155 |
| 0x0A | IDLPAY | R/W | — | Transmit Idle Cell Payload Control Register | page 155 |
| 0x0B | ERRPAT | R/W | — | Error Pattern Control Register | page 156 |
| 0x0C | CVAL | R/W | — | Cell Validation Control Register | page 156 |
| 0x0D | UTOP1 | R/W | — | UTOPIA Control Register 1 | page 157 |
| 0x0E | UTOP2 | R/W | — | UTOPIA Control Register 2 | page 157 |

Table 2-3. Port Control and Status Registers (2 of 3)

| Port Offset Address | Name | Type | One-second Latching | Description (Continued) | Page Number |
|---------------------|-----------|------|---------------------|---|--------------------------|
| 0x0F | UDF2 | R/W | — | UDF2 Control Register | page 158 |
| 0x10 | TXHDR1 | R/W | — | Transmit Cell Header Control Register 1 | page 158 |
| 0x11 | TXHDR2 | R/W | — | Transmit Cell Header Control Register 2 | page 159 |
| 0x12 | TXHDR3 | R/W | — | Transmit Cell Header Control Register 3 | page 159 |
| 0x13 | TXHDR4 | R/W | — | Transmit Cell Header Control Register 4 | page 160 |
| 0x14 | TXIDL1 | R/W | — | Transmit Idle Cell Header Control Register 1 | page 160 |
| 0x15 | TXIDL2 | R/W | — | Transmit Idle Cell Header Control Register 2 | page 161 |
| 0x16 | TXIDL3 | R/W | — | Transmit Idle Cell Header Control Register 3 | page 161 |
| 0x17 | TXIDL4 | R/W | — | Transmit Idle Cell Header Control Register 4 | page 162 |
| 0x18 | RXHDR1 | R/W | — | Receive Cell Header Control Register 1 | page 162 |
| 0x19 | RXHDR2 | R/W | — | Receive Cell Header Control Register 2 | page 163 |
| 0x1A | RXHDR3 | R/W | — | Receive Cell Header Control Register 3 | page 163 |
| 0x1B | RXHDR4 | R/W | — | Receive Cell Header Control Register 4 | page 164 |
| 0x1C | RXMSK1 | R/W | — | Receive Cell Mask Control Register 1 | page 164 |
| 0x1D | RXMSK2 | R/W | — | Receive Cell Mask Control Register 2 | page 165 |
| 0x1E | RXMSK3 | R/W | — | Receive Cell Mask Control Register 3 | page 165 |
| 0x1F | RXMSK4 | R/W | — | Receive Cell Mask Control Register 4 | page 166 |
| 0x20 | RXIDL1 | R/W | — | Receive Idle Cell Header Control Register 1 | page 166 |
| 0x21 | RXIDL2 | R/W | — | Receive Idle Cell Header Control Register 2 | page 167 |
| 0x22 | RXIDL3 | R/W | — | Receive Idle Cell Header Control Register 3 | page 167 |
| 0x23 | RXIDL4 | R/W | — | Receive Idle Cell Header Control Register 4 | page 168 |
| 0x24 | IDLMSK1 | R/W | — | Receive Idle Cell Mask Control Register 1 | page 168 |
| 0x25 | IDLMSK2 | R/W | — | Receive Idle Cell Mask Control Register 2 | page 169 |
| 0x26 | IDLMSK3 | R/W | — | Receive Idle Cell Mask Control Register 3 | page 169 |
| 0x27 | IDLMSK4 | R/W | — | Receive Idle Cell Mask Control Register 4 | page 170 |
| 0x28 | ENCELLT | R/W | — | Transmit Cell Interrupt Control Register | page 170 |
| 0x29 | ENCELLR | R/W | — | Receive Cell Interrupt Control Register | page 171 |
| 0x2A | — | — | — | Reserved, set to a logical 0 | — |
| 0x2B | — | — | — | Reserved, set to a logical 0 | — |
| 0x2C | TXCELLINT | R | — | Transmit Cell Interrupt Indication Control Register | page 171 |
| 0x2D | RXCELLINT | R | — | Receive Cell Interrupt Indication Control Register | page 172 |
| 0x2E | TXCELL | R | (1) | Transmit Cell Status Control Register | page 172 |
| 0x2F | RXCELL | R | (1) | Receive Cell Status Control Register | page 173 |
| 0x30 | IDLCNTL | R | (2) | Idle Cell Receive Counter (low byte) | page 173 |
| 0x31 | IDLCNTH | R | (2) | Idle Cell Receive Counter (high byte) | page 174 |

Table 2-3. Port Control and Status Registers (3 of 3)

| Port Offset Address | Name | Type | One-second Latching | Description (Continued) | Page Number |
|---------------------|---------|------|---------------------|---------------------------------------|--------------------------|
| 0x33 | LODCNT | R | (2) | LOCD Event Counter | page 174 |
| 0x34 | TXCNTL | R | (2) | Transmitted Cell Counter (low byte) | page 175 |
| 0x35 | TXCNTH | R | (2) | Transmitted Cell Counter (high byte) | page 175 |
| 0x37 | CORRCNT | R | (2) | Corrected HEC Error Counter | page 176 |
| 0x38 | RXCNTL | R | (2) | Received Cell Counter (low byte) | page 176 |
| 0x39 | RXCNTH | R | (2) | Received Cell Counter (high byte) | page 177 |
| 0x3B | UNCCNT | R | (2) | Uncorrected HEC Error Counter | page 177 |
| 0x3C | NONCNTL | R | (2) | Non-Matching Cell Counter (low byte) | page 178 |
| 0x3D | NONCNTH | R | (2) | Non-Matching Cell Counter (high byte) | page 178 |
| 0x3E | — | — | — | Reserved, set to a logical 0 | — |
| 0x3F | — | — | — | Reserved, set to a logical 0 | — |

Footnote:

(1) One-second latching is enabled by setting EnStatLat (bit 5) in the GENCTRL register (0xF00) to a logical 1.

(2) One-second latching is enabled by setting EnCntrLat (bit 4) in the MODE register (0xF00) to a logical 1.

Table 2-4 lists the control registers used for transmission of traffic.

Table 2-4. Cell Transmit Registers

| Port Offset Address | Name | Description | Page Number |
|---------------------|----------|--|--------------------------|
| 0x08 | CGEN | Cell Generation Control Register | page 154 |
| 0x09 | HDRFIELD | Header Field Control Register | page 155 |
| 0x0A | IDLPAY | Transmit Idle Cell Payload Control Register | page 155 |
| 0x0B | ERRPAT | Error Pattern Control Register | page 156 |
| 0x10 | TXHDR1 | Transmit Cell Header Control Register 1 | page 158 |
| 0x11 | TXHDR2 | Transmit Cell Header Control Register 2 | page 159 |
| 0x12 | TXHDR3 | Transmit Cell Header Control Register 3 | page 159 |
| 0x13 | TXHDR4 | Transmit Cell Header Control Register 4 | page 160 |
| 0x14 | TXIDL1 | Transmit Idle Cell Header Control Register 1 | page 160 |
| 0x15 | TXIDL2 | Transmit Idle Cell Header Control Register 2 | page 161 |
| 0x16 | TXIDL3 | Transmit Idle Cell Header Control Register 3 | page 161 |
| 0x17 | TXIDL4 | Transmit Idle Cell Header Control Register 4 | page 162 |

Table 2-5 lists the control registers used for reception of traffic.

Table 2-5. Cell Receive Registers

| Port Offset Address | Name | Description | Page Number |
|---------------------|---------|---|--------------------------|
| 0x0C | CVAL | Cell Validation Control Register | page 156 |
| 0x18 | RXHDR1 | Receive Cell Header Control Register 1 | page 162 |
| 0x19 | RXHDR2 | Receive Cell Header Control Register 2 | page 163 |
| 0x1A | RXHDR3 | Receive Cell Header Control Register 3 | page 163 |
| 0x1B | RXHDR4 | Receive Cell Header Control Register 4 | page 164 |
| 0x1C | RXMSK1 | Receive Cell Mask Control Register 1 | page 164 |
| 0x1D | RXMSK2 | Receive Cell Mask Control Register 2 | page 165 |
| 0x1E | RXMSK3 | Receive Cell Mask Control Register 3 | page 165 |
| 0x1F | RXMSK4 | Receive Cell Mask Control Register 4 | page 166 |
| 0x20 | RXIDL1 | Receive Idle Cell Header Control Register 1 | page 166 |
| 0x21 | RXIDL2 | Receive Idle Cell Header Control Register 2 | page 167 |
| 0x22 | RXIDL3 | Receive Idle Cell Header Control Register 3 | page 167 |
| 0x23 | RXIDL4 | Receive Idle Cell Header Control Register 4 | page 168 |
| 0x24 | IDLMSK1 | Receive Idle Cell Mask Control Register 1 | page 168 |
| 0x25 | IDLMSK2 | Receive Idle Cell Mask Control Register 2 | page 169 |
| 0x26 | IDLMSK3 | Receive Idle Cell Mask Control Register 3 | page 169 |
| 0x27 | IDLMSK4 | Receive Idle Cell Mask Control Register 4 | page 170 |

Table 2-6 lists the control registers for the UTOPIA operations.

Table 2-6. UTOPIA Registers

| Port Offset Address | Name | Description | Page Number |
|---------------------|-------|---------------------------|--------------------------|
| 0x0D | UTOP1 | UTOPIA Control Register 1 | page 157 |
| 0x0E | UTOP2 | UTOPIA Control Register 2 | page 157 |

Table 2-7 and Table 2-8 list interrupt enables, interrupt indications, and status information.

Table 2-7. Status and Interrupt Registers

| Port Address | Name | Description | Page Number |
|--------------|------------|---|--------------------------|
| 0xF05 | SUMPORT0 | Summary Port Interrupt Status Register 0 | page 181 |
| 0xF06 | ENSUMPORT0 | Summary Port Interrupt Control Register 0 | page 181 |
| 0xF07 | SUMPORT1 | Summary Port Interrupt Status Register 1 | page 182 |
| 0xF08 | ENSUMPORT1 | Summary Port Interrupt Control Register 1 | page 182 |
| 0xF09 | SUMPORT2 | Summary Port Interrupt Status Register 2 | page 183 |
| 0xF0A | ENSUMPORT2 | Summary Port Interrupt Control Register 2 | page 183 |
| 0xF0B | SUMPORT3 | Summary Port Interrupt Status Register 3 | page 184 |
| 0xF0C | ENSUMPORT3 | Summary Port Interrupt Control Register 3 | page 184 |

Table 2-8. Status and Interrupt Registers (Offset Registers)

| Port Offset Address | Name | Description | Page Number |
|---------------------|-----------|--|--------------------------|
| 0x00 | SUMINT | Summary Interrupt Indication Status Register | page 150 |
| 0x01 | ENSUMINT | Summary Interrupt Control Register | page 151 |
| 0x28 | ENCELLT | Transmit Cell Interrupt Control Register | page 170 |
| 0x29 | ENCELLR | Receive Cell Interrupt Control Register) | page 171 |
| 0x2C | TXCELLINT | Transmit Cell Interrupt Indication Status Register | page 171 |
| 0x2D | RXCELLINT | Receive Cell Interrupt Indication Status Register | page 172 |
| 0x2E | TXCELL | Transmit Cell Status Register | page 172 |
| 0x2F | RXCELL | Receive Cell Status Register | page 173 |

Table 2-9 lists the M2852x's counters. When the counters fill, they saturate and do not roll over. The counts have been sized to ensure against saturation within a one-second interval. Therefore, when one-second latching is enabled, the counters are read and cleared before they can saturate. All counters are cleared when read.

Table 2-9. Counters

| Port Offset Address | Name | Description | Page Number |
|---------------------|---------|---------------------------------------|--------------------------|
| 0x30 | IDLCNTL | Idle Cell Receive Counter [Low Byte] | page 173 |
| 0x31 | IDLCNTH | Idle Cell Receive Counter [High Byte] | page 174 |
| 0x33 | LODCNT | LOCD Event Counter | page 174 |
| 0x34 | TXCNTL | Transmitted Cell Counter [Low Byte] | page 175 |
| 0x35 | TXCNTH | Transmitted Cell Counter [High Byte] | page 175 |
| 0x37 | CORRCNT | Corrected HEC Error Counter | page 176 |
| 0x38 | RXCNTL | Received Cell Counter [Low Byte] | page 176 |
| 0x39 | RXCNTH | Received Cell Counter [High Byte] | page 177 |
| 0x3B | UNCCNT | Uncorrected HEC Error Counter | page 177 |
| 0x3C | NONCNTL | Non-matching Cell Counter [Low Byte] | page 178 |
| 0x3D | NONCNTH | Non-matching Cell Counter [High Byte] | page 178 |

Table 2-10 lists IMA control and status information.

Table 2-10. IMA Control and Status Registers (1 of 33)

| Address | Name | Description | Page Number |
|---------|--------------------------|------------------------------|--------------------------|
| 0x800 | IMA_VER_1_CONFIG | Device Version I | page 189 |
| 0x801 | IMA_VER_2_CONFIG | Device Version II | page 189 |
| 0x802 | IMA_SUBSYS_CONFIG | Configuration Control | page 190 |
| 0x803 | IMA_MISC_STATUS | Miscellaneous Status | page 190 |
| 0x804 | IMA_MISC_CONFIG | Miscellaneous Control | page 191 |
| 0x805 | IMA_MEM_LOW_TEST | Memory Test Address | page 191 |
| 0x806 | IMA_MEM_HI_TEST | Memory Test Address | page 192 |
| 0x807 | IMA_MEM_TEST_CTL | Memory Test Control | page 192 |
| 0x808 | IMA_MEM_TEST_DATA | Memory Test Data | page 192 |
| 0x809 | IMA_LNK_DIAG_CTL | Link Diagnostic Control | page 192 |
| 0x80a | IMA_LNK_DIFF_DEL | Link Differential Delay | page 192 |
| 0x80b | IMA_RCV_LNK_ANOMALIES | Receive Link Anomalies | page 193 |
| 0x80c | IMA_PHY_LOOPBACK | IMA Phy Side UTOPIA Loopback | page 194 |
| 0x80e | IMA_DIAG_XOR_BIT | Address Diagnostic | page 194 |
| 0x80f | IMA_DIAG | Diagnostic Register | page 194 |
| 0x810 | IMA_TIM_REF_MUX_CTL_ADDR | TRL Control Address | page 195 |

Table 2-10. IMA Control and Status Registers (2 of 33)

| Address | Name | Description (Continued) | Page Number |
|---|-----------------------------|---|--------------------------|
| 0x811 | IMA_TIM_REF_MUX_CTL_DATA | TRL Control Data | page 196 |
| 0x812 | IMA_RX_PERSIST_CONFIG | Receive Persistence | page 197 |
| 0x813 | IMA_ATM_UTOPIA_BUS_CTL | ATM UTOPIA Control | page 197 |
| 0x814 | IMA_DIFF_DELAY_ADDR | Diff. Delay Control Address | page 198 |
| 0x815 | IMA_DIFF_DELAY_DATA | Diff. Delay Control Data | page 198 |
| 0x816 | IMA_DSL_CLOCK_GEN_ADDR | DSL Clock Generator Control Address | page 199 |
| 0x817 | IMA_DSL_CLOCK_GEN_DATA | DSL Clock Generator Control Data | page 200 |
| 0x818 | IMA_RX_TRANS_TABLE | Receive Translation Table Address | page 201 |
| 0x819 | IMA_RX_ATM_TRANS_TABLE | Receive Translation Table Internal Channel | page 202 |
| 0x81b | IMA_TX_TRANS_TABLE | Transmit Translation Table Address | page 203 |
| 0x81c | IMA_TX_ATM_TRANS_TABLE | Transmit Translation Table Internal Channel | page 203 |
| 0x81e | IMA_LNK_SEM | Link Table Control | page 230 |
| 0x81f | IMA_GRP_1TO4_SEM | Groups 1–4 Table Control | page 204 |
| 0x91f | IMA_GRP_5TO8_SEM | Groups 5–8 Table Control | page 204 |
| 0xa1f | IMA_GRP_9TO12_SEM | Groups 9–12 Table Control | page 205 |
| 0xb1f | IMA_GRP_13TO16_SEM | Groups 13–16 Table Control | page 206 |
| 0xc1f | IMA_GRP_17TO20_SEM | Groups 17–20 Table Control | page 206 |
| 0xc9f | IMA_GRP_21TO24_SEM | Groups 21–24 Table Control | page 207 |
| 0xd1f | IMA_GRP_25TO28_SEM | Groups 25–28 Table Control | page 207 |
| 0xd9f | IMA_GRP_29TO32_SEM | Groups 29–32 Table Control | page 208 |
| Transmit Groups 1–4 Configuration Tables | | | |
| 0x820 | IMA_TX_GRP1_RX_TEST_PATTERN | Tx GRP 1 Rx Test Pattern | page 208 |
| 0x821 | IMA_TX_GRP1_CTL | Tx GRP 1 Control | page 209 |
| 0x822 | IMA_TX_GRP1_FIRST_PHY_ADDR | Tx GRP 1 First Link Address | page 210 |
| 0x823 | IMA_TX_GRP1_ID | Tx GRP 1 Tx Group ID | page 211 |
| 0x824 | IMA_TX_GRP1_STAT_CTL | Tx GRP 1 Status / Control | page 212 |
| 0x825 | IMA_TX_GRP1_TIMING_INFO | Tx GRP 1 Timing Control | page 213 |
| 0x826 | IMA_TX_GRP1_TEST_CTL | Tx GRP 1 Test Control | page 214 |
| 0x827 | IMA_TX_GRP1_TX_TEST_PATTERN | Tx GRP 1 Tx Test Pattern | page 215 |
| 0x828 | IMA_TX_GRP2_RX_TEST_PATTERN | Tx GRP 2 Rx Test Pattern | page 208 |
| 0x829 | IMA_TX_GRP2_CTL | Tx GRP 2 Control | page 209 |
| 0x82a | IMA_TX_GRP2_FIRST_PHY_ADDR | Tx GRP 2 First Link Address | page 210 |
| 0x82b | IMA_TX_GRP2_ID | Tx GRP 2 Tx Group ID | page 211 |
| 0x82c | IMA_TX_GRP2_STAT_CTL | Tx GRP 2 Status / Control | page 212 |
| 0x82d | IMA_TX_GRP2_TIMING_INFO | Tx GRP 2 Timing Control | page 213 |

Table 2-10. IMA Control and Status Registers (3 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|-----------------------------|--|--------------------------|
| 0x82e | IMA_TX_GRP2_TEST_CTL | Tx GRP 2 Test Control | page 214 |
| 0x82f | IMA_TX_GRP2_TX_TEST_PATTERN | Tx GRP 2 Tx Test Pattern | page 215 |
| 0x830 | IMA_TX_GRP3_RX_TEST_PATTERN | Tx GRP 3 Rx Test Pattern | page 208 |
| 0x831 | IMA_TX_GRP3_CTL | Tx GRP 3 Control | page 209 |
| 0x832 | IMA_TX_GRP3_FIRST_PHY_ADDR | Tx GRP 3 First Link Address | page 210 |
| 0x833 | IMA_TX_GRP3_ID | Tx GRP 3 Tx Group ID | page 211 |
| 0x834 | IMA_TX_GRP3_STAT_CTL | Tx GRP 3 Status / Control | page 212 |
| 0x835 | IMA_TX_GRP3_TIMING_INFO | Tx GRP 3 Timing Control | page 213 |
| 0x836 | IMA_TX_GRP3_TEST_CTL | Tx GRP 3 Test Control | page 214 |
| 0x837 | IMA_TX_GRP3_TX_TEST_PATTERN | Tx GRP 3 Tx Test Pattern | page 215 |
| 0x838 | IMA_TX_GRP4_RX_TEST_PATTERN | Tx GRP 4 Rx Test Pattern | page 208 |
| 0x839 | IMA_TX_GRP4_CTL | Tx GRP 4 Control | page 209 |
| 0x83a | IMA_TX_GRP4_FIRST_PHY_ADDR | Tx GRP 4 First Link Address | page 210 |
| 0x83b | IMA_TX_GRP4_ID | Tx GRP 4 Tx Group ID | page 211 |
| 0x83c | IMA_TX_GRP4_STAT_CTL | Tx GRP 4 Status / Control | page 212 |
| 0x83d | IMA_TX_GRP4_TIMING_INFO | Tx GRP 4 Timing Control | page 213 |
| 0x83e | IMA_TX_GRP4_TEST_CTL | Tx GRP 4 Test Control | page 214 |
| 0x83f | IMA_TX_GRP4_TX_TEST_PATTERN | Tx GRP 4 Tx Test Pattern | page 215 |
| Tx UTOPIA Addresses 0 - 3 Cell Counters | | | |
| 0x840 | IMA_TX_ATM0_CELL_COUNT_LSB | Transmit UTOPIA Address 0x00 Cell Count LSBs | page 216 |
| 0x841 | IMA_TX_ATM0_CELL_COUNT_MSB | Transmit UTOPIA Address 0x00 Cell Count MSBs | |
| 0x842 | IMA_TX_ATM1_CELL_COUNT_LSB | Transmit UTOPIA Address 0x01 Cell Count LSBs | |
| 0x843 | IMA_TX_ATM1_CELL_COUNT_MSB | Transmit UTOPIA Address 0x01 Cell Count MSBs | |
| 0x844 | IMA_TX_ATM2_CELL_COUNT_LSB | Transmit UTOPIA Address 0x02 Cell Count LSBs | |
| 0x845 | IMA_TX_ATM2_CELL_COUNT_MSB | Transmit UTOPIA Address 0x02 Cell Count MSBs | |
| 0x846 | IMA_TX_ATM3_CELL_COUNT_LSB | Transmit UTOPIA Address 0x03 Cell Count LSBs | |
| 0x847 | IMA_TX_ATM3_CELL_COUNT_MSB | Transmit UTOPIA Address 0x03 Cell Count MSBs | |
| Rx UTOPIA Addresses 0 - 3 Cell Counters | | | |
| 0x850 | IMA_RX_ATM0_CELL_COUNT_LSB | Receive UTOPIA Address 0x00 Cell Count LSBs | page 218 |
| 0x851 | IMA_RX_ATM0_CELL_COUNT_MSB | Receive UTOPIA Address 0x00 Cell Count MSBs | |
| 0x852 | IMA_RX_ATM1_CELL_COUNT_LSB | Receive UTOPIA Address 0x01 Cell Count LSBs | |
| 0x853 | IMA_RX_ATM1_CELL_COUNT_MSB | Receive UTOPIA Address 0x01 Cell Count MSBs | |
| 0x854 | IMA_RX_ATM2_CELL_COUNT_LSB | Receive UTOPIA Address 0x02 Cell Count LSBs | |
| 0x855 | IMA_RX_ATM2_CELL_COUNT_MSB | Receive UTOPIA Address 0x02 Cell Count MSBs | |
| 0x856 | IMA_RX_ATM3_CELL_COUNT_LSB | Receive UTOPIA Address 0x03 Cell Count LSBs | |
| 0x857 | IMA_RX_ATM3_CELL_COUNT_MSB | Receive UTOPIA Address 0x03 Cell Count MSBs | |

Table 2-10. IMA Control and Status Registers (4 of 33)

| Address | Name | Description (Continued) | Page Number |
|------------------------------------|-------------------|-------------------------|-------------|
| Port 0–7 Control and Status | | | |
| 0x860 | IMA_TX_LNK0_CTL | Tx Link 0 Control | page 232 |
| 0x861 | IMA_TX_LNK1_CTL | Tx Link 1 Control | |
| 0x862 | IMA_TX_LNK2_CTL | Tx Link 2 Control | |
| 0x863 | IMA_TX_LNK3_CTL | Tx Link 3 Control | |
| 0x864 | IMA_TX_LNK4_CTL | Tx Link 4 Control | |
| 0x865 | IMA_TX_LNK5_CTL | Tx Link 5 Control | |
| 0x866 | IMA_TX_LNK6_CTL | Tx Link 6 Control | |
| 0x867 | IMA_TX_LNK7_CTL | Tx Link 7 Control | |
| 0x868 | IMA_TX_LNK0_STATE | Tx Link 0 Status | page 233 |
| 0x869 | IMA_TX_LNK1_STATE | Tx Link 1 Status | |
| 0x86a | IMA_TX_LNK2_STATE | Tx Link 2 Status | |
| 0x86b | IMA_TX_LNK3_STATE | Tx Link 3 Status | |
| 0x86c | IMA_TX_LNK4_STATE | Tx Link 4 Status | |
| 0x86d | IMA_TX_LNK5_STATE | Tx Link 5 Status | |
| 0x86e | IMA_TX_LNK6_STATE | Tx Link 6 Status | |
| 0x86f | IMA_TX_LNK7_STATE | Tx Link 7 Status | |
| 0x870 | IMA_TX_LNK0_ID | Tx Link 0 Assigned LID | page 234 |
| 0x871 | IMA_TX_LNK1_ID | Tx Link 1 Assigned LID | |
| 0x872 | IMA_TX_LNK2_ID | Tx Link 2 Assigned LID | |
| 0x873 | IMA_TX_LNK3_ID | Tx Link 3 Assigned LID | |
| 0x874 | IMA_TX_LNK4_ID | Tx Link 4 Assigned LID | |
| 0x875 | IMA_TX_LNK5_ID | Tx Link 5 Assigned LID | |
| 0x876 | IMA_TX_LNK6_ID | Tx Link 6 Assigned LID | |
| 0x877 | IMA_TX_LNK7_ID | Tx Link 7 Assigned LID | |
| 0x880 | IMA_RX_LNK0_CTL | Rx Link 0 Control | page 235 |
| 0x881 | IMA_RX_LNK1_CTL | Rx Link 1 Control | |
| 0x882 | IMA_RX_LNK2_CTL | Rx Link 2 Control | |
| 0x883 | IMA_RX_LNK3_CTL | Rx Link 3 Control | |
| 0x884 | IMA_RX_LNK4_CTL | Rx Link 4 Control | |
| 0x885 | IMA_RX_LNK5_CTL | Rx Link 5 Control | |
| 0x886 | IMA_RX_LNK6_CTL | Rx Link 6 Control | |
| 0x887 | IMA_RX_LNK7_CTL | Rx Link 7 Control | |
| 0x888 | IMA_RX_LNK0_STATE | Rx Link 0 Status | page 236 |
| 0x889 | IMA_RX_LNK1_STATE | Rx Link 1 Status | |
| 0x88a | IMA_RX_LNK2_STATE | Rx Link 2 Status | |
| 0x88b | IMA_RX_LNK3_STATE | Rx Link 3 Status | |
| 0x88c | IMA_RX_LNK4_STATE | Rx Link 4 Status | |
| 0x88d | IMA_RX_LNK5_STATE | Rx Link 5 Status | |
| 0x88e | IMA_RX_LNK6_STATE | Rx Link 6 Status | |
| 0x88f | IMA_RX_LNK7_STATE | Rx Link 7 Status | |

Table 2-10. IMA Control and Status Registers (5 of 33)

| Address | Name | Description (Continued) | Page Number |
|---------|---------------------|---------------------------|-------------|
| 0x890 | IMA_RX_LNK0_DEFECT | Rx Link 0 Defects | page 237 |
| 0x891 | IMA_RX_LNK1_DEFECT | Rx Link 1 Defects | |
| 0x892 | IMA_RX_LNK2_DEFECT | Rx Link 2 Defects | |
| 0x893 | IMA_RX_LNK3_DEFECT | Rx Link 3 Defects | |
| 0x894 | IMA_RX_LNK4_DEFECT | Rx Link 4 Defects | |
| 0x895 | IMA_RX_LNK5_DEFECT | Rx Link 5 Defects | |
| 0x896 | IMA_RX_LNK6_DEFECT | Rx Link 6 Defects | |
| 0x897 | IMA_RX_LNK7_DEFECT | Rx Link 7 Defects | |
| 0x898 | IMA_FE_TX_LNK0_CFG | FE Tx Link 0 Link Config | page 238 |
| 0x899 | IMA_FE_TX_LNK1_CFG | FE Tx Link 1 Link Config | |
| 0x89a | IMA_FE_TX_LNK2_CFG | FE Tx Link 2 Link Config | |
| 0x89b | IMA_FE_TX_LNK3_CFG | FE Tx Link 3 Link Config | |
| 0x89c | IMA_FE_TX_LNK4_CFG | FE Tx Link 4 Link Config | |
| 0x89d | IMA_FE_TX_LNK5_CFG | FE Tx Link 5 Link Config | |
| 0x89e | IMA_FE_TX_LNK6_CFG | FE Tx Link 6 Link Config | |
| 0x89f | IMA_FE_TX_LNK7_CFG | FE Tx Link 7 Link Config | |
| 0x8a0 | IMA_FE_LNK0_STATE | Rx Link 0 FE Status | page 239 |
| 0x8a1 | IMA_FE_LNK1_STATE | Rx Link 1 FE Status | |
| 0x8a2 | IMA_FE_LNK2_STATE | Rx Link 2 FE Status | |
| 0x8a3 | IMA_FE_LNK3_STATE | Rx Link 3 FE Status | |
| 0x8a4 | IMA_FE_LNK4_STATE | Rx Link 4 FE Status | |
| 0x8a5 | IMA_FE_LNK5_STATE | Rx Link 5 FE Status | |
| 0x8a6 | IMA_FE_LNK6_STATE | Rx Link 6 FE Status | |
| 0x8a7 | IMA_FE_LNK7_STATE | Rx Link 7 FE Status | |
| 0x8a8 | IMA_RX_LNK0_ID | Rx Link 0 Assigned LID | page 240 |
| 0x8a9 | IMA_RX_LNK1_ID | Rx Link 1 Assigned LID | |
| 0x8aa | IMA_RX_LNK2_ID | Rx Link 2 Assigned LID | |
| 0x8ab | IMA_RX_LNK3_ID | Rx Link 3 Assigned LID | |
| 0x8ac | IMA_RX_LNK4_ID | Rx Link 4 Assigned LID | |
| 0x8ad | IMA_RX_LNK5_ID | Rx Link 5 Assigned LID | |
| 0x8ae | IMA_RX_LNK6_ID | Rx Link 6 Assigned LID | |
| 0x8af | IMA_RX_LNK7_ID | Rx Link 7 Assigned LID | |
| 0x8b0 | IMA_RX_LNK0_IV_CNT | Rx Link 0 IV-IMA Counter | page 241 |
| 0x8b1 | IMA_RX_LNK1_IV_CNT | Rx Link 1 IV-IMA Counter | |
| 0x8b2 | IMA_RX_LNK2_IV_CNT | Rx Link 2 IV-IMA Counter | |
| 0x8b3 | IMA_RX_LNK3_IV_CNT | Rx Link 3 IV-IMA Counter | |
| 0x8b4 | IMA_RX_LNK4_IV_CNT | Rx Link 4 IV-IMA Counter | |
| 0x8b5 | IMA_RX_LNK5_IV_CNT | Rx Link 5 IV-IMA Counter | |
| 0x8b6 | IMA_RX_LNK6_IV_CNT | Rx Link 6 IV-IMA Counter | |
| 0x8b7 | IMA_RX_LNK7_IV_CNT | Rx Link 7 IV-IMA Counter | |
| 0x8b8 | IMA_RX_LNK0_OIF_CNT | Rx Link 0 OIF-IMA Counter | page 242 |
| 0x8b9 | IMA_RX_LNK1_OIF_CNT | Rx Link 1 OIF-IMA Counter | |
| 0x8ba | IMA_RX_LNK2_OIF_CNT | Rx Link 2 OIF-IMA Counter | |
| 0x8bb | IMA_RX_LNK3_OIF_CNT | Rx Link 3 OIF-IMA Counter | |
| 0x8bc | IMA_RX_LNK4_OIF_CNT | Rx Link 4 OIF-IMA Counter | |
| 0x8bd | IMA_RX_LNK5_OIF_CNT | Rx Link 5 OIF-IMA Counter | |
| 0x8be | IMA_RX_LNK6_OIF_CNT | Rx Link 6 OIF-IMA Counter | |
| 0x8bf | IMA_RX_LNK7_OIF_CNT | Rx Link 7 OIF-IMA Counter | |

Table 2-10. IMA Control and Status Registers (6 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|-----------------------------|-----------------------------|--------------------------|
| 0x8c0 | IMA_FE_TX_LNK0_GRP_ID | Rx Link 0 Captured GRP ID | page 243 |
| 0x8c1 | IMA_FE_TX_LNK1_GRP_ID | Rx Link 1 Captured GRP ID | |
| 0x8c2 | IMA_FE_TX_LNK2_GRP_ID | Rx Link 2 Captured GRP ID | |
| 0x8c3 | IMA_FE_TX_LNK3_GRP_ID | Rx Link 3 Captured GRP ID | |
| 0x8c4 | IMA_FE_TX_LNK4_GRP_ID | Rx Link 4 Captured GRP ID | |
| 0x8c5 | IMA_FE_TX_LNK5_GRP_ID | Rx Link 5 Captured GRP ID | |
| 0x8c6 | IMA_FE_TX_LNK6_GRP_ID | Rx Link 6 Captured GRP ID | |
| 0x8c7 | IMA_FE_TX_LNK7_GRP_ID | Rx Link 7 Captured GRP ID | |
| Receive Groups 1–4 Configuration Tables | | | |
| 0x8d0 | IMA_RX_GRP1_CFG | Rx GRP 1 Configuration | page 220 |
| 0x8d1 | IMA_RX_GRP1_CTL | Rx GRP 1 Control | page 221 |
| 0x8d2 | IMA_RX_GRP1_FIRST_PHY_ADDR | Rx GRP 1 First Link Address | page 222 |
| 0x8d3 | IMA_RX_GRP1_ID | Rx GRP 1 Rx Group ID | page 223 |
| 0x8d4 | IMA_RX_GRP2_CFG | Rx GRP 2 Configuration | page 220 |
| 0x8d5 | IMA_RX_GRP2_CTL | Rx GRP 2 Control | page 221 |
| 0x8d6 | IMA_RX_GRP2_FIRST_PHY_ADDR | Rx GRP 2 First Link Address | page 222 |
| 0x8d7 | IMA_RX_GRP2_ID | Rx GRP 2 Rx Group ID | page 223 |
| 0x8d8 | IMA_RX_GRP3_CFG | Rx GRP 3 Configuration | page 220 |
| 0x8d9 | IMA_RX_GRP3_CTL | Rx GRP 3 Control | page 221 |
| 0x8da | IMA_RX_GRP3_FIRST_PHY_ADDR | Rx GRP 3 First Link Address | page 222 |
| 0x8db | IMA_RX_GRP3_ID | Rx GRP 3 Rx Group ID | page 223 |
| 0x8dc | IMA_RX_GRP4_CFG | Rx GRP 4 Configuration | page 220 |
| 0x8dd | IMA_RX_GRP4_CTL | Rx GRP 4 Control | page 221 |
| 0x8de | IMA_RX_GRP4_FIRST_PHY_ADDR | Rx GRP 4 First Link Address | page 222 |
| 0x8df | IMA_RX_GRP4_ID | Rx GRP 4 Rx Group ID | page 223 |
| Receive Groups 1–4 Far-End Status | | | |
| 0x8e0 | IMA_RX_GRP1_RX_TEST_PATTERN | Rx GRP 1 Rx Test Pattern | page 224 |
| 0x8e2 | IMA_RX_GRP1_STAT_CTL_CHANGE | Rx GRP 1 SCCI | page 225 |
| 0x8e3 | IMA_RX_GRP1_ACTUAL_GRP_ID | Rx GRP 1 Rx Group ID | page 226 |
| 0x8e4 | IMA_RX_GRP1_STAT_CTL | Rx GRP 1 Status / Control | page 227 |
| 0x8e5 | IMA_RX_GRP1_TIMING_INFO | Rx GRP 1 Timing Control | page 228 |
| 0x8e6 | IMA_RX_GRP1_TEST_CTL | Rx GRP 1 Test Control | page 229 |
| 0x8e7 | IMA_RX_GRP1_TX_TEST_PATTERN | Rx GRP 1 Tx Test Pattern | page 230 |
| 0x8e8 | IMA_RX_GRP2_RX_TEST_PATTERN | Rx GRP 2 Rx Test Pattern | page 224 |
| 0x8ea | IMA_RX_GRP2_STAT_CTL_CHANGE | Rx GRP 2 SCCI | page 225 |
| 0x8eb | IMA_RX_GRP2_ACTUAL_GRP_ID | Rx GRP 2 Rx Group ID | page 226 |
| 0x8ec | IMA_RX_GRP2_STAT_CTL | Rx GRP 2 Status / Control | page 227 |

Table 2-10. IMA Control and Status Registers (7 of 33)

| Address | Name | Description (Continued) | Page Number |
|---|-----------------------------|-----------------------------|--------------------------|
| 0x8ed | IMA_RX_GRP2_TIMING_INFO | Rx GRP 2 Timing Control | page 228 |
| 0x8ee | IMA_RX_GRP2_TEST_CTL | Rx GRP 2 Test Control | page 229 |
| 0x8ef | IMA_RX_GRP2_TX_TEST_PATTERN | Rx GRP 2 Tx Test Pattern | page 230 |
| 0x8f0 | IMA_RX_GRP3_RX_TEST_PATTERN | Rx GRP 3 Rx Test Pattern | page 224 |
| 0x8f2 | IMA_RX_GRP3_STAT_CTL_CHANGE | Rx GRP 3 SCCI | page 225 |
| 0x8f3 | IMA_RX_GRP3_ACTUAL_GRP_ID | Rx GRP 3 Rx Group ID | page 226 |
| 0x8f4 | IMA_RX_GRP3_STAT_CTL | Rx GRP 3 Status / Control | page 227 |
| 0x8f5 | IMA_RX_GRP3_TIMING_INFO | Rx GRP 3 Timing Control | page 228 |
| 0x8f6 | IMA_RX_GRP3_TEST_CTL | Rx GRP 3 Test Control | page 229 |
| 0x8f7 | IMA_RX_GRP3_TX_TEST_PATTERN | Rx GRP 3 Tx Test Pattern | page 230 |
| 0x8f8 | IMA_RX_GRP4_RX_TEST_PATTERN | Rx GRP 4 Rx Test Pattern | page 224 |
| 0x8fa | IMA_RX_GRP4_STAT_CTL_CHANGE | Rx GRP 4 SCCI | page 225 |
| 0x8fb | IMA_RX_GRP4_ACTUAL_GRP_ID | Rx GRP 4 Rx Group ID | page 226 |
| 0x8fc | IMA_RX_GRP4_STAT_CTL | Rx GRP 4 Status / Control | page 227 |
| 0x8fd | IMA_RX_GRP4_TIMING_INFO | Rx GRP 4 Timing Control | page 228 |
| 0x8fe | IMA_RX_GRP4_TEST_CTL | Rx GRP 4 Test Control | page 229 |
| 0x8ff | IMA_RX_GRP4_TX_TEST_PATTERN | Rx GRP 4 Tx Test Pattern | page 230 |
| Transmit Groups 5–8 Configuration Tables | | | |
| 0x920 | IMA_TX_GRP5_RX_TEST_PATTERN | Tx GRP 5 Rx Test Pattern | page 208 |
| 0x921 | IMA_TX_GRP5_CTL | Tx GRP 5 Control | page 209 |
| 0x922 | IMA_TX_GRP5_FIRST_PHY_ADDR | Tx GRP 5 First Link Address | page 210 |
| 0x923 | IMA_TX_GRP5_ID | Tx GRP 5 Tx Group ID | page 211 |
| 0x924 | IMA_TX_GRP5_STAT_CTL | Tx GRP 5 Status / Control | page 212 |
| 0x925 | IMA_TX_GRP5_TIMING_INFO | Tx GRP 5 Timing Control | page 213 |
| 0x926 | IMA_TX_GRP5_TEST_CTL | Tx GRP 5 Test Control | page 214 |
| 0x927 | IMA_TX_GRP5_TX_TEST_PATTERN | Tx GRP 5 Tx Test Pattern | page 215 |
| 0x928 | IMA_TX_GRP6_RX_TEST_PATTERN | Tx GRP 6 Rx Test Pattern | page 208 |
| 0x929 | IMA_TX_GRP6_CTL | Tx GRP 6 Control | page 209 |
| 0x92a | IMA_TX_GRP6_FIRST_PHY_ADDR | Tx GRP 6 First Link Address | page 210 |
| 0x92b | IMA_TX_GRP6_ID | Tx GRP 6 Tx Group ID | page 211 |
| 0x92c | IMA_TX_GRP6_STAT_CTL | Tx GRP 6 Status / Control | page 212 |
| 0x92d | IMA_TX_GRP6_TIMING_INFO | Tx GRP 6 Timing Control | page 213 |
| 0x92e | IMA_TX_GRP6_TEST_CTL | Tx GRP 6 Test Control | page 214 |
| 0x92f | IMA_TX_GRP6_TX_TEST_PATTERN | Tx GRP 6 Tx Test Pattern | page 215 |
| 0x930 | IMA_TX_GRP7_RX_TEST_PATTERN | Tx GRP 7 Rx Test Pattern | page 208 |

Table 2-10. IMA Control and Status Registers (8 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|-----------------------------|--|--------------------------|
| 0x931 | IMA_TX_GRP7_CTL | Tx GRP 7 Control | page 209 |
| 0x932 | IMA_TX_GRP7_FIRST_PHY_ADDR | Tx GRP 7 First Link Address | page 210 |
| 0x933 | IMA_TX_GRP7_ID | Tx GRP 7 Tx Group ID | page 211 |
| 0x934 | IMA_TX_GRP7_STAT_CTL | Tx GRP 7 Status / Control | page 212 |
| 0x935 | IMA_TX_GRP7_TIMING_INFO | Tx GRP 7 Timing Control | page 213 |
| 0x936 | IMA_TX_GRP7_TEST_CTL | Tx GRP 7 Test Control | page 214 |
| 0x937 | IMA_TX_GRP7_TX_TEST_PATTERN | Tx GRP 7 Tx Test Pattern | page 215 |
| 0x938 | IMA_TX_GRP8_RX_TEST_PATTERN | Tx GRP 8 Rx Test Pattern | page 208 |
| 0x939 | IMA_TX_GRP8_CTL | Tx GRP 8 Control | page 209 |
| 0x93a | IMA_TX_GRP8_FIRST_PHY_ADDR | Tx GRP 8 First Link Address | page 210 |
| 0x93b | IMA_TX_GRP8_ID | Tx GRP 8 Tx Group ID | page 211 |
| 0x93c | IMA_TX_GRP8_STAT_CTL | Tx GRP 8 Status / Control | page 212 |
| 0x93d | IMA_TX_GRP8_TIMING_INFO | Tx GRP 8 Timing Control | page 213 |
| 0x93e | IMA_TX_GRP8_TEST_CTL | Tx GRP 8 Test Control | page 214 |
| 0x93f | IMA_TX_GRP8_TX_TEST_PATTERN | Tx GRP 8 Tx Test Pattern | page 215 |
| Tx UTOPIA Addresses 4 - 7 Cell Counters | | | |
| 0x940 | IMA_TX_ATM4_CELL_COUNT_LSB | Transmit UTOPIA Address 0x04 Cell Count LSBs | page 216 |
| 0x941 | IMA_TX_ATM4_CELL_COUNT_MSB | Transmit UTOPIA Address 0x04 Cell Count MSBs | |
| 0x942 | IMA_TX_ATM5_CELL_COUNT_LSB | Transmit UTOPIA Address 0x05 Cell Count LSBs | |
| 0x943 | IMA_TX_ATM5_CELL_COUNT_MSB | Transmit UTOPIA Address 0x05 Cell Count MSBs | |
| 0x944 | IMA_TX_ATM6_CELL_COUNT_LSB | Transmit UTOPIA Address 0x06 Cell Count LSBs | |
| 0x945 | IMA_TX_ATM6_CELL_COUNT_MSB | Transmit UTOPIA Address 0x06 Cell Count MSBs | |
| 0x946 | IMA_TX_ATM7_CELL_COUNT_LSB | Transmit UTOPIA Address 0x07 Cell Count LSBs | |
| 0x947 | IMA_TX_ATM7_CELL_COUNT_MSB | Transmit UTOPIA Address 0x07 Cell Count MSBs | |
| Rx UTOPIA Addresses 4 - 7 Cell Counters | | | |
| 0x950 | IMA_RX_ATM4_CELL_COUNT_LSB | Receive UTOPIA Address 0x04 Cell Count LSBs | page 218 |
| 0x951 | IMA_RX_ATM4_CELL_COUNT_MSB | Receive UTOPIA Address 0x04 Cell Count MSBs | |
| 0x952 | IMA_RX_ATM5_CELL_COUNT_LSB | Receive UTOPIA Address 0x05 Cell Count LSBs | |
| 0x953 | IMA_RX_ATM5_CELL_COUNT_MSB | Receive UTOPIA Address 0x05 Cell Count MSBs | |
| 0x954 | IMA_RX_ATM6_CELL_COUNT_LSB | Receive UTOPIA Address 0x06 Cell Count LSBs | |
| 0x955 | IMA_RX_ATM6_CELL_COUNT_MSB | Receive UTOPIA Address 0x06 Cell Count MSBs | |
| 0x956 | IMA_RX_ATM7_CELL_COUNT_LSB | Receive UTOPIA Address 0x07 Cell Count LSBs | |
| 0x957 | IMA_RX_ATM7_CELL_COUNT_MSB | Receive UTOPIA Address 0x07 Cell Count MSBs | |

Table 2-10. IMA Control and Status Registers (9 of 33)

| Address | Name | Description (Continued) | Page Number |
|-------------------------------------|--------------------|-------------------------|-------------|
| Port 8–15 Control and Status | | | |
| 0x960 | IMA_TX_LNK8_CTL | Tx Link 8 Control | page 232 |
| 0x961 | IMA_TX_LNK9_CTL | Tx Link 9 Control | |
| 0x962 | IMA_TX_LNK10_CTL | Tx Link 10 Control | |
| 0x963 | IMA_TX_LNK11_CTL | Tx Link 11 Control | |
| 0x964 | IMA_TX_LNK12_CTL | Tx Link 12 Control | |
| 0x965 | IMA_TX_LNK13_CTL | Tx Link 13 Control | |
| 0x966 | IMA_TX_LNK14_CTL | Tx Link 14 Control | |
| 0x967 | IMA_TX_LNK15_CTL | Tx Link 15 Control | |
| 0x968 | IMA_TX_LNK8_STATE | Tx Link 8 Status | |
| 0x969 | IMA_TX_LNK9_STATE | Tx Link 9 Status | |
| 0x96a | IMA_TX_LNK10_STATE | Tx Link 10 Status | |
| 0x96b | IMA_TX_LNK11_STATE | Tx Link 11 Status | |
| 0x96c | IMA_TX_LNK12_STATE | Tx Link 12 Status | |
| 0x96d | IMA_TX_LNK13_STATE | Tx Link 13 Status | |
| 0x96e | IMA_TX_LNK14_STATE | Tx Link 14 Status | |
| 0x96f | IMA_TX_LNK15_STATE | Tx Link 15 Status | |
| 0x970 | IMA_TX_LNK8_ID | Tx Link 8 Assigned LID | page 234 |
| 0x971 | IMA_TX_LNK9_ID | Tx Link 9 Assigned LID | |
| 0x972 | IMA_TX_LNK10_ID | Tx Link 10 Assigned LID | |
| 0x973 | IMA_TX_LNK11_ID | Tx Link 11 Assigned LID | |
| 0x974 | IMA_TX_LNK12_ID | Tx Link 12 Assigned LID | |
| 0x975 | IMA_TX_LNK13_ID | Tx Link 13 Assigned LID | |
| 0x976 | IMA_TX_LNK14_ID | Tx Link 14 Assigned LID | |
| 0x977 | IMA_TX_LNK15_ID | Tx Link 15 Assigned LID | |
| 0x980 | IMA_RX_LNK8_CTL | Rx Link 8 Control | |
| 0x981 | IMA_RX_LNK9_CTL | Rx Link 9 Control | |
| 0x982 | IMA_RX_LNK10_CTL | Rx Link 10 Control | |
| 0x983 | IMA_RX_LNK11_CTL | Rx Link 11 Control | |
| 0x984 | IMA_RX_LNK12_CTL | Rx Link 12 Control | |
| 0x985 | IMA_RX_LNK13_CTL | Rx Link 13 Control | |
| 0x986 | IMA_RX_LNK14_CTL | Rx Link 14 Control | |
| 0x987 | IMA_RX_LNK15_CTL | Rx Link 15 Control | |
| 0x988 | IMA_RX_LNK8_STATE | Rx Link 8 Status | page 236 |
| 0x989 | IMA_RX_LNK9_STATE | Rx Link 9 Status | |
| 0x98a | IMA_RX_LNK10_STATE | Rx Link 10 Status | |
| 0x98b | IMA_RX_LNK11_STATE | Rx Link 11 Status | |
| 0x98c | IMA_RX_LNK12_STATE | Rx Link 12 Status | |
| 0x98d | IMA_RX_LNK13_STATE | Rx Link 13 Status | |
| 0x98e | IMA_RX_LNK14_STATE | Rx Link 14 Status | |
| 0x98f | IMA_RX_LNK15_STATE | Rx Link 15 Status | |

Table 2-10. IMA Control and Status Registers (10 of 33)

| Address | Name | Description (Continued) | Page Number |
|---------|----------------------|----------------------------|-------------|
| 0x990 | IMA_RX_LNK8_DEFECT | Rx Link 8 Defects | page 237 |
| 0x991 | IMA_RX_LNK9_DEFECT | Rx Link 9 Defects | |
| 0x992 | IMA_RX_LNK10_DEFECT | Rx Link 10 Defects | |
| 0x993 | IMA_RX_LNK11_DEFECT | Rx Link 11 Defects | |
| 0x994 | IMA_RX_LNK12_DEFECT | Rx Link 12 Defects | |
| 0x995 | IMA_RX_LNK13_DEFECT | Rx Link 13 Defects | |
| 0x996 | IMA_RX_LNK14_DEFECT | Rx Link 14 Defects | |
| 0x997 | IMA_RX_LNK15_DEFECT | Rx Link 15 Defects | |
| 0x998 | IMA_FE_TX_LNK8_CFG | FE Tx Link 8 Link Config | page 238 |
| 0x999 | IMA_FE_TX_LNK9_CFG | FE Tx Link 9 Link Config | |
| 0x99a | IMA_FE_TX_LNK10_CFG | FE Tx Link 10 Link Config | |
| 0x99b | IMA_FE_TX_LNK11_CFG | FE Tx Link 11 Link Config | |
| 0x99c | IMA_FE_TX_LNK12_CFG | FE Tx Link 12 Link Config | |
| 0x99d | IMA_FE_TX_LNK13_CFG | FE Tx Link 13 Link Config | |
| 0x99e | IMA_FE_TX_LNK14_CFG | FE Tx Link 14 Link Config | |
| 0x99f | IMA_FE_TX_LNK15_CFG | FE Tx Link 15 Link Config | |
| 0x9a0 | IMA_FE_LNK8_STATE | Rx Link 8 FE Status | page 239 |
| 0x9a1 | IMA_FE_LNK9_STATE | Rx Link 9 FE Status | |
| 0x9a2 | IMA_FE_LNK10_STATE | Rx Link 10 FE Status | |
| 0x9a3 | IMA_FE_LNK11_STATE | Rx Link 11 FE Status | |
| 0x9a4 | IMA_FE_LNK12_STATE | Rx Link 12 FE Status | |
| 0x9a5 | IMA_FE_LNK13_STATE | Rx Link 13 FE Status | |
| 0x9a6 | IMA_FE_LNK14_STATE | Rx Link 14 FE Status | |
| 0x9a7 | IMA_FE_LNK15_STATE | Rx Link 15 FE Status | |
| 0x9a8 | IMA_RX_LNK8_ID | Rx Link 8 Assigned LID | page 240 |
| 0x9a9 | IMA_RX_LNK9_ID | Rx Link 9 Assigned LID | |
| 0x9aa | IMA_RX_LNK10_ID | Rx Link 10 Assigned LID | |
| 0x9ab | IMA_RX_LNK11_ID | Rx Link 11 Assigned LID | |
| 0x9ac | IMA_RX_LNK12_ID | Rx Link 12 Assigned LID | |
| 0x9ad | IMA_RX_LNK13_ID | Rx Link 13 Assigned LID | |
| 0x9ae | IMA_RX_LNK14_ID | Rx Link 14 Assigned LID | |
| 0x9af | IMA_RX_LNK15_ID | Rx Link 15 Assigned LID | |
| 0x9b0 | IMA_RX_LNK8_IV_CNT | Rx Link 8 IV-IMA Counter | page 241 |
| 0x9b1 | IMA_RX_LNK9_IV_CNT | Rx Link 9 IV-IMA Counter | |
| 0x9b2 | IMA_RX_LNK10_IV_CNT | Rx Link 10 IV-IMA Counter | |
| 0x9b3 | IMA_RX_LNK11_IV_CNT | Rx Link 11 IV-IMA Counter | |
| 0x9b4 | IMA_RX_LNK12_IV_CNT | Rx Link 12 IV-IMA Counter | |
| 0x9b5 | IMA_RX_LNK13_IV_CNT | Rx Link 13 IV-IMA Counter | |
| 0x9b6 | IMA_RX_LNK14_IV_CNT | Rx Link 14 IV-IMA Counter | |
| 0x9b7 | IMA_RX_LNK15_IV_CNT | Rx Link 15 IV-IMA Counter | |
| 0x9b8 | IMA_RX_LNK8_OIF_CNT | Rx Link 8 OIF-IMA Counter | page 242 |
| 0x9b9 | IMA_RX_LNK9_OIF_CNT | Rx Link 9 OIF-IMA Counter | |
| 0x9ba | IMA_RX_LNK10_OIF_CNT | Rx Link 10 OIF-IMA Counter | |
| 0x9bb | IMA_RX_LNK11_OIF_CNT | Rx Link 11 OIF-IMA Counter | |
| 0x9bc | IMA_RX_LNK12_OIF_CNT | Rx Link 12 OIF-IMA Counter | |
| 0x9bd | IMA_RX_LNK13_OIF_CNT | Rx Link 13 OIF-IMA Counter | |
| 0x9be | IMA_RX_LNK14_OIF_CNT | Rx Link 14 OIF-IMA Counter | |
| 0x9bf | IMA_RX_LNK15_OIF_CNT | Rx Link 15 OIF-IMA Counter | |

Table 2-10. IMA Control and Status Registers (11 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|-----------------------------|-----------------------------|-------------|
| 0x9c0 | IMA_FE_TX_LNK8_GRP_ID | Rx Link 8 Captured GRP ID | page 243 |
| 0x9c1 | IMA_FE_TX_LNK9_GRP_ID | Rx Link 9 Captured GRP ID | |
| 0x9c2 | IMA_FE_TX_LNK10_GRP_ID | Rx Link 10 Captured GRP ID | |
| 0x9c3 | IMA_FE_TX_LNK11_GRP_ID | Rx Link 11 Captured GRP ID | |
| 0x9c4 | IMA_FE_TX_LNK12_GRP_ID | Rx Link 12 Captured GRP ID | |
| 0x9c5 | IMA_FE_TX_LNK13_GRP_ID | Rx Link 13 Captured GRP ID | |
| 0x9c6 | IMA_FE_TX_LNK14_GRP_ID | Rx Link 14 Captured GRP ID | |
| 0x9c7 | IMA_FE_TX_LNK15_GRP_ID | Rx Link 15 Captured GRP ID | |
| Receive Groups 5–8 Configuration Tables | | | |
| 0x9d0 | IMA_RX_GRP5_CFG | Rx GRP 5 Configuration | page 220 |
| 0x9d1 | IMA_RX_GRP5_CTL | Rx GRP 5 Control | page 221 |
| 0x9d2 | IMA_RX_GRP5_FIRST_PHY_ADDR | Rx GRP 5 First Link Address | page 222 |
| 0x9d3 | IMA_RX_GRP5_ID | Rx GRP 5 Rx Group ID | page 223 |
| 0x9d4 | IMA_RX_GRP6_CFG | Rx GRP 6 Configuration | page 220 |
| 0x9d5 | IMA_RX_GRP6_CTL | Rx GRP 6 Control | page 221 |
| 0x9d6 | IMA_RX_GRP6_FIRST_PHY_ADDR | Rx GRP 6 First Link Address | page 222 |
| 0x9d7 | IMA_RX_GRP6_ID | Rx GRP 6 Rx Group ID | page 223 |
| 0x9d8 | IMA_RX_GRP7_CFG | Rx GRP 7 Configuration | page 220 |
| 0x9d9 | IMA_RX_GRP7_CTL | Rx GRP 7 Control | page 221 |
| 0x9da | IMA_RX_GRP7_FIRST_PHY_ADDR | Rx GRP 7 First Link Address | page 222 |
| 0x9db | IMA_RX_GRP7_ID | Rx GRP 7 Rx Group ID | page 223 |
| 0x9dc | IMA_RX_GRP8_CFG | Rx GRP 8 Configuration | page 220 |
| 0x9dd | IMA_RX_GRP8_CTL | Rx GRP 8 Control | page 221 |
| 0x9de | IMA_RX_GRP8_FIRST_PHY_ADDR | Rx GRP 8 First Link Address | page 222 |
| 0x9df | IMA_RX_GRP8_ID | Rx GRP 8 Rx Group ID | page 223 |
| Receive Groups 5–8 Far-End Status | | | |
| 0x9e0 | IMA_RX_GRP5_RX_TEST_PATTERN | Rx GRP 5 Rx Test Pattern | page 224 |
| 0x9e2 | IMA_RX_GRP5_STAT_CTL_CHANGE | Rx GRP 5 SCCI | page 225 |
| 0x9e3 | IMA_RX_GRP5_ACTUAL_GRP_ID | Rx GRP 5 Rx Group ID | page 226 |
| 0x9e4 | IMA_RX_GRP5_STAT_CTL | Rx GRP 5 Status / Control | page 227 |
| 0x9e5 | IMA_RX_GRP5_TIMING_INFO | Rx GRP 5 Timing Control | page 228 |
| 0x9e6 | IMA_RX_GRP5_TEST_CTL | Rx GRP 5 Test Control | page 229 |
| 0x9e7 | IMA_RX_GRP5_TX_TEST_PATTERN | Rx GRP 5 Tx Test Pattern | page 230 |
| 0x9e8 | IMA_RX_GRP6_RX_TEST_PATTERN | Rx GRP 6 Rx Test Pattern | page 224 |
| 0x9ea | IMA_RX_GRP6_STAT_CTL_CHANGE | Rx GRP 6 SCCI | page 225 |
| 0x9eb | IMA_RX_GRP6_ACTUAL_GRP_ID | Rx GRP 6 Rx Group ID | page 226 |
| 0x9ec | IMA_RX_GRP6_STAT_CTL | Rx GRP 6 Status / Control | page 227 |

Table 2-10. IMA Control and Status Registers (12 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|------------------------------|--------------------------|
| 0x9ed | IMA_RX_GRP6_TIMING_INFO | Rx GRP 6 Timing Control | page 228 |
| 0x9ee | IMA_RX_GRP6_TEST_CTL | Rx GRP 6 Test Control | page 229 |
| 0x9ef | IMA_RX_GRP6_TX_TEST_PATTERN | Rx GRP 6 Tx Test Pattern | page 230 |
| 0x9f0 | IMA_RX_GRP7_RX_TEST_PATTERN | Rx GRP 7 Rx Test Pattern | page 224 |
| 0x9f2 | IMA_RX_GRP7_STAT_CTL_CHANGE | Rx GRP 7 SCCI | page 225 |
| 0x9f3 | IMA_RX_GRP7_ACTUAL_GRP_ID | Rx GRP 7 Rx Group ID | page 226 |
| 0x9f4 | IMA_RX_GRP7_STAT_CTL | Rx GRP 7 Status / Control | page 227 |
| 0x9f5 | IMA_RX_GRP7_TIMING_INFO | Rx GRP 7 Timing Control | page 228 |
| 0x9f6 | IMA_RX_GRP7_TEST_CTL | Rx GRP 7 Test Control | page 229 |
| 0x9f7 | IMA_RX_GRP7_TX_TEST_PATTERN | Rx GRP 7 Tx Test Pattern | page 230 |
| 0x9f8 | IMA_RX_GRP8_RX_TEST_PATTERN | Rx GRP 8 Rx Test Pattern | page 224 |
| 0x9fa | IMA_RX_GRP8_STAT_CTL_CHANGE | Rx GRP 8 SCCI | page 225 |
| 0x9fb | IMA_RX_GRP8_ACTUAL_GRP_ID | Rx GRP 8 Rx Group ID | page 226 |
| 0x9fc | IMA_RX_GRP8_STAT_CTL | Rx GRP 8 Status / Control | page 227 |
| 0x9fd | IMA_RX_GRP8_TIMING_INFO | Rx GRP 8 Timing Control | page 228 |
| 0x9fe | IMA_RX_GRP8_TEST_CTL | Rx GRP 8 Test Control | page 229 |
| 0x9ff | IMA_RX_GRP8_TX_TEST_PATTERN | Rx GRP 8 Tx Test Pattern | page 230 |
| Transmit Groups 9–12 Configuration Tables | | | |
| 0xa20 | IMA_TX_GRP9_RX_TEST_PATTERN | Tx GRP 9 Rx Test Pattern | page 208 |
| 0xa21 | IMA_TX_GRP9_CTL | Tx GRP 9 Control | page 209 |
| 0xa22 | IMA_TX_GRP9_FIRST_PHY_ADDR | Tx GRP 9 First Link Address | page 210 |
| 0xa23 | IMA_TX_GRP9_ID | Tx GRP 9 Tx Group ID | page 211 |
| 0xa24 | IMA_TX_GRP9_STAT_CTL | Tx GRP 9 Status / Control | page 212 |
| 0xa25 | IMA_TX_GRP9_TIMING_INFO | Tx GRP 9 Timing Control | page 213 |
| 0xa26 | IMA_TX_GRP9_TEST_CTL | Tx GRP 9 Test Control | page 214 |
| 0xa27 | IMA_TX_GRP9_TX_TEST_PATTERN | Tx GRP 9 Tx Test Pattern | page 215 |
| 0xa28 | IMA_TX_GRP10_RX_TEST_PATTERN | Tx GRP 10 Rx Test Pattern | page 208 |
| 0xa29 | IMA_TX_GRP10_CTL | Tx GRP 10 Control | page 209 |
| 0xa2a | IMA_TX_GRP10_FIRST_PHY_ADDR | Tx GRP 10 First Link Address | page 210 |
| 0xa2b | IMA_TX_GRP10_ID | Tx GRP 10 Tx Group ID | page 211 |
| 0xa2c | IMA_TX_GRP10_STAT_CTL | Tx GRP 10 Status / Control | page 212 |
| 0xa2d | IMA_TX_GRP10_TIMING_INFO | Tx GRP 10 Timing Control | page 213 |
| 0xa2e | IMA_TX_GRP10_TEST_CTL | Tx GRP 10 Test Control | page 214 |
| 0xa2f | IMA_TX_GRP10_TX_TEST_PATTERN | Tx GRP 10 Tx Test Pattern | page 215 |
| 0xa30 | IMA_TX_GRP11_RX_TEST_PATTERN | Tx GRP 11 Rx Test Pattern | page 208 |

Table 2-10. IMA Control and Status Registers (13 of 33)

| Address | Name | Description (Continued) | Page Number |
|---|------------------------------|--|--------------------------|
| 0xa31 | IMA_TX_GRP11_CTL | Tx GRP 11 Control | page 209 |
| 0xa32 | IMA_TX_GRP11_FIRST_PHY_ADDR | Tx GRP 11 First Link Address | page 210 |
| 0xa33 | IMA_TX_GRP11_ID | Tx GRP 11 Tx Group ID | page 211 |
| 0xa34 | IMA_TX_GRP11_STAT_CTL | Tx GRP 11 Status / Control | page 212 |
| 0xa35 | IMA_TX_GRP11_TIMING_INFO | Tx GRP 11 Timing Control | page 213 |
| 0xa36 | IMA_TX_GRP11_TEST_CTL | Tx GRP 11 Test Control | page 214 |
| 0xa37 | IMA_TX_GRP11_TX_TEST_PATTERN | Tx GRP 11 Tx Test Pattern | page 215 |
| 0xa38 | IMA_TX_GRP12_RX_TEST_PATTERN | Tx GRP 12 Rx Test Pattern | page 208 |
| 0xa39 | IMA_TX_GRP12_CTL | Tx GRP 12 Control | page 209 |
| 0xa3a | IMA_TX_GRP12_FIRST_PHY_ADDR | Tx GRP 12 First Link Address | page 210 |
| 0xa3b | IMA_TX_GRP12_ID | Tx GRP 12 Tx Group ID | page 211 |
| 0xa3c | IMA_TX_GRP12_STAT_CTL | Tx GRP 12 Status / Control | page 212 |
| 0xa3d | IMA_TX_GRP12_TIMING_INFO | Tx GRP 12 Timing Control | page 213 |
| 0xa3e | IMA_TX_GRP12_TEST_CTL | Tx GRP 12 Test Control | page 214 |
| 0xa3f | IMA_TX_GRP12_TX_TEST_PATTERN | Tx GRP 12 Tx Test Pattern | page 215 |
| Tx UTOPIA Addresses 8 - 11 Cell Counters | | | |
| 0xa40 | IMA_TX_ATM8_CELL_COUNT_LSB | Transmit UTOPIA Address 0x08 Cell Count LSBs | page 216 |
| 0xa41 | IMA_TX_ATM8_CELL_COUNT_MSB | Transmit UTOPIA Address 0x08 Cell Count MSBs | |
| 0xa42 | IMA_TX_ATM9_CELL_COUNT_LSB | Transmit UTOPIA Address 0x09 Cell Count LSBs | |
| 0xa43 | IMA_TX_ATM9_CELL_COUNT_MSB | Transmit UTOPIA Address 0x09 Cell Count MSBs | |
| 0xa44 | IMA_TX_ATM10_CELL_COUNT_LSB | Transmit UTOPIA Address 0x0A Cell Count LSBs | |
| 0xa45 | IMA_TX_ATM10_CELL_COUNT_MSB | Transmit UTOPIA Address 0x0A Cell Count MSBs | |
| 0xa46 | IMA_TX_ATM11_CELL_COUNT_LSB | Transmit UTOPIA Address 0x0B Cell Count LSBs | |
| 0xa47 | IMA_TX_ATM11_CELL_COUNT_MSB | Transmit UTOPIA Address 0x0B Cell Count MSBs | |
| Rx UTOPIA Addresses 8 - 11 Cell Counters | | | |
| 0xa50 | IMA_RX_ATM8_CELL_COUNT_LSB | Receive UTOPIA Address 0x08 Cell Count LSBs | page 218 |
| 0xa51 | IMA_RX_ATM8_CELL_COUNT_MSB | Receive UTOPIA Address 0x08 Cell Count MSBs | |
| 0xa52 | IMA_RX_ATM9_CELL_COUNT_LSB | Receive UTOPIA Address 0x09 Cell Count LSBs | |
| 0xa53 | IMA_RX_ATM9_CELL_COUNT_MSB | Receive UTOPIA Address 0x09 Cell Count MSBs | |
| 0xa54 | IMA_RX_ATM10_CELL_COUNT_LSB | Receive UTOPIA Address 0x0A Cell Count LSBs | |
| 0xa55 | IMA_RX_ATM10_CELL_COUNT_MSB | Receive UTOPIA Address 0x0A Cell Count MSBs | |
| 0xa56 | IMA_RX_ATM11_CELL_COUNT_LSB | Receive UTOPIA Address 0x0B Cell Count LSBs | |
| 0xa57 | IMA_RX_ATM11_CELL_COUNT_MSB | Receive UTOPIA Address 0x0B Cell Count MSBs | |

Table 2-10. IMA Control and Status Registers (14 of 33)

| Address | Name | Description (Continued) | Page Number |
|--------------------------------------|--------------------|-------------------------|-------------|
| Port 16–23 Control and Status | | | |
| 0xa60 | IMA_TX_LNK16_CTL | Tx Link 16 Control | page 232 |
| 0xa61 | IMA_TX_LNK17_CTL | Tx Link 17 Control | |
| 0xa62 | IMA_TX_LNK18_CTL | Tx Link 18 Control | |
| 0xa63 | IMA_TX_LNK19_CTL | Tx Link 19 Control | |
| 0xa64 | IMA_TX_LNK20_CTL | Tx Link 20 Control | |
| 0xa65 | IMA_TX_LNK21_CTL | Tx Link 21 Control | |
| 0xa66 | IMA_TX_LNK22_CTL | Tx Link 22 Control | |
| 0xa67 | IMA_TX_LNK23_CTL | Tx Link 23 Control | |
| 0xa68 | IMA_TX_LNK16_STATE | Tx Link 16 Status | page 233 |
| 0xa69 | IMA_TX_LNK17_STATE | Tx Link 17 Status | |
| 0xa6a | IMA_TX_LNK18_STATE | Tx Link 18 Status | |
| 0xa6b | IMA_TX_LNK19_STATE | Tx Link 19 Status | |
| 0xa6c | IMA_TX_LNK20_STATE | Tx Link 20 Status | |
| 0xa6d | IMA_TX_LNK21_STATE | Tx Link 21 Status | |
| 0xa6e | IMA_TX_LNK22_STATE | Tx Link 22 Status | |
| 0xa6f | IMA_TX_LNK23_STATE | Tx Link 23 Status | |
| 0xa70 | IMA_TX_LNK16_ID | Tx Link 16 Assigned LID | page 234 |
| 0xa71 | IMA_TX_LNK17_ID | Tx Link 17 Assigned LID | |
| 0xa72 | IMA_TX_LNK18_ID | Tx Link 18 Assigned LID | |
| 0xa73 | IMA_TX_LNK19_ID | Tx Link 19 Assigned LID | |
| 0xa74 | IMA_TX_LNK20_ID | Tx Link 20 Assigned LID | |
| 0xa75 | IMA_TX_LNK21_ID | Tx Link 21 Assigned LID | |
| 0xa76 | IMA_TX_LNK22_ID | Tx Link 22 Assigned LID | |
| 0xa77 | IMA_TX_LNK23_ID | Tx Link 23 Assigned LID | |
| 0xa80 | IMA_RX_LNK16_CTL | Rx Link 16 Control | page 235 |
| 0xa81 | IMA_RX_LNK17_CTL | Rx Link 17 Control | |
| 0xa82 | IMA_RX_LNK18_CTL | Rx Link 18 Control | |
| 0xa83 | IMA_RX_LNK19_CTL | Rx Link 19 Control | |
| 0xa84 | IMA_RX_LNK20_CTL | Rx Link 20 Control | |
| 0xa85 | IMA_RX_LNK21_CTL | Rx Link 21 Control | |
| 0xa86 | IMA_RX_LNK22_CTL | Rx Link 22 Control | |
| 0xa87 | IMA_RX_LNK23_CTL | Rx Link 23 Control | |
| 0xa88 | IMA_RX_LNK16_STATE | Rx Link 16 Status | page 236 |
| 0xa89 | IMA_RX_LNK17_STATE | Rx Link 17 Status | |
| 0xa8a | IMA_RX_LNK18_STATE | Rx Link 18 Status | |
| 0xa8b | IMA_RX_LNK19_STATE | Rx Link 19 Status | |
| 0xa8c | IMA_RX_LNK20_STATE | Rx Link 20 Status | |
| 0xa8d | IMA_RX_LNK21_STATE | Rx Link 21 Status | |
| 0xa8e | IMA_RX_LNK22_STATE | Rx Link 22 Status | |
| 0xa8f | IMA_RX_LNK23_STATE | Rx Link 23 Status | |

Table 2-10. IMA Control and Status Registers (15 of 33)

| Address | Name | Description (Continued) | Page Number |
|---------|----------------------|----------------------------|-------------|
| 0xa90 | IMA_RX_LNK16_DEFECT | Rx Link 16 Defects | page 237 |
| 0xa91 | IMA_RX_LNK17_DEFECT | Rx Link 17 Defects | |
| 0xa92 | IMA_RX_LNK18_DEFECT | Rx Link 18 Defects | |
| 0xa93 | IMA_RX_LNK19_DEFECT | Rx Link 19 Defects | |
| 0xa94 | IMA_RX_LNK20_DEFECT | Rx Link 20 Defects | |
| 0xa95 | IMA_RX_LNK21_DEFECT | Rx Link 21 Defects | |
| 0xa96 | IMA_RX_LNK22_DEFECT | Rx Link 22 Defects | |
| 0xa97 | IMA_RX_LNK23_DEFECT | Rx Link 23 Defects | |
| 0xa98 | IMA_FE_TX_LNK16_CFG | FE Tx Link 16 Link Config | page 238 |
| 0xa99 | IMA_FE_TX_LNK17_CFG | FE Tx Link 17 Link Config | |
| 0xa9a | IMA_FE_TX_LNK18_CFG | FE Tx Link 18 Link Config | |
| 0xa9b | IMA_FE_TX_LNK19_CFG | FE Tx Link 19 Link Config | |
| 0xa9c | IMA_FE_TX_LNK20_CFG | FE Tx Link 20 Link Config | |
| 0xa9d | IMA_FE_TX_LNK21_CFG | FE Tx Link 21 Link Config | |
| 0xa9e | IMA_FE_TX_LNK22_CFG | FE Tx Link 22 Link Config | |
| 0xa9f | IMA_FE_TX_LNK23_CFG | FE Tx Link 23 Link Config | |
| 0xaa0 | IMA_FE_LNK16_STATE | Rx Link 16 FE Status | page 239 |
| 0xaa1 | IMA_FE_LNK17_STATE | Rx Link 17 FE Status | |
| 0xaa2 | IMA_FE_LNK18_STATE | Rx Link 18 FE Status | |
| 0xaa3 | IMA_FE_LNK19_STATE | Rx Link 19 FE Status | |
| 0xaa4 | IMA_FE_LNK20_STATE | Rx Link 20 FE Status | |
| 0xaa5 | IMA_FE_LNK21_STATE | Rx Link 21 FE Status | |
| 0xaa6 | IMA_FE_LNK22_STATE | Rx Link 22 FE Status | |
| 0xaa7 | IMA_FE_LNK23_STATE | Rx Link 23 FE Status | |
| 0xaa8 | IMA_RX_LNK16_ID | Rx Link 16 Assigned LID | page 240 |
| 0xaa9 | IMA_RX_LNK17_ID | Rx Link 17 Assigned LID | |
| 0xaaa | IMA_RX_LNK18_ID | Rx Link 18 Assigned LID | |
| 0xaab | IMA_RX_LNK19_ID | Rx Link 19 Assigned LID | |
| 0xaac | IMA_RX_LNK20_ID | Rx Link 20 Assigned LID | |
| 0xaad | IMA_RX_LNK21_ID | Rx Link 21 Assigned LID | |
| 0xaae | IMA_RX_LNK22_ID | Rx Link 22 Assigned LID | |
| 0xaaf | IMA_RX_LNK23_ID | Rx Link 23 Assigned LID | |
| 0xab0 | IMA_RX_LNK16_IV_CNT | Rx Link 16 IV-IMA Counter | page 241 |
| 0xab1 | IMA_RX_LNK17_IV_CNT | Rx Link 17 IV-IMA Counter | |
| 0xab2 | IMA_RX_LNK18_IV_CNT | Rx Link 18 IV-IMA Counter | |
| 0xab3 | IMA_RX_LNK19_IV_CNT | Rx Link 19 IV-IMA Counter | |
| 0xab4 | IMA_RX_LNK20_IV_CNT | Rx Link 20 IV-IMA Counter | |
| 0xab5 | IMA_RX_LNK21_IV_CNT | Rx Link 21 IV-IMA Counter | |
| 0xab6 | IMA_RX_LNK22_IV_CNT | Rx Link 22 IV-IMA Counter | |
| 0xab7 | IMA_RX_LNK23_IV_CNT | Rx Link 23 IV-IMA Counter | |
| 0xab8 | IMA_RX_LNK16_OIF_CNT | Rx Link 16 OIF-IMA Counter | page 242 |
| 0xab9 | IMA_RX_LNK17_OIF_CNT | Rx Link 17 OIF-IMA Counter | |
| 0xaba | IMA_RX_LNK18_OIF_CNT | Rx Link 18 OIF-IMA Counter | |
| 0xabb | IMA_RX_LNK19_OIF_CNT | Rx Link 19 OIF-IMA Counter | |
| 0xabc | IMA_RX_LNK20_OIF_CNT | Rx Link 20 OIF-IMA Counter | |
| 0xabd | IMA_RX_LNK21_OIF_CNT | Rx Link 21 OIF-IMA Counter | |
| 0xabe | IMA_RX_LNK22_OIF_CNT | Rx Link 22 OIF-IMA Counter | |
| 0xabf | IMA_RX_LNK23_OIF_CNT | Rx Link 23 OIF-IMA Counter | |

Table 2-10. IMA Control and Status Registers (16 of 33)

| Address | Name | Description (Continued) | Page Number |
|---|------------------------------|------------------------------|-------------|
| 0xac0 | IMA_FE_TX_LNK16_GRP_ID | Rx Link 16 Captured GRP ID | page 243 |
| 0xac1 | IMA_FE_TX_LNK17_GRP_ID | Rx Link 17 Captured GRP ID | |
| 0xac2 | IMA_FE_TX_LNK18_GRP_ID | Rx Link 18 Captured GRP ID | |
| 0xac3 | IMA_FE_TX_LNK19_GRP_ID | Rx Link 19 Captured GRP ID | |
| 0xac4 | IMA_FE_TX_LNK20_GRP_ID | Rx Link 20 Captured GRP ID | |
| 0xac5 | IMA_FE_TX_LNK21_GRP_ID | Rx Link 21 Captured GRP ID | |
| 0xac6 | IMA_FE_TX_LNK22_GRP_ID | Rx Link 22 Captured GRP ID | |
| 0xac7 | IMA_FE_TX_LNK23_GRP_ID | Rx Link 23 Captured GRP ID | |
| Receive Groups 9–12 Configuration Tables | | | |
| 0xad0 | IMA_RX_GRP9_CFG | Rx GRP 9 Configuration | page 220 |
| 0xad1 | IMA_RX_GRP9_CTL | Rx GRP 9 Control | page 221 |
| 0xad2 | IMA_RX_GRP9_FIRST_PHY_ADDR | Rx GRP 9 First Link Address | page 222 |
| 0xad3 | IMA_RX_GRP9_ID | Rx GRP 9 Rx Group ID | page 223 |
| 0xad4 | IMA_RX_GRP10_CFG | Rx GRP 10 Configuration | page 220 |
| 0xad5 | IMA_RX_GRP10_CTL | Rx GRP 10 Control | page 221 |
| 0xad6 | IMA_RX_GRP10_FIRST_PHY_ADDR | Rx GRP 10 First Link Address | page 222 |
| 0xad7 | IMA_RX_GRP10_ID | Rx GRP 10 Rx Group ID | page 223 |
| 0xad8 | IMA_RX_GRP11_CFG | Rx GRP 11 Configuration | page 220 |
| 0xad9 | IMA_RX_GRP11_CTL | Rx GRP 11 Control | page 221 |
| 0xada | IMA_RX_GRP11_FIRST_PHY_ADDR | Rx GRP 11 First Link Address | page 222 |
| 0xadb | IMA_RX_GRP11_ID | Rx GRP 11 Rx Group ID | page 223 |
| 0xadc | IMA_RX_GRP12_CFG | Rx GRP 12 Configuration | page 220 |
| 0xadd | IMA_RX_GRP12_CTL | Rx GRP 12 Control | page 221 |
| 0xade | IMA_RX_GRP12_FIRST_PHY_ADDR | Rx GRP 12 First Link Address | page 222 |
| 0xadf | IMA_RX_GRP12_ID | Rx GRP 12 Rx Group ID | page 223 |
| Receive Groups 9–12 Far-End Status | | | |
| 0xae0 | IMA_RX_GRP9_RX_TEST_PATTERN | Rx GRP 9 Rx Test Pattern | page 224 |
| 0xae2 | IMA_RX_GRP9_STAT_CTL_CHANGE | Rx GRP 9 SCCI | page 225 |
| 0xae3 | IMA_RX_GRP9_ACTUAL_GRP_ID | Rx GRP 9 Rx Group ID | page 226 |
| 0xae4 | IMA_RX_GRP9_STAT_CTL | Rx GRP 9 Status / Control | page 227 |
| 0xae5 | IMA_RX_GRP9_TIMING_INFO | Rx GRP 9 Timing Control | page 228 |
| 0xae6 | IMA_RX_GRP9_TEST_CTL | Rx GRP 9 Test Control | page 229 |
| 0xae7 | IMA_RX_GRP9_TX_TEST_PATTERN | Rx GRP 9 Tx Test Pattern | page 230 |
| 0xae8 | IMA_RX_GRP10_RX_TEST_PATTERN | Rx GRP 10 Rx Test Pattern | page 224 |
| 0xaea | IMA_RX_GRP10_STAT_CTL_CHANGE | Rx GRP 10 SCCI | page 225 |
| 0xaeb | IMA_RX_GRP10_ACTUAL_GRP_ID | Rx GRP 10 Rx Group ID | page 226 |
| 0xaec | IMA_RX_GRP10_STAT_CTL | Rx GRP 10 Status / Control | page 227 |

Table 2-10. IMA Control and Status Registers (17 of 33)

| Address | Name | Description (Continued) | Page Number |
|---|------------------------------|------------------------------|--------------------------|
| 0xaed | IMA_RX_GRP10_TIMING_INFO | Rx GRP 10 Timing Control | page 228 |
| 0xae | IMA_RX_GRP10_TEST_CTL | Rx GRP 10 Test Control | page 229 |
| 0xaef | IMA_RX_GRP10_TX_TEST_PATTERN | Rx GRP 10 Tx Test Pattern | page 230 |
| 0xaf0 | IMA_RX_GRP11_RX_TEST_PATTERN | Rx GRP 11 Rx Test Pattern | page 224 |
| 0xaf2 | IMA_RX_GRP11_STAT_CTL_CHANGE | Rx GRP 11 SCCI | page 225 |
| 0xaf3 | IMA_RX_GRP11_ACTUAL_GRP_ID | Rx GRP 11 Rx Group ID | page 226 |
| 0xaf4 | IMA_RX_GRP11_STAT_CTL | Rx GRP 11 Status / Control | page 227 |
| 0xaf5 | IMA_RX_GRP11_TIMING_INFO | Rx GRP 11 Timing Control | page 228 |
| 0xaf6 | IMA_RX_GRP11_TEST_CTL | Rx GRP 11 Test Control | page 229 |
| 0xaf7 | IMA_RX_GRP11_TX_TEST_PATTERN | Rx GRP 11 Tx Test Pattern | page 230 |
| 0xaf8 | IMA_RX_GRP12_RX_TEST_PATTERN | Rx GRP 12 Rx Test Pattern | page 224 |
| 0xafa | IMA_RX_GRP12_STAT_CTL_CHANGE | Rx GRP 12 SCCI | page 225 |
| 0xafb | IMA_RX_GRP12_ACTUAL_GRP_ID | Rx GRP 12 Rx Group ID | page 226 |
| 0xafc | IMA_RX_GRP12_STAT_CTL | Rx GRP 12 Status / Control | page 227 |
| 0xafd | IMA_RX_GRP12_TIMING_INFO | Rx GRP 12 Timing Control | page 228 |
| 0xaf | IMA_RX_GRP12_TEST_CTL | Rx GRP 12 Test Control | page 229 |
| 0xaff | IMA_RX_GRP12_TX_TEST_PATTERN | Rx GRP 12 Tx Test Pattern | page 230 |
| Transmit Groups 13–16 Configuration Tables | | | |
| 0xb20 | IMA_TX_GRP13_RX_TEST_PATTERN | Tx GRP 13 Rx Test Pattern | page 208 |
| 0xb21 | IMA_TX_GRP13_CTL | Tx GRP 13 Control | page 209 |
| 0xb22 | IMA_TX_GRP13_FIRST_PHY_ADDR | Tx GRP 13 First Link Address | page 210 |
| 0xb23 | IMA_TX_GRP13_ID | Tx GRP 13 Tx Group ID | page 211 |
| 0xb24 | IMA_TX_GRP13_STAT_CTL | Tx GRP 13 Status / Control | page 212 |
| 0xb25 | IMA_TX_GRP13_TIMING_INFO | Tx GRP 13 Timing Control | page 213 |
| 0xb26 | IMA_TX_GRP13_TEST_CTL | Tx GRP 13 Test Control | page 214 |
| 0xb27 | IMA_TX_GRP13_TX_TEST_PATTERN | Tx GRP 13 Tx Test Pattern | page 215 |
| 0xb28 | IMA_TX_GRP14_RX_TEST_PATTERN | Tx GRP 14 Rx Test Pattern | page 208 |
| 0xb29 | IMA_TX_GRP14_CTL | Tx GRP 14 Control | page 209 |
| 0xb2a | IMA_TX_GRP14_FIRST_PHY_ADDR | Tx GRP 14 First Link Address | page 210 |
| 0xb2b | IMA_TX_GRP14_ID | Tx GRP 14 Tx Group ID | page 211 |
| 0xb2c | IMA_TX_GRP14_STAT_CTL | Tx GRP 14 Status / Control | page 212 |
| 0xb2d | IMA_TX_GRP14_TIMING_INFO | Tx GRP 14 Timing Control | page 213 |
| 0xb2e | IMA_TX_GRP14_TEST_CTL | Tx GRP 14 Test Control | page 214 |
| 0xb2f | IMA_TX_GRP14_TX_TEST_PATTERN | Tx GRP 14 Tx Test Pattern | page 215 |
| 0xb30 | IMA_TX_GRP15_RX_TEST_PATTERN | Tx GRP 15 Rx Test Pattern | page 208 |

Table 2-10. IMA Control and Status Registers (18 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|--|--------------------------|
| 0xb31 | IMA_TX_GRP15_CTL | Tx GRP 15 Control | page 209 |
| 0xb32 | IMA_TX_GRP15_FIRST_PHY_ADDR | Tx GRP 15 First Link Address | page 210 |
| 0xb33 | IMA_TX_GRP15_ID | Tx GRP 15 Tx Group ID | page 211 |
| 0xb34 | IMA_TX_GRP15_STAT_CTL | Tx GRP 15 Status / Control | page 212 |
| 0xb35 | IMA_TX_GRP15_TIMING_INFO | Tx GRP 15 Timing Control | page 213 |
| 0xb36 | IMA_TX_GRP15_TEST_CTL | Tx GRP 15 Test Control | page 214 |
| 0xb37 | IMA_TX_GRP15_TX_TEST_PATTERN | Tx GRP 15 Tx Test Pattern | page 215 |
| 0xb38 | IMA_TX_GRP16_RX_TEST_PATTERN | Tx GRP 16 Rx Test Pattern | page 208 |
| 0xb39 | IMA_TX_GRP16_CTL | Tx GRP 16 Control | page 209 |
| 0xb3a | IMA_TX_GRP16_FIRST_PHY_ADDR | Tx GRP 16 First Link Address | page 210 |
| 0xb3b | IMA_TX_GRP16_ID | Tx GRP 16 Tx Group ID | page 211 |
| 0xb3c | IMA_TX_GRP16_STAT_CTL | Tx GRP 16 Status / Control | page 212 |
| 0xb3d | IMA_TX_GRP16_TIMING_INFO | Tx GRP 16 Timing Control | page 213 |
| 0xb3e | IMA_TX_GRP16_TEST_CTL | Tx GRP 16 Test Control | page 214 |
| 0xb3f | IMA_TX_GRP16_TX_TEST_PATTERN | Tx GRP 16 Tx Test Pattern | page 215 |
| Tx UTOPIA Addresses 12 - 15 Cell Counters | | | |
| 0xb40 | IMA_TX_ATM12_CELL_COUNT_LSB | Transmit UTOPIA Address 0x0C Cell Count LSBs | page 216 |
| 0xb41 | IMA_TX_ATM12_CELL_COUNT_MSB | Transmit UTOPIA Address 0x0C Cell Count MSBs | |
| 0xb42 | IMA_TX_ATM13_CELL_COUNT_LSB | Transmit UTOPIA Address 0x0D Cell Count LSBs | |
| 0xb43 | IMA_TX_ATM13_CELL_COUNT_MSB | Transmit UTOPIA Address 0x0D Cell Count MSBs | |
| 0xb44 | IMA_TX_ATM14_CELL_COUNT_LSB | Transmit UTOPIA Address 0x0E Cell Count LSBs | |
| 0xb45 | IMA_TX_ATM14_CELL_COUNT_MSB | Transmit UTOPIA Address 0x0E Cell Count MSBs | |
| 0xb46 | IMA_TX_ATM15_CELL_COUNT_LSB | Transmit UTOPIA Address 0x0F Cell Count LSBs | |
| 0xb47 | IMA_TX_ATM15_CELL_COUNT_MSB | Transmit UTOPIA Address 0x0F Cell Count MSBs | |
| Rx UTOPIA Addresses 12 - 15 Cell Counters | | | |
| 0xb50 | IMA_RX_ATM12_CELL_COUNT_LSB | Receive UTOPIA Address 0x0C Cell Count LSBs | page 218 |
| 0xb51 | IMA_RX_ATM12_CELL_COUNT_MSB | Receive UTOPIA Address 0x0C Cell Count MSBs | |
| 0xb52 | IMA_RX_ATM13_CELL_COUNT_LSB | Receive UTOPIA Address 0x0D Cell Count LSBs | |
| 0xb53 | IMA_RX_ATM13_CELL_COUNT_MSB | Receive UTOPIA Address 0x0D Cell Count MSBs | |
| 0xb54 | IMA_RX_ATM14_CELL_COUNT_LSB | Receive UTOPIA Address 0x0E Cell Count LSBs | |
| 0xb55 | IMA_RX_ATM14_CELL_COUNT_MSB | Receive UTOPIA Address 0x0E Cell Count MSBs | |
| 0xb56 | IMA_RX_ATM15_CELL_COUNT_LSB | Receive UTOPIA Address 0x0F Cell Count LSBs | |
| 0xb57 | IMA_RX_ATM15_CELL_COUNT_MSB | Receive UTOPIA Address 0x0F Cell Count MSBs | |

Table 2-10. IMA Control and Status Registers (19 of 33)

| Address | Name | Description (Continued) | Page Number |
|--------------------------------------|--------------------|-------------------------|-------------|
| Port 24–31 Control and Status | | | |
| 0xb60 | IMA_TX_LNK24_CTL | Tx Link 24 Control | page 232 |
| 0xb61 | IMA_TX_LNK25_CTL | Tx Link 25 Control | |
| 0xb62 | IMA_TX_LNK26_CTL | Tx Link 26 Control | |
| 0xb63 | IMA_TX_LNK27_CTL | Tx Link 27 Control | |
| 0xb64 | IMA_TX_LNK28_CTL | Tx Link 28 Control | |
| 0xb65 | IMA_TX_LNK29_CTL | Tx Link 29 Control | |
| 0xb66 | IMA_TX_LNK30_CTL | Tx Link 30 Control | |
| 0xb67 | IMA_TX_LNK31_CTL | Tx Link 31 Control | |
| 0xb68 | IMA_TX_LNK24_STATE | Tx Link 24 Status | |
| 0xb69 | IMA_TX_LNK25_STATE | Tx Link 25 Status | |
| 0xb6a | IMA_TX_LNK26_STATE | Tx Link 26 Status | |
| 0xb6b | IMA_TX_LNK27_STATE | Tx Link 27 Status | |
| 0xb6c | IMA_TX_LNK28_STATE | Tx Link 28 Status | |
| 0xb6d | IMA_TX_LNK29_STATE | Tx Link 29 Status | |
| 0xb6e | IMA_TX_LNK30_STATE | Tx Link 30 Status | |
| 0xb6f | IMA_TX_LNK31_STATE | Tx Link 31 Status | |
| 0xb70 | IMA_TX_LNK24_ID | Tx Link 24 Assigned LID | page 234 |
| 0xb71 | IMA_TX_LNK25_ID | Tx Link 25 Assigned LID | |
| 0xb72 | IMA_TX_LNK26_ID | Tx Link 26 Assigned LID | |
| 0xb73 | IMA_TX_LNK27_ID | Tx Link 27 Assigned LID | |
| 0xb74 | IMA_TX_LNK28_ID | Tx Link 28 Assigned LID | |
| 0xb75 | IMA_TX_LNK29_ID | Tx Link 29 Assigned LID | |
| 0xb76 | IMA_TX_LNK30_ID | Tx Link 30 Assigned LID | |
| 0xb77 | IMA_TX_LNK31_ID | Tx Link 31 Assigned LID | |
| 0xb80 | IMA_RX_LNK24_CTL | Rx Link 24 Control | |
| 0xb81 | IMA_RX_LNK25_CTL | Rx Link 25 Control | |
| 0xb82 | IMA_RX_LNK26_CTL | Rx Link 26 Control | |
| 0xb83 | IMA_RX_LNK27_CTL | Rx Link 27 Control | |
| 0xb84 | IMA_RX_LNK28_CTL | Rx Link 28 Control | |
| 0xb85 | IMA_RX_LNK29_CTL | Rx Link 29 Control | |
| 0xb86 | IMA_RX_LNK30_CTL | Rx Link 30 Control | |
| 0xb87 | IMA_RX_LNK31_CTL | Rx Link 31 Control | |
| 0xb88 | IMA_RX_LNK24_STATE | Rx Link 24 Status | page 236 |
| 0xb89 | IMA_RX_LNK25_STATE | Rx Link 25 Status | |
| 0xb8a | IMA_RX_LNK26_STATE | Rx Link 26 Status | |
| 0xb8b | IMA_RX_LNK27_STATE | Rx Link 27 Status | |
| 0xb8c | IMA_RX_LNK28_STATE | Rx Link 28 Status | |
| 0xb8d | IMA_RX_LNK29_STATE | Rx Link 29 Status | |
| 0xb8e | IMA_RX_LNK30_STATE | Rx Link 30 Status | |
| 0xb8f | IMA_RX_LNK31_STATE | Rx Link 31 Status | |

Table 2-10. IMA Control and Status Registers (20 of 33)

| Address | Name | Description (Continued) | Page Number |
|---------|----------------------|----------------------------|-------------|
| 0xb90 | IMA_RX_LNK24_DEFECT | Rx Link 24 Defects | page 237 |
| 0xb91 | IMA_RX_LNK25_DEFECT | Rx Link 25 Defects | |
| 0xb92 | IMA_RX_LNK26_DEFECT | Rx Link 26 Defects | |
| 0xb93 | IMA_RX_LNK27_DEFECT | Rx Link 27 Defects | |
| 0xb94 | IMA_RX_LNK28_DEFECT | Rx Link 28 Defects | |
| 0xb95 | IMA_RX_LNK29_DEFECT | Rx Link 29 Defects | |
| 0xb96 | IMA_RX_LNK30_DEFECT | Rx Link 30 Defects | |
| 0xb97 | IMA_RX_LNK31_DEFECT | Rx Link 31 Defects | |
| 0xb98 | IMA_FE_TX_LNK24_CFG | FE Tx Link 24 Link Config | page 238 |
| 0xb99 | IMA_FE_TX_LNK25_CFG | FE Tx Link 25 Link Config | |
| 0xb9a | IMA_FE_TX_LNK26_CFG | FE Tx Link 26 Link Config | |
| 0xb9b | IMA_FE_TX_LNK27_CFG | FE Tx Link 27 Link Config | |
| 0xb9c | IMA_FE_TX_LNK28_CFG | FE Tx Link 28 Link Config | |
| 0xb9d | IMA_FE_TX_LNK29_CFG | FE Tx Link 29 Link Config | |
| 0xb9e | IMA_FE_TX_LNK30_CFG | FE Tx Link 30 Link Config | |
| 0xb9f | IMA_FE_TX_LNK31_CFG | FE Tx Link 31 Link Config | |
| 0xba0 | IMA_FE_LNK24_STATE | Rx Link 24 FE Status | page 239 |
| 0xba1 | IMA_FE_LNK25_STATE | Rx Link 25 FE Status | |
| 0xba2 | IMA_FE_LNK26_STATE | Rx Link 26 FE Status | |
| 0xba3 | IMA_FE_LNK27_STATE | Rx Link 27 FE Status | |
| 0xba4 | IMA_FE_LNK28_STATE | Rx Link 28 FE Status | |
| 0xba5 | IMA_FE_LNK29_STATE | Rx Link 29 FE Status | |
| 0xba6 | IMA_FE_LNK30_STATE | Rx Link 30 FE Status | |
| 0xba7 | IMA_FE_LNK31_STATE | Rx Link 31 FE Status | |
| 0xba8 | IMA_RX_LNK24_ID | Rx Link 24 Assigned LID | page 240 |
| 0xba9 | IMA_RX_LNK25_ID | Rx Link 25 Assigned LID | |
| 0xbaa | IMA_RX_LNK26_ID | Rx Link 26 Assigned LID | |
| 0xbab | IMA_RX_LNK27_ID | Rx Link 27 Assigned LID | |
| 0xbac | IMA_RX_LNK28_ID | Rx Link 28 Assigned LID | |
| 0xbad | IMA_RX_LNK29_ID | Rx Link 29 Assigned LID | |
| 0xbae | IMA_RX_LNK30_ID | Rx Link 30 Assigned LID | |
| 0xbaf | IMA_RX_LNK31_ID | Rx Link 31 Assigned LID | |
| 0xbb0 | IMA_RX_LNK24_IV_CNT | Rx Link 24 IV-IMA Counter | page 241 |
| 0xbb1 | IMA_RX_LNK25_IV_CNT | Rx Link 25 IV-IMA Counter | |
| 0xbb2 | IMA_RX_LNK26_IV_CNT | Rx Link 26 IV-IMA Counter | |
| 0xbb3 | IMA_RX_LNK27_IV_CNT | Rx Link 27 IV-IMA Counter | |
| 0xbb4 | IMA_RX_LNK28_IV_CNT | Rx Link 28 IV-IMA Counter | |
| 0xbb5 | IMA_RX_LNK29_IV_CNT | Rx Link 29 IV-IMA Counter | |
| 0xbb6 | IMA_RX_LNK30_IV_CNT | Rx Link 30 IV-IMA Counter | |
| 0xbb7 | IMA_RX_LNK31_IV_CNT | Rx Link 31 IV-IMA Counter | |
| 0xbb8 | IMA_RX_LNK24_OIF_CNT | Rx Link 24 OIF-IMA Counter | page 242 |
| 0xbb9 | IMA_RX_LNK25_OIF_CNT | Rx Link 25 OIF-IMA Counter | |
| 0xbba | IMA_RX_LNK26_OIF_CNT | Rx Link 26 OIF-IMA Counter | |
| 0xbbb | IMA_RX_LNK27_OIF_CNT | Rx Link 27 OIF-IMA Counter | |
| 0xbbc | IMA_RX_LNK28_OIF_CNT | Rx Link 28 OIF-IMA Counter | |
| 0xbbd | IMA_RX_LNK29_OIF_CNT | Rx Link 29 OIF-IMA Counter | |
| 0xbbe | IMA_RX_LNK30_OIF_CNT | Rx Link 30 OIF-IMA Counter | |
| 0xbbf | IMA_RX_LNK31_OIF_CNT | Rx Link 31 OIF-IMA Counter | |

Table 2-10. IMA Control and Status Registers (21 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|------------------------------|--------------------------|
| 0xbc0 | IMA_FE_TX_LNK24_GRP_ID | Rx Link 24 Captured GRP ID | page 243 |
| 0xbc1 | IMA_FE_TX_LNK25_GRP_ID | Rx Link 25 Captured GRP ID | |
| 0xbc2 | IMA_FE_TX_LNK26_GRP_ID | Rx Link 26 Captured GRP ID | |
| 0xbc3 | IMA_FE_TX_LNK27_GRP_ID | Rx Link 27 Captured GRP ID | |
| 0xbc4 | IMA_FE_TX_LNK28_GRP_ID | Rx Link 28 Captured GRP ID | |
| 0xbc5 | IMA_FE_TX_LNK29_GRP_ID | Rx Link 29 Captured GRP ID | |
| 0xbc6 | IMA_FE_TX_LNK30_GRP_ID | Rx Link 30 Captured GRP ID | |
| 0xbc7 | IMA_FE_TX_LNK31_GRP_ID | Rx Link 31 Captured GRP ID | |
| Receive Groups 13–16 Configuration Tables | | | |
| 0xbd0 | IMA_RX_GRP13_CFG | Rx GRP 13 Configuration | page 220 |
| 0xbd1 | IMA_RX_GRP13_CTL | Rx GRP 13 Control | page 221 |
| 0xbd2 | IMA_RX_GRP13_FIRST_PHY_ADDR | Rx GRP 13 First Link Address | page 222 |
| 0xbd3 | IMA_RX_GRP13_ID | Rx GRP 13 Rx Group ID | page 223 |
| 0xbd4 | IMA_RX_GRP14_CFG | Rx GRP 14 Configuration | page 220 |
| 0xbd5 | IMA_RX_GRP14_CTL | Rx GRP 14 Control | page 221 |
| 0xbd6 | IMA_RX_GRP14_FIRST_PHY_ADDR | Rx GRP 14 First Link Address | page 222 |
| 0xbd7 | IMA_RX_GRP14_ID | Rx GRP 14 Rx Group ID | page 223 |
| 0xbd8 | IMA_RX_GRP15_CFG | Rx GRP 15 Configuration | page 220 |
| 0xbd9 | IMA_RX_GRP15_CTL | Rx GRP 15 Control | page 221 |
| 0xbda | IMA_RX_GRP15_FIRST_PHY_ADDR | Rx GRP 15 First Link Address | page 222 |
| 0xbdb | IMA_RX_GRP15_ID | Rx GRP 15 Rx Group ID | page 223 |
| 0xbdc | IMA_RX_GRP16_CFG | Rx GRP 16 Configuration | page 220 |
| 0xbdd | IMA_RX_GRP16_CTL | Rx GRP 16 Control | page 221 |
| 0xbde | IMA_RX_GRP16_FIRST_PHY_ADDR | Rx GRP 16 First Link Address | page 222 |
| 0xbdf | IMA_RX_GRP16_ID | Rx GRP 16 Rx Group ID | page 223 |
| Receive Groups 13–16 Far-End Status | | | |
| 0xbe0 | IMA_RX_GRP13_RX_TEST_PATTERN | Rx GRP 13 Rx Test Pattern | page 224 |
| 0xbe2 | IMA_RX_GRP13_STAT_CTL_CHANGE | Rx GRP 13 SCCI | page 225 |
| 0xbe3 | IMA_RX_GRP13_ACTUAL_GRP_ID | Rx GRP 13 Rx Group ID | page 226 |
| 0xbe4 | IMA_RX_GRP13_STAT_CTL | Rx GRP 13 Status / Control | page 227 |
| 0xbe5 | IMA_RX_GRP13_TIMING_INFO | Rx GRP 13 Timing Control | page 228 |
| 0xbe6 | IMA_RX_GRP13_TEST_CTL | Rx GRP 13 Test Control | page 229 |
| 0xbe7 | IMA_RX_GRP13_TX_TEST_PATTERN | Rx GRP 13 Tx Test Pattern | page 230 |
| 0xbe8 | IMA_RX_GRP14_RX_TEST_PATTERN | Rx GRP 14 Rx Test Pattern | page 224 |
| 0xbea | IMA_RX_GRP14_STAT_CTL_CHANGE | Rx GRP 14 SCCI | page 225 |
| 0xbeb | IMA_RX_GRP14_ACTUAL_GRP_ID | Rx GRP 14 Rx Group ID | page 226 |
| 0xbec | IMA_RX_GRP14_STAT_CTL | Rx GRP 14 Status / Control | page 227 |

Table 2-10. IMA Control and Status Registers (22 of 33)

| Address | Name | Description (Continued) | Page Number |
|---|------------------------------|------------------------------|--------------------------|
| 0xbed | IMA_RX_GRP14_TIMING_INFO | Rx GRP 14 Timing Control | page 228 |
| 0xbee | IMA_RX_GRP14_TEST_CTL | Rx GRP 14 Test Control | page 229 |
| 0xbef | IMA_RX_GRP14_TX_TEST_PATTERN | Rx GRP 14 Tx Test Pattern | page 230 |
| 0xbf0 | IMA_RX_GRP15_RX_TEST_PATTERN | Rx GRP 15 Rx Test Pattern | page 224 |
| 0xbf2 | IMA_RX_GRP15_STAT_CTL_CHANGE | Rx GRP 15 SCCI | page 225 |
| 0xbf3 | IMA_RX_GRP15_ACTUAL_GRP_ID | Rx GRP 15 Rx Group ID | page 226 |
| 0xbf4 | IMA_RX_GRP15_STAT_CTL | Rx GRP 15 Status / Control | page 227 |
| 0xbf5 | IMA_RX_GRP15_TIMING_INFO | Rx GRP 15 Timing Control | page 228 |
| 0xbf6 | IMA_RX_GRP15_TEST_CTL | Rx GRP 15 Test Control | page 229 |
| 0xbf7 | IMA_RX_GRP15_TX_TEST_PATTERN | Rx GRP 15 Tx Test Pattern | page 230 |
| 0xbf8 | IMA_RX_GRP16_RX_TEST_PATTERN | Rx GRP 16 Rx Test Pattern | page 224 |
| 0xbfa | IMA_RX_GRP16_STAT_CTL_CHANGE | Rx GRP 16 SCCI | page 225 |
| 0xbfb | IMA_RX_GRP16_ACTUAL_GRP_ID | Rx GRP 16 Rx Group ID | page 226 |
| 0xbfc | IMA_RX_GRP16_STAT_CTL | Rx GRP 16 Status / Control | page 227 |
| 0xbfd | IMA_RX_GRP16_TIMING_INFO | Rx GRP 16 Timing Control | page 228 |
| 0xbfe | IMA_RX_GRP16_TEST_CTL | Rx GRP 16 Test Control | page 229 |
| 0xbff | IMA_RX_GRP16_TX_TEST_PATTERN | Rx GRP 16 Tx Test Pattern | page 230 |
| Transmit Groups 17–20 Configuration Tables | | | |
| 0xc20 | IMA_TX_GRP17_RX_TEST_PATTERN | Tx GRP 17 Rx Test Pattern | page 208 |
| 0xc21 | IMA_TX_GRP17_CTL | Tx GRP 17 Control | page 209 |
| 0xc22 | IMA_TX_GRP17_FIRST_PHY_ADDR | Tx GRP 17 First Link Address | page 210 |
| 0xc23 | IMA_TX_GRP17_ID | Tx GRP 17 Tx Group ID | page 211 |
| 0xc24 | IMA_TX_GRP17_STAT_CTL | Tx GRP 17 Status / Control | page 212 |
| 0xc25 | IMA_TX_GRP17_TIMING_INFO | Tx GRP 17 Timing Control | page 213 |
| 0xc26 | IMA_TX_GRP17_TEST_CTL | Tx GRP 17 Test Control | page 214 |
| 0xc27 | IMA_TX_GRP17_TX_TEST_PATTERN | Tx GRP 17 Tx Test Pattern | page 215 |
| 0xc28 | IMA_TX_GRP18_RX_TEST_PATTERN | Tx GRP 18 Rx Test Pattern | page 208 |
| 0xc29 | IMA_TX_GRP18_CTL | Tx GRP 18 Control | page 209 |
| 0xc2a | IMA_TX_GRP18_FIRST_PHY_ADDR | Tx GRP 18 First Link Address | page 210 |
| 0xc2b | IMA_TX_GRP18_ID | Tx GRP 18 Tx Group ID | page 211 |
| 0xc2c | IMA_TX_GRP18_STAT_CTL | Tx GRP 18 Status / Control | page 212 |
| 0xc2d | IMA_TX_GRP18_TIMING_INFO | Tx GRP 18 Timing Control | page 213 |
| 0xc2e | IMA_TX_GRP18_TEST_CTL | Tx GRP 18 Test Control | page 214 |
| 0xc2f | IMA_TX_GRP18_TX_TEST_PATTERN | Tx GRP 18 Tx Test Pattern | page 215 |
| 0xc30 | IMA_TX_GRP19_RX_TEST_PATTERN | Tx GRP 19 Rx Test Pattern | page 208 |

Table 2-10. IMA Control and Status Registers (23 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|--|--------------------------|
| 0xc31 | IMA_TX_GRP19_CTL | Tx GRP 19 Control | page 209 |
| 0xc32 | IMA_TX_GRP19_FIRST_PHY_ADDR | Tx GRP 19 First Link Address | page 210 |
| 0xc33 | IMA_TX_GRP19_ID | Tx GRP 19 Tx Group ID | page 211 |
| 0xc34 | IMA_TX_GRP19_STAT_CTL | Tx GRP 19 Status / Control | page 212 |
| 0xc35 | IMA_TX_GRP19_TIMING_INFO | Tx GRP 19 Timing Control | page 213 |
| 0xc36 | IMA_TX_GRP19_TEST_CTL | Tx GRP 19 Test Control | page 214 |
| 0xc37 | IMA_TX_GRP19_TX_TEST_PATTERN | Tx GRP 19 Tx Test Pattern | page 215 |
| 0xc38 | IMA_TX_GRP20_RX_TEST_PATTERN | Tx GRP 20 Rx Test Pattern | page 208 |
| 0xc39 | IMA_TX_GRP20_CTL | Tx GRP 20 Control | page 209 |
| 0xc3a | IMA_TX_GRP20_FIRST_PHY_ADDR | Tx GRP 20 First Link Address | page 210 |
| 0xc3b | IMA_TX_GRP20_ID | Tx GRP 20 Tx Group ID | page 211 |
| 0xc3c | IMA_TX_GRP20_STAT_CTL | Tx GRP 20 Status / Control | page 212 |
| 0xc3d | IMA_TX_GRP20_TIMING_INFO | Tx GRP 20 Timing Control | page 213 |
| 0xc3e | IMA_TX_GRP20_TEST_CTL | Tx GRP 20 Test Control | page 214 |
| 0xc3f | IMA_TX_GRP20_TX_TEST_PATTERN | Tx GRP 20 Tx Test Pattern | page 215 |
| Tx UTOPIA Addresses 16 - 19 Cell Counters | | | |
| 0xc40 | IMA_TX_ATM16_CELL_COUNT_LSB | Transmit UTOPIA Address 0x10 Cell Count LSBs | page 216 |
| 0xc41 | IMA_TX_ATM16_CELL_COUNT_MSB | Transmit UTOPIA Address 0x10 Cell Count MSBs | |
| 0xc42 | IMA_TX_ATM17_CELL_COUNT_LSB | Transmit UTOPIA Address 0x11 Cell Count LSBs | |
| 0xc43 | IMA_TX_ATM17_CELL_COUNT_MSB | Transmit UTOPIA Address 0x11 Cell Count MSBs | |
| 0xc44 | IMA_TX_ATM18_CELL_COUNT_LSB | Transmit UTOPIA Address 0x12 Cell Count LSBs | |
| 0xc45 | IMA_TX_ATM18_CELL_COUNT_MSB | Transmit UTOPIA Address 0x12 Cell Count MSBs | |
| 0xc46 | IMA_TX_ATM19_CELL_COUNT_LSB | Transmit UTOPIA Address 0x13 Cell Count LSBs | |
| 0xc47 | IMA_TX_ATM19_CELL_COUNT_MSB | Transmit UTOPIA Address 0x13 Cell Count MSBs | |
| Rx UTOPIA Addresses 16 - 19 Cell Counters | | | |
| 0xc48 | IMA_RX_ATM16_CELL_COUNT_LSB | Receive UTOPIA Address 0x10 Cell Count LSBs | page 218 |
| 0xc49 | IMA_RX_ATM16_CELL_COUNT_MSB | Receive UTOPIA Address 0x10 Cell Count MSBs | |
| 0xc4a | IMA_RX_ATM17_CELL_COUNT_LSB | Receive UTOPIA Address 0x11 Cell Count LSBs | |
| 0xc4b | IMA_RX_ATM17_CELL_COUNT_MSB | Receive UTOPIA Address 0x11 Cell Count MSBs | |
| 0xc4c | IMA_RX_ATM18_CELL_COUNT_LSB | Receive UTOPIA Address 0x12 Cell Count LSBs | |
| 0xc4d | IMA_RX_ATM18_CELL_COUNT_MSB | Receive UTOPIA Address 0x12 Cell Count MSBs | |
| 0xc4e | IMA_RX_ATM19_CELL_COUNT_LSB | Receive UTOPIA Address 0x13 Cell Count LSBs | |
| 0xc4f | IMA_RX_ATM19_CELL_COUNT_MSB | Receive UTOPIA Address 0x13 Cell Count MSBs | |
| Receive Groups 17–20 Configuration Tables | | | |
| 0xc50 | IMA_RX_GRP17_CFG | Rx GRP 17 Configuration | page 220 |
| 0xc51 | IMA_RX_GRP17_CTL | Rx GRP 17 Control | page 221 |
| 0xc52 | IMA_RX_GRP17_FIRST_PHY_ADDR | Rx GRP 17 First Link Address | page 222 |
| 0xc53 | IMA_RX_GRP17_ID | Rx GRP 17 Rx Group ID | page 223 |
| 0xc54 | IMA_RX_GRP18_CFG | Rx GRP 18 Configuration | page 220 |

Table 2-10. IMA Control and Status Registers (24 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|------------------------------|--------------------------|
| 0xc55 | IMA_RX_GRP18_CTL | Rx GRP 18 Control | page 221 |
| 0xc56 | IMA_RX_GRP18_FIRST_PHY_ADDR | Rx GRP 18 First Link Address | page 222 |
| 0xc57 | IMA_RX_GRP18_ID | Rx GRP 18 Rx Group ID | page 223 |
| 0xc58 | IMA_RX_GRP19_CFG | Rx GRP 19 Configuration | page 220 |
| 0xc59 | IMA_RX_GRP19_CTL | Rx GRP 19 Control | page 221 |
| 0xc5a | IMA_RX_GRP19_FIRST_PHY_ADDR | Rx GRP 19 First Link Address | page 222 |
| 0xc5b | IMA_RX_GRP19_ID | Rx GRP 19 Rx Group ID | page 223 |
| 0xc5c | IMA_RX_GRP20_CFG | Rx GRP 20 Configuration | page 220 |
| 0xc5d | IMA_RX_GRP20_CTL | Rx GRP 20 Control | page 221 |
| 0xc5e | IMA_RX_GRP20_FIRST_PHY_ADDR | Rx GRP 20 First Link Address | page 222 |
| 0xc5f | IMA_RX_GRP20_ID | Rx GRP 20 Rx Group ID | page 223 |
| Receive Groups 17–20 Far-End Status | | | |
| 0xc60 | IMA_RX_GRP17_RX_TEST_PATTERN | Rx GRP 17 Rx Test Pattern | page 224 |
| 0xc62 | IMA_RX_GRP17_STAT_CTL_CHANGE | Rx GRP 17 SCCI | page 225 |
| 0xc63 | IMA_RX_GRP17_ACTUAL_GRP_ID | Rx GRP 17 Rx Group ID | page 226 |
| 0xc64 | IMA_RX_GRP17_STAT_CTL | Rx GRP 17 Status / Control | page 227 |
| 0xc65 | IMA_RX_GRP17_TIMING_INFO | Rx GRP 17 Timing Control | page 228 |
| 0xc66 | IMA_RX_GRP17_TEST_CTL | Rx GRP 17 Test Control | page 229 |
| 0xc67 | IMA_RX_GRP17_TX_TEST_PATTERN | Rx GRP 17 Tx Test Pattern | page 230 |
| 0xc68 | IMA_RX_GRP18_RX_TEST_PATTERN | Rx GRP 18 Rx Test Pattern | page 224 |
| 0xc6a | IMA_RX_GRP18_STAT_CTL_CHANGE | Rx GRP 18 SCCI | page 225 |
| 0xc6b | IMA_RX_GRP18_ACTUAL_GRP_ID | Rx GRP 18 Rx Group ID | page 226 |
| 0xc6c | IMA_RX_GRP18_STAT_CTL | Rx GRP 18 Status / Control | page 227 |
| 0xc6d | IMA_RX_GRP18_TIMING_INFO | Rx GRP 18 Timing Control | page 228 |
| 0xc6e | IMA_RX_GRP18_TEST_CTL | Rx GRP 18 Test Control | page 229 |
| 0xc6f | IMA_RX_GRP18_TX_TEST_PATTERN | Rx GRP 18 Tx Test Pattern | page 230 |
| 0xc70 | IMA_RX_GRP19_RX_TEST_PATTERN | Rx GRP 19 Rx Test Pattern | page 224 |
| 0xc72 | IMA_RX_GRP19_STAT_CTL_CHANGE | Rx GRP 19 SCCI | page 225 |
| 0xc73 | IMA_RX_GRP19_ACTUAL_GRP_ID | Rx GRP 19 Rx Group ID | page 226 |
| 0xc74 | IMA_RX_GRP19_STAT_CTL | Rx GRP 19 Status / Control | page 227 |
| 0xc75 | IMA_RX_GRP19_TIMING_INFO | Rx GRP 19 Timing Control | page 228 |
| 0xc76 | IMA_RX_GRP19_TEST_CTL | Rx GRP 19 Test Control | page 229 |
| 0xc77 | IMA_RX_GRP19_TX_TEST_PATTERN | Rx GRP 19 Tx Test Pattern | page 230 |
| 0xc78 | IMA_RX_GRP20_RX_TEST_PATTERN | Rx GRP 20 Rx Test Pattern | page 224 |
| 0xc7a | IMA_RX_GRP20_STAT_CTL_CHANGE | Rx GRP 20 SCCI | page 225 |

Table 2-10. IMA Control and Status Registers (25 of 33)

| Address | Name | Description (Continued) | Page Number |
|---|------------------------------|------------------------------|--------------------------|
| 0xc7b | IMA_RX_GRP20_ACTUAL_GRP_ID | Rx GRP 20 Rx Group ID | page 226 |
| 0xc7c | IMA_RX_GRP20_STAT_CTL | Rx GRP 20 Status / Control | page 227 |
| 0xc7d | IMA_RX_GRP20_TIMING_INFO | Rx GRP 20 Timing Control | page 228 |
| 0xc7e | IMA_RX_GRP20_TEST_CTL | Rx GRP 20 Test Control | page 229 |
| 0xc7f | IMA_RX_GRP20_TX_TEST_PATTERN | Rx GRP 20 Tx Test Pattern | page 230 |
| Transmit Groups 21–24 Configuration Tables | | | |
| 0xca0 | IMA_TX_GRP21_RX_TEST_PATTERN | Tx GRP 21 Rx Test Pattern | page 208 |
| 0xca1 | IMA_TX_GRP21_CTL | Tx GRP 21 Control | page 209 |
| 0xca2 | IMA_TX_GRP21_FIRST_PHY_ADDR | Tx GRP 21 First Link Address | page 210 |
| 0xca3 | IMA_TX_GRP21_ID | Tx GRP 21 Tx Group ID | page 211 |
| 0xca4 | IMA_TX_GRP21_STAT_CTL | Tx GRP 21 Status / Control | page 212 |
| 0xca5 | IMA_TX_GRP21_TIMING_INFO | Tx GRP 21 Timing Control | page 213 |
| 0xca6 | IMA_TX_GRP21_TEST_CTL | Tx GRP 21 Test Control | page 214 |
| 0xca7 | IMA_TX_GRP21_TX_TEST_PATTERN | Tx GRP 21 Tx Test Pattern | page 215 |
| 0xca8 | IMA_TX_GRP22_RX_TEST_PATTERN | Tx GRP 22 Rx Test Pattern | page 208 |
| 0xca9 | IMA_TX_GRP22_CTL | Tx GRP 22 Control | page 209 |
| 0xcaa | IMA_TX_GRP22_FIRST_PHY_ADDR | Tx GRP 22 First Link Address | page 210 |
| 0xcab | IMA_TX_GRP22_ID | Tx GRP 22 Tx Group ID | page 211 |
| 0xcac | IMA_TX_GRP22_STAT_CTL | Tx GRP 22 Status / Control | page 212 |
| 0xcad | IMA_TX_GRP22_TIMING_INFO | Tx GRP 22 Timing Control | page 213 |
| 0xcae | IMA_TX_GRP22_TEST_CTL | Tx GRP 22 Test Control | page 214 |
| 0xcaf | IMA_TX_GRP22_TX_TEST_PATTERN | Tx GRP 22 Tx Test Pattern | page 215 |
| 0xcb0 | IMA_TX_GRP23_RX_TEST_PATTERN | Tx GRP 23 Rx Test Pattern | page 208 |
| 0xcb1 | IMA_TX_GRP23_CTL | Tx GRP 23 Control | page 209 |
| 0xcb2 | IMA_TX_GRP23_FIRST_PHY_ADDR | Tx GRP 23 First Link Address | page 210 |
| 0xcb3 | IMA_TX_GRP23_ID | Tx GRP 23 Tx Group ID | page 211 |
| 0xcb4 | IMA_TX_GRP23_STAT_CTL | Tx GRP 23 Status / Control | page 212 |
| 0xcb5 | IMA_TX_GRP23_TIMING_INFO | Tx GRP 23 Timing Control | page 213 |
| 0xcb6 | IMA_TX_GRP23_TEST_CTL | Tx GRP 23 Test Control | page 214 |
| 0xcb7 | IMA_TX_GRP23_TX_TEST_PATTERN | Tx GRP 23 Tx Test Pattern | page 215 |
| 0xcb8 | IMA_TX_GRP24_RX_TEST_PATTERN | Tx GRP 24 Rx Test Pattern | page 208 |
| 0xcb9 | IMA_TX_GRP24_CTL | Tx GRP 24 Control | page 209 |
| 0xcba | IMA_TX_GRP24_FIRST_PHY_ADDR | Tx GRP 24 First Link Address | page 210 |
| 0xcbb | IMA_TX_GRP24_ID | Tx GRP 24 Tx Group ID | page 211 |
| 0xcbc | IMA_TX_GRP24_STAT_CTL | Tx GRP 24 Status / Control | page 212 |

Table 2-10. IMA Control and Status Registers (26 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|--|--------------------------|
| 0xcbd | IMA_TX_GRP24_TIMING_INFO | Tx GRP 24 Timing Control | page 213 |
| 0xcbe | IMA_TX_GRP24_TEST_CTL | Tx GRP 24 Test Control | page 214 |
| 0xcbf | IMA_TX_GRP24_TX_TEST_PATTERN | Tx GRP 24 Tx Test Pattern | page 215 |
| Tx UTOPIA Addresses 20 - 23 Cell Counters | | | |
| 0xcc0 | IMA_TX_ATM20_CELL_COUNT_LSB | Transmit UTOPIA Address 0x14 Cell Count LSBs | page 216 |
| 0xcc1 | IMA_TX_ATM20_CELL_COUNT_MSB | Transmit UTOPIA Address 0x14 Cell Count MSBs | |
| 0xcc2 | IMA_TX_ATM21_CELL_COUNT_LSB | Transmit UTOPIA Address 0x15 Cell Count LSBs | |
| 0xcc3 | IMA_TX_ATM21_CELL_COUNT_MSB | Transmit UTOPIA Address 0x15 Cell Count MSBs | |
| 0xcc4 | IMA_TX_ATM22_CELL_COUNT_LSB | Transmit UTOPIA Address 0x16 Cell Count LSBs | |
| 0xcc5 | IMA_TX_ATM22_CELL_COUNT_MSB | Transmit UTOPIA Address 0x16 Cell Count MSBs | |
| 0xcc6 | IMA_TX_ATM23_CELL_COUNT_LSB | Transmit UTOPIA Address 0x17 Cell Count LSBs | |
| 0xcc7 | IMA_TX_ATM23_CELL_COUNT_MSB | Transmit UTOPIA Address 0x17 Cell Count MSBs | |
| Rx UTOPIA Addresses 20 - 23 Cell Counters | | | |
| 0xcc8 | IMA_RX_ATM20_CELL_COUNT_LSB | Receive UTOPIA Address 0x14 Cell Count LSBs | page 218 |
| 0xcc9 | IMA_RX_ATM20_CELL_COUNT_MSB | Receive UTOPIA Address 0x14 Cell Count MSBs | |
| 0xcca | IMA_RX_ATM21_CELL_COUNT_LSB | Receive UTOPIA Address 0x15 Cell Count LSBs | |
| 0xccb | IMA_RX_ATM21_CELL_COUNT_MSB | Receive UTOPIA Address 0x15 Cell Count MSBs | |
| 0xccc | IMA_RX_ATM22_CELL_COUNT_LSB | Receive UTOPIA Address 0x16 Cell Count LSBs | |
| 0xccd | IMA_RX_ATM22_CELL_COUNT_MSB | Receive UTOPIA Address 0x16 Cell Count MSBs | |
| 0xcce | IMA_RX_ATM23_CELL_COUNT_LSB | Receive UTOPIA Address 0x17 Cell Count LSBs | |
| 0xccf | IMA_RX_ATM23_CELL_COUNT_MSB | Receive UTOPIA Address 0x17 Cell Count MSBs | |
| Receive Groups 21–24 Configuration Tables | | | |
| 0xcd0 | IMA_RX_GRP21_CFG | Rx GRP 21 Configuration | page 220 |
| 0xcd1 | IMA_RX_GRP21_CTL | Rx GRP 21 Control | page 221 |
| 0xcd2 | IMA_RX_GRP21_FIRST_PHY_ADDR | Rx GRP 21 First Link Address | page 222 |
| 0xcd3 | IMA_RX_GRP21_ID | Rx GRP 21 Rx Group ID | page 223 |
| 0xcd4 | IMA_RX_GRP22_CFG | Rx GRP 22 Configuration | page 220 |
| 0xcd5 | IMA_RX_GRP22_CTL | Rx GRP 22 Control | page 221 |
| 0xcd6 | IMA_RX_GRP22_FIRST_PHY_ADDR | Rx GRP 22 First Link Address | page 222 |
| 0xcd7 | IMA_RX_GRP22_ID | Rx GRP 22 Rx Group ID | page 223 |
| 0xcd8 | IMA_RX_GRP23_CFG | Rx GRP 23 Configuration | page 220 |
| 0xcd9 | IMA_RX_GRP23_CTL | Rx GRP 23 Control | page 221 |
| 0xcda | IMA_RX_GRP23_FIRST_PHY_ADDR | Rx GRP 23 First Link Address | page 222 |
| 0xcdb | IMA_RX_GRP23_ID | Rx GRP 23 Rx Group ID | page 223 |
| 0xcdc | IMA_RX_GRP24_CFG | Rx GRP 24 Configuration | page 220 |
| 0xcdde | IMA_RX_GRP24_CTL | Rx GRP 24 Control | page 221 |
| 0xcde | IMA_RX_GRP24_FIRST_PHY_ADDR | Rx GRP 24 First Link Address | page 222 |
| 0xcdf | IMA_RX_GRP24_ID | Rx GRP 24 Rx Group ID | page 223 |

Table 2-10. IMA Control and Status Registers (27 of 33)

| Address | Name | Description (Continued) | Page Number |
|---|------------------------------|------------------------------|--------------------------|
| Receive Groups 21–24 Far-End Status | | | |
| 0xce0 | IMA_RX_GRP21_RX_TEST_PATTERN | Rx GRP 21 Rx Test Pattern | page 224 |
| 0xce2 | IMA_RX_GRP21_STAT_CTL_CHANGE | Rx GRP 21 SCCI | page 225 |
| 0xce3 | IMA_RX_GRP21_ACTUAL_GRP_ID | Rx GRP 21 Rx Group ID | page 226 |
| 0xce4 | IMA_RX_GRP21_STAT_CTL | Rx GRP 21 Status / Control | page 227 |
| 0xce5 | IMA_RX_GRP21_TIMING_INFO | Rx GRP 21 Timing Control | page 228 |
| 0xce6 | IMA_RX_GRP21_TEST_CTL | Rx GRP 21 Test Control | page 229 |
| 0xce7 | IMA_RX_GRP21_TX_TEST_PATTERN | Rx GRP 21 Tx Test Pattern | page 230 |
| 0xce8 | IMA_RX_GRP22_RX_TEST_PATTERN | Rx GRP 22 Rx Test Pattern | page 224 |
| 0xcea | IMA_RX_GRP22_STAT_CTL_CHANGE | Rx GRP 22 SCCI | page 225 |
| 0xceb | IMA_RX_GRP22_ACTUAL_GRP_ID | Rx GRP 22 Rx Group ID | page 226 |
| 0xcec | IMA_RX_GRP22_STAT_CTL | Rx GRP 22 Status / Control | page 227 |
| 0xced | IMA_RX_GRP22_TIMING_INFO | Rx GRP 22 Timing Control | page 228 |
| 0xcee | IMA_RX_GRP22_TEST_CTL | Rx GRP 22 Test Control | page 229 |
| 0xcef | IMA_RX_GRP22_TX_TEST_PATTERN | Rx GRP 22 Tx Test Pattern | page 230 |
| 0xcf0 | IMA_RX_GRP23_RX_TEST_PATTERN | Rx GRP 23 Rx Test Pattern | page 224 |
| 0xcf2 | IMA_RX_GRP23_STAT_CTL_CHANGE | Rx GRP 23 SCCI | page 225 |
| 0xcf3 | IMA_RX_GRP23_ACTUAL_GRP_ID | Rx GRP 23 Rx Group ID | page 226 |
| 0xcf4 | IMA_RX_GRP23_STAT_CTL | Rx GRP 23 Status / Control | page 227 |
| 0xcf5 | IMA_RX_GRP23_TIMING_INFO | Rx GRP 23 Timing Control | page 228 |
| 0xcf6 | IMA_RX_GRP23_TEST_CTL | Rx GRP 23 Test Control | page 229 |
| 0xcf7 | IMA_RX_GRP23_TX_TEST_PATTERN | Rx GRP 23 Tx Test Pattern | page 230 |
| 0xcf8 | IMA_RX_GRP24_RX_TEST_PATTERN | Rx GRP 24 Rx Test Pattern | page 224 |
| 0xcfa | IMA_RX_GRP24_STAT_CTL_CHANGE | Rx GRP 24 SCCI | page 225 |
| 0xcfb | IMA_RX_GRP24_ACTUAL_GRP_ID | Rx GRP 24 Rx Group ID | page 226 |
| 0xcfc | IMA_RX_GRP24_STAT_CTL | Rx GRP 24 Status / Control | page 227 |
| 0xcfd | IMA_RX_GRP24_TIMING_INFO | Rx GRP 24 Timing Control | page 228 |
| 0xcfe | IMA_RX_GRP24_TEST_CTL | Rx GRP 24 Test Control | page 229 |
| 0xcff | IMA_RX_GRP24_TX_TEST_PATTERN | Rx GRP 24 Tx Test Pattern | page 230 |
| Transmit Groups 25–28 Configuration Tables | | | |
| 0xd20 | IMA_TX_GRP25_RX_TEST_PATTERN | Tx GRP 25 Rx Test Pattern | page 208 |
| 0xd21 | IMA_TX_GRP25_CTL | Tx GRP 25 Control | page 209 |
| 0xd22 | IMA_TX_GRP25_FIRST_PHY_ADDR | Tx GRP 25 First Link Address | page 210 |
| 0xd23 | IMA_TX_GRP25_ID | Tx GRP 25 Tx Group ID | page 211 |
| 0xd24 | IMA_TX_GRP25_STAT_CTL | Tx GRP 25 Status / Control | page 212 |

Table 2-10. IMA Control and Status Registers (28 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|--|--------------------------|
| 0xd25 | IMA_TX_GRP25_TIMING_INFO | Tx GRP 25 Timing Control | page 213 |
| 0xd26 | IMA_TX_GRP25_TEST_CTL | Tx GRP 25 Test Control | page 214 |
| 0xd27 | IMA_TX_GRP25_TX_TEST_PATTERN | Tx GRP 25 Tx Test Pattern | page 215 |
| 0xd28 | IMA_TX_GRP26_RX_TEST_PATTERN | Tx GRP 26 Rx Test Pattern | page 208 |
| 0xd29 | IMA_TX_GRP26_CTL | Tx GRP 26 Control | page 209 |
| 0xd2a | IMA_TX_GRP26_FIRST_PHY_ADDR | Tx GRP 26 First Link Address | page 210 |
| 0xd2b | IMA_TX_GRP26_ID | Tx GRP 26 Tx Group ID | page 211 |
| 0xd2c | IMA_TX_GRP26_STAT_CTL | Tx GRP 26 Status / Control | page 212 |
| 0xd2d | IMA_TX_GRP26_TIMING_INFO | Tx GRP 26 Timing Control | page 213 |
| 0xd2e | IMA_TX_GRP26_TEST_CTL | Tx GRP 26 Test Control | page 214 |
| 0xd2f | IMA_TX_GRP26_TX_TEST_PATTERN | Tx GRP 26 Tx Test Pattern | page 215 |
| 0xd30 | IMA_TX_GRP27_RX_TEST_PATTERN | Tx GRP 27 Rx Test Pattern | page 208 |
| 0xd31 | IMA_TX_GRP27_CTL | Tx GRP 27 Control | page 209 |
| 0xd32 | IMA_TX_GRP27_FIRST_PHY_ADDR | Tx GRP 27 First Link Address | page 210 |
| 0xd33 | IMA_TX_GRP27_ID | Tx GRP 27 Tx Group ID | page 211 |
| 0xd34 | IMA_TX_GRP27_STAT_CTL | Tx GRP 27 Status / Control | page 212 |
| 0xd35 | IMA_TX_GRP27_TIMING_INFO | Tx GRP 27 Timing Control | page 213 |
| 0xd36 | IMA_TX_GRP27_TEST_CTL | Tx GRP 27 Test Control | page 214 |
| 0xd37 | IMA_TX_GRP27_TX_TEST_PATTERN | Tx GRP 27 Tx Test Pattern | page 215 |
| 0xd38 | IMA_TX_GRP28_RX_TEST_PATTERN | Tx GRP 28 Rx Test Pattern | page 208 |
| 0xd39 | IMA_TX_GRP28_CTL | Tx GRP 28 Control | page 209 |
| 0xd3a | IMA_TX_GRP28_FIRST_PHY_ADDR | Tx GRP 28 First Link Address | page 210 |
| 0xd3b | IMA_TX_GRP28_ID | Tx GRP 28 Tx Group ID | page 211 |
| 0xd3c | IMA_TX_GRP28_STAT_CTL | Tx GRP 28 Status / Control | page 212 |
| 0xd3d | IMA_TX_GRP28_TIMING_INFO | Tx GRP 28 Timing Control | page 213 |
| 0xd3e | IMA_TX_GRP28_TEST_CTL | Tx GRP 28 Test Control | page 214 |
| 0xd3f | IMA_TX_GRP28_TX_TEST_PATTERN | Tx GRP 28 Tx Test Pattern | page 215 |
| Tx UTOPIA Addresses 24 - 27 Cell Counters | | | |
| 0xd40 | IMA_TX_ATM24_CELL_COUNT_LSB | Transmit UTOPIA Address 0x18 Cell Count LSBs | page 216 |
| 0xd41 | IMA_TX_ATM24_CELL_COUNT_MSB | Transmit UTOPIA Address 0x18 Cell Count MSBs | |
| 0xd42 | IMA_TX_ATM25_CELL_COUNT_LSB | Transmit UTOPIA Address 0x19 Cell Count LSBs | |
| 0xd43 | IMA_TX_ATM25_CELL_COUNT_MSB | Transmit UTOPIA Address 0x19 Cell Count MSBs | |
| 0xd44 | IMA_TX_ATM26_CELL_COUNT_LSB | Transmit UTOPIA Address 0x1A Cell Count LSBs | |
| 0xd45 | IMA_TX_ATM26_CELL_COUNT_MSB | Transmit UTOPIA Address 0x1A Cell Count MSBs | |
| 0xd46 | IMA_TX_ATM27_CELL_COUNT_LSB | Transmit UTOPIA Address 0x1B Cell Count LSBs | |
| 0xd47 | IMA_TX_ATM27_CELL_COUNT_MSB | Transmit UTOPIA Address 0x1B Cell Count MSBs | |

Table 2-10. IMA Control and Status Registers (29 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|---|-------------|
| Rx UTOPIA Addresses 24 - 27 Cell Counters | | | |
| 0xd48 | IMA_RX_ATM24_CELL_COUNT_LSB | Receive UTOPIA Address 0x18 Cell Count LSBs | page 218 |
| 0xd49 | IMA_RX_ATM24_CELL_COUNT_MSB | Receive UTOPIA Address 0x18 Cell Count MSBs | |
| 0xd4a | IMA_RX_ATM25_CELL_COUNT_LSB | Receive UTOPIA Address 0x19 Cell Count LSBs | |
| 0xd4b | IMA_RX_ATM25_CELL_COUNT_MSB | Receive UTOPIA Address 0x19 Cell Count MSBs | |
| 0xd4c | IMA_RX_ATM26_CELL_COUNT_LSB | Receive UTOPIA Address 0x1A Cell Count LSBs | |
| 0xd4d | IMA_RX_ATM26_CELL_COUNT_MSB | Receive UTOPIA Address 0x1A Cell Count MSBs | |
| 0xd4e | IMA_RX_ATM27_CELL_COUNT_LSB | Receive UTOPIA Address 0x1B Cell Count LSBs | |
| 0xd4f | IMA_RX_ATM27_CELL_COUNT_MSB | Receive UTOPIA Address 0x1B Cell Count MSBs | |
| Receive Groups 25–28 Configuration Tables | | | |
| 0xd50 | IMA_RX_GRP25_CFG | Rx GRP 25 Configuration | page 220 |
| 0xd51 | IMA_RX_GRP25_CTL | Rx GRP 25 Control | page 221 |
| 0xd52 | IMA_RX_GRP25_FIRST_PHY_ADDR | Rx GRP 25 First Link Address | page 222 |
| 0xd53 | IMA_RX_GRP25_ID | Rx GRP 25 Rx Group ID | page 223 |
| 0xd54 | IMA_RX_GRP26_CFG | Rx GRP 26 Configuration | page 220 |
| 0xd55 | IMA_RX_GRP26_CTL | Rx GRP 26 Control | page 221 |
| 0xd56 | IMA_RX_GRP26_FIRST_PHY_ADDR | Rx GRP 26 First Link Address | page 222 |
| 0xd57 | IMA_RX_GRP26_ID | Rx GRP 26 Rx Group ID | page 223 |
| 0xd58 | IMA_RX_GRP27_CFG | Rx GRP 27 Configuration | page 220 |
| 0xd59 | IMA_RX_GRP27_CTL | Rx GRP 27 Control | page 221 |
| 0xd5a | IMA_RX_GRP27_FIRST_PHY_ADDR | Rx GRP 27 First Link Address | page 222 |
| 0xd5b | IMA_RX_GRP27_ID | Rx GRP 27 Rx Group ID | page 223 |
| 0xd5c | IMA_RX_GRP28_CFG | Rx GRP 28 Configuration | page 220 |
| 0xd5d | IMA_RX_GRP28_CTL | Rx GRP 28 Control | page 221 |
| 0xd5e | IMA_RX_GRP28_FIRST_PHY_ADDR | Rx GRP 28 First Link Address | page 222 |
| 0xd5f | IMA_RX_GRP28_ID | Rx GRP 28 Rx Group ID | page 223 |
| Receive Groups 25–28 Far-End Status | | | |
| 0xd60 | IMA_RX_GRP25_RX_TEST_PATTERN | Rx GRP 25 Rx Test Pattern | page 224 |
| 0xd62 | IMA_RX_GRP25_STAT_CTL_CHANGE | Rx GRP 25 SCCI | page 225 |
| 0xd63 | IMA_RX_GRP25_ACTUAL_GRP_ID | Rx GRP 25 Rx Group ID | page 226 |
| 0xd64 | IMA_RX_GRP25_STAT_CTL | Rx GRP 25 Status / Control | page 227 |
| 0xd65 | IMA_RX_GRP25_TIMING_INFO | Rx GRP 25 Timing Control | page 228 |
| 0xd66 | IMA_RX_GRP25_TEST_CTL | Rx GRP 25 Test Control | page 229 |
| 0xd67 | IMA_RX_GRP25_TX_TEST_PATTERN | Rx GRP 25 Tx Test Pattern | page 230 |
| 0xd68 | IMA_RX_GRP26_RX_TEST_PATTERN | Rx GRP 26 Rx Test Pattern | page 224 |
| 0xd6a | IMA_RX_GRP26_STAT_CTL_CHANGE | Rx GRP 26 SCCI | page 225 |
| 0xd6b | IMA_RX_GRP26_ACTUAL_GRP_ID | Rx GRP 26 Rx Group ID | page 226 |

Table 2-10. IMA Control and Status Registers (30 of 33)

| Address | Name | Description (Continued) | Page Number |
|---|------------------------------|------------------------------|--------------------------|
| 0xd6c | IMA_RX_GRP26_STAT_CTL | Rx GRP 26 Status / Control | page 227 |
| 0xd6d | IMA_RX_GRP26_TIMING_INFO | Rx GRP 26 Timing Control | page 228 |
| 0xd6e | IMA_RX_GRP26_TEST_CTL | Rx GRP 26 Test Control | page 229 |
| 0xd6f | IMA_RX_GRP26_TX_TEST_PATTERN | Rx GRP 26 Tx Test Pattern | page 230 |
| 0xd70 | IMA_RX_GRP27_RX_TEST_PATTERN | Rx GRP 27 Rx Test Pattern | page 224 |
| 0xd72 | IMA_RX_GRP27_STAT_CTL_CHANGE | Rx GRP 27 SCCI | page 225 |
| 0xd73 | IMA_RX_GRP27_ACTUAL_GRP_ID | Rx GRP 27 Rx Group ID | page 226 |
| 0xd74 | IMA_RX_GRP27_STAT_CTL | Rx GRP 27 Status / Control | page 227 |
| 0xd75 | IMA_RX_GRP27_TIMING_INFO | Rx GRP 27 Timing Control | page 228 |
| 0xd76 | IMA_RX_GRP27_TEST_CTL | Rx GRP 27 Test Control | page 229 |
| 0xd77 | IMA_RX_GRP27_TX_TEST_PATTERN | Rx GRP 27 Tx Test Pattern | page 230 |
| 0xd78 | IMA_RX_GRP28_RX_TEST_PATTERN | Rx GRP 28 Rx Test Pattern | page 224 |
| 0xd7a | IMA_RX_GRP28_STAT_CTL_CHANGE | Rx GRP 28 SCCI | page 225 |
| 0xd7b | IMA_RX_GRP28_ACTUAL_GRP_ID | Rx GRP 28 Rx Group ID | page 226 |
| 0xd7c | IMA_RX_GRP28_STAT_CTL | Rx GRP 28 Status / Control | page 227 |
| 0xd7d | IMA_RX_GRP28_TIMING_INFO | Rx GRP 28 Timing Control | page 228 |
| 0xd7e | IMA_RX_GRP28_TEST_CTL | Rx GRP 28 Test Control | page 229 |
| 0xd7f | IMA_RX_GRP28_TX_TEST_PATTERN | Rx GRP 28 Tx Test Pattern | page 230 |
| Transmit Groups 29–32 Configuration Tables | | | |
| 0xda0 | IMA_TX_GRP29_RX_TEST_PATTERN | Tx GRP 29 Rx Test Pattern | page 208 |
| 0xda1 | IMA_TX_GRP29_CTL | Tx GRP 29 Control | page 209 |
| 0xda2 | IMA_TX_GRP29_FIRST_PHY_ADDR | Tx GRP 29 First Link Address | page 210 |
| 0xda3 | IMA_TX_GRP29_ID | Tx GRP 29 Tx Group ID | page 211 |
| 0xda4 | IMA_TX_GRP29_STAT_CTL | Tx GRP 29 Status / Control | page 212 |
| 0xda5 | IMA_TX_GRP29_TIMING_INFO | Tx GRP 29 Timing Control | page 213 |
| 0xda6 | IMA_TX_GRP29_TEST_CTL | Tx GRP 29 Test Control | page 214 |
| 0xda7 | IMA_TX_GRP29_TX_TEST_PATTERN | Tx GRP 29 Tx Test Pattern | page 215 |
| 0xda8 | IMA_TX_GRP30_RX_TEST_PATTERN | Tx GRP 30 Rx Test Pattern | page 208 |
| 0xda9 | IMA_TX_GRP30_CTL | Tx GRP 30 Control | page 209 |
| 0xdaa | IMA_TX_GRP30_FIRST_PHY_ADDR | Tx GRP 30 First Link Address | page 210 |
| 0xdab | IMA_TX_GRP30_ID | Tx GRP 30 Tx Group ID | page 211 |
| 0xdac | IMA_TX_GRP30_STAT_CTL | Tx GRP 30 Status / Control | page 212 |
| 0xdad | IMA_TX_GRP30_TIMING_INFO | Tx GRP 30 Timing Control | page 213 |
| 0xdae | IMA_TX_GRP30_TEST_CTL | Tx GRP 30 Test Control | page 214 |
| 0xdaf | IMA_TX_GRP30_TX_TEST_PATTERN | Tx GRP 30 Tx Test Pattern | page 215 |

Table 2-10. IMA Control and Status Registers (31 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|--|--------------------------|
| 0xdb0 | IMA_TX_GRP31_RX_TEST_PATTERN | Tx GRP 31 Rx Test Pattern | page 208 |
| 0xdb1 | IMA_TX_GRP31_CTL | Tx GRP 31 Control | page 209 |
| 0xdb2 | IMA_TX_GRP31_FIRST_PHY_ADDR | Tx GRP 31 First Link Address | page 210 |
| 0xdb3 | IMA_TX_GRP31_ID | Tx GRP 31 Tx Group ID | page 211 |
| 0xdb4 | IMA_TX_GRP31_STAT_CTL | Tx GRP 31 Status / Control | page 212 |
| 0xdb5 | IMA_TX_GRP31_TIMING_INFO | Tx GRP 31 Timing Control | page 213 |
| 0xdb6 | IMA_TX_GRP31_TEST_CTL | Tx GRP 31 Test Control | page 214 |
| 0xdb7 | IMA_TX_GRP31_TX_TEST_PATTERN | Tx GRP 31 Tx Test Pattern | page 215 |
| 0xdb8 | IMA_TX_GRP32_RX_TEST_PATTERN | Tx GRP 32 Rx Test Pattern | page 208 |
| 0xdb9 | IMA_TX_GRP32_CTL | Tx GRP 32 Control | page 209 |
| 0xdba | IMA_TX_GRP32_FIRST_PHY_ADDR | Tx GRP 32 First Link Address | page 210 |
| 0xdbb | IMA_TX_GRP32_ID | Tx GRP 32 Tx Group ID | page 211 |
| 0xdbc | IMA_TX_GRP32_STAT_CTL | Tx GRP 32 Status / Control | page 212 |
| 0xdbd | IMA_TX_GRP32_TIMING_INFO | Tx GRP 32 Timing Control | page 213 |
| 0xdbe | IMA_TX_GRP32_TEST_CTL | Tx GRP 32 Test Control | page 214 |
| 0xdbf | IMA_TX_GRP32_TX_TEST_PATTERN | Tx GRP 32 Tx Test Pattern | page 215 |
| Tx UTOPIA Addresses 28 - 31 Cell Counters | | | |
| 0xdc0 | IMA_TX_ATM28_CELL_COUNT_LSB | Transmit UTOPIA Address 0x1C Cell Count LSBs | page 216 |
| 0xdc1 | IMA_TX_ATM28_CELL_COUNT_MSB | Transmit UTOPIA Address 0x1C Cell Count MSBs | |
| 0xdc2 | IMA_TX_ATM29_CELL_COUNT_LSB | Transmit UTOPIA Address 0x1D Cell Count LSBs | |
| 0xdc3 | IMA_TX_ATM29_CELL_COUNT_MSB | Transmit UTOPIA Address 0x1D Cell Count MSBs | |
| 0xdc4 | IMA_TX_ATM30_CELL_COUNT_LSB | Transmit UTOPIA Address 0x1E Cell Count LSBs | |
| 0xdc5 | IMA_TX_ATM30_CELL_COUNT_MSB | Transmit UTOPIA Address 0x1E Cell Count MSBs | |
| 0xdc6 | IMA_TX_ATM31_CELL_COUNT_LSB | Transmit UTOPIA Address 0x1F Cell Count LSBs | |
| 0xdc7 | IMA_TX_ATM31_CELL_COUNT_MSB | Transmit UTOPIA Address 0x1F Cell Count MSBs | |
| Rx UTOPIA Addresses 28 - 31 Cell Counters | | | |
| 0xdc8 | IMA_RX_ATM28_CELL_COUNT_LSB | Receive UTOPIA Address 0x1C Cell Count LSBs | page 218 |
| 0xdc9 | IMA_RX_ATM28_CELL_COUNT_MSB | Receive UTOPIA Address 0x1C Cell Count MSBs | |
| 0xdca | IMA_RX_ATM29_CELL_COUNT_LSB | Receive UTOPIA Address 0x1D Cell Count LSBs | |
| 0xdcb | IMA_RX_ATM29_CELL_COUNT_MSB | Receive UTOPIA Address 0x1D Cell Count MSBs | |
| 0xdcc | IMA_RX_ATM30_CELL_COUNT_LSB | Receive UTOPIA Address 0x1E Cell Count LSBs | |
| 0xdcd | IMA_RX_ATM30_CELL_COUNT_MSB | Receive UTOPIA Address 0x1E Cell Count MSBs | |
| 0xdce | IMA_RX_ATM31_CELL_COUNT_LSB | Receive UTOPIA Address 0x1F Cell Count LSBs | |
| 0xdcf | IMA_RX_ATM31_CELL_COUNT_MSB | Receive UTOPIA Address 0x1F Cell Count MSBs | |
| Receive Groups 29–32 Configuration Tables | | | |
| 0xdd0 | IMA_RX_GRP29_CFG | Rx GRP 29 Configuration | page 220 |
| 0xdd1 | IMA_RX_GRP29_CTL | Rx GRP 29 Control | page 221 |
| 0xdd2 | IMA_RX_GRP29_FIRST_PHY_ADDR | Rx GRP 29 First Link Address | page 222 |
| 0xdd3 | IMA_RX_GRP29_ID | Rx GRP 29 Rx Group ID | page 223 |

Table 2-10. IMA Control and Status Registers (32 of 33)

| Address | Name | Description (Continued) | Page Number |
|--|------------------------------|------------------------------|--------------------------|
| 0xdd4 | IMA_RX_GRP30_CFG | Rx GRP 30 Configuration | page 220 |
| 0xdd5 | IMA_RX_GRP30_CTL | Rx GRP 30 Control | page 221 |
| 0xdd6 | IMA_RX_GRP30_FIRST_PHY_ADDR | Rx GRP 30 First Link Address | page 222 |
| 0xdd7 | IMA_RX_GRP30_ID | Rx GRP 30 Rx Group ID | page 223 |
| 0xdd8 | IMA_RX_GRP31_CFG | Rx GRP 31 Configuration | page 220 |
| 0xdd9 | IMA_RX_GRP31_CTL | Rx GRP 31 Control | page 221 |
| 0xdda | IMA_RX_GRP31_FIRST_PHY_ADDR | Rx GRP 31 First Link Address | page 222 |
| 0xddb | IMA_RX_GRP31_ID | Rx GRP 31 Rx Group ID | page 223 |
| 0xddc | IMA_RX_GRP32_CFG | Rx GRP 32 Configuration | page 220 |
| 0xddd | IMA_RX_GRP32_CTL | Rx GRP 32 Control | page 221 |
| 0xdde | IMA_RX_GRP32_FIRST_PHY_ADDR | Rx GRP 32 First Link Address | page 222 |
| 0xddf | IMA_RX_GRP32_ID | Rx GRP 32 Rx Group ID | page 223 |
| Receive Groups 29–32 Far-End Status | | | |
| 0xde0 | IMA_RX_GRP29_RX_TEST_PATTERN | Rx GRP 29 Rx Test Pattern | page 224 |
| 0xde2 | IMA_RX_GRP29_STAT_CTL_CHANGE | Rx GRP 29 SCCI | page 225 |
| 0xde3 | IMA_RX_GRP29_ACTUAL_GRP_ID | Rx GRP 29 Rx Group ID | page 226 |
| 0xde4 | IMA_RX_GRP29_STAT_CTL | Rx GRP 29 Status / Control | page 227 |
| 0xde5 | IMA_RX_GRP29_TIMING_INFO | Rx GRP 29 Timing Control | page 228 |
| 0xde6 | IMA_RX_GRP29_TEST_CTL | Rx GRP 29 Test Control | page 229 |
| 0xde7 | IMA_RX_GRP29_TX_TEST_PATTERN | Rx GRP 29 Tx Test Pattern | page 230 |
| 0xde8 | IMA_RX_GRP30_RX_TEST_PATTERN | Rx GRP 30 Rx Test Pattern | page 224 |
| 0xdea | IMA_RX_GRP30_STAT_CTL_CHANGE | Rx GRP 30 SCCI | page 225 |
| 0xdeb | IMA_RX_GRP30_ACTUAL_GRP_ID | Rx GRP 30 Rx Group ID | page 226 |
| 0xdec | IMA_RX_GRP30_STAT_CTL | Rx GRP 30 Status / Control | page 227 |
| 0xded | IMA_RX_GRP30_TIMING_INFO | Rx GRP 30 Timing Control | page 228 |
| 0xdee | IMA_RX_GRP30_TEST_CTL | Rx GRP 30 Test Control | page 229 |
| 0xdef | IMA_RX_GRP30_TX_TEST_PATTERN | Rx GRP 30 Tx Test Pattern | page 230 |
| 0xdf0 | IMA_RX_GRP31_RX_TEST_PATTERN | Rx GRP 31 Rx Test Pattern | page 224 |
| 0xdf2 | IMA_RX_GRP31_STAT_CTL_CHANGE | Rx GRP 31 SCCI | page 225 |
| 0xdf3 | IMA_RX_GRP31_ACTUAL_GRP_ID | Rx GRP 31 Rx Group ID | page 226 |
| 0xdf4 | IMA_RX_GRP31_STAT_CTL | Rx GRP 31 Status / Control | page 227 |
| 0xdf5 | IMA_RX_GRP31_TIMING_INFO | Rx GRP 31 Timing Control | page 228 |
| 0xdf6 | IMA_RX_GRP31_TEST_CTL | Rx GRP 31 Test Control | page 229 |
| 0xdf7 | IMA_RX_GRP31_TX_TEST_PATTERN | Rx GRP 31 Tx Test Pattern | page 230 |
| 0xdf8 | IMA_RX_GRP32_RX_TEST_PATTERN | Rx GRP 32 Rx Test Pattern | page 224 |

Table 2-10. IMA Control and Status Registers (33 of 33)

| Address | Name | Description (Continued) | Page Number |
|-----------------------------------|------------------------------|---|--------------------------|
| 0xdfa | IMA_RX_GRP32_STAT_CTL_CHANGE | Rx GRP 32 SCCI | page 225 |
| 0xdfb | IMA_RX_GRP32_ACTUAL_GRP_ID | Rx GRP 32 Rx Group ID | page 226 |
| 0xdfc | IMA_RX_GRP32_STAT_CTL | Rx GRP 32 Status / Control | page 227 |
| 0xdfd | IMA_RX_GRP32_TIMING_INFO | Rx GRP 32 Timing Control | page 228 |
| 0xdfe | IMA_RX_GRP32_TEST_CTL | Rx GRP 32 Test Control | page 229 |
| 0xdff | IMA_RX_GRP32_TX_TEST_PATTERN | Rx GRP 32 Tx Test Pattern | page 230 |
| ATM Cell Capture Registers | | | |
| 0xe00-0xe2F | CELL_CAP_PAYLDn | Cell Capture Payload Contents Registers | page 244 |
| 0xe30 | CAP_FAC | Capture Facility Register | page 244 |
| 0xe31 | CAP_CNTL | Capture Control Register | page 244 |
| 0xe32 | CAP_STAT | Capture Status Register | page 245 |

2.2 TC Registers

2.2.1 0x00—SUMINT (Summary Interrupt Indication Status Register)

The SUMINT register indicates the one-second interrupts, external framer interrupts, and port summary interrupts.

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7 | 0 | — | Reserved, set to a logical 0. |
| 6 | 0 | — | Reserved, set to a logical 0. |
| 5 | 0 | — | Reserved, set to a logical 0. |
| 4 | 0 | — | Reserved, set to a logical 0. |
| 3 | 0 | — | Reserved, set to a logical 0. |
| 2 | 0 | — | Reserved, set to a logical 0. |
| 1 | — | TxCeIIInt ⁽¹⁾ | When a logical 1 is read, this bit indicates a Transmit Cell Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication occurred in the TxCeIIInt register (0x2C). |
| 0 | — | RxCeIIInt ⁽¹⁾ | When a logical 1 is read, this bit indicates a Receive Cell Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication occurred in the RxCeIIInt register (0x2D). |

Footnote:

(1) This bit is a summary indication of any interrupt events that occurred in the indicated registers. This bit is a pointer to the next interrupt indication register to be read. This bit will be cleared when the interrupt bits in the corresponding interrupt indication registers are read and automatically cleared.

2.2.2 0x01—ENSUMINT (Summary Interrupt Control Register)

The ENSUMINT register controls which of the interrupts listed in the SUMINT register (0x00) appear in the SUMPORT register and on the MicroInt* (pin AA1), provided the corresponding ENSUMPORT bit is enabled and EnIntPin (bit 3) in the GENCTRL register (0xF00) is enabled.

| Bit | Default | Name | Description |
|-----|---------|-------------|--|
| 7 | 0 | — | Reserved, set to a logical 0. |
| 6 | 0 | — | Reserved, set to a logical 0. |
| 5 | 0 | — | Reserved, set to a logical 0. |
| 4 | 0 | — | Reserved, set to a logical 0. |
| 3 | 0 | — | Reserved, set to a logical 0. |
| 2 | 0 | — | Reserved, set to a logical 0. |
| 1 | 0 | EnTxCellInt | When written to a logical 1, this bit enables the transmit cell interrupts located in the TxCellInt register (0x2C). These interrupts appear can on the MicroInt* pin (pin AA1), provided that EnPortInt in the ENSUMPORT0-3 register (0x0F06, 0x0F08, 0x0F0A, 0x0F0C) is enabled for this port and EnIntPin (bit 3) in the GENCTRL register (0xF00) is enabled. |
| 0 | 0 | EnRxCellInt | When written to a logical 1, this bit enables the receive cell interrupts located in the RxCellInt register (0x2D). These interrupts can appear on the MicroInt* pin (pin AA1), provided that EnPortInt in the ENSUMPORT0-3 register (0x0F06, 0x0F08, 0x0F0A, 0x0F0C) is enabled for this port and EnIntPin (bit 3) in the GENCTRL register (0xF00) is enabled. |

2.2.3 0x04—PMODE (Port Mode Control Register)

The PMODE register controls the port-level software resets, source loopback, and physical layer interface mode.

| Bit | Default | Name | Description | | | | | | | | | |
|--------------|---------------------|----------------------------|---|-------------|--------------|--------------|-------------|--------------|----------------|--------------|---------------------|--|
| 7 | 0 | PrtMstRst | When written to a logical 1, this bit initiates a Port Master Reset. All internal state machines associated with this port are reset and all control registers for this port, except this one, assume their default values. Only bits 0–6 in this register are overwritten with their default values. | | | | | | | | | |
| 6 | 0 | PrtLgcRst | When written to a logical 1, this bit initiates a Port Logic Reset. All internal state machines associated with this port are reset but all registers (0x00–0x3F) listed as “Type: W/R” in Table 2-3 are unaltered. Output signals for this port are three-state during Port Logic Reset. | | | | | | | | | |
| 5 | 0 | SrcLoop ⁽¹⁾ | When written to a logical 1, this bit enables a source loopback. The line transmit clock and data outputs are connected to the line receive clock and data inputs. Refer to Figure 1-12 . During Source loopback mode 0, the device is automatically configured for General Purpose mode (ignoring the contents of the PhyType[2:0] bits). | | | | | | | | | |
| 4 | 0 | FeLnLoop ⁽¹⁾ | Enables Far-end line loopback. In this mode, the receive data is processed by the TC block and looped back at the UTOPIA interface to the transmit side. Refer to Figure 1-13 . | | | | | | | | | |
| 3 | 0 | SrcLoopMode ⁽¹⁾ | When source loopback is enabled (when SrcLoop is written to a logic 1), this bit select between the two types of source loopback as follows: 0 - Source Loopback 0 selected 1 - Source Loopback 1 selected | | | | | | | | | |
| 2 | 0 | PhyType[2] ⁽¹⁾ | These bits determine the Physical Layer Interface Mode: <table style="width: 100%; border: none;"> <tr> <td style="width: 33%;">000—T1 mode</td> <td style="width: 33%;">011—Reserved</td> <td style="width: 33%;">110—DSL Mode</td> </tr> <tr> <td>001—E1 mode</td> <td>100—Reserved</td> <td>111—Power Down</td> </tr> <tr> <td>010—Reserved</td> <td>101—General Purpose</td> <td></td> </tr> </table> <p>In General Purpose Mode, the SPRxSync and SPTxSync pins are ignored. (However, good design practice would have them tied high.)</p> | 000—T1 mode | 011—Reserved | 110—DSL Mode | 001—E1 mode | 100—Reserved | 111—Power Down | 010—Reserved | 101—General Purpose | |
| 000—T1 mode | 011—Reserved | 110—DSL Mode | | | | | | | | | | |
| 001—E1 mode | 100—Reserved | 111—Power Down | | | | | | | | | | |
| 010—Reserved | 101—General Purpose | | | | | | | | | | | |
| 1 | 0 | PhyType[1] ⁽¹⁾ | | | | | | | | | | |
| 0 | 0 | PhyType[0] ⁽¹⁾ | | | | | | | | | | |

Footnote:
(1) These bits should only be changed when the device or port logic reset is asserted.

2.2.4 0x05—IOMODE (Input/Output Mode Control Register)

The IOMODE register controls the line interface signal polarities and status outputs.

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7 | 0 | — | Reserved, set to 0. |
| 6 | 0 | RxSyncPol ⁽¹⁾ | This bit determines the Receiver Synchronization input Polarity. When written to a logical 1, the active level on the SPRxSync input is high. When written to a logical 0, the active level is low. |
| 5 | 0 | RxCkPol ⁽¹⁾ | This bit determines the Receiver Clock Input Polarity. When written to a logical 1, the active edge on the SPRxCk input is the falling edge. When written to a logical 0, the active edge is the rising edge. |
| 4 | 0 | TxSyncPol ⁽¹⁾ | This bit determines the Transmitter Synchronization input Polarity. When written to a logical 1, the active level on the SPTxSync input is high. When written to a logical 0, the active level is low. |
| 3 | 0 | TxCkPol ⁽¹⁾ | This bit determines the Transmitter Clock Input Polarity. When written to a logical 1, the active edge on the SPTxCk input is the falling edge. When written to a logical 0, the active edge is the rising edge. |
| 2 | 0 | TxDatShft ⁽¹⁾ | This bit when set to a logical 1 shifts the serial Tx data by 1/2 a cycle. This results in the Tx data being output a 1/2 SPTxCk cycle later than when the Tx inputs are sampled. This feature is disabled when set to 0. |
| 1 | 0 | — | Reserved, set to 0. |
| 0 | 0 | — | Reserved, set to 0. |

Footnote:
 (1) These bits should only be changed when the device or port logic reset is asserted.

2.2.5 0x08—CGEN (Cell Generation Control Register)

The CGEN register controls the device's cell generation functions.

| Bit | Default | Name | Description |
|-----|---------|-------------|--|
| 7 | 0 | DisHEC | When written to a logical 1, this bit disables internal generation of the HEC field. When disabled, the HEC field from the UTOPIA interface remains unchanged in the transmitted cell. When written to a logical 0, HEC is internally calculated and inserted in the transmitted cell. |
| 6 | 1 | EnTxCos | When written to a logical 1, this bit enables the Transmit HEC Coset. When written to a logical 0, the HEC Coset is disabled. |
| 5 | 1 | EnTxCellScr | When written to a logical 1, this bit enables the Transmit Cell Scrambler. When written to a logical 0, the Transmit Cell Scrambler is disabled. |
| 4 | 0 | ErrHEC | When written to a logical 1, this bit causes the ERRPAT register to be XORed with the calculated HEC byte for one transmit cell. These bits are cleared automatically by internal circuitry after the indicated error insertion has taken place. Clearing takes precedence over a simultaneous write operation to this register. |
| 3 | 0 | DSL SyncPol | This bit controls the polarity of the sync pulse in DSL mode. Set to 1 for active high and to 0 for active low. |
| 2 | 0 | — | Reserved, write to a logical 0. |
| 1 | 0 | EnTxDSSScr | When written to a logical 1, this bit enables the Transmit DSS Scrambler. When written to a logical 0, the Transmit DSS Scrambler is disabled. |
| 0 | 0 | EnRxDSSScr | When written to a logical 1, this bit enables the Receive DSS Scrambler. When written to a logical 0, the Receive DSS Scrambler is disabled. |

2.2.6 0x09—HDRFIELD (Header Field Control Register)

The HDRFIELD register controls the header insertion elements.

| Bit | Default | Name | Description |
|-----|---------|--------|--|
| 7 | 0 | — | Reserved, write to a logical 0. |
| 6 | 0 | — | Reserved, write to a logical 0. |
| 5 | 0 | — | Reserved, write to a logical 0. |
| 4 | 0 | InsGFC | When written to a logical 1, this bit inserts a Generic Flow Control (GFC) field in the outgoing header from the TXHDR registers. When written to a logical 0, the GFC field is not changed prior to transmission. |
| 3 | 0 | InsVPI | When written to a logical 1, this bit inserts a Virtual Path Identifier (VPI) field in the outgoing header from the TXHDR registers. When written to a logical 0, the VPI field is not changed prior to transmission. |
| 2 | 0 | InsVCI | When written to a logical 1, this bit inserts a Virtual Channel Identifier (VCI) field in the outgoing header from the TXHDR registers. When written to a logical 0, the VCI field is not changed prior to transmission. |
| 1 | 0 | InsPT | When written to a logical 1, this bit inserts a Payload Type (PT) field in the outgoing header from the TXHDR registers. When written to a logical 0, the PT field is not changed prior to transmission. |
| 0 | 0 | InsCLP | When written to a logical 1, this bit inserts a Cell Loss Priority (CLP) bit in the outgoing header from the TXHDR registers. When written to a logical 0, the CLP field is not changed prior to transmission. |

2.2.7 0x0A—IDLPAY (Transmit Idle Cell Payload Control Register)

The IDLPAY register contains the transmit idle cell payload.

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | 0 | IdlPay[7] | These bits hold the Transmit Idle Cell Payload values for outgoing idle cells. |
| 6 | 1 | IdlPay[6] | |
| 5 | 1 | IdlPay[5] | |
| 4 | 0 | IdlPay[4] | |
| 3 | 1 | IdlPay[3] | |
| 2 | 0 | IdlPay[2] | |
| 1 | 1 | IdlPay[1] | |
| 0 | 0 | IdlPay[0] | |

2.2.8 0x0B—ERRPAT (Error Pattern Control Register)

The ERRPAT register provides the error pattern for the HEC error insertion function. ErrHEC (bit 4) in the CGEN register (0x08) enables this function. Each bit in the error pattern register is XORed with the corresponding bit of the calculated HEC byte to be errored.

| Bit | Default | Name | Description |
|-----|---------|-----------|----------------------|
| 7 | 0 | ErrPat[7] | Error pattern bit 7. |
| 6 | 0 | ErrPat[6] | Error pattern bit 6. |
| 5 | 0 | ErrPat[5] | Error pattern bit 5. |
| 4 | 0 | ErrPat[4] | Error pattern bit 4. |
| 3 | 0 | ErrPat[3] | Error pattern bit 3. |
| 2 | 0 | ErrPat[2] | Error pattern bit 2. |
| 1 | 0 | ErrPat[1] | Error pattern bit 1. |
| 0 | 0 | ErrPat[0] | Error pattern bit 0. |

2.2.9 0x0C—CVAL (Cell Validation Control Register)

The CVAL register controls the validation of incoming cells.

| Bit | Default | Name | Description |
|-----|---------|-------------|---|
| 7 | 0 | RejHdr | When written to a logical 1, this bit enables the Rejection of certain Header cells. When enabled, cells with headers matching the RXHDRx/RXMSKx definition are rejected and all others are accepted. When written to a logical 0, cells with matching headers are accepted and cells with non-matching headers are rejected. |
| 6 | 1 | DelIdle | When written to a logical 1, this bit enables the Deletion of Idle Cells. When enabled, cells matching the RXIDL/IDLMSK definition are deleted from the received cell stream. When written to a logical 0, idle cells are included in the received stream. |
| 5 | 1 | EnRxCos | When written to a logical 1, this bit enables the Receive HEC Coset. When written to a logical 0, the HEC Coset is disabled. |
| 4 | 1 | EnRxCellScr | When written to a logical 1, this bit enables the Receive Cell Scrambler. When written to a logical 0, the Receive Cell Scrambler is disabled. |
| 3 | 0 | EnHECCorr | When written to a logical 1, this bit enables HEC Correction. When written to a logical 0, HEC Correction is disabled. |
| 2 | 0 | DisHECChk | When written to a logical 1, this bit disables HEC Checking. When written to a logical 0, HEC checking is performed as a cell validation criterion. See Table 1-26 . |
| 1 | 0 | DisCellRcvr | When written to a logical 1, this bit disables the Cell Receiver. When disabled, all cell reception is disabled on the next cell boundary. When written to a logical 0, cell reception begins or resumes on the next cell boundary. |
| 0 | 0 | DisLOCD | When written to a logical 1, this bit disables Loss of Cell Delineation. When disabled, cells are passed even if cell delineation has not been found. When written to a logical 0, cells are passed only while cell alignment has been achieved. See Table 1-26 . |

2.2.10 0x0D—UTOP1 (UTOPIA Control Register 1)

The UTOP1 register controls the UTOPIA resets.

| Bit | Default | Name | Description |
|-----|---------|---------|---|
| 7 | 0 | TxReset | When written to a logical 1, this bit resets the transmit FIFO pointers. This reset should only be used as a test function because it can create short cells. |
| 6 | 0 | RxReset | When written to a logical 1, this bit resets the receive FIFO pointers. This reset should only be used as a test function because it can create short cells. |
| 5 | 0 | — | Reserved, write to a logical 0. |
| 4 | 0 | — | Reserved, write to a logical 0. |
| 3 | 0 | — | Reserved, write to a logical 0. |
| 2 | 0 | — | Reserved, write to a logical 0. |
| 1 | 0 | — | Reserved, write to a logical 0. |
| 0 | 0 | — | Reserved, write to a logical 0. |

2.2.11 0x0E—UTOP2 (UTOPIA Control Register 2) (TC Block)

The UTOP2 register contains the multi-PHY address value for the port.

| Bit | Default | Name | Description |
|-----|---------|--------------------------------|--|
| 7 | 0 | — | Reserved, write to a logical 0. |
| 6 | 0 | — | Reserved, write to a logical 0. |
| 5 | 1 | UtopDis ⁽¹⁾ | When written to a logical 1, this bit disables UTOPIA outputs for this port. |
| 4 | 0 | MphyAddr[4]—MSB ⁽¹⁾ | These bits are the Multi-PHY Device Address. Each M2852x port should have a unique address. These bits correspond to the URxAddr and UTxAddr pins. When the pin matches the bit values, the port is accessed. This port ignores any transactions meant for another port or PHY device. |
| 3 | (2) | MphyAddr[3] ⁽¹⁾ | |
| 2 | (2) | MphyAddr[2] ⁽¹⁾ | |
| 1 | (2) | MphyAddr[1] ⁽¹⁾ | |
| 0 | (2) | MphyAddr[0]—LSB ⁽¹⁾ | |

Footnote:

(1) These bits should only be changed when the device or port logic reset is asserted.

(2) The default for these bits is the port number for each port. (0000—Port 0, 0001—Port 1, 0010—Port 2, 0011—Port 3, 0100—Port 4, 0101—Port 5, 0110—Port 6, 0111—Port 7, 1000—Port 8, 1001—Port 9, 1010—Port 10, 1011—Port 11, 1100—Port 12, 1101—Port 13, 1110—Port 14, 1111—Port 15, 0000—Port 16, 0001—Port 17, 0010—Port 18, 0011—Port 19, 0100—Port 20, 0101—Port 21, 0110—Port 22, 0111—Port 23, 1000—Port 24, 1001—Port 25, 1010—Port 26, 1011—Port 27, 1100—Port 28, 1101—Port 29, 1110—Port 30, 1111—Port 31)

2.2.12 0x0F—UDF2 (UDF2 Control Register)

The contents of the UDF2 register are inserted into the UDF2 byte on the UTOPIA receive bus when operating in 16-bit UTOPIA mode.

| Bit | Default | Name | Description |
|-----|---------|---------|--|
| 7 | 0 | UDF2[7] | The contents of this register are output over the UTOPIA receive bus when operating in UTOPIA 16-bit mode. The default matches the port address. |
| 6 | 0 | UDF2[6] | |
| 5 | 0 | UDF2[5] | |
| 4 | 0 | UDF2[4] | |
| 3 | (1) | UDF2[3] | |
| 2 | (1) | UDF2[2] | |
| 1 | (1) | UDF2[1] | |
| 0 | (1) | UDF2[0] | |

Footnote:
 (1) The default for these bits is the port number for each port. (0000—Port 0, 0001—Port 1, 0010—Port 2, 0011—Port 3, 0100—Port 4, 0101—Port 5, 0110—Port 6, 0111—Port 7, 1000—Port 8, 1001—Port 9, 1010—Port 10, 1011—Port 11, 1100—Port 12, 1101—Port 13, 1110—Port 14, 1111—Port 15, 0000—Port 16, 0001—Port 17, 0010—Port 18, 0011—Port 19, 0100—Port 20, 0101—Port 21, 0110—Port 22, 0111—Port 23, 1000—Port 24, 1001—Port 25, 1010—Port 26, 1011—Port 27, 1100—Port 28, 1101—Port 29, 1110—Port 30, 1111—Port 31)

2.2.13 0x10—TXHDR1 (Transmit Cell Header Control Register 1)

The TXHDR1 register contains the first byte of the Transmit Cell Header. It controls the header value that is inserted in the transmitted cell. This header consists of 32 bits divided among four registers (TXHDR1–4).

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 0 | TxHdr1[7] | These bits hold the Transmit Header values for Octet 1 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). |
| 6 | 0 | TxHdr1[6] | |
| 5 | 0 | TxHdr1[5] | GFC/VPI bits (for UNI they are GFC bits, for NNI they are VPI bits) |
| 4 | 0 | TxHdr1[4] | |
| 3 | 0 | TxHdr1[3] | VPI bits |
| 2 | 0 | TxHdr1[2] | |
| 1 | 0 | TxHdr1[1] | |
| 0 | 0 | TxHdr1[0] | |

2.2.14 0x11—TXHDR2 (Transmit Cell Header Control Register 2)

The TXHDR2 register contains the second byte of the Transmit Cell Header. (See 0x10—TXHDR1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 0 | TxHdr2[7] | These bits hold the Transmit Header values for Octet 2 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). |
| 6 | 0 | TxHdr2[6] | |
| 5 | 0 | TxHdr2[5] | |
| 4 | 0 | TxHdr2[4] | |
| 3 | 0 | TxHdr2[3] | VPI bits |
| 2 | 0 | TxHdr2[2] | |
| 1 | 0 | TxHdr2[1] | |
| 0 | 0 | TxHdr2[0] | |

2.2.15 0x12—TXHDR3 (Transmit Cell Header Control Register 3)

The TXHDR3 register contains the third byte of the Transmit Cell Header. (See 0x10—TXHDR1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 0 | TxHdr3[7] | These bits hold the Transmit Header values for Octet 3 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). |
| 6 | 0 | TxHdr3[6] | |
| 5 | 0 | TxHdr3[5] | |
| 4 | 0 | TxHdr3[4] | |
| 3 | 0 | TxHdr3[3] | |
| 2 | 0 | TxHdr3[2] | |
| 1 | 0 | TxHdr3[1] | |
| 0 | 0 | TxHdr3[0] | |

2.2.16 0x13—TXHDR4 (Transmit Cell Header Control Register 4)

The TXHDR4 register contains the fourth byte of the Transmit Cell Header. (See 0x10—TXHDR1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 0 | TxHdr4[7] | These bits hold the Transmit Header values for Octet 4 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). VCI bits |
| 6 | 0 | TxHdr4[6] | |
| 5 | 0 | TxHdr4[5] | |
| 4 | 0 | TxHdr4[4] | |
| 3 | 0 | TxHdr4[3] | Payload-type bits |
| 2 | 0 | TxHdr4[2] | |
| 1 | 0 | TxHdr4[1] | |
| 0 | 0 | TxHdr4[0] | Cell Loss Priority bit |

2.2.17 0x14—TXIDL1 (Transmit Idle Cell Header Control Register 1)

The TXIDL1 register contains the first byte of the Transmit Idle Cell Header. It controls the header value that is inserted in the transmitted idle cells. This header consists of 32 bits divided among four registers.

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 0 | TxIdl1[7] | These bits hold the Transmit Idle Cell Header values for Octet 1 of the outgoing cell. GFC/VPI bits (for UNI they are GFC bits, for NNI the are VPI bits) |
| 6 | 0 | TxIdl1[6] | |
| 5 | 0 | TxIdl1[5] | |
| 4 | 0 | TxIdl1[4] | |
| 3 | 0 | TxIdl1[3] | VPI bits |
| 2 | 0 | TxIdl1[2] | |
| 1 | 0 | TxIdl1[1] | |
| 0 | 0 | TxIdl1[0] | |

2.2.18 0x15—TXIDL2 (Transmit Idle Cell Header Control Register 2)

The TXIDL2 register contains the second byte of the Transmit Idle Cell Header. (See 0x14—TXIDL1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | 0 | TxIdl2[7] | These bits hold the Transmit Idle Cell Header values for Octet 2 of the outgoing cell. |
| 6 | 0 | TxIdl2[6] | |
| 5 | 0 | TxIdl2[5] | |
| 4 | 0 | TxIdl2[4] | |
| 3 | 0 | TxIdl2[3] | VPI bits |
| 2 | 0 | TxIdl2[2] | |
| 1 | 0 | TxIdl2[1] | |
| 0 | 0 | TxIdl2[0] | |

2.2.19 0x16—TXIDL3 (Transmit Idle Cell Header Control Register 3)

The TXIDL3 register contains the third byte of the Transmit Idle Cell Header. (See 0x14—TXIDL1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | 0 | TxIdl3[7] | These bits hold the Transmit Idle Cell Header values for Octet 3 of the outgoing cell. |
| 6 | 0 | TxIdl3[6] | |
| 5 | 0 | TxIdl3[5] | |
| 4 | 0 | TxIdl3[4] | |
| 3 | 0 | TxIdl3[3] | |
| 2 | 0 | TxIdl3[2] | |
| 1 | 0 | TxIdl3[1] | |
| 0 | 0 | TxIdl3[0] | |

2.2.20 0x17—TXIDL4 (Transmit Idle Cell Header Control Register 4)

The TXIDL4 register contains the fourth byte of the Transmit Idle Cell Header. (See 0x14—TXIDL1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | 0 | TxIdl4[7] | These bits hold the Transmit Idle Cell Header values for Octet 4 of the outgoing cell. |
| 6 | 0 | TxIdl4[6] | |
| 5 | 0 | TxIdl4[5] | |
| 4 | 0 | TxIdl4[4] | |
| 3 | 0 | TxIdl4[3] | VCI bits |
| 2 | 0 | TxIdl4[2] | |
| 1 | 0 | TxIdl4[1] | |
| 0 | 1 | TxIdl4[0] | Cell Loss Priority bit |

2.2.21 0x18—RXHDR1 (Receive Cell Header Control Register 1)

The RXHDR1 register contains the first byte of the Receive Cell Header. The header values direct ATM cells to the UTOPIA port if an incoming ATM cell header matches the value in the header register. Receive Header Mask Registers further qualify ATM cell reception. This header consists of 32 bits divided among four registers.

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 0 | RxHdr1[7] | These bits hold the Receive Header values for Octet 1 of the incoming cell. |
| 6 | 0 | RxHdr1[6] | |
| 5 | 0 | RxHdr1[5] | |
| 4 | 0 | RxHdr1[4] | |
| 3 | 0 | RxHdr1[3] | |
| 2 | 0 | RxHdr1[2] | |
| 1 | 0 | RxHdr1[1] | |
| 0 | 0 | RxHdr1[0] | |

2.2.22 0x19—RXHDR2 (Receive Cell Header Control Register 2)

The RXHDR2 register contains the second byte of the Receive Cell Header. (See 0x18—RXHDR1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 0 | RxHdr2[7] | These bits hold the Receive Header values for Octet 2 of the incoming cell. |
| 6 | 0 | RxHdr2[6] | |
| 5 | 0 | RxHdr2[5] | |
| 4 | 0 | RxHdr2[4] | |
| 3 | 0 | RxHdr2[3] | |
| 2 | 0 | RxHdr2[2] | |
| 1 | 0 | RxHdr2[1] | |
| 0 | 0 | RxHdr2[0] | |

2.2.23 0x1A—RXHDR3 (Receive Cell Header Control Register 3)

The RXHDR3 register contains the third byte of the Receive Cell Header. (See 0x18—RXHDR1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 0 | RxHdr3[7] | These bits hold the Receive Header values for Octet 3 of the incoming cell. |
| 6 | 0 | RxHdr3[6] | |
| 5 | 0 | RxHdr3[5] | |
| 4 | 0 | RxHdr3[4] | |
| 3 | 0 | RxHdr3[3] | |
| 2 | 0 | RxHdr3[2] | |
| 1 | 0 | RxHdr3[1] | |
| 0 | 0 | RxHdr3[0] | |

2.2.24 0x1B—RXHDR4 (Receive Cell Header Control Register 4)

The RXHDR4 register contains the fourth byte of the Receive Cell Header. (See 0x18—RXHDR1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 0 | RxHdr4[7] | These bits hold the Receive Header values for Octet 4 of the incoming cell. |
| 6 | 0 | RxHdr4[6] | |
| 5 | 0 | RxHdr4[5] | |
| 4 | 0 | RxHdr4[4] | |
| 3 | 0 | RxHdr4[3] | |
| 2 | 0 | RxHdr4[2] | |
| 1 | 0 | RxHdr4[1] | |
| 0 | 0 | RxHdr4[0] | |

2.2.25 0x1C—RXMSK1 (Receive Cell Mask Control Register 1)

The RXMSK1 register contains the first byte of the Receive Cell Mask. It modifies ATM cell screening, which compares the Receive Cell Header Registers to the incoming cells. Setting a bit in the Mask Register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1 bit 0 to 1 causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 1 | RxMsk1[7] | These bits hold the Receive Header Mask for Octet 1 of the incoming cell. |
| 6 | 1 | RxMsk1[6] | |
| 5 | 1 | RxMsk1[5] | |
| 4 | 1 | RxMsk1[4] | |
| 3 | 1 | RxMsk1[3] | |
| 2 | 1 | RxMsk1[2] | |
| 1 | 1 | RxMsk1[1] | |
| 0 | 1 | RxMsk1[0] | |

2.2.26 0x1D—RXMSK2 (Receive Cell Mask Control Register 2)

The RXMSK2 register contains the second byte of the Receive Cell Mask. (See 0x1D—RXMSK1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 1 | RxMsk2[7] | These bits hold the Receive Header Mask for Octet 2 of the incoming cell. |
| 6 | 1 | RxMsk2[6] | |
| 5 | 1 | RxMsk2[5] | |
| 4 | 1 | RxMsk2[4] | |
| 3 | 1 | RxMsk2[3] | |
| 2 | 1 | RxMsk2[2] | |
| 1 | 1 | RxMsk2[1] | |
| 0 | 1 | RxMsk2[0] | |

2.2.27 0x1E—RXMSK3 (Receive Cell Mask Control Register 3)

The RXMSK3 register contains the third byte of the Receive Cell Mask. (See 0x1D—RXMSK1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 1 | RxMsk3[7] | These bits hold the Receive Header Mask for Octet 3 of the incoming cell. |
| 6 | 1 | RxMsk3[6] | |
| 5 | 1 | RxMsk3[5] | |
| 4 | 1 | RxMsk3[4] | |
| 3 | 1 | RxMsk3[3] | |
| 2 | 1 | RxMsk3[2] | |
| 1 | 1 | RxMsk3[1] | |
| 0 | 1 | RxMsk3[0] | |

2.2.28 0x1F—RXMSK4 (Receive Cell Mask Control Register 4)

The RXMSK4 register contains the fourth byte of the Receive Cell Mask. (See 0x1D—RXMSK1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7 | 1 | RxMsk4[7] | These bits hold the Receive Header Mask for Octet 4 of the incoming cell. |
| 6 | 1 | RxMsk4[6] | |
| 5 | 1 | RxMsk4[5] | |
| 4 | 1 | RxMsk4[4] | |
| 3 | 1 | RxMsk4[3] | |
| 2 | 1 | RxMsk4[2] | |
| 1 | 1 | RxMsk4[1] | |
| 0 | 1 | RxMsk4[0] | |

2.2.29 0x20—RXIDL1 (Receive Idle Cell Header Control Register 1)

The RXIDL1 register contains the first byte of the Receive Idle Cell Header. It defines ATM idle cells for the cell receiver. Idle cells are discarded from the received stream if register CVAL (0x0C) bit 6 is set to 1. This header consists of 32 bits divided among four registers.

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | 0 | RxIdl1[7] | These bits hold the Receive Idle cell header for Octet 1 of the incoming cell. |
| 6 | 0 | RxIdl1[6] | |
| 5 | 0 | RxIdl1[5] | |
| 4 | 0 | RxIdl1[4] | |
| 3 | 0 | RxIdl1[3] | |
| 2 | 0 | RxIdl1[2] | |
| 1 | 0 | RxIdl1[1] | |
| 0 | 0 | RxIdl1[0] | |

2.2.30 0x21—RXIDL2 (Receive Idle Cell Header Control Register 2)

The RXIDL2 register contains the second byte of the Receive Idle Cell Header. (See 0x20—RXIDL1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | 0 | RxIdl2[7] | These bits hold the Receive Idle cell header for Octet 2 of the incoming cell. |
| 6 | 0 | RxIdl2[6] | |
| 5 | 0 | RxIdl2[5] | |
| 4 | 0 | RxIdl2[4] | |
| 3 | 0 | RxIdl2[3] | |
| 2 | 0 | RxIdl2[2] | |
| 1 | 0 | RxIdl2[1] | |
| 0 | 0 | RxIdl2[0] | |

2.2.31 0x22—RXIDL3 (Receive Idle Cell Header Control Register 3)

The RXIDL3 register contains the third byte of the Receive Idle Cell Header. (See 0x20—RXIDL1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | 0 | RxIdl3[7] | These bits hold the Receive Idle cell header for Octet 3 of the incoming cell. |
| 6 | 0 | RxIdl3[6] | |
| 5 | 0 | RxIdl3[5] | |
| 4 | 0 | RxIdl3[4] | |
| 3 | 0 | RxIdl3[3] | |
| 2 | 0 | RxIdl3[2] | |
| 1 | 0 | RxIdl3[1] | |
| 0 | 0 | RxIdl3[0] | |

2.2.32 0x23—RXIDL4 (Receive Idle Cell Header Control Register 4)

The RXIDL4 register contains the fourth byte of the Receive Idle Cell Header. (See 0x20—RXIDL1.)

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | 0 | RxIdl4[7] | These bits hold the Receive Idle cell header for Octet 4 of the incoming cell. |
| 6 | 0 | RxIdl4[6] | |
| 5 | 0 | RxIdl4[5] | |
| 4 | 0 | RxIdl4[4] | |
| 3 | 0 | RxIdl4[3] | |
| 2 | 0 | RxIdl4[2] | |
| 1 | 0 | RxIdl4[1] | |
| 0 | 1 | RxIdl4[0] | |

2.2.33 0x24—IDLMSK1 (Receive Idle Cell Mask Control Register 1)

The IDLMSK1 register contains the first byte of the Receive Idle Cell Mask. It modifies ATM cell screening, which compares the Receive Idle Cell Header Registers to the incoming cells. Setting a bit in the Mask Register causes the corresponding bit in the received ATM idle cell header to be disregarded for screening. For example, setting IDLMSK1 bit 0 to 1 causes cells to be accepted as ATM idle cells with either 1 or 0 in the octet 1, bit 0 position. This header consists of 32 bits divided among four registers.

| Bit | Default | Name | Description |
|-----|---------|------------|---|
| 7 | 0 | IdlMsk1[7] | These bits hold the Receive Idle cell header mask for Octet 1 of the incoming cell. |
| 6 | 0 | IdlMsk1[6] | |
| 5 | 0 | IdlMsk1[5] | |
| 4 | 0 | IdlMsk1[4] | |
| 3 | 0 | IdlMsk1[3] | |
| 2 | 0 | IdlMsk1[2] | |
| 1 | 0 | IdlMsk1[1] | |
| 0 | 0 | IdlMsk1[0] | |

2.2.34 0x25—IDLMSK2 (Receive Idle Cell Mask Control Register 2)

The IDLMSK2 register contains the second byte of the Receive Idle Cell Mask. (See 0x24—RXMSKL1.)

| Bit | Default | Name | Description |
|-----|---------|------------|---|
| 7 | 0 | IdlMsk2[7] | These bits hold the Receive Idle cell header mask for Octet 2 of the incoming cell. |
| 6 | 0 | IdlMsk2[6] | |
| 5 | 0 | IdlMsk2[5] | |
| 4 | 0 | IdlMsk2[4] | |
| 3 | 0 | IdlMsk2[3] | |
| 2 | 0 | IdlMsk2[2] | |
| 1 | 0 | IdlMsk2[1] | |
| 0 | 0 | IdlMsk2[0] | |

2.2.35 0x26—IDLMSK3 (Receive Idle Cell Mask Control Register 3)

The IDLMSK3 register contains the third byte of the Receive Idle Cell Mask. (See 0x24—RXMSKL1.)

| Bit | Default | Name | Description |
|-----|---------|------------|---|
| 7 | 0 | IdlMsk3[7] | These bits hold the Receive Idle cell header mask for Octet 3 of the incoming cell. |
| 6 | 0 | IdlMsk3[6] | |
| 5 | 0 | IdlMsk3[5] | |
| 4 | 0 | IdlMsk3[4] | |
| 3 | 0 | IdlMsk3[3] | |
| 2 | 0 | IdlMsk3[2] | |
| 1 | 0 | IdlMsk3[1] | |
| 0 | 0 | IdlMsk3[0] | |

2.2.36 0x27—IDLMSK4 (Receive Idle Cell Mask Control Register 4)

The IDLMSK4 register contains the fourth byte of the Receive Idle Cell Mask. (See 0x24—RXMSKL1.)

| Bit | Default | Name | Description |
|-----|---------|------------|---|
| 7 | 0 | IdlMsk4[7] | These bits hold the Receive Idle cell header mask for Octet 4 of the incoming cell. |
| 6 | 0 | IdlMsk4[6] | |
| 5 | 0 | IdlMsk4[5] | |
| 4 | 0 | IdlMsk4[4] | |
| 3 | 0 | IdlMsk4[3] | |
| 2 | 0 | IdlMsk4[2] | |
| 1 | 0 | IdlMsk4[1] | |
| 0 | 0 | IdlMsk4[0] | |

2.2.37 0x28—ENCELLT (Transmit Cell Interrupt Control Register)

The ENCELLT register controls which of the interrupts listed in the TxCellInt register (0x2C) appear on the MicroInt* pin (pin AA1), provided that both EnTxCellInt (bit 1) in the ENSUMINT register (0x01) and EnPortInt bit in the appropriate ENSUMPORTn (n= 0 - 3) register (0xF06, 0xF08, 0xF0A or 0xF0C) for this port are enabled, and EnIntPin (bit 3) in the GENCTRL register (0xF00) is enabled.

| Bit | Default | Name | Description |
|-----|---------|---------------|---|
| 7 | 1 | EnParErrInt | When written to a logical 1, this bit enables the Parity Error Interrupt. |
| 6 | 1 | EnSOCErrInt | When written to a logical 1, this bit enables the Start of Cell Error Interrupt. |
| 5 | 1 | EnTxOvflInt | When written to a logical 1, this bit enables the Transmit FIFO Overflow Interrupt. |
| 4 | 1 | EnRxOvflInt | When written to a logical 1, this bit enables the Receive FIFO Overflow Interrupt. |
| 3 | 1 | EnCellSentInt | When written to a logical 1, this bit enables the Cell Sent Interrupt. |
| 2 | 0 | — | Reserved for factory test, ignore. |
| 1 | 0 | — | Reserved, set to a logical 0. |
| 0 | 0 | — | Reserved, set to a logical 0. |

2.2.38 0x29—ENCELLR (Receive Cell Interrupt Control Register)

The ENCELLR register controls which of the interrupts listed in the RxCellInt register (0x2D) appear on the MicroInt* pin (pin AA1), provided that both EnRxCellInt (bit 0) in the ENSUMINT register (0x01) and EnPortInt bit in the appropriate ENSUMPORTn (n= 0 - 3) register (0xF06, 0xF08, 0xF0A or 0xF0C) for this port are enabled, and EnIntPin (bit 3) in the GENCTRL register (0xF00) is enabled.

| Bit | Default | Name | Description |
|-----|---------|----------------|---|
| 7 | 1 | EnLOCDInt | When written to a logical 1, this bit enables a Loss of Cell Delineation Interrupt. |
| 6 | 1 | EnHECDetInt | When written to a logical 1, this bit enables a HEC Error Detected Interrupt. |
| 5 | 1 | EnHECCorrInt | When written to a logical 1, this bit enables a HEC Error Corrected Interrupt. |
| 4 | 1 | — | Reserved, write to a logical 0. |
| 3 | 1 | EnCellRcvdInt | When written to a logical 1, this bit enables a Cell Received Interrupt. |
| 2 | 1 | EnIdleRcvdInt | When written to a logical 1, this bit enables an Idle Cell Received Interrupt. |
| 1 | 1 | EnNonMatchInt | When written to a logical 1, this bit enables a Non-matching Cell Received Interrupt. |
| 0 | 1 | EnNonZerGFCInt | When written to a logical 1, this bit enables a Non-zero GFC Received Interrupt. |

2.2.39 0x2C—TXCELLINT (Transmit Cell Interrupt Indication Status Register)

The TXCELLINT register indicates that a change of status has occurred within the transmit status signals.

| Bit | Default | Name | Description |
|-----|---------|----------------------------|--|
| 7 | — | ParErrInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that a Parity Error occurred. |
| 6 | — | SOCErrInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that a Start of Cell Error occurred. |
| 5 | — | TxOvflInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that a Transmit FIFO Overflow occurred. |
| 4 | — | RxOvflInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that a Receive FIFO Overflow occurred. |
| 3 | — | CellSentInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that a cell has been sent. |
| 2 | — | — | Reserved for factory test, ignore. |
| 1 | 0 | — | Reserved, set to a logical 0. |
| 0 | 0 | — | Reserved, write to a logical 0. |

Footnote:

(1) Single event—A 0 to 1 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

2.2.40 0x2D—RXCELLINT (Receive Cell Interrupt Indication Status Register)

The RXCELLINT register indicates that a change of status has occurred within the receive status signals.

| Bit | Default | Name | Description |
|-----|---------|-----------------------------|--|
| 7 | — | LOCDInt ⁽²⁾ | When a logical 1 is read, this bit indicates that a Loss of Cell Delineation has occurred. |
| 6 | — | HECDetInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that a HEC Error was detected. |
| 5 | — | HECCorrInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that a HEC Error was corrected. |
| 4 | — | — | Reserved, write to a logical 0. |
| 3 | — | CellRcvdInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that a cell has been received. |
| 2 | — | IdleRcvdInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that an Idle Cell has been received. |
| 1 | — | NonMatchInt ⁽¹⁾ | When a logical 1 is read, this bit indicates that a Non-matching Cell has been received. |
| 0 | — | NonZerGFCInt ⁽¹⁾ | When a logic 1 is read, this bit indicates that a Non-zero GFC has been received. |

Footnote:
 (1) Single event—A 0 to 1 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.
 (2) Dual event—Either a 0 to 1 or a 1 to 0 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

2.2.41 0x2E—TXCELL (Transmit Cell Status Register)

The TXCELL register contains status for the cell transmitter. This register is cleared on read. Bits 1-7 are **read-only**.

| Bit | Default | Name | Description |
|-----|---------|-------------------------|--|
| 7 | — | ParErr ⁽¹⁾ | When a logical 1 is read, this bit indicates that a parity error was received on the transmit UTOPIA input data octet. |
| 6 | — | SOCErr ⁽¹⁾ | When a logical 1 is read, this bit indicates that a Start of Cell Error was received on the UTxSOC pin (pin TBD). |
| 5 | — | TxOvfl ⁽¹⁾ | When a logical 1 is read, this bit indicates that a Transmit FIFO Overflow condition occurred in the transmit UTOPIA FIFO. |
| 4 | — | RxOvfl ⁽¹⁾ | When a logical 1 is read, this bit indicates that a Receive FIFO Overflow condition occurred in the receive UTOPIA FIFO. |
| 3 | — | CellSent ⁽¹⁾ | When a logical 1 is read, this bit indicates that a non-idle cell was formatted and transmitted. |
| 2 | — | — | Reserved for factory test, ignore. |
| 1 | 0 | — | Reserved, set to a logical 0. |
| 0 | 0 | — | Reserved, set to a logical 0. |

Footnote:
 (1) This status indicates an event that occurred since the register was last read.

2.2.42 0x2F—RXCELL (Receive Cell Status Register)

The RXCELL register contains status for the cell receiver. This register is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|--------------------------|--|
| 7 | — | LOCD ⁽²⁾ | When a logical 1 is read, this bit indicates a Loss of Cell Delineation. |
| 6 | — | HECDef ⁽¹⁾ | When a logical 1 is read, this bit indicates that an uncorrected HEC Error was detected. |
| 5 | — | HECCorr ⁽¹⁾ | When a logical 1 is read, this bit indicates that a HEC Error was corrected. |
| 4 | — | — | Reserved, ignore this bit. |
| 3 | — | CellRcvd | When logical 1 is read, this bit indicates that a valid cell was received. |
| 2 | — | IdleRcvd ⁽¹⁾ | When a logical 1 is read, this bit indicates that a cell with a header matching the receive idle cell header value and mask criteria was received. |
| 1 | — | NonMatch ⁽¹⁾ | When a logical 1 is read, this bit indicates that a cell has been rejected by the cell screening function. |
| 0 | — | NonZerGFC ⁽¹⁾ | When a logical 1 is read, this bit indicates that a cell with a Non-zero GFC field in the header was received. |

Footnote:

(1) This status indicates an event that occurred since the register was last read.

(2) This status reflects the current state of the circuit.

2.2.43 0x30—IDLNTL (Idle Cell Receive Counter [Low Byte])

The IDLNTL counter tracks the number of received idle cells. This byte of the counter should be read first. The counter is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|------------|------------------------------------|
| 7 | — | IdleCnt[7] | Received cell counter bit 7. |
| 6 | — | IdleCnt[6] | Received cell counter bit 6. |
| 5 | — | IdleCnt[5] | Received cell counter bit 5. |
| 4 | — | IdleCnt[4] | Received cell counter bit 4. |
| 3 | — | IdleCnt[3] | Received cell counter bit 3. |
| 2 | — | IdleCnt[2] | Received cell counter bit 2. |
| 1 | — | IdleCnt[1] | Received cell counter bit 1. |
| 0 | — | IdleCnt[0] | Received cell counter bit 0 (LSB). |

2.2.44 0x31—IDLCNTH (Idle Cell Receive Counter [High Byte])

The IDLCNTH counter tracks the number of received cells. The counter is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|-------------|-------------------------------|
| 7 | — | IdleCnt[15] | Received cell counter bit 15. |
| 6 | — | IdleCnt[14] | Received cell counter bit 14. |
| 5 | — | IdleCnt[13] | Received cell counter bit 13. |
| 4 | — | IdleCnt[12] | Received cell counter bit 12. |
| 3 | — | IdleCnt[11] | Received cell counter bit 11. |
| 2 | — | IdleCnt[10] | Received cell counter bit 10. |
| 1 | — | IdleCnt[9] | Received cell counter bit 9. |
| 0 | — | IdleCnt[8] | Received cell counter bit 8. |

2.2.45 0x33—LODCNT (LOCD Event Counter)

This counter tracks the number of times that cell delineation was lost. Note that the LOCD interrupt is a dual event interrupt and is set when cell delineation is lost or regained. Thus the number of LOCD events will not match the number of LOCD interrupts.

| Bit | Default | Name | Description |
|-----|---------|------------|---------------------------------|
| 7 | — | LODCCnt[7] | LOCD Event counter bit 7 (MSB). |
| 6 | — | LODCCnt[6] | LOCD Event counter bit 6. |
| 5 | — | LODCCnt[5] | LOCD Event counter bit 5. |
| 4 | — | LODCCnt[4] | LOCD Event counter bit 4. |
| 3 | — | LODCCnt[3] | LOCD Event counter bit 3. |
| 2 | — | LODCCnt[2] | LOCD Event counter bit 2. |
| 1 | — | LODCCnt[1] | LOCD Event counter bit 1. |
| 0 | — | LODCCnt[0] | LOCD Event counter bit 0 (LSB). |

2.2.46 0x34—TXCNTL (Transmitted Cell Counter [Low Byte])

The TXCNTL counter tracks the number of transmitted cells. This byte of the counter should be read first. The counter is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|----------|---------------------------------------|
| 7 | — | TxCnt[7] | Transmitted cell counter bit 7. |
| 6 | — | TxCnt[6] | Transmitted cell counter bit 6. |
| 5 | — | TxCnt[5] | Transmitted cell counter bit 5. |
| 4 | — | TxCnt[4] | Transmitted cell counter bit 4. |
| 3 | — | TxCnt[3] | Transmitted cell counter bit 3. |
| 2 | — | TxCnt[2] | Transmitted cell counter bit 2. |
| 1 | — | TxCnt[1] | Transmitted cell counter bit 1. |
| 0 | — | TxCnt[0] | Transmitted cell counter bit 0 (LSB). |

2.2.47 0x35—TXCNTH (Transmitted Cell Counter [High Byte])

The TXCNTH counter tracks the number of transmitted cells. The counter is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|-----------|----------------------------------|
| 7 | — | TxCnt[15] | Transmitted cell counter bit 15. |
| 6 | — | TxCnt[14] | Transmitted cell counter bit 14. |
| 5 | — | TxCnt[13] | Transmitted cell counter bit 13. |
| 4 | — | TxCnt[12] | Transmitted cell counter bit 12. |
| 3 | — | TxCnt[11] | Transmitted cell counter bit 11. |
| 2 | — | TxCnt[10] | Transmitted cell counter bit 10. |
| 1 | — | TxCnt[9] | Transmitted cell counter bit 9. |
| 0 | — | TxCnt[8] | Transmitted cell counter bit 8. |

2.2.48 0x37—CORRCNT (Corrected HEC Error Counter)

The CORRCNT counter tracks the number of corrected HEC errors. The counter is cleared on read 0x38—RXCNTL (Received Cell Counter [Low Byte]).

| Bit | Default | Name | Description |
|-----|---------|------------|--|
| 7 | — | CorrCnt[7] | Corrected HEC Error counter bit 7 (MSB). |
| 6 | — | CorrCnt[6] | Corrected HEC Error counter bit 6. |
| 5 | — | CorrCnt[5] | Corrected HEC Error counter bit 5. |
| 4 | — | CorrCnt[4] | Corrected HEC Error counter bit 4. |
| 3 | — | CorrCnt[3] | Corrected HEC Error counter bit 3. |
| 2 | — | CorrCnt[2] | Corrected HEC Error counter bit 2. |
| 1 | — | CorrCnt[1] | Corrected HEC Error counter bit 1. |
| 0 | — | CorrCnt[0] | Corrected HEC Error counter bit 0 (LSB). |

2.2.49 0x38—RXCNTL (Received Cell Counter [Low Byte])

The RXCNTL counter tracks the number of received cells. This byte of the counter should be read first. The counter is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|----------|------------------------------------|
| 7 | — | RxCnt[7] | Received cell counter bit 7. |
| 6 | — | RxCnt[6] | Received cell counter bit 6. |
| 5 | — | RxCnt[5] | Received cell counter bit 5. |
| 4 | — | RxCnt[4] | Received cell counter bit 4. |
| 3 | — | RxCnt[3] | Received cell counter bit 3. |
| 2 | — | RxCnt[2] | Received cell counter bit 2. |
| 1 | — | RxCnt[1] | Received cell counter bit 1. |
| 0 | — | RxCnt[0] | Received cell counter bit 0 (LSB). |

2.2.50 0x39—RXCNTH (Received Cell Counter [High Byte])

The RXCNTH register tracks the number of received cells. The counter is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|-----------|-------------------------------|
| 7 | — | RxCnt[15] | Received cell counter bit 15. |
| 6 | — | RxCnt[14] | Received cell counter bit 14. |
| 5 | — | RxCnt[13] | Received cell counter bit 13. |
| 4 | — | RxCnt[12] | Received cell counter bit 12. |
| 3 | — | RxCnt[11] | Received cell counter bit 11. |
| 2 | — | RxCnt[10] | Received cell counter bit 10. |
| 1 | — | RxCnt[9] | Received cell counter bit 9. |
| 0 | — | RxCnt[8] | Received cell counter bit 8. |

2.2.51 0x3B—UNCCNT (Uncorrected HEC Error Counter)

The UNCCNT counter tracks the number of uncorrected HEC errors. The counter is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | — | UncCnt[7] | Uncorrected HEC Error counter bit 7 (MSB). |
| 6 | — | UncCnt[6] | Uncorrected HEC Error counter bit 6. |
| 5 | — | UncCnt[5] | Uncorrected HEC Error counter bit 5. |
| 4 | — | UncCnt[4] | Uncorrected HEC Error counter bit 4. |
| 3 | — | UncCnt[3] | Uncorrected HEC Error counter bit 3. |
| 2 | — | UncCnt[2] | Uncorrected HEC Error counter bit 2. |
| 1 | — | UncCnt[1] | Uncorrected HEC Error counter bit 1. |
| 0 | — | UncCnt[0] | Uncorrected HEC Error counter bit 0 (LSB). |

2.2.52 0x3C—NONCNTL (Non-matching Cell Counter [Low Byte])

The NONCNTL counter tracks the number of non-matching cells. This byte of the counter should be read first. The counter is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | — | NonCnt[7] | Non-matching cell counter bit 7. |
| 6 | — | NonCnt[6] | Non-matching cell counter bit 6. |
| 5 | — | NonCnt[5] | Non-matching cell counter bit 5. |
| 4 | — | NonCnt[4] | Non-matching cell counter bit 4. |
| 3 | — | NonCnt[3] | Non-matching cell counter bit 3. |
| 2 | — | NonCnt[2] | Non-matching cell counter bit 2. |
| 1 | — | NonCnt[1] | Non-matching cell counter bit 1. |
| 0 | — | NonCnt[0] | Non-matching cell counter bit 0 (LSB). |

2.2.53 0x3D—NONCNTH (Non-matching Cell Counter [High Byte])

The NONCNTH counter tracks the number of non-matching cells. The counter is cleared on read.

| Bit | Default | Name | Description |
|-----|---------|------------|---|
| 7 | — | NonCnt[15] | Non-matching cell counter bit 15 (MSB). |
| 6 | — | NonCnt[14] | Non-matching cell counter bit 14. |
| 5 | — | NonCnt[13] | Non-matching cell counter bit 13. |
| 4 | — | NonCnt[12] | Non-matching cell counter bit 12. |
| 3 | — | NonCnt[11] | Non-matching cell counter bit 11. |
| 2 | — | NonCnt[10] | Non-matching cell counter bit 10. |
| 1 | — | NonCnt[9] | Non-matching cell counter bit 9. |
| 0 | — | NonCnt[8] | Non-matching cell counter bit 8. |

2.3 General Control Registers

2.3.1 0xF00—GENCTRL (General Device Control Register)

| Bit | Default | Name | Description |
|-----|---------|-----------|--|
| 7 | 0 | DevMstRst | Device master reset. When set high, all internal state machines in the TC block are held in reset and all registers (except this bit) assume their default values. If configuring the device for pass-through operation, a minimum delay of 25 uS for IMA_Sysclk of 66 MHz or 33uS for IMA_Sysclk of 50 MHz is required from the release of device reset to the first access of the IMA_RX_TRANS_TABLE register or IMA_RX_ATM_TRANS_TABLE register (0x818/0x819). |
| 6 | 0 | DevLgcRst | Device logic reset. When set high, all internal state machines in the TC block are held in reset but register values are unaffected. |
| 5 | 0 | EnStatLat | When set to 1, the one-second status latching is enabled. The value of the status bits are the events which occurred between the last two one-second events. Any events occurring after the last one-second event is not reflected when the status register is read. Those events are reflected in the status register upon the next one-second event. When a status register is read, the status is cleared and is not updated until the next one-second event. When set to 0, the one-second status latching is disabled. The value of a status register is the events occurred since the last read of the status register. |
| 4 | 0 | EnCntrLat | When set to 1, the one-second counter latching is enabled. The value of the counter is the number of events counted between the last two one-second events. Any events occurring after the last one-second event is not reflected when the counter is read. Those events are reflected in the counter upon the next one-second event. When a counter is read, the count is cleared and is not updated until the next one-second event. When set to 0, the one-second counter latching is disabled. The value of a counter is the number of events counted since the last read of the counter. |
| 3 | 0 | EnIntPin | Enables the MicroInt* output pin. |
| 2–1 | 00 | — | Reserved, set to zero. |
| 0 | 0 | OneSecOut | When set to 1, the OneSecIO pin is configured as an output. The pin provides a one-second event pulse. The one-second event is generated internally of the device. The event occurs after the device has counted 8000 periods of a 8 KHz clock. When set to 0, the OneSecIO pin is configured as an input. The one-second event must be generated externally, by pulsing the OneSecIO pin for low-high-low. |

2.3.2 0xF01—PARTNUM (Part and Version Number Register)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7–4 | pppp | PartNum[3:0] | Part number controlled by bondout: 16 TC Port version - 0101 32 TC Port version - 1001 |
| 3–0 | 0000 | Version[3:0] | Version number of the device. Number starts at “0000” for the initial version |

2.3.3 0xF02—PHYINTFC (PHY-side Interface Control Register)

| Bit | Default | Name | Description |
|-----|---------|--------------|---|
| 7 | 0 | — | Reserved, set to 0. |
| 6 | — | PHYIntSelPin | This bit reflects the level of the external PhyIntFcSel pin (read only) |
| 5 | 1 | PHYBusWidth | When set to 0, the PHY-side UTOPIA interface is set to 16-bit mode. When set to 1, the PHY-side UTOPIA interface is set to 8-bit mode. |
| 4-0 | 00000 | — | Reserved, set to zero. |

2.3.4 0xF03—ATMINTFC (ATM-side Interface Control Register)

| Bit | Default | Name | Description |
|-----|---------|-------------|--|
| 7-6 | 00 | ATMmux[1:0] | Controls the ATM-side UTOPIA interface mux. 00 – External interface is placed in Tristate mode. 01 – UTOPIA level 2 interface to IMA32 block is enabled. 10 – UTOPIA level 2 interface to TC block is enabled. 11 – External interface is placed in Tristate mode. |
| 5 | 0 | ATMBusWidth | When set to 0, the 16-bit UTOPIA bus is enabled When set to 1, the 8-bit UTOPIA bus is enabled. |
| 4 | 0 | DualClavEnb | When set to 1, Dual Clav/Enb mode on the interface is enabled. When set to 0, single clav/enb is enabled. For single Clav mode, UrxEnb[1] and UtxEnb[1] are not used but must be pulled up. |
| 3-0 | 0000 | — | Reserved, set to zero. |

2.3.5 0xF04—STATOUT (Output Status Control Register)

| Bit | Default | Name | Description |
|-----|---------|--------------|---|
| 7-2 | 000000 | — | Reserved, set to zero. |
| 1-0 | 00 | StatOut[1:0] | The value written into these bits will be asserted on the StatOut[1:0] output pins. |

2.3.6 0xF05—SUMPORT0 (Summary Port Interrupt Status Register for TC ports 0-7)

| Bit | Default | Name | Description |
|-----|---------|-------------------------|--|
| 7 | 0 | PortInt[7] ¹ | This bit is a summary indicator of the interrupts from the Port 7 SUMINT register (0x1C0). |
| 6 | 0 | PortInt[6] ¹ | This bit is a summary indicator of the interrupts from the Port 6 SUMINT register (0x180). |
| 5 | 0 | PortInt[5] ¹ | This bit is a summary indicator of the interrupts from the Port 5 SUMINT register (0x140). |
| 4 | 0 | PortInt[4] ¹ | This bit is a summary indicator of the interrupts from the Port 4 SUMINT register (0x100). |
| 3 | 0 | PortInt[3] ¹ | This bit is a summary indicator of the interrupts from the Port 3 SUMINT register (0x0C0). |
| 2 | 0 | PortInt[2] ¹ | This bit is a summary indicator of the interrupts from the Port 2 SUMINT register (0x080). |
| 1 | 0 | PortInt[1] ¹ | This bit is a summary indicator of the interrupts from the Port 1 SUMINT register (0x040). |
| 0 | 0 | PortInt[0] ¹ | This bit is a summary indicator of the interrupts from the Port 0 SUMINT register (0x000). |

Footnote:

(1) This bit is a pointer to the next interrupt indication register to be read. This bit will be cleared when the interrupt bit in the corresponding interrupt indication register is read and automatically cleared.

2.3.7 0xF06—ENSUMPORT0 (Summary Port Interrupt Control Register for TC Ports 0-7)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7 | 1 | EnPortInt[7] | When set, this bit enables PortInt[7] to appear on the MicroInt* output. |
| 6 | 1 | EnPortInt[6] | When set, this bit enables PortInt[6] to appear on the MicroInt* output. |
| 5 | 1 | EnPortInt[5] | When set, this bit enables PortInt[5] to appear on the MicroInt* output. |
| 4 | 1 | EnPortInt[4] | When set, this bit enables PortInt[4] to appear on the MicroInt* output. |
| 3 | 1 | EnPortInt[3] | When set, this bit enables PortInt[3] to appear on the MicroInt* output. |
| 2 | 1 | EnPortInt[2] | When set, this bit enables PortInt[2] to appear on the MicroInt* output. |
| 1 | 1 | EnPortInt[1] | When set, this bit enables PortInt[1] to appear on the MicroInt* output. |
| 0 | 1 | EnPortInt[0] | When set, this bit enables PortInt[0] to appear on the MicroInt* output. |

2.3.8 0xF07—SUMPORT1 (Summary Port Interrupt Status Register for TC ports 8-15)

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7 | 0 | PortInt[15] ¹ | This bit is a summary indicator of the interrupts from the Port 15 SUMINT register (0x3C0). |
| 6 | 0 | PortInt[14] ¹ | This bit is a summary indicator of the interrupts from the Port 14 SUMINT register (0x380). |
| 5 | 0 | PortInt[13] ¹ | This bit is a summary indicator of the interrupts from the Port 13 SUMINT register (0x340). |
| 4 | 0 | PortInt[12] ¹ | This bit is a summary indicator of the interrupts from the Port 12 SUMINT register (0x300). |
| 3 | 0 | PortInt[11] ¹ | This bit is a summary indicator of the interrupts from the Port 11 SUMINT register (0x2C0). |
| 2 | 0 | PortInt[10] ¹ | This bit is a summary indicator of the interrupts from the Port 10 SUMINT register (0x280). |
| 1 | 0 | PortInt[9] ¹ | This bit is a summary indicator of the interrupts from the Port 9 SUMINT register (0x240). |
| 0 | 0 | PortInt[8] ¹ | This bit is a summary indicator of the interrupts from the Port 8 SUMINT register (0x200). |

Footnote:

(1) This bit is a pointer to the next interrupt indication register to be read. This bit will be cleared when the interrupt bit in the corresponding interrupt indication register is read and automatically cleared.

2.3.9 0xF08—ENSUMPORT1 (Summary Port Interrupt Control Register for TC Ports 8-15)

| Bit | Default | Name | Description |
|-----|---------|---------------|---|
| 7 | 1 | EnPortInt[15] | When set, this bit enables PortInt[15] to appear on the MicroInt* output. |
| 6 | 1 | EnPortInt[14] | When set, this bit enables PortInt[14] to appear on the MicroInt* output. |
| 5 | 1 | EnPortInt[13] | When set, this bit enables PortInt[13] to appear on the MicroInt* output. |
| 4 | 1 | EnPortInt[12] | When set, this bit enables PortInt[12] to appear on the MicroInt* output. |
| 3 | 1 | EnPortInt[11] | When set, this bit enables PortInt[11] to appear on the MicroInt* output. |
| 2 | 1 | EnPortInt[10] | When set, this bit enables PortInt[10] to appear on the MicroInt* output. |
| 1 | 1 | EnPortInt[9] | When set, this bit enables PortInt[9] to appear on the MicroInt* output. |
| 0 | 1 | EnPortInt[8] | When set, this bit enables PortInt[8] to appear on the MicroInt* output. |

2.3.10 0xF09—SUMPORT2 (Summary Port Interrupt Status Register for TC ports 16-23)

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7 | 0 | PortInt[23] ¹ | This bit is a summary indicator of the interrupts from the Port 23 SUMINT register (0x5C0). |
| 6 | 0 | PortInt[22] ¹ | This bit is a summary indicator of the interrupts from the Port 22 SUMINT register (0x580). |
| 5 | 0 | PortInt[21] ¹ | This bit is a summary indicator of the interrupts from the Port 21 SUMINT register (0x540). |
| 4 | 0 | PortInt[20] ¹ | This bit is a summary indicator of the interrupts from the Port 20 SUMINT register (0x500). |
| 3 | 0 | PortInt[19] ¹ | This bit is a summary indicator of the interrupts from the Port 19 SUMINT register (0x4C0). |
| 2 | 0 | PortInt[18] ¹ | This bit is a summary indicator of the interrupts from the Port 18 SUMINT register (0x480). |
| 1 | 0 | PortInt[17] ¹ | This bit is a summary indicator of the interrupts from the Port 17 SUMINT register (0x440). |
| 0 | 0 | PortInt[16] ¹ | This bit is a summary indicator of the interrupts from the Port 16 SUMINT register (0x400). |

Footnote:

(1) This bit is a pointer to the next interrupt indication register to be read. This bit will be cleared when the interrupt bit in the corresponding interrupt indication register is read and automatically cleared.

2.3.11 0xF0A—ENSUMPORT2 (Summary Port Interrupt Control Register for TC Ports 16-23)

| Bit | Default | Name | Description |
|-----|---------|---------------|---|
| 7 | 1 | EnPortInt[23] | When set, this bit enables PortInt[23] to appear on the MicroInt* output. |
| 6 | 1 | EnPortInt[22] | When set, this bit enables PortInt[22] to appear on the MicroInt* output. |
| 5 | 1 | EnPortInt[21] | When set, this bit enables PortInt[21] to appear on the MicroInt* output. |
| 4 | 1 | EnPortInt[20] | When set, this bit enables PortInt[20] to appear on the MicroInt* output. |
| 3 | 1 | EnPortInt[19] | When set, this bit enables PortInt[19] to appear on the MicroInt* output. |
| 2 | 1 | EnPortInt[18] | When set, this bit enables PortInt[18] to appear on the MicroInt* output. |
| 1 | 1 | EnPortInt[17] | When set, this bit enables PortInt[17] to appear on the MicroInt* output. |
| 0 | 1 | EnPortInt[16] | When set, this bit enables PortInt[16] to appear on the MicroInt* output. |

2.3.12 0xF0B—SUMPORT3 (Summary Port Interrupt Status Register for TC ports 24-31)

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7 | 0 | PortInt[31] ¹ | This bit is a summary indicator of the interrupts from the Port 31 SUMINT register (0x7C0). |
| 6 | 0 | PortInt[30] ¹ | This bit is a summary indicator of the interrupts from the Port 30 SUMINT register (0x780). |
| 5 | 0 | PortInt[29] ¹ | This bit is a summary indicator of the interrupts from the Port 29 SUMINT register (0x740). |
| 4 | 0 | PortInt[28] ¹ | This bit is a summary indicator of the interrupts from the Port 28 SUMINT register (0x700). |
| 3 | 0 | PortInt[27] ¹ | This bit is a summary indicator of the interrupts from the Port 27 SUMINT register (0x6C0). |
| 2 | 0 | PortInt[26] ¹ | This bit is a summary indicator of the interrupts from the Port 26 SUMINT register (0x680). |
| 1 | 0 | PortInt[25] ¹ | This bit is a summary indicator of the interrupts from the Port 25 SUMINT register (0x640). |
| 0 | 0 | PortInt[24] ¹ | This bit is a summary indicator of the interrupts from the Port 24 SUMINT register (0x600). |

Footnote:

(1) This bit is a pointer to the next interrupt indication register to be read. This bit will be cleared when the interrupt bit in the corresponding interrupt indication register is read and automatically cleared.

2.3.13 0xF0C—ENSUMPORT3 (Summary Port Interrupt Control Register for TC Ports 24-31)

| Bit | Default | Name | Description |
|-----|---------|---------------|---|
| 7 | 1 | EnPortInt[31] | When set, this bit enables PortInt[31] to appear on the MicroInt* output. |
| 6 | 1 | EnPortInt[30] | When set, this bit enables PortInt[30] to appear on the MicroInt* output. |
| 5 | 1 | EnPortInt[29] | When set, this bit enables PortInt[29] to appear on the MicroInt* output. |
| 4 | 1 | EnPortInt[28] | When set, this bit enables PortInt[28] to appear on the MicroInt* output. |
| 3 | 1 | EnPortInt[27] | When set, this bit enables PortInt[27] to appear on the MicroInt* output. |
| 2 | 1 | EnPortInt[26] | When set, this bit enables PortInt[26] to appear on the MicroInt* output. |
| 1 | 1 | EnPortInt[25] | When set, this bit enables PortInt[25] to appear on the MicroInt* output. |
| 0 | 1 | EnPortInt[24] | When set, this bit enables PortInt[24] to appear on the MicroInt* output. |

2.3.14 0xF0F—SCRATCH (Scratch Pad Register)

| Bit | Default | Name | Description |
|-----|----------|---------|--|
| 7-0 | 00000000 | Scratch | These bits can be written and read by the system. These bits are not used for any purpose inside the device. |

2.3.15 0xF10—TCCTRL0 (TC Control Register for TC ports 0-3)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7 | 0 | IhTxDatShft0 | When set to 1, the Tx data on the Interleaved Highway Data Bus 0 will be output 1/2 IHTxClk0 cycle later than when the Tx inputs are sampled. Set to 0 to disable 1/2 cycle shift. |
| 6 | 0 | IhTxClkPol0 | Interleaved Highway Bus 0 Tx Clock Polarity. Set to 0 for rising edge of IHTxClk0, set to 1 for falling edge. |
| 5 | 0 | IhRxClkPol0 | Interleaved Highway Bus 0 Rx Clock Polarity. Set to 0 for rising edge of IHRxClk0, set to 1 for falling edge. |
| 4 | 0 | EnIH0 | When set, this bit enables interleaved highway interface for TC Ports 0-3. |
| 3 | 0 | EnFrac[3] | When set, this bit enables fractional T1/E1 logic for TC port 3. |
| 2 | 0 | EnFrac[2] | When set, this bit enables fractional T1/E1 logic for TC port 2. |
| 1 | 0 | EnFrac[1] | When set, this bit enables fractional T1/E1 logic for TC port 1. |
| 0 | 0 | EnFrac[0] | When set, this bit enables fractional T1/E1 logic for TC port 0. |

2.3.16 0xF11—TCCTRL1 (TC Control Register for TC ports 4-7)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7 | 0 | IhTxDatShft1 | When set to 1, the Tx data on the Interleaved Highway Data Bus 1 will be output 1/2 IHTxClk1 cycle later than when the Tx inputs are sampled. Set to 0 to disable 1/2 cycle shift. |
| 6 | 0 | IhTxClkPol1 | Interleaved Highway Bus 1 Tx Clock Polarity. Set to 0 for rising edge of IHTxClk1, set to 1 for falling edge. |
| 5 | 0 | IhRxClkPol1 | Interleaved Highway Bus 1 Rx Clock Polarity. Set to 0 for rising edge of IHRxClk1, set to 1 for falling edge. |
| 4 | 0 | EnIH1 | When set, this bit enables interleaved highway interface for TC Ports 4-7. |
| 3 | 0 | EnFrac[7] | When set, this bit enables fractional T1/E1 logic for TC port 7. |
| 2 | 0 | EnFrac[6] | When set, this bit enables fractional T1/E1 logic for TC port 6. |
| 1 | 0 | EnFrac[5] | When set, this bit enables fractional T1/E1 logic for TC port 5. |
| 0 | 0 | EnFrac[4] | When set, this bit enables fractional T1/E1 logic for TC port 4. |

2.3.17 0xF12—TCCTRL2 (TC Control Register for TC ports 8-11)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7 | 0 | IhTxDatShft2 | When set to 1, the Tx data on the Interleaved Highway Data Bus 2 will be output 1/2 IHTxClk2 cycle later than when the Tx inputs are sampled. Set to 0 to disable 1/2 cycle shift. |
| 6 | 0 | IhTxClkPol2 | Interleaved Highway Bus 2 Tx Clock Polarity. Set to 0 for rising edge of IHTxClk2, set to 1 for falling edge. |
| 5 | 0 | IhRxClkPol2 | Interleaved Highway Bus 2 Rx Clock Polarity. Set to 0 for rising edge of IHRxClk2, set to 1 for falling edge. |
| 4 | 0 | EnIH2 | When set, this bit enables interleaved highway interface for TC Ports 8-11. |
| 3 | 0 | EnFrac[11] | When set, this bit enables fractional T1/E1 logic for TC port 11. |
| 2 | 0 | EnFrac[10] | When set, this bit enables fractional T1/E1 logic for TC port 10. |
| 1 | 0 | EnFrac[9] | When set, this bit enables fractional T1/E1 logic for TC port 9. |
| 0 | 0 | EnFrac[8] | When set, this bit enables fractional T1/E1 logic for TC port 8. |

2.3.18 0xF13—TCCTRL3 (TC Control Register for TC ports 12-15)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7 | 0 | IhTxDatShft3 | When set to 1, the Tx data on the Interleaved Highway Data Bus 3 will be output 1/2 IHTxClk3 cycle later than when the Tx inputs are sampled. Set to 0 to disable 1/2 cycle shift. |
| 6 | 0 | IhTxClkPol3 | Interleaved Highway Bus 3 Tx Clock Polarity. Set to 0 for rising edge of IHTxClk3, set to 1 for falling edge. |
| 5 | 0 | IhRxClkPol3 | Interleaved Highway Bus 3 Rx Clock Polarity. Set to 0 for rising edge of IHTxClk3, set to 1 for falling edge. |
| 4 | 0 | EnIH3 | When set, this bit enables interleaved highway interface for TC Ports 12-15. |
| 3 | 0 | EnFrac[15] | When set, this bit enables fractional T1/E1 logic for TC port 15. |
| 2 | 0 | EnFrac[14] | When set, this bit enables fractional T1/E1 logic for TC port 14. |
| 1 | 0 | EnFrac[13] | When set, this bit enables fractional T1/E1 logic for TC port 13. |
| 0 | 0 | EnFrac[12] | When set, this bit enables fractional T1/E1 logic for TC port 12. |

2.3.19 0xF14—TCCTRL4 (TC Control Register for TC ports 16-19)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7 | 0 | IhTxDatShft4 | When set to 1, the Tx data on the Interleaved Highway Data Bus 4 will be output 1/2 IHTxClk4 cycle later than when the Tx inputs are sampled. Set to 0 to disable 1/2 cycle shift. |
| 6 | 0 | IhTxClkPol4 | Interleaved Highway Bus 4 Tx Clock Polarity. Set to 0 for rising edge of IHTxClk4, set to 1 for falling edge. |
| 5 | 0 | IhRxClkPol4 | Interleaved Highway Bus 4 Rx Clock Polarity. Set to 0 for rising edge of IHRxClk4, set to 1 for falling edge. |
| 4 | 0 | EnIH4 | When set, this bit enables interleaved highway interface for TC Ports 16-19. |
| 3 | 0 | EnFrac[19] | When set, this bit enables fractional T1/E1 logic for TC port 19. |
| 2 | 0 | EnFrac[18] | When set, this bit enables fractional T1/E1 logic for TC port 18. |
| 1 | 0 | EnFrac[17] | When set, this bit enables fractional T1/E1 logic for TC port 17. |
| 0 | 0 | EnFrac[16] | When set, this bit enables fractional T1/E1 logic for TC port 16. |

2.3.20 0xF15—TCCTRL5 (TC Control Register for TC ports 20-23)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7 | 0 | IhTxDatShft5 | When set to 1, the Tx data on the Interleaved Highway Data Bus 5 will be output 1/2 IHTxClk5 cycle later than when the Tx inputs are sampled. Set to 0 to disable 1/2 cycle shift. |
| 6 | 0 | IhTxClkPol5 | Interleaved Highway Bus 5 Tx Clock Polarity. Set to 0 for rising edge of IHTxClk5, set to 1 for falling edge. |
| 5 | 0 | IhRxClkPol5 | Interleaved Highway Bus 5 Rx Clock Polarity. Set to 0 for rising edge of IHRxClk5, set to 1 for falling edge. |
| 4 | 0 | EnIH5 | When set, this bit enables interleaved highway interface for TC Ports 20-23. |
| 3 | 0 | EnFrac[23] | When set, this bit enables fractional T1/E1 logic for TC port 23. |
| 2 | 0 | EnFrac[22] | When set, this bit enables fractional T1/E1 logic for TC port 22. |
| 1 | 0 | EnFrac[21] | When set, this bit enables fractional T1/E1 logic for TC port 21. |
| 0 | 0 | EnFrac[20] | When set, this bit enables fractional T1/E1 logic for TC port 20. |

2.3.21 0xF16—TCCTRL6 (TC Control Register for TC ports 24-27)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7 | 0 | IhTxDatShft6 | When set to 1, the Tx data on the Interleaved Highway Data Bus 6 will be output 1/2 IHTxClk6 cycle later than when the Tx inputs are sampled. Set to 0 to disable 1/2 cycle shift. |
| 6 | 0 | IhTxClkPol6 | Interleaved Highway Bus 6 Tx Clock Polarity. Set to 0 for rising edge of IHTxClk6, set to 1 for falling edge. |
| 5 | 0 | IhRxClkPol6 | Interleaved Highway Bus 6 Rx Clock Polarity. Set to 0 for rising edge of IHRxClk6, set to 1 for falling edge. |
| 4 | 0 | EnIH6 | When set, this bit enables interleaved highway interface for TC Ports 24-27. |
| 3 | 0 | EnFrac[27] | When set, this bit enables fractional T1/E1 logic for TC port 27. |
| 2 | 0 | EnFrac[26] | When set, this bit enables fractional T1/E1 logic for TC port 26. |
| 1 | 0 | EnFrac[25] | When set, this bit enables fractional T1/E1 logic for TC port 25. |
| 0 | 0 | EnFrac[24] | When set, this bit enables fractional T1/E1 logic for TC port 24. |

2.3.22 0xF17—TCCTRL7 (TC Control Register for TC ports 28-31)

| Bit | Default | Name | Description |
|-----|---------|--------------|--|
| 7 | 0 | IhTxDatShft7 | When set to 1, the Tx data on the Interleaved Highway Data Bus 7 will be output 1/2 IHTxClk7 cycle later than when the Tx inputs are sampled. Set to 0 to disable 1/2 cycle shift. |
| 6 | 0 | IhTxClkPol7 | Interleaved Highway Bus 7 Tx Clock Polarity. Set to 0 for rising edge of IHTxClk7, set to 1 for falling edge. |
| 5 | 0 | IhRxClkPol7 | Interleaved Highway Bus 7 Rx Clock Polarity. Set to 0 for rising edge of IHRxClk7, set to 1 for falling edge. |
| 4 | 0 | EnIH7 | When set, this bit enables interleaved highway interface for TC Ports 28-31. |
| 3 | 0 | EnFrac[31] | When set, this bit enables fractional T1/E1 logic for TC port 31. |
| 2 | 0 | EnFrac[30] | When set, this bit enables fractional T1/E1 logic for TC port 30. |
| 1 | 0 | EnFrac[29] | When set, this bit enables fractional T1/E1 logic for TC port 29. |
| 0 | 0 | EnFrac[28] | When set, this bit enables fractional T1/E1 logic for TC port 28. |

2.3.23 0xF18—ONESECINT (One Second Interrupt Status Register)

| Bit | Default | Name | Description |
|-----|---------|-----------|---|
| 7-1 | 0000000 | - | Reserved, set to zero |
| 0 | 0 | OneSecInt | This bit is the indicator of the one second interrupt |

2.3.24 0xF19—ONESECINT (One Second Interrupt Control Register)

| Bit | Default | Name | Description |
|-----|---------|-------------|---|
| 7-1 | 0000000 | - | Reserved, set to zero |
| 0 | 1 | EnOneSecInt | When set, this bit enables OneSecInt to appear on the Microint* output pin. |

2.4 IMA Subsystem Registers

The IMA Subsystem layer contains configuration and status information that is common to all IMA groups.

2.4.1 0x800—IMA_VER_1_CONFIG (IMA Type and Version Code I)

The IMA_Version I and II registers contain the type and revision level of the IMA core. **Read-only.**

| Bit | Default | Name | Description |
|-----|---------|------------------|--|
| 7-4 | | IMA Core Type I | 0xa = M28529, 32 ports 32 IMA groups 0xb = M28525, 16 ports 16 IMA groups |
| 3 | 1 | IMA Core Type II | 1 = Internal memory present |
| 2-0 | | Version Code I | 0x4 = M2852x family major revision level |

2.4.2 0x801—IMA_VER_2_CONFIG (IMA Version Codes II and III)

This register is **read-only.**

| Bit | Default | Name | Description |
|-----|---------|------------------|--------------------------------|
| 7-4 | | Version Code II | 4 bit code: 0x4 = M2852x-12 |
| 3-0 | | Version Code III | 4 bit code: 0x0 = M2852x-12 |

2.4.3 0x802—IMA_SUBSYS_CONFIG (IMA Configuration Control)

This register contains some of the basic IMA Subsystem configuration.

| Bit | Default | Name | Description |
|-----|---------|-----------------|--|
| 7–6 | 0 | Link Type | Sets default link type for all IMA groups. Not used with variable rate facilities 0 = T1 1 = E1 2 = Alternate T1 (1.544 Mbps payload) 3 = Alternate E1 (1.984 Mbps payload) |
| 5–4 | 0 | SRAM size | 0 = 25 ms (E1 mode) 1 = 50 ms 2 = 100 ms 3 = 200 ms |
| 3 | 0 | Number of SRAMs | 0 = 1 SRAM, Set to 0 for all M2852x devices |
| 2–0 | 0 | Number of Ports | This field indicates the range of valid PHY addresses. 0: addresses 0x00–0x03 are valid 1: addresses 0x00–0x07 are valid 2: addresses 0x00–0x0B are valid 3: addresses 0x00–0x0F are valid 4: addresses 0x00–0x13 are valid 5: addresses 0x00–0x17 are valid 6: addresses 0x00–0x1B are valid 7: addresses 0x00–0x1F are valid This field has different ranges depending on Product type: M28525: Range: 0–3 M28529: Range: 0–7 |

2.4.4 0x803—IMA_MISC_STATUS (IMA Miscellaneous Status)

This register contains miscellaneous status information for the IMA Subsystem. **Read-only.**

| Bit | Default | Name | Description |
|-----|---------|---------------------|---|
| 7 | — | — | Reserved |
| 6 | — | — | Reserved |
| 5 | — | — | Reserved |
| 4 | — | ATM Data Width | This bit indicates whether the ATM UTOPIA bus is operating in 16 bit (high) or 8 bit (low) data mode. |
| 3 | — | IMA_RefClk Error | This bit is set high if a transition detector for IMA_RefClk detects a bad signal. This bit is active high and is reset upon reading this address. |
| 2 | — | Tx ATM Parity Error | This bit indicates that a parity error has been detected on the Transmit ATM side UTOPIA bus. This bit is active high and is reset upon reading this address. |
| 1 | — | — | Reserved. |
| 0 | — | Rx PHY Parity Error | This bit indicates that a parity error has been detected on the Receive PHY side cell bus. This bit is active high and is reset upon reading this address. |

2.4.5 0x804—IMA_MISC_CONFIG (IMA Miscellaneous Control)

This register contains some of the basic IMA Subsystem configuration.

| Bit | Default | Name | Description |
|-----|---------|---------------------------------------|--|
| 7 | — | — | Reserved. Set to 0 |
| 6 | 0 | Alternate GTSM Mode | 1 = When the GTSM is down, ATMUTxClAv for that group is controlled as if all configured links in the group are Active. 0 = When the GTSM is down, ATMUTxClAv for that group is inactive. |
| 5–4 | 0 | PHY Size | This two bit field determines the use of the PHY side ClAv and En* signals. When using Utopia-to-Serial mode, PHY Size should be set to 16 ports per ClAv and En*. Thus for M28525, PHY Size should be 2 while for M28529, PHY Size should be 1. 0 = ClAv and En* for every 4 PHY addresses (support 8 ports total) (Ports 0-3 assigned to Clav0/Enb0*) (Ports 4-7 assigned to Clav1/En1*) 1 = ClAv and En* for every 16 PHY addresses (support 32 ports total) (Ports 0-15 assigned to Clav0/Enb0*) (Ports 16-31 assigned to Clav1/Enb1*) 2 = ClAv and En* for all PHY addresses (support 32 ports total) (Ports 0-31 assigned to Clav0/Enb0*) For Utopia-to-Utopia mode, PhyUrxEna[1] and PhyUtxEna[1] should be pull high when PHY Size is set to 2. 3 = ClAv and En* for every 8 PHY addresses (support 16 ports total) (Ports 0-7 assigned to Clav0/Enb0*) (Ports 8-15 assigned to Clav1/Enb1*) |
| 3 | 0 | Enable External HEC Checker | 1 = Bit 7 of the HEC Byte is a HEC error flag 0 = Use the HEC Error checker within the IMA block |
| 2 | 0 | Check ATMUTxAddr[4] and ATMURxAddr[4] | 0 = mask bits (don't care) 1 = Check ATMUTxAddr[4] and TMURxAddr[4] for correct value |
| 1 | 0 | Check ATMUTxAddr[3] and ATMURxAddr[3] | 0 = mask bits (don't care) 1 = Check ATMUTxAddr[3] and ATMURxAddr[3] for correct value |
| 0 | 0 | Check ATMUTxAddr[2] and ATMURxAddr[2] | 0 = mask bits (don't care) 1 = Check ATMUTxAddr[2] and ATMURxAddr[2] for correct value |

2.4.6 0x805—IMA_MEM_LOW_TEST (IMA Memory Test Address (Bits 0–7))

Registers 0x805—0x808 are used to perform memory diagnostic tests on the internal or external differential delay SRAM.

| Bit | Default | Name | Description |
|-----|---------|---------------------|---|
| 7–0 | 0x00 | Memory Test Address | This field contains the least significant bits of the memory test address for the selected memory component. Range: 0x00–0xFF |

2.4.7 0x806—IMA_MEM_HI_TEST (IMA Memory Test Address (Bits 8–15))

| Bit | Default | Name | Description |
|-----|---------|---------------------|--|
| 7–0 | 0x00 | Memory Test Address | This field contains the middle significant bits of the memory test address for the selected memory component. Range: 0x00–0xFF |

2.4.8 0x807—IMA_MEM_TEST_CTL (IMA Memory Test Control / Address MSBs)

| Bit | Default | Name | Description |
|-----|---------|--------------------------------|--|
| 7 | 0 | Memory Test Address Bit 20 | This field contains the most significant bit of the memory test address for the selected memory component. |
| 6–4 | 0 | RAM Test Access | 0 = no test selected, normal operation 1 = SRAM Test 2–7 = Reserved |
| 3–0 | 0 | Memory Test Address Bits 19–16 | This field contains the most significant bits of the memory test address for the selected memory component. Range: 0x00–0x0F |

2.4.9 0x808—IMA_MEM_TEST_DATA (IMA Memory Test Data)

| Bit | Default | Name | Description |
|-----|---------|------------------|---|
| 7–0 | 0x00 | Memory Test Data | This field contains the data to be written or read from the memory test address for the selected memory component. Range: 0x00–0xFF |

2.4.10 0x809—IMA_LNK_DIAG_CTL (IMA Link Diagnostic Control Register)

This register is used to specify a port number for observation of link differential delay and anomalies. The contents of this register are used to report the link information via registers 0x809–0x80B. Bit 5 of this register is **read-only**.

| Bit | Default | Name | Description |
|-----|---------|-----------------------------|--|
| 7 | — | — | Reserved. Set to 0 |
| 6 | — | — | Reserved. Set to 0 |
| 5 | — | Link Delay Write Counter | This field contains the most significant bit of the SRAM write counter for the diagnostic link (selected using the field below). |
| 4–0 | 0x00 | Link Diagnostic PHY Address | This field contains the PHY Cell Bus Address of the port for which a diagnostic measurement is to be performed. Range: 0x00–0x1F |

2.4.11 0x80A—IMA_LNK_DIFF_DEL (IMA Link Differential Delay Write Counter)

This register, along with bit 5 of address 0x809, reports the value of the SRAM write phase at the time when the read phase is 0. This phase information is used to calculate the link differential delay.

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7-0 | — | Link Delay Write Counter | This field contains a snapshot of 8 of the least significant bits of the SRAM write counter for the diagnostic link (selected using address 0x809). All others (Range: 0x00-0xFF) Delay Window = 0 (see register 0x815): Value = Cell_count >> 1 Delay Window = 1-3 (see register 0x815): Value = Cell_count Delay Window = 4 (see register 0x815): Value = Cell_count >> 2 |

2.4.12 0x80B—IMA_RCV_LNK_ANOMALIES (IMA Receive Link Anomalies)

These anomalies are for the diagnostic link selected using address 0x809. The bits in this register are **read-only** and are cleared upon read.

| Bit | Default | Name | Description |
|-----|---------|--|---|
| 7 | — | ICP-ERR Anomaly | 1 = ICP-ERR anomaly was active sometime since the last time this register was read 0 = ICP-ERR defect was inactive |
| 6 | — | ICP-INV Anomaly— Unexpected IMA Label | 1 = Unexpected IMA Label condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected IMA Label condition was inactive |
| 5 | — | ICP-INV Anomaly— Unexpected LID | 1 = Unexpected LID condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected LID condition was inactive |
| 4 | — | ICP-INV Anomaly— Unexpected IMA ID | 1 = Unexpected IMA ID condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected IMA ID condition was inactive |
| 3 | — | ICP-INV Anomaly— Unexpected M | 1 = Unexpected M condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected M condition was inactive |
| 2 | — | ICP-INV Anomaly— Unexpected IMA Frame Number | 1 = Unexpected IMA Frame Number condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected IMA Frame Number condition was inactive |
| 1 | — | ICP-INV Anomaly— Unexpected IMA Cell Offset | 1 = Unexpected IMA Cell Offset condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected IMA Cell Offset condition was inactive |
| 0 | — | ICP-MIS Anomaly | 1 = ICP-MIS anomaly was active sometime since the last time this register was read 0 = ICP-MIS defect was inactive |

2.4.13 0x80C—IMA_PHY_LOOPBACK (IMA Phy Side UTOPIA Loopback)

This register controls the UTOPIA loopbacks on the PHY side of the IMA block.

| Bit | Default | Name | Description |
|-----|---------|------------------|---|
| 7-3 | — | — | Reserved. Set to 0 |
| 2 | — | Loopback Enable | 0 = PHY side loopback disabled. 1 = PHY side loopback enabled per bits 1:0 of this register. |
| 1-0 | — | Loopback Type(s) | 0 = IMA System Loopback 0 -- uses TxClav signal(s) from PHY (TC or external) 1 = IMA System Loopback 1 -- ignores TxClav signal(s) from PHY layer 2 = IMA Line Loopback -- ignores TxClav signal(s) from PHY layer 3 = Not Defined |

2.4.14 0x80E—IMA_DIAG_XOR_BIT (IMA Diagnostic Bit)

This register provides a single bit that can be used by a diagnostic test routine to verify the connectivity of the microprocessor address lines to the IMA device. This bit is **read-only**.

| Bit | Default | Name | Description |
|-----|---------|------------------------|--|
| 7 | — | — | Reserved. |
| 6 | — | — | Reserved. |
| 5 | — | — | Reserved. |
| 4 | — | — | Reserved. |
| 3 | — | — | Reserved. |
| 2 | — | — | Reserved. |
| 1 | — | — | Reserved. |
| 0 | — | Address Diagnostic Bit | Exclusive OR of address bits from previous IMA core Read access. The number of bits in the exclusive OR operation is 11. |

2.4.15 0x80F—IMA_DIAG (IMA Diagnostic Register)

This register provides an isolated 8 bit storage register that can be used by a diagnostic test routine to verify the connectivity of the microprocessor data lines to the IMA device.

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7-0 | 0x00 | Data Diagnostic Register | An 8 bit register that can be written and read by the processor. The register is not used within the IMA Block. |

2.4.16 0x810—IMA_TIM_REF_MUX_CTL_ADDR (IMA Timing Reference Multiplexer Control Address)

This register is used in conjunction with 0x811 to configure various timing elements within the IMA core. Register 0x810 and 0x811 are an indirect register pair in that a particular timing element is selected using register 0x810 and the configuration for that timing element is programmed using register 0x811.

| Bit | Default | Name | Description |
|-----|---------|------------------|--|
| 7–6 | 0 | Multiplexer Type | 0 = Set timing reference for a Rx IMA Group 1 = Set timing reference for a Tx IMA Group 2 = Set timing source for Tx_TRL Outputs 3 = Set the Clock Divisor for an IMA group |
| 5 | — | — | Reserved. Set to 0. |
| 4–0 | 0 | Multiplexer ID | For Multiplexer Type = 0, Multiplexer Type = 1, and Multiplexer Type = 3: M28525: 0–0xF: IMA Group 1–16 M28529: 0–0x1F: IMA Group 1–32 For Multiplexer Type = 2: 0–1: Tx_TRL[0]–Tx_TRL[1] output |

2.4.17 0x811—IMA_TIM_REF_MUX_CTL_DATA (IMA Timing Reference Multiplexer Control Data)

| Bit | Default | Name | Description |
|-------------------------------------|---------|---------------|--|
| 7 | — | — | Reserved. Set to 0. |
| 6 | — | — | Reserved. Set to 0. |
| For Multiplexer Type 0 and 1 | | | |
| 5–0 | 0x00 | Timing Source | 0x00–0x1F: Select timing from a Receive Port (see register 0x816) M28525: 0–0xF: Port 0–15 M28529: 0–0x1F: Port 0–31 0x20: Use IMA_SysClk/24 or DSL generator output as source (see register 0x816) 0x21: Use IMA_RefClk as source |
| For Multiplexer Type 2 | | | |
| 5–0 | 0x00 | Timing Source | 0x00–0x1F: Select timing from a Receive Port (see register 0x816) M28525: 0–0xF: Port 0–15 M28529: 0–0x1F: Port 0–31 0x20: IMA_SysClk/24 0x21: IMA_RefClk 0x22: 8 kHz |
| For Multiplexer Type 3 | | | |
| 5 | — | — | Reserved. Set to 0. |
| 4 | — | — | Reserved. Set to 0. |
| 3–0 | 0x0 | Clock Divisor | This field contains the clock divider multiplier for the group. The IMA group number is set by writing to the Multiplexer ID field in address 0x810. 0 = Based on Link Type field in address 0x002 1 = 1/1 2 = 192/193 3 = 15/16 |

2.4.18 0x812—IMA_RX_PERSIST_CONFIG (IMA Receive Persistence Configuration)

| Bit | Default | Name | Description |
|---|---------|----------------------------|---|
| 7 | 0 | — | Reserved. Set to 0. |
| 6 | 0 | Alpha Value ⁽¹⁾ | 0: $\alpha = 1$ 1: $\alpha = 2$ |
| 5–3 | 0 | Beta Value ⁽²⁾ | 0: $\beta = 1$ 1: $\beta = 2$ 2: $\beta = 3$ 3: $\beta = 4$ 4: $\beta = 5$ |
| 2–0 | 0 | Gamma Value ⁽³⁾ | 0: $\gamma = 1$ 1: $\gamma = 2$ 2: $\gamma = 3$ 3: $\gamma = 4$ 4: $\gamma = 5$ |
| Footnote: (1) The Alpha Value is the number of consecutive invalid ICP cells needed for the link to leave the IMA Sync state. (2) The Beta Value is the number of consecutive errored ICP cells needed for the link to leave the IMA Sync state. (3) The Gamma Value is the number of consecutive valid ICP cells needed for the link to enter the IMA Sync state. | | | |

2.4.19 0x813—IMA_ATM_UTOPIA_BUS_CTL (IMA ATM UTOPIA Bus Control)

This register configures the operation of the ATM side UTOPIA bus and the sample time of PhyUTxCIAv for an IMA group.

| Bit | Default | Name | Description |
|-----|---------|------------------------------------|--|
| 7 | — | — | Reserved. Set to 0. |
| 6 | 0 | ATM Address Mode | 0 = UTOPIA Level 2 (multiple addresses) 1 = UTOPIA Level 1 (single fixed address, no address latching) |
| 5 | 0 | — | Reserved. Set to 0. |
| 4 | 0 | ATMURxCIAv Mode | 0 = ATMURxCIAv is set active for selected channel during cell transfer 1 = ATMURxCIAv is set inactive for selected channel during cell transfer |
| 3 | 0 | ATMUTxCIAv Last 4 Bytes/Words Mode | 0 = ATMUTxCIAv is forced inactive/active (based on the state of bit 2) during last 4 bytes/words for selected channel during cell transfer 1 = ATMUTxCIAv reflects true cell available status during last 4 bytes/words for selected channel during cell transfer |
| 2 | 0 | ATMUTxCIAv Mode | 0 = ATMUTxCIAv is set inactive for selected channel during cell transfer 1 = ATMUTxCIAv is set active for selected channel during cell transfer |
| 1 | 0 | CIAv Three-state Disable | 0 = ATMURxCIAv and ATMUTxCIAv threestate when not selected 1 = ATMURxCIAv and ATMUTxCIAv do not threestate |
| 0 | 0 | PHYUTxCIAv Sample Time | 0 = For an IMA group, sample PhyUTxCIAv during an ICP cell to determine SICP rate 1 = For an IMA group, delay sampling PhyUTxCIAv until >5 payload byte periods after an ICP transfer |

2.4.20 0x814—IMA_DIFF_DELAY_ADDR (IMA Differential Delay Control Address)

This register is used in conjunction with 0x815 to configure the differential delay operation of the IMA core. Register 0x814 and 0x815 are an indirect register pair in that a particular IMA group is selected using register 0x814 and the configuration for that IMA group is programmed using register 0x815.

| Bit | Default | Name | Description |
|-----|---------|--------------|---|
| 7 | — | — | Reserved. Set to 0. |
| 6 | 0 | Control Type | 0 = Set Delay Threshold for an IMA group 1 = Set Delay Window for an IMA group |
| 5 | — | — | Reserved. Set to 0. |
| 4–0 | 0x0 | Group Number | M28525: 0–0xF: IMA Group 1–16 M28529: 0–0x1F: IMA Group 1–32 |

2.4.21 0x815—IMA_DIFF_DELAY_DATA (IMA Differential Delay Control Data)

| Bit | Default | Name | Description |
|-----------------------------|---------|------------------------------|---|
| For Control Type = 0 | | | |
| 7–0 | 0x00 | Differential Delay Threshold | This field contains the cell offset that corresponds to differential delay threshold setting for the group. Delay Window = 0, 5: Value = 255–(Cell_count >> 1) Delay Window = 1–3, 6–7: Value = 255–Cell_count Delay Window = 4: Value = 255–(Cell_count >> 2) |
| For Control Type = 1 | | | |
| 7 | — | — | Reserved. Set to 0. |
| 6 | — | — | Reserved. Set to 0. |
| 5 | — | — | Reserved. Set to 0. |
| 4 | — | — | Reserved. Set to 0. |
| 3 | — | — | Reserved. Set to 0. |
| 2–0 | | Delay Window | This field contains the number of IMA frames (assuming M=128) that are examined when setting the differential delay buffer. This field is set based on the facility payload rate. 0 = 8 frames (1024 cells), for payload rates ≥ 1024 kbps 1 = 4 frames (512 cells), for 1024 kbps > payload rates ≥ 512 kbps 2 = 2 frames (256 cells), for 512 kbps > payload rates ≥ 256 kbps 3 = 1 frame (128 cells), for payload rates < 256 kbps 4 = 16 frames (2048 cells), for payload rates ≥ 1024 kbps 5 = 8 frames (1024 cells), for 1024 kbps > payload rates ≥ 512 kbps 6 = 4 frames (512 cells), for 512 kbps > payload rates ≥ 256 kbps 7 = 2 frame (256 cells), for payload rates < 256 kbps |

2.4.22 0x816—IMA_DSL_CLOCK_GEN_ADDR (IMA DSL Clock Generator Control)

This register is used in conjunction with 0x817 to configure the operation of the DSL Clock Generator in the IMA core. Register 0x816 and 0x817 are an indirect register pair in that a particular clock generator element is selected using register 0x816 and the configuration for that element is programmed using register 0x817.

The overall operation of the clock generators are governed by the following equations:

- Prescaler Factor = Prescaler Numerator / (Prescaler Terminal Count + 1)
- Intermediate Frequency = Reference Clock Frequency * Prescaler Factor
- Reference Denominator = 257 + Reference Clock Divisor
- 8 kHz = Intermediate Frequency / (Reference Denominator)

Link Payload Rate = 8 kbps * (Multiplier Factor) * (Rate Multiplier)

A further constraint is:

- (Maximum Link Payload Rate) / (Rate Multiplier) ≤ Intermediate Frequency ≤ IMA_SysClk/16

In a typical G.shdsl application, Intermediate Frequency is set to 2.56 MHz, Rate Multiplier = 1, and the Reference Denominator is set to 320. Other settings are possible as long as the above equations and constraints are met.

| Bit | Default | Name | Description |
|--------------------------------------|---------|--------------|--|
| 7-5 | 0 | Control Type | 0 = Basic Setup 1 = Pre-scaler and Reference Divisor Setup 2 = Tx IMA Group Factor LSBs 3 = Tx IMA Group Factor MSB 4 = Rx IMA Group Factor LSBs 5 = Rx IMA Group Factor MSB 6 = Rx Timing Synthesizer Factor LSBs 7 = Rx Timing Synthesizer Factor MSB |
| For Control Type = 0 | | | |
| 4-0 | — | — | Reserved. Set to 0. |
| For Control Type = 1 | | | |
| 4-2 | — | — | Reserved. Set to 0. |
| 1-0 | — | Sub Type | 0 = Pre-scaler Terminal Count 1 = Pre-scaler Numerator 2 = Reference Divisor 3 = Reserved |
| For Control Type = 2, 3, 4, 5 | | | |
| 4-0 | 0x0 | Group Number | M28525: 0-0xF: IMA Group 1-16 M28529: 0-0x1F: IMA Group 1-32 |
| For Control Type = 6, 7 | | | |
| 4-0 | 0x00 | Port Number | M28525: 0-0xF: Port 0-15 M28529: 0-0x1F: Port 0-31 |

2.4.23 0x817—IMA_DSL_CLOCK_GEN_DATA (IMA_DSL Clock Generator Data)

This register is used in conjunction with 0x816 to configure the operation of the DSL Clock Generator in the IMA core. Register 0x816 and 0x817 are an indirect register pair in that a particular clock generator element is selected using register 0x816 and the configuration for that element is programmed using register 0x817.

| Bit | Default | Name | Description |
|--|---------|--------------------------------------|---|
| For Control Type = 0 | | | |
| 7 | — | — | Reserved. Set to 0. |
| 6 | 0 | EnRxSyn | Enable Rx Timing Synthesizers 0 = Use SPRxCik inputs 1 = Use synthesizers instead of SPRxCik inputs |
| 5 | 0 | DSLClkGen | Substitute DSL clock generator 0 = Use IMA_SysCik/24 in IMA group clock and Tx_TRL selectors 1 = Use DSL Clock generator outputs when Timing Source is set to 0x20 in register 0x811. |
| 4 | 0 | IMA_CikSel | 0 = Use IMA_SysCik as input to DSL Clock Generators 1 = Use IMA_RefCik as input to DSL Clock Generators |
| 3-0 | — | — | Reserved. Set to 0. |
| For Control Type = 1/Sub-type = 0 | | | |
| 7-0 | 0x00 | Pre-scaler Terminal Count | This field contains the terminal count of the pre-scaler clock divider. The pre-scaler denominator is the value of this field plus 1. |
| For Control Type = 1/Sub-type = 1 | | | |
| 7-0 | 0x00 | Pre-scaler Numerator | This field contains the numerator for the pre-scaler. |
| For Control Type = 1/Sub-type = 2 | | | |
| 7-0 | 0x00 | Reference Clock Divisor | This field contains 8 of the 9 bits of the terminal count for the reference clock divisor. The reference clock divisor counts from 0 to the terminal count which is given by the value of this field plus 257. As an example if the value of this register is 63 decimal, then the reference clock divisor will be 320. |
| For Control Type = 2, 4 | | | |
| 7-0 | 0x00 | Group Clock Multiplier Factor (lsbs) | This register contains the 8 lsbs of the payload bandwidth for the ports used in the IMA group. The contents of this register are multiplied by 8kbps and the Rate Multiplier in order to obtain the bandwidth. |
| For Control Type = 3, 5 | | | |
| 7-6 | — | — | Reserved. Set to 0. |
| 5-4 | 0 | Rate Multiplier | Scale factor used to generate link rates > Intermediate Frequency 0 = Multiply rate by 1 (typically used by link rates < 3.072 Mbps) 1 = Multiply rate by 2 (typically used by 3.072 < link rates < 6.144 Mbps) 2 = Multiply rate by 4 (typically used by link rates > 6.144 Mbps) 3 = Not defined. |
| 3-1 | — | — | Reserved. Set to 0. |
| 0 | 0 | Group Clock Multiplier Factor (msb) | This register contains the msb of the payload bandwidth for the ports used in the IMA group. The contents of this register are multiplied by 2048kbps and the Rate Multiplier in order to obtain the bandwidth. |

| Bit | Default | Name | Description (Continued) |
|-----------------------------|---------|-------------------------------------|---|
| For Control Type = 6 | | | |
| 7-0 | 0x00 | Port Clock Multiplier Factor (lsbs) | This register contains the 8 lsbs of the payload bandwidth for the specific port of the Rx Timing clock synthesizer. The contents of this register are multiplied by 8kbps and the Rate Multiplier in order to obtain the bandwidth. |
| For Control Type = 7 | | | |
| 7-6 | — | — | Reserved. Set to 0. |
| 5-4 | 0 | Rate Multiplier | Scale factor used to generate link rates > Intermediate Frequency 0 = Multiply rate by 1 (typically used by link rates < 3.072 Mbps) 1 = Multiply rate by 2 (typically used by 3.072 < link rates < 6.144 Mbps) 2 = Multiply rate by 4 (typically used by link rates > 6.144 Mbps) 3 = Not defined. |
| 3-1 | — | — | Reserved. Set to 0. |
| 0 | 0 | Port Clock Multiplier Factor (msb) | This register contains the msb of the payload bandwidth for the specific port of the Rx Timing clock synthesizer. The contents of this register are multiplied by 2048kbps and the Rate Multiplier in order to obtain the bandwidth. |

2.4.24 0x818—IMA_RX_TRANS_TABLE (IMA Receive Translation Table Address)

This register is used in conjunction with 0x819 for configure the translation between the ATM side UTOPIA addresses and the internal channels (bypass ports and IMA groups) associated with the IMA core. Register 0x818 and 0x819 are an indirect register pair in that a address is selected using register 0x818 and the configuration for that address is programmed using register 0x819.

| Bit | Default | Name | Description |
|---------------------------------|---------|----------------------|---|
| 7 | 0 | Translation Type | 0 = the value in bits 5-0 enables ATM address → IMA internal channel translations 1 = the value in bits 5-0 enables IMA internal channel → ATM address translations |
| 6 | — | — | Don't care. Ignore. |
| For Translation Type = 0 | | | |
| 5 | — | — | Don't care. Ignore. |
| 4-0 | 0x00 | ATM UTOPIA Address | For Type 0, this field contains the ATM Side UTOPIA address. Range: 0x00-0x1F |
| For Translation Type = 1 | | | |
| 5-0 | 0x00 | Internal IMA Channel | For Type 1, this field contains the IMA internal channel address. Range 0x00-0x1F: Receive Port M28525: 0-0xF: Port 0-15 M28529: 0-0x1F: Port 0-31 Range 0x20-0x3F: IMA Group M28525: 0x20-0x2F: IMA Group 1-16 M28529: 0x20-0x3F: IMA Group 1-32 |

2.4.25 0x819—IMA_RX_ATM_TRANS_TABLE (IMA Receive ATM Translation Table Internal Channel)

This register is used in conjunction with 0x818 for configure the translation between the ATM side UTOPIA addresses and the internal channels (bypass ports and IMA groups) associated with the IMA core. Register 0x818 and 0x819 are an indirect register pair in that an address is selected using register 0x818 and the configuration for that address is programmed using register 0x819.

| Bit | Default | Name | Description |
|---------------------------------|---------|----------------------|---|
| For Translation Type = 0 | | | |
| 7 | — | — | Don't care. Ignore. |
| 6 | 1 | Internal IMA Channel | 1=ATM address is not assigned to this device 0=ATM address is assigned to this device |
| 5-0 | — | — | Don't care. Ignore. |
| For Translation Type = 1 | | | |
| 7 | 0 | Channel Active | 1 = Internal Channel Active 0 = Internal Channel Inactive |
| 6 | — | — | Don't care. Ignore. |
| 5 | — | — | Don't care. Ignore. |
| 4-0 | 0x00 | ATM UTOPIA Address | This field contains the mapping for the Internal IMA channel set in register 0x818. Range: 0x00–0x1F |

2.4.26 0x81B—IMA_TX_TRANS_TABLE (IMA Transmit Translation Table Address)

This register is used in conjunction with 0x81C for configure the translation between the ATM side UTOPIA addresses and the internal channels (bypass ports and IMA groups) associated with the IMA core. Register 0x81B and 0x81C are an indirect register pair in that a address is selected using register 0x81B and the configuration for that address is programmed using register 0x81C.

| Bit | Default | Name | Description |
|---------------------------------|---------|----------------------|--|
| 7 | 0 | Translation Type | 0 = the value in bits 5–0 enables ATM address → IMA internal channel translations 1 = the value in bits 5–0 enables IMA internal channel → ATM address translations |
| 6 | — | — | Don't care. Ignore. |
| For Translation Type = 0 | | | |
| 5 | — | — | Don't care. Ignore. |
| 4–0 | 0x00 | ATM UTOPIA Address | For Type 0, this field contains the ATM Side UTOPIA address. Range: 0x00–0x1F |
| For Translation Type = 1 | | | |
| 5–0 | 0x00 | Internal IMA Channel | For Type 1, this field contains the IMA internal channel address. Range 0x00–0x1F: Transmit Port M28525: 0–0xF: Port 0–15 M28529: 0–0x1F: Port 0–31 Range 0x20–0x3F: IMA Group M28525: 0x20–0x2F: IMA Group 1–16 M28529: 0x20–0x3F: IMA Group 1–32 |

2.4.27 0x81C—IMA_TX_ATM_TRANS_TABLE (Transmit ATM Translation Table Internal Channel)

This register is used in conjunction with 0x81B for configure the translation between the ATM side UTOPIA addresses and the internal channels (bypass ports and IMA groups) associated with the IMA core. Register 0x81B and 0x81C are an indirect register pair in that a address is selected using register 0x81B and the configuration for that address is programmed using register 0x81C.

| Bit | Default | Name | Description |
|---------------------------------|---------|----------------------|--|
| For Translation Type = 0 | | | |
| 7 | — | — | Don't care. Ignore. |
| 6 | 1 | Internal IMA Channel | 1=ATM address is not assigned to this device 0=ATM address is assigned to this device |
| 5-0 | — | — | Don't care. Ignore |

| Bit | Default | Name | Description |
|---------------------------------|---------|--------------------|---|
| For Translation Type = 1 | | | |
| 7 | 0 | Channel Active | 1 = Internal Channel Active 0 = Internal Channel Inactive |
| 6 | — | — | Don't care. Ignore. |
| 5 | — | — | Don't care. Ignore. |
| 4-0 | 0x00 | ATM UTOPIA Address | This field contains the mapping for the Internal IMA channel set in register 0x81B. Range: 0x00-0x1F |

2.5 IMA Group

The IMA Group layer contains configuration and status information that is associated with IMA groups.

2.5.1 0x81F—IMA_GRP_1T04_SEM (Group Table Control I)

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

| Bit | Default | Name | Description |
|-----|---------|------------------------------------|-----------------------|
| 7 | 0 | Update Enable for Receive group 4 | addresses 0x8DC-0x8DF |
| 6 | 0 | Update Enable for Receive group 3 | addresses 0x8D8-0x8DB |
| 5 | 0 | Update Enable for Receive group 2 | addresses 0x8D4-0x8D7 |
| 4 | 0 | Update Enable for Receive group 1 | addresses 0x8D0-0x8D3 |
| 3 | 0 | Update Enable for Transmit group 4 | addresses 0x838-0x83F |
| 2 | 0 | Update Enable for Transmit group 3 | addresses 0x830-0x837 |
| 1 | 0 | Update Enable for Transmit group 2 | addresses 0x828-0x82F |
| 0 | 0 | Update Enable for Transmit group 1 | addresses 0x820-0x827 |

2.5.2 0x91F—IMA_GRP_5T08_SEM (Group Table Control II)

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

| Bit | Default | Name | Description |
|-----|---------|------------------------------------|-----------------------|
| 7 | 0 | Update Enable for Receive group 8 | addresses 0x9DC–0x9DF |
| 6 | 0 | Update Enable for Receive group 7 | addresses 0x9D8–0x9DB |
| 5 | 0 | Update Enable for Receive group 6 | addresses 0x9D4–0x9D7 |
| 4 | 0 | Update Enable for Receive group 5 | addresses 0x9D0–0x9D3 |
| 3 | 0 | Update Enable for Transmit group 8 | addresses 0x938–0x93F |
| 2 | 0 | Update Enable for Transmit group 7 | addresses 0x930–0x937 |
| 1 | 0 | Update Enable for Transmit group 6 | addresses 0x928–0x92F |
| 0 | 0 | Update Enable for Transmit group 5 | addresses 0x920–0x927 |

2.5.3 0xA1F—IMA_GRP_9T012_SEM (Group Table Control III)

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

| Bit | Default | Name | Description |
|-----|---------|-------------------------------------|-----------------------|
| 7 | 0 | Update Enable for Receive group 12 | addresses 0xAD8–0xADF |
| 6 | 0 | Update Enable for Receive group 11 | addresses 0xAD4–0xADB |
| 5 | 0 | Update Enable for Receive group 10 | addresses 0xAD0–0xAD7 |
| 4 | 0 | Update Enable for Receive group 9 | addresses 0xA38–0xA3F |
| 3 | 0 | Update Enable for Transmit group 12 | addresses 0xA34–0xA37 |
| 2 | 0 | Update Enable for Transmit group 11 | addresses 0xA28–0xA2F |
| 1 | 0 | Update Enable for Transmit group 10 | addresses 0xA24–0xA27 |
| 0 | 0 | Update Enable for Transmit group 9 | addresses 0xA20–0xA27 |

2.5.4 0xB1F—IMA_GRP_13T016_SEM (Group Table Control IV)

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

| Bit | Default | Name | Description |
|-----|---------|-------------------------------------|-----------------------|
| 7 | 0 | Update Enable for Receive group 16 | addresses 0xBDC–0xBDF |
| 6 | 0 | Update Enable for Receive group 15 | addresses 0xBD8–0xBDB |
| 5 | 0 | Update Enable for Receive group 14 | addresses 0xBD4–0xBD7 |
| 4 | 0 | Update Enable for Receive group 13 | addresses 0xBD0–0xBD3 |
| 3 | 0 | Update Enable for Transmit group 16 | addresses 0xB38–0xB3F |
| 2 | 0 | Update Enable for Transmit group 15 | addresses 0xB30–0xB37 |
| 1 | 0 | Update Enable for Transmit group 14 | addresses 0xB28–0xB2F |
| 0 | 0 | Update Enable for Transmit group 13 | addresses 0xB20–0xB27 |

2.5.5 0xC1F—IMA_GRP_17T020_SEM (Group Table Control V (M28529 Only))

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

| Bit | Default | Name | Description |
|-----|---------|-------------------------------------|--|
| 7 | 0 | Update Enable for Receive group 20 | addresses 0xC5C–0xC5F (Not defined for M28525) |
| 6 | 0 | Update Enable for Receive group 19 | addresses 0xC58–0xC5B (Not defined for M28525) |
| 5 | 0 | Update Enable for Receive group 18 | addresses 0xC54–0xC57 (Not defined for M28525) |
| 4 | 0 | Update Enable for Receive group 17 | addresses 0xC50–0xC53 (Not defined for M28525) |
| 3 | 0 | Update Enable for Transmit group 20 | addresses 0xC38–0xC3F (Not defined for M28525) |
| 2 | 0 | Update Enable for Transmit group 19 | addresses 0xC30–0xC37 (Not defined for M28525) |
| 1 | 0 | Update Enable for Transmit group 18 | addresses 0xC28–0xC2F (Not defined for M28525) |
| 0 | 0 | Update Enable for Transmit group 17 | addresses 0xC20–0xC27 (Not defined for M28525) |

2.5.6 0xC9F—IMA_GRP_21T024_SEM (Group Table Control V (M28529 Only))

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

| Bit | Default | Name | Description |
|-----|---------|-------------------------------------|--|
| 7 | 0 | Update Enable for Receive group 24 | addresses 0xCDC–0xCDF (Not defined for M28525) |
| 6 | 0 | Update Enable for Receive group 23 | addresses 0xCD8–0xCDB (Not defined for M28525) |
| 5 | 0 | Update Enable for Receive group 22 | addresses 0xCD4–0xCD7 (Not defined for M28525) |
| 4 | 0 | Update Enable for Receive group 21 | addresses 0xCD0–0xCD3 (Not defined for M28525) |
| 3 | 0 | Update Enable for Transmit group 24 | addresses 0xCB8–0CBF (Not defined for M28525) |
| 2 | 0 | Update Enable for Transmit group 23 | addresses 0xCB0–0xCB7 (Not defined for M28525) |
| 1 | 0 | Update Enable for Transmit group 22 | addresses 0xCA8–0CAF (Not defined for M28525) |
| 0 | 0 | Update Enable for Transmit group 21 | addresses 0xCA0–0xCA7 (Not defined for M28525) |

2.5.7 0xD1F—IMA_GRP_25T028_SEM (Group Table Control V (M28529 Only))

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

| Bit | Default | Name | Description |
|-----|---------|-------------------------------------|--|
| 7 | 0 | Update Enable for Receive group 28 | addresses 0xD5C–0xD5F (Not defined for M28525) |
| 6 | 0 | Update Enable for Receive group 27 | addresses 0xD58–0xD5B (Not defined for M28525) |
| 5 | 0 | Update Enable for Receive group 26 | addresses 0xD54–0xD57 (Not defined for M28525) |
| 4 | 0 | Update Enable for Receive group 25 | addresses 0xD50–0xD53 (Not defined for M28525) |
| 3 | 0 | Update Enable for Transmit group 28 | addresses 0xD38–0xD3F (Not defined for M28525) |
| 2 | 0 | Update Enable for Transmit group 27 | addresses 0xD30–0xD37 (Not defined for M28525) |
| 1 | 0 | Update Enable for Transmit group 26 | addresses 0xD28–0xD2F (Not defined for M28525) |
| 0 | 0 | Update Enable for Transmit group 25 | addresses 0xD20–0xD27 (Not defined for M28525) |

2.5.8 0xD9F—IMA_GRP_29T032_SEM (Group Table Control V (M28529 Only))

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

| Bit | Default | Name | Description |
|-----|---------|-------------------------------------|--|
| 7 | 0 | Update Enable for Receive group 32 | addresses 0xDDC–0xDDF (Not defined for M28525) |
| 6 | 0 | Update Enable for Receive group 31 | addresses 0xDD8–0xDDB (Not defined for M28525) |
| 5 | 0 | Update Enable for Receive group 30 | addresses 0xDD4–0xDD7 (Not defined for M28525) |
| 4 | 0 | Update Enable for Receive group 29 | addresses 0xDD0–0xDD3 (Not defined for M28525) |
| 3 | 0 | Update Enable for Transmit group 32 | addresses 0xDB8–0xDBF (Not defined for M28525) |
| 2 | 0 | Update Enable for Transmit group 31 | addresses 0xDB0–0xDB7 (Not defined for M28525) |
| 1 | 0 | Update Enable for Transmit group 30 | addresses 0xDA8–0xDAF (Not defined for M28525) |
| 0 | 0 | Update Enable for Transmit group 29 | addresses 0xDA0–0xDA7 (Not defined for M28525) |

2.5.9 IMA_TX_GRP_n_RX_TEST_PATTERN (Transmit Group Rx Test Pattern)

This register contains the value of the Rx Test Pattern field for the transmitted ICP cells.

Group 1–16 Address

| n=1 | n=2 | n=3 | n=4 | n=5 | n=6 | n=7 | n=8 | n=9 | n=10 | n=11 | n=12 | n=13 | n=14 | n=15 | n=16 |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0x820 | 0x828 | 0x830 | 0x838 | 0x920 | 0x928 | 0x930 | 0x938 | 0xA20 | 0xA28 | 0xA30 | 0xA38 | 0xB20 | 0xB28 | 0xB30 | 0xB38 |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| n=17 | n=18 | n=19 | n=20 | n=21 | n=22 | n=23 | n=24 | n=25 | n=26 | n=27 | n=28 | n=29 | n=30 | n=31 | n=32 |
|--------------------------|-------|-------|-------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0xC20 | 0xC28 | 0xC30 | 0xC38 | 0xCA 0 | 0xCA 8 | 0xCB 0 | 0xCB 8 | 0xD2 0 | 0xD2 8 | 0xD3 0 | 0xD3 8 | 0xDA 0 | 0xDA 8 | 0xDB 0 | 0xDB 8 |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|-----------------|---|
| 7-0 | 0x00 | Rx Test Pattern | In support of the Test Pattern Procedure, this field is set equal to the value acquired from the Receive side test link. See address 0x8E7. When the Test Pattern Procedure is inactive, the Rx Test Pattern field should be set to 0xFF. Range: 0x00-0xFF |

2.5.10 IMA_TX_GRP n _CTL (Transmit Group Control Register)

This register, in conjunction with the IMA_TX_GRP n _FIRST_PHY_ADDR register, controls the operation of the Transmit IMA group.

Group 1-16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x821 | 0x829 | 0x831 | 0x839 | 0x921 | 0x929 | 0x931 | 0x939 | 0xA21 | 0xA29 | 0xA31 | 0xA39 | 0xB21 | 0xB29 | 0xB31 | 0xB39 |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17-32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|--------|--------|--------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0xC21 | 0xC29 | 0xC31 | 0xC39 | 0xCA 1 | 0xCA 9 | 0xCB 1 | 0xCB 9 | 0xD2 1 | 0xD2 9 | 0xD3 1 | 0xD3 9 | 0xDA 1 | 0xDA 9 | 0xDB 1 | 0xDB 9 |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|--------------------|--|
| 7 | 0 | Group Enable | 1 = Group is established and a round-robin is created 0 = Group is not established |
| 6 | 0 | SW Timeout Expired | 1 = certain LSM transitions (Unusable → Usable, Usable → Active) are allowed 0 = certain LSM transitions (Unusable → Usable, Usable → Active) are blocked |
| 5 | — | — | Reserved. Set to 0. |
| 4-0 | 0x0 | Group Size | Sets the number of configured links within group. Range: 0x0-0x1F (1-32 links in group) |

2.5.11 IMA_TX_GRP n _FIRST_PHY_ADDR (Transmit First PHY Address)

This register, in conjunction with the IMA_TX_GRP n _CTL register, controls the operation of the Transmit IMA group.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|-----------|-------|-----------|-------|-----------|-------|-----------|-------|-----------|--------|-----------|--------|-----------|--------|-----------|--------|
| 0x82 2 | 0x82A | 0x83 2 | 0x83A | 0x92 2 | 0x92A | 0x93 2 | 0x93A | 0xA2 2 | 0xA2A | 0xA3 2 | 0xA3A | 0xB2 2 | 0xB2A | 0xB3 2 | 0xB3A |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|-----------|--------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0xC22 | 0xC2 A | 0xC32 | 0xC3 A | 0xCA 2 | 0xCA A | 0xCB 2 | 0xCB A | 0xD2 2 | 0xD2 A | 0xD3 2 | 0xD3 A | 0xDA 2 | 0xDA A | 0xDB 2 | 0xDB A |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|------------------|--|
| 7 | — | — | Reserved. Set to 0. |
| 6 | 0 | Group Inhibit | 1 = Group is inhibited from carrying traffic 0 = Group is not inhibited |
| 5 | 0x0 | Tx IMA Version | IMA OAM Label value 1 = IMA v1.1 0 = IMA v1.0 |
| 4–0 | 0x00 | Link PHY Address | This field contains the PHY port address of the Transmit link with the lowest LID in the group. M28525: Range: 0–0xF M28529: Range: 0–0x1F |

2.5.12 IMA_TX_GRP n _ID (Transmit Group ID)

This register contains the value of the IMA Group ID field for the transmitted ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|-----------|-------|-----------|-------|-------|-------|-------|-------|-----------|--------|-----------|--------|-----------|--------|-----------|--------|
| 0x82 3 | 0x82B | 0x83 3 | 0x83B | 0x923 | 0x92B | 0x933 | 0x93B | 0xA2 3 | 0xA2B | 0xA3 3 | 0xA3B | 0xB2 3 | 0xB2B | 0xB3 3 | 0xB3B |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|-----------|--------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0xC23 | 0xC2 B | 0xC33 | 0xC3 B | 0xCA 3 | 0xCA B | 0xCB 3 | 0xCB B | 0xD2 3 | 0xD2 B | 0xD3 3 | 0xD3 B | 0xDA 3 | 0xDA B | 0xDB 3 | 0xDB B |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|-------------|--|
| 7–0 | 0x00 | Tx Group ID | This field contains the Transmit Group ID sent in the Transmit ICP cells of all links within the group. Range: 0x00–0xFF |

2.5.13 IMA_TX_GRP n _STAT_CTL (Transmit Group Status and Control)

This register contains the value of the Group Status and Control field for the transmitted ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x824 | 0x82C | 0x834 | 0x83C | 0x924 | 0x92C | 0x934 | 0x93C | 0xA24 | 0xA2C | 0xA34 | 0xA3C | 0xB24 | 0xB2C | 0xB34 | 0xB3C |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0xC24 | 0xC2C | 0xC34 | 0xC3C | 0xCA4 | 0xCA C | 0xCB4 | 0xCB C | 0xD24 | 0xD2 C | 0xD34 | 0xD3 C | 0xDA4 | 0xDA C | 0xDB4 | 0xDB C |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|------------------|--|
| 7–4 | 0x00 | Group State | 0 = Start-up 1 = Start-up-Ack 2 = Config-Abort–Unsupported M 3 = Config-Abort–Incompatible Symmetry 4 = Config-Abort–Unsupported IMA Version 5–7 = Reserved for other Config-Abort states 8 = Insufficient Links 9 = Blocked 0xA = Operational 0xB–F = reserved |
| 3–2 | 0 | Group Symmetry | 0 = Symmetrical configuration and operation 1 = Symmetrical configuration and asymmetrical operation 2 = Asymmetrical configuration and operation 3 = Alternate symmetrical configuration and operation |
| 1–0 | 0 | Frame Length (M) | 0 = M is 32 1 = M is 64 2 = M is 128 3 = M is 256 |

2.5.14 IMA_TX_GRP n _TIMING_INFO (Transmit Timing Information)

This register contains the value of the Transmit Timing Information field for the transmitted ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x825 | 0x82D | 0x835 | 0x83D | 0x925 | 0x92D | 0x935 | 0x93D | 0xA25 | 0xA2D | 0xA35 | 0xA3D | 0xB25 | 0xB2D | 0xB35 | 0xB3D |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0xC25 | 0xC2D | 0xC35 | 0xC3D | 0xCA5 | 0xCAD | 0xCB5 | 0xCBD | 0xD25 | 0xD2D | 0xD35 | 0xD3D | 0xDA5 | 0xDAD | 0xDB5 | 0xDBD |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7 | 0 | | Unused: Set to 0. |
| 6 | 0 | | Unused: Set to 0. |
| 5 | 0 | Tx Clock Mode | 0 = Independent Transmit Clock (ITC) 1 = Common Transmit Clock (CTC) |
| 4–0 | 0 | Timing Reference Link ID | This field contains the LID of the Transmit TRL. Range: 0x0–0x1F |

2.5.15 IMA_TX_GRP n _TEST_CTL (Transmit Test Control)

This register contains the value of the Tx Test Control field for the transmitted ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x826 | 0x82E | 0x836 | 0x83E | 0x926 | 0x92E | 0x936 | 0x93E | 0xA26 | 0xA2E | 0xA36 | 0xA3E | 0xB26 | 0xB2E | 0xB36 | 0xB3E |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0xC26 | 0xC2E | 0xC36 | 0xC3E | 0xCA6 | 0xCAE | 0xCB6 | 0xCBE | 0xD26 | 0xD2E | 0xD36 | 0xD3E | 0xDA6 | 0xDAE | 0xDB6 | 0xDBE |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|-------------------|--|
| 7 | 0 | | Unused: Set to 0. |
| 6 | 0 | | Unused: Set to 0. |
| 5 | 0 | Test Link Command | 0 = Inactive 1 = Active |
| 4–0 | 0 | Test Link ID | This field contains the LID of the Transmit Test Link. Range: 0x0–0x1F |

2.5.16 IMA_TX_GRP n _TX_TEST_PATTERN (Transmit Group Tx Test Pattern)

This register contains the value of the Tx Test Pattern field for the transmitted ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x827 | 0x82F | 0x837 | 0x83F | 0x927 | 0x92F | 0x937 | 0x93F | 0xA27 | 0xA2F | 0xA37 | 0xA3F | 0xB27 | 0xB2F | 0xB37 | 0xB3F |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|--------|--------|--------|-----------|--------|-----------|--------|-----------|--------|-----------|--------|-----------|-----------|-----------|-----------|
| 0xC27 | 0xC2F | 0xC37 | 0xC3F | 0xCA 7 | 0xCAF | 0xCB 7 | 0xCBF | 0xD2 7 | 0xD2F | 0xD3 7 | 0xD3F | 0xDA 7 | 0xDA F | 0xDB 7 | 0xDB F |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|-----------------|---|
| 7–0 | 0x0 | Tx Test Pattern | If the Test Link Command is set to Active, the Tx Test Pattern is sent in the ICP cell of the Transmit Test Link. For other links and when the Test Link Command is Inactive, the Tx Test Pattern in the Transmit ICP cells will automatically be set to 0x00. Range: 0x00–0xFF |

2.5.17 IMA_TX_ATM n _CELL_COUNT_LSB (Transmit Cell Count LSBs)

This register contains the least significant bits of a 16 bit count of the number of ATM layer cells transmitted over the Transmit ATM side UTOPIA bus for a particular UTOPIA address. The register is read only.

Tx UTOPIA Address 0 - 15

| $n=0$ | $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|
| 0x840 | 0x842 | 0x844 | 0x846 | 0x940 | 0x942 | 0x944 | 0x946 | 0xA40 | 0xA42 | 0xA44 | 0xA46 | 0xB40 | 0xB42 | 0xB44 | 0xB46 |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Tx UTOPIA Address 16–31

| $n=16$ | $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ |
|--------------------------|--------|--------|--------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0xC40 | 0xC42 | 0xC44 | 0xC46 | 0xCC 0 | 0xCC 2 | 0xCC 4 | 0xCC 6 | 0xD4 0 | 0xD4 2 | 0xD4 4 | 0xD4 6 | 0xDC 0 | 0xDC 2 | 0xDC 4 | 0xDC 6 |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7-0 | 0 | Transmit Cell Count LSBs | <u>Transmit Cell Count</u> : This field contains the least significant bits of a 16-bit count of the number of ATM layer cells transmitted over the specific UTOPIA address. A write operation with data = 0x01 to the first address (0x840 for Address 0, 0x842 for Address 1, etc.) transfers the state of all 16 bits of the counter to registers that are accessible to the microprocessor bus and clears the state of the counter. The first address should be read first. The second address (0x841 for Address 0, 0x843 for Address 1, etc.) is read next. A write operation with data = 0x00 to the first address of each group returns back to the raw counters. |

2.5.18 IMA_TX_ATM n _CELL_COUNT_MSB (Transmit Cell Count MSBs)

This register contains the most significant bits of a 16 bit count of the number of ATM layer cells transmitted over the Transmit ATM side UTOPIA bus for a particular UTOPIA address. The register is read only.

Tx UTOPIA Address 0 - 15

| $n=0$ | $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|
| 0x841 | 0x843 | 0x845 | 0x847 | 0x941 | 0x943 | 0x945 | 0x947 | 0xA41 | 0xA43 | 0xA45 | 0xA47 | 0xB41 | 0xB43 | 0xB45 | 0xB47 |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Tx UTOPIA Address 16–31

| $n=16$ | $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ |
|--------------------------|--------|--------|--------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0xC41 | 0xC43 | 0xC45 | 0xC47 | 0xCC 1 | 0xCC 3 | 0xCC 5 | 0xCC 7 | 0xD4 1 | 0xD4 3 | 0xD4 5 | 0xD4 7 | 0xDC 1 | 0xDC 3 | 0xDC 5 | 0xDC 7 |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|--------------------------|--|
| 7-0 | 0 | Transmit Cell Count MSBs | <u>Transmit Cell Count</u> : This field contains the most significant bits of a 16 bit count of the number of ATM layer cells transmitted over the specific UTOPIA address. A write operation with data = 0x01 to the first address (0x840 for Address 0, 0x842 for Address 1, etc.) transfers the state of all 16 bits of the counter to registers that are accessible to the microprocessor bus and clears the counter. A read operation should then be performed to read the previous state of the counter. The first address should be read first. The second address (0x841 for Address 0, 0x843 for Address 1, etc.) is read next. A write operation with data = 0x00 to the first address of each group returns back to the raw counters. |

2.5.19 IMA_RX_ATM n _CELL_COUNT_LSB (Receive Cell Count LSBs)

This register contains the least significant bits of a 16 bit count of the number of ATM layer cells received over the Receive ATM side UTOPIA bus for a particular UTOPIA address. The register is read only.

Rx UTOPIA Address 0 - 15

| $n=0$ | $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|
| 0x850 | 0x852 | 0x854 | 0x856 | 0x950 | 0x952 | 0x954 | 0x956 | 0xA50 | 0xA52 | 0xA54 | 0xA56 | 0xB50 | 0xB52 | 0xB54 | 0xB56 |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Rx UTOPIA Address 16–31

| $n=16$ | $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0xC48 | 0xC4A | 0xC4C | 0xC4E | 0xCC8 | 0xCCA | 0xCCC | 0xCCE | 0xD48 | 0xD4A | 0xD4C | 0xD4E | 0xDC8 | 0xDCA | 0xDCC | 0xDCE |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|-------------------------|---|
| 7-0 | 0 | Receive Cell Count LSBs | <u>Receive Cell Count</u> : This field contains the least significant bits of a 16 bit count of the number of ATM layer cells received over the specific UTOPIA address. A write operation with data = 0x01 to the first address (0x850 for Address 0, 0x852 for Address 1, etc.) transfers the state of all 16 bits of the counter to registers that are accessible to the microprocessor bus and clears the counter. A read operation should then be performed to read the previous state of the counter. The first address should be read first. The second address (0x851 for Address 0, 0x853 for Address 1, etc.) is read next. A write operation with data = 0x00 to the first address of each group returns back to the raw counters. |

2.5.20 IMA_RX_ATM n _CELL_COUNT_MSB (Receive Cell Count MSBs)

This register contains the most significant bits of a 16 bit count of the number of ATM layer cells received over the Receive ATM side UTOPIA bus for a particular UTOPIA address. The register is read only.

Rx UTOPIA Address 0 - 15

| $n=0$ | $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|
| 0x851 | 0x853 | 0x855 | 0x857 | 0x951 | 0x953 | 0x955 | 0x957 | 0xA51 | 0xA53 | 0xA55 | 0xA57 | 0xB51 | 0xB53 | 0xB55 | 0xB57 |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Rx UTOPIA Address 16–31

| $n=16$ | $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0xC49 | 0xC4B | 0xC4D | 0xC4F | 0xCC9 | 0xCCB | 0xCCD | 0xCCF | 0xD49 | 0xD4B | 0xD4D | 0xD4F | 0xDC9 | 0xDCB | 0xDCD | 0xDCF |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|-------------------------|--|
| 7-0 | 0 | Receive Cell Count MSBs | <u>Receive Cell Count</u> : This field contains the most significant bits of a 16 bit count of the number of ATM layer cells received over the specific UTOPIA address. A write operation with data = 0x01 to the first address (0x850 for Address 0, 0x852 for Address 1, etc.) transfers the state of all 16 bits of the counter to registers that are accessible to the microprocessor bus and clears the counter. A read operation should then be performed to read the previous state of the counter. The first address should be read first. The second address (0x851 for Address 0, 0x853 for Address 1, etc.) is read next. A write operation with data = 0x00 to the first address of each group returns back to the raw counters. |

2.5.21 IMA_RX_GRPn_CFG (Receive Group Status and Control)

This register, in conjunction with the IMA_RX_GRPn_CTL and IMA_RX_GRPn_FIRST_PHY_ADDR registers, controls the operation of the Receive IMA group.

Group 1–16 Address

| n=1 | n=2 | n=3 | n=4 | n=5 | n=6 | n=7 | n=8 | n=9 | n=10 | n=11 | n=12 | n=13 | n=14 | n=15 | n=16 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0x8D 0 | 0x8D 4 | 0x8D 8 | 0x8D C | 0x9D 0 | 0x9D 4 | 0x9D 8 | 0x9D C | 0xAD 0 | 0xAD 4 | 0xAD 8 | 0xAD C | 0xBD 0 | 0xBD 4 | 0xBD 8 | 0xBD C |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| n=17 | n=18 | n=19 | n=20 | n=21 | n=22 | n=23 | n=24 | n=25 | n=26 | n=27 | n=28 | n=29 | n=30 | n=31 | n=32 |
|--------------------------|-------|-------|-------|-------|-------|-------|--------|-------|-------|-------|-------|-------|-------|-------|--------|
| 0xC50 | 0xC54 | 0xC58 | 0xC5C | 0xCD0 | 0xCD4 | 0xCD8 | 0xCD C | 0xD50 | 0xD54 | 0xD58 | 0xD5C | 0xDD0 | 0xDD4 | 0xDD8 | 0xDD C |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|----------------------------|---|
| 7 | 0 | Check Group ID | 1 = The receive group ID is compared with the expected Group ID as part of link framing 0 = the receive group ID is ignored |
| 6 | 0 | Acquire Frame Length | 1 = The frame length and IMA version acquired from the received link is used as part of link framing 0 = The frame length and IMA version from the received link is compared against the expected frame length and IMA version as part of link framing |
| 5–4 | 0 | Maximum Differential Delay | Reserved. Set to 0. |
| 3–2 | 0 | Group Symmetry | 0 = Symmetrical configuration and operation 1 = Symmetrical configuration and asymmetrical operation 2 = Asymmetrical configuration and operation 3 = Alternate symmetrical configuration and operation |
| 1–0 | 0 | Frame Length (M) | 0 = M is 32 1 = M is 64 2 = M is 128 3 = M is 256 |

2.5.22 IMA_RX_GRPn_CTL (Receive Group Control Register)

This register, in conjunction with the IMA_RX_GRPn_CFG and IMA_RX_GRPn_FIRST_PHY_ADDR registers, controls the operation of the Receive IMA group.

Group 1–16 Address

| n=1 | n=2 | n=3 | n=4 | n=5 | n=6 | n=7 | n=8 | n=9 | n=10 | n=11 | n=12 | n=13 | n=14 | n=15 | n=16 |
|-----------|-----------|-----------|-------|-----------|-----------|-----------|-------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0x8D 1 | 0x8D 5 | 0x8D 9 | 0x8DD | 0x9D 1 | 0x9D 5 | 0x9D 9 | 0x9DD | 0xAD 1 | 0xAD 5 | 0xAD 9 | 0xAD D | 0xBD 1 | 0xBD 5 | 0xBD 9 | 0xBD D |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| n=17 | n=18 | n=19 | n=20 | n=21 | n=22 | n=23 | n=24 | n=25 | n=26 | n=27 | n=28 | n=29 | n=30 | n=31 | n=32 |
|--------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0xC5 1 | 0xC5 5 | 0xC5 9 | 0xC5 D | 0xCD 1 | 0xCD 5 | 0xCD 9 | 0xCD D | 0xD5 1 | 0xD5 5 | 0xD5 9 | 0xD5 D | 0xDD 1 | 0xDD 5 | 0xDD 9 | 0xDD D |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|--------------------|--|
| 7 | 0 | Group Enable | 1 = Group is established and a round-robin is created 0 = Group is not established |
| 6 | 0 | SW Timeout Expired | 1 = certain LSM transitions (Usable → Active) are allowed 0 = certain LSM transitions (Usable → Active) are blocked |
| 5 | — | — | Reserved. Set to 0. |
| 4–0 | 0x0 | Group Size | Sets the number of configured links within group. Range: 0x0–0x1F (1–32 links in group) |

2.5.23 IMA_RX_GRP n _FIRST_PHY_ADDR (Receive First PHY Address)

This register, in conjunction with the IMA_RX_GRP n _CTL and IMA_RX_GRP n _CFG registers, controls the operation of the Receive IMA group.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|-----------|-----------|-------|-------|-----------|-----------|-------|-------|-----------|-----------|--------|-----------|-----------|-----------|--------|-----------|
| 0x8D 2 | 0x8D 6 | 0x8DA | 0x8DE | 0x9D 2 | 0x9D 6 | 0x9DA | 0x9DE | 0xAD 2 | 0xAD 6 | 0xADA | 0xAD E | 0xBD 2 | 0xBD 6 | 0xBDA | 0xBD E |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|-----------|-----------|--------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|--------|-----------|-----------|-----------|-----------|
| 0xC5 2 | 0xC5 6 | 0xC5 A | 0xC5E | 0xCD 2 | 0xCD 6 | 0xCD A | 0xCD E | 0xD5 2 | 0xD5 6 | 0xD5 A | 0xD5E | 0xDD 2 | 0xDD 6 | 0xDD A | 0xDD E |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|------------------|---|
| 7 | 0 | Resync Group | 1 = Enables the link differential delay synchronization process 0 = Disables the link differential delay synchronization process |
| 6 | 0 | Drain Buffer | This bit is used by the software driver to reset the differential delay in T1/E1 mode: 1 = Allows the differential delay buffer to drain excess cell buffering. 0 = Normal delay buffering. |
| 5 | 0 | Rx IMA Version | IMA OAM Label value 1 = IMA v1.1 0 = IMA v1.0 |
| 4–0 | 0x00 | Link PHY Address | This field contains the PHY port address of the Receive link with the lowest LID in the group. M28525: Range: 0–0xF M28529: Range: 0–0x1F |

2.5.24 IMA_RX_GRP n _ID (Expected Receive Group ID)

This register contains the value of the Expected IMA Group ID field for the received ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|-----------|-----------|-------|-------|-----------|-----------|-------|-------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0x8D 3 | 0x8D 7 | 0x8DB | 0x8DF | 0x9D 3 | 0x9D 7 | 0x9DB | 0x9DF | 0xAD 3 | 0xAD 7 | 0xAD B | 0xAD F | 0xBD 3 | 0xBD 7 | 0xBD B | 0xBD F |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|-----------|-----------|--------|-----------|-----------|-----------|--------|-----------|-----------|-----------|--------|-----------|-----------|-----------|--------|
| 0xC5 3 | 0xC5 7 | 0xC5 B | 0xC5F | 0xCD 3 | 0xCD 7 | 0xCD B | 0xCDF | 0xD5 3 | 0xD5 7 | 0xD5 B | 0xD5F | 0xDD 3 | 0xDD 7 | 0xDD B | 0xDDF |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|----------------------|---|
| 7–0 | 0x00 | Expected Rx Group ID | This field contains the Group ID expected in the Receive ICP cells of all links in this group. Range: 0x00–0xFF |

2.5.25 IMA_RX_GRP n _RX_TEST_PATTERN (Receive Group Rx Test Pattern)

This **read-only** register contains the value of the Rx Test Pattern field acquired from the received ICP cells.

Group 1–16 Address

| | | | | | | | | | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
| 0x8E0 | 0x8E8 | 0x8F0 | 0x8F8 | 0x9E0 | 0x9E8 | 0x9F0 | 0x9F8 | 0xAE0 | 0xAE8 | 0xAF0 | 0xAF8 | 0xBE0 | 0xBE8 | 0xBF0 | 0xBF8 |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| | | | | | | | | | | | | | | | |
|--------------------------|-----------|-----------|--------|--------|--------|--------|--------|-----------|-----------|--------|--------|--------|--------|--------|--------|
| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
| 0xC6 0 | 0xC6 8 | 0xC7 0 | 0xC78 | 0xCE0 | 0xCE8 | 0xCF0 | 0xCF8 | 0xD6 0 | 0xD6 8 | 0xD70 | 0xD78 | 0xDE0 | 0xDE8 | 0xDF0 | 0xDF8 |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|-----------------|--|
| 7–0 | — | Rx Test Pattern | This field reflects the value of the Rx Test Pattern byte acquired from the Receive side test link. Range: 0x00–0xFF |

2.5.26 IMA_RX_GRP n _STAT_CTL_CHANGE (Receive Group Status & Control Change Indication)

This **read-only** register contains the value of the Status and Control Indication field acquired from the received ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x8E2 | 0x8EA | 0x8F2 | 0x8FA | 0x9E2 | 0x9EA | 0x9F2 | 0x9FA | 0xAE2 | 0xAEA | 0xAF2 | 0xAFA | 0xBE2 | 0xBEA | 0xBF2 | 0xBFA |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0xC62 | 0xC6A | 0xC72 | 0xC7A | 0xCE2 | 0xCEA | 0xCF2 | 0xCFA | 0xD62 | 0xD6A | 0xD72 | 0xD7A | 0xDE2 | 0xDEA | 0xDF2 | 0xDFA |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|---------|--|
| 7–0 | — | Rx SCCI | This field reflects the value of the Status & Change Control Indication byte acquired from the Receive ICP cells of the monitored link. Range: 0x00–0xFF |

2.5.27 IMA_RX_GRP n _ACTUAL_GRP_ID (Actual Receive Group ID)

This **read-only** register contains the value of the IMA ID field acquired from the received ICP cells.

Group 1–16 Address

| | | | | | | | | | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
| 0x8E3 | 0x8EB | 0x8F3 | 0x8FB | 0x9E3 | 0x9EB | 0x9F3 | 0x9FB | 0xAE3 | 0xAEB | 0xAF3 | 0AFB | 0xBE3 | 0xBEB | 0xBF3 | 0BFB |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| | | | | | | | | | | | | | | | |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
| 0xC63 | 0xC6B | 0xC73 | 0xC7B | 0xCE3 | 0CEB | 0xCF3 | 0CFB | 0xD63 | 0xD6B | 0xD73 | 0xD7B | 0xDE3 | 0DEB | 0xDF3 | 0DFB |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|--------------------|--|
| 7–0 | — | Actual Rx Group ID | This field contains the Group ID acquired from the Receive ICP cells of the monitored link. Range: 0x00–0xFF |

2.5.28 IMA_RX_GRP n _STAT_CTL (Receive Group Status and Control)

This **read-only** register contains the value of the Group Status and Control field acquired from the received ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x8E4 | 0x8EC | 0x8F4 | 0x8FC | 0x9E4 | 0x9EC | 0x9F4 | 0x9FC | 0xAE4 | 0xAEC | 0xAF4 | 0xAFC | 0xBE4 | 0xBEC | 0xBF4 | 0xBFC |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0xC64 | 0xC6C | 0xC74 | 0xC7C | 0xCE4 | 0xCEC | 0xCF4 | 0xCFC | 0xD64 | 0xD6C | 0xD74 | 0xD7C | 0xDE4 | 0xDEC | 0xDF4 | 0xDFC |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|------------------|--|
| 7–4 | — | Group State | 0 = Start-up 1 = Start-up-Ack 2 = Config-Abort–Unsupported M 3 = Config-Abort–Incompatible Symmetry 4 = Config-Abort–Unsupported IMA Version 5–7 = Reserved for other Config-Abort states 8 = Insufficient Links 9 = Blocked 0xA = Operational 0xB–F = reserved |
| 3–2 | — | Group Symmetry | 0 = Symmetrical configuration and operation 1 = Symmetrical configuration and asymmetrical operation 2 = Asymmetrical configuration and operation |
| 1–0 | — | Frame Length (M) | 0 = M is 32 1 = M is 64 2 = M is 128 3 = M is 256 |

2.5.29 IMA_RX_GRP n _TIMING_INFO (Receive Timing Information)

This **read-only** register contains the value of the Transmit Timing Information field acquired from the received ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x8E5 | 0x8ED | 0x8F5 | 0x8FD | 0x9E5 | 0x9ED | 0x9F5 | 0x9FD | 0xAE5 | 0xAED | 0xAF5 | 0AFD | 0xBE5 | 0xBED | 0xBF5 | 0BFD |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0xC65 | 0xC6D | 0xC75 | 0xC7D | 0xCE5 | 0xCED | 0xCF5 | 0CFD | 0xD65 | 0xD6D | 0xD75 | 0xD7D | 0xDE5 | 0xDED | 0xDF5 | 0DFD |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|--------------------------|---|
| 7 | — | — | Unused |
| 6 | — | — | Unused |
| 5 | — | Rx Clock Mode | 0 = Independent Transmit Clock (ITC) 1 = Common Transmit Clock (CTC) |
| 4–0 | — | Timing Reference Link ID | This field contains the LID of the Receive TRL. Range: 0x0–0x1F |

2.5.30 IMA_RX_GRP n _TEST_CTL (Receive Test Control)

This read-only register contains the value of the Tx Test Control field acquired from the received ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x8E6 | 0x8EE | 0x8F6 | 0x8FE | 0x9E6 | 0x9EE | 0x9F6 | 0x9FE | 0xAE6 | 0xAEE | 0xAF6 | 0xAFE | 0xBE6 | 0xBEE | 0xBF6 | 0xBFE |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0xC66 | 0xC6E | 0xC76 | 0xC7E | 0xCE6 | 0xCEE | 0xCF6 | 0xCFE | 0xD66 | 0xD6E | 0xD76 | 0xD7E | 0xDE6 | 0xDEE | 0xDF6 | 0DFE |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|-------------------|---|
| 7 | — | — | Unused |
| 6 | — | — | Unused |
| 5 | — | Test Link Command | 0 = Inactive 1 = Active |
| 4–0 | — | Test Link ID | This field contains the LID of the Receive Test Link. Range: 0x0–0x1F |

2.5.31 IMA_RX_GRP n _TX_TEST_PATTERN (Receive Group Tx Test Pattern)

This **read-only** register contains the value of the Tx Test Pattern field acquired from the received ICP cells.

Group 1–16 Address

| $n=1$ | $n=2$ | $n=3$ | $n=4$ | $n=5$ | $n=6$ | $n=7$ | $n=8$ | $n=9$ | $n=10$ | $n=11$ | $n=12$ | $n=13$ | $n=14$ | $n=15$ | $n=16$ |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|
| 0x8E7 | 0x8EF | 0x8F7 | 0x8FF | 0x9E7 | 0x9EF | 0x9F7 | 0x9FF | 0xAE7 | 0xAEF | 0xAF7 | 0xAFF | 0xBE7 | 0BEF | 0xBF7 | 0xBFF |
| M28525 | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

Group 17–32 Address

| $n=17$ | $n=18$ | $n=19$ | $n=20$ | $n=21$ | $n=22$ | $n=23$ | $n=24$ | $n=25$ | $n=26$ | $n=27$ | $n=28$ | $n=29$ | $n=30$ | $n=31$ | $n=32$ |
|--------------------------|------------|-----------|--------|--------|--------|--------|--------|-----------|--------|-----------|--------|-----------|--------|--------|--------|
| 0xC6 7 | 0xC6F 7 | 0xC7 7 | 0xC7F | 0xCE7 | 0xCEF | 0xCF7 | 0xCFF | 0xD6 7 | 0xD6F | 0xD7 7 | 0xD7F | 0xDE 7 | 0DEF | 0xDF7 | 0DFF |
| M28525 -- Not Applicable | | | | | | | | | | | | | | | |
| M28529 | | | | | | | | | | | | | | | |

| Bit | Default | Name | Description |
|-----|---------|-----------------|---|
| 7–0 | — | Tx Test Pattern | If the Test Link Command is set to Active, the Tx Test Pattern is accessed from the ICP cell of the Transmit Test Link. This register should be read multiple times (debounced) to ensure receipt of a valid test pattern. Range: 0x00–0xFF |

2.6 IMA Link Registers

The IMA Link layer contains configuration and status information that is associated with IMA groups or pass-through facilities.

2.6.1 0x81E—IMA_LNK_SEM (Link Table Control Register)

For the following bits, 1 = the link table is being updated, 0 = the link table is not being updated. The update enable must be set to 1 prior to writing the link table. All elements of the link table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The link tables are described below.

NOTE: This register cannot be read back.

| Bit | Default | Name | Description |
|-----|---------|--|---|
| 7 | 0 | Update Enable for Receive facilities 24–31 | addresses 0xB80–0xB87, 0xBA8–0BAF (Not defined for M28525) |
| 6 | 0 | Update Enable for Receive facilities 16–23 | addresses 0xA80–0xA87, 0xAA8–0AAF (Not defined for M28525) |

| Bit | Default | Name | Description |
|------------|----------------|---|--|
| 5 | 0 | Update Enable for Receive facilities 8–15 | addresses 0x980–0x987, 0x9A8–0x9AF (Not defined for M28525) |
| 4 | 0 | Update Enable for Receive facilities 0–7 | addresses 0x880–0x887, 0x8A8–0x8AF (Not defined for M28525) |
| 3 | 0 | Update Enable for Transmit facilities 24–31 | addresses 0xB60–0xB67, 0xB70–0xB77 (Not defined for M28525) |
| 2 | 0 | Update Enable for Transmit facilities 16–23 | addresses 0xA60–0xA67, 0xA70–0xA77 (Not defined for M28525) |
| 1 | 0 | Update Enable for Transmit facilities 8–15 | addresses 0x960–0x967, 0x970–0x977 (Not defined for M28525) |
| 0 | 0 | Update Enable for Transmit facilities 0–7 | addresses 0x860–0x867, 0x870–0x877 |

2.6.2 IMA_TX_LNK n _CTL (Transmit Link Control Register)

This register, in conjunction with IMA_TX_LNK n _ID register, configures the IMA link attributes for the Transmit port.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x860 |
| 1 | 0x861 |
| 2 | 0x862 |
| 3 | 0x863 |
| 4 | 0x864 |
| 5 | 0x865 |
| 6 | 0x866 |
| 7 | 0x867 |
| 8 | 0x960 |
| 9 | 0x961 |
| 10 | 0x962 |
| 11 | 0x963 |
| 12 | 0x964 |
| 13 | 0x965 |
| 14 | 0x966 |
| 15 | 0x967 |

| n | Address |
|----|---------|
| 16 | 0xA60 |
| 17 | 0xA61 |
| 18 | 0xA62 |
| 19 | 0xA63 |
| 20 | 0xA64 |
| 21 | 0xA65 |
| 22 | 0xA66 |
| 23 | 0xA67 |
| 24 | 0xB60 |
| 25 | 0xB61 |
| 26 | 0xB62 |
| 27 | 0xB63 |
| 28 | 0xB64 |
| 29 | 0xB65 |
| 30 | 0xB66 |
| 31 | 0xB67 |

| Bit | Default | Name | Description |
|-----|---------|-----------------------|---|
| 7 | 0 | Link Assigned | 1 = Facility is part of IMA Group 0 = Facility is a bypass channel (pass-through or unassigned) |
| 6 | 0 | Link Inhibit | 1 = Link is blocked from use 0 = Link is not inhibited |
| 5 | 0 | Link Fault | 1 = Link Fault Failure is active 0 = Link Fault Failure is inactive |
| 4-0 | 0 | Next Link PHY Address | This field contains the PHY address of the next link in the IMA Group. If the link is a pass-through facility, this field is ignored but is recommended to be set to the PHY address of the pass-through facility (i.e., set to 0 for PHY address 0, set to 1 for PHY address 1, etc.). M28525: Range: 0-0x0F M28529: Range: 0-0x1F |

2.6.3 IMA_TX_LNK n _STATE (Transmit Link Status Register)

This **read-only** register provides state and status information for the Transmit link.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x868 |
| 1 | 0x869 |
| 2 | 0x86A |
| 3 | 0x86B |
| 4 | 0x86C |
| 5 | 0x86D |
| 6 | 0x86E |
| 7 | 0x86F |
| 8 | 0x968 |
| 9 | 0x969 |
| 10 | 0x96A |
| 11 | 0x96B |
| 12 | 0x96C |
| 13 | 0x96D |
| 14 | 0x96E |
| 15 | 0x96F |

| n | Address |
|----|---------|
| 16 | 0xA68 |
| 17 | 0xA69 |
| 18 | 0xA6A |
| 19 | 0xA6B |
| 20 | 0xA6C |
| 21 | 0xA6D |
| 22 | 0xA6E |
| 23 | 0xA6F |
| 24 | 0xB68 |
| 25 | 0xB69 |
| 26 | 0xB6A |
| 27 | 0xB6B |
| 28 | 0xB6C |
| 29 | 0xB6D |
| 30 | 0xB6E |
| 31 | 0xB6F |

| Bit | Default | Name | Description |
|-----|---------|----------------------|---|
| 7–6 | — | Tx-Stuff-IMA Counter | This field contains a count of the number of Near-End Transmit cell stuffing events. Upon a read of this address, the contents of the counter is transferred to a register that is accessible to the microprocessor bus and the counter is cleared. |
| 5 | — | — | Reserved. |
| 4 | — | — | Reserved. |
| 3 | — | Waiting for SW Timer | 1 = a transition of the Transmit LSM is waiting for an enable from software 0 = no transition of the LSM is waiting for software |
| 2–0 | — | NE Tx LSM State | 0 = Not In Group 1 = Unusable—no reason given 2 = Unusable—Fault 3 = Unusable—Mis-connected 4 = Unusable—Blocked 5 = Unusable—Failed 6 = Usable 7 = Active |

2.6.4 IMA_TX_LNK n _ID (Transmit Link ID Register)

This register, in conjunction with IMA_TX_LNK n _CTL register, configures the IMA link attributes for the Transmit port.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x870 |
| 1 | 0x871 |
| 2 | 0x872 |
| 3 | 0x873 |
| 4 | 0x874 |
| 5 | 0x875 |
| 6 | 0x876 |
| 7 | 0x877 |
| 8 | 0x970 |
| 9 | 0x971 |
| 10 | 0x972 |
| 11 | 0x973 |
| 12 | 0x974 |
| 13 | 0x975 |
| 14 | 0x976 |
| 15 | 0x977 |

| n | Address |
|----|---------|
| 16 | 0xA70 |
| 17 | 0xA71 |
| 18 | 0xA72 |
| 19 | 0xA73 |
| 20 | 0xA74 |
| 21 | 0xA75 |
| 22 | 0xA76 |
| 23 | 0xA77 |
| 24 | 0xB70 |
| 25 | 0xB71 |
| 26 | 0xB72 |
| 27 | 0xB73 |
| 28 | 0xB74 |
| 29 | 0xB75 |
| 30 | 0xB76 |
| 31 | 0xB77 |

| Bit | Default | Name | Description |
|-----|---------|-----------------|---|
| 7 | — | — | Reserved. Set to 0 |
| 6 | — | — | Reserved. Set to 0 |
| 5 | 0 | Link Misconnect | 1 = Link Misconnect Failure is active 0 = Link Misconnect Failure is inactive |
| 4–0 | 0x00 | Link ID | This field contains the Transmit Link ID assigned to this facility. Range: 0x00–0x1F |

2.6.5 IMA_RX_LNK n _CTL (Receive Link Control Register)

This register, in conjunction with IMA_RX_LNK n _ID register, configures the IMA link attributes for the Receive port.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x880 |
| 1 | 0x881 |
| 2 | 0x882 |
| 3 | 0x883 |
| 4 | 0x884 |
| 5 | 0x885 |
| 6 | 0x886 |
| 7 | 0x887 |
| 8 | 0x980 |
| 9 | 0x981 |
| 10 | 0x982 |
| 11 | 0x983 |
| 12 | 0x984 |
| 13 | 0x985 |
| 14 | 0x986 |
| 15 | 0x987 |

| n | Address |
|----|---------|
| 16 | 0xA80 |
| 17 | 0xA81 |
| 18 | 0xA82 |
| 19 | 0xA83 |
| 20 | 0xA84 |
| 21 | 0xA85 |
| 22 | 0xA86 |
| 23 | 0xA87 |
| 24 | 0xB80 |
| 25 | 0xB81 |
| 26 | 0xB82 |
| 27 | 0xB83 |
| 28 | 0xB84 |
| 29 | 0xB85 |
| 30 | 0xB86 |
| 31 | 0xB87 |

| Bit | Default | Name | Description |
|-----|---------|-----------------------|--|
| 7 | 0 | Link Assigned | 1 = Facility is part of IMA Group 0 = Facility is a bypass channel (pass-through or unassigned) |
| 6-5 | 0 | Link State | 0 = Link is not inhibited 1 = Link Fault Failure is active 2 = Link is blocked from use 3 = Rx Failed condition |
| 4-0 | 0 | Next Link PHY Address | This field contains the PHY address of the next link in the IMA Group. If the link is a pass-through facility, this field is ignored but is recommended to be set to the PHY address of the pass-through facility (i.e., set to 0 for PHY address 0, set to 1 for PHY address 1, etc.). M28525: Range: 0-F M28529: Range: 0-0x1F |

2.6.6 IMA_RX_LNK n _STATE (Receive Link Status Register)

This **read-only** register provides state and status information for the Receive link.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x888 |
| 1 | 0x889 |
| 2 | 0x88A |
| 3 | 0x88B |
| 4 | 0x88C |
| 5 | 0x88D |
| 6 | 0x88E |
| 7 | 0x88F |
| 8 | 0x988 |
| 9 | 0x989 |
| 10 | 0x98A |
| 11 | 0x98B |
| 12 | 0x98C |
| 13 | 0x98D |
| 14 | 0x98E |
| 15 | 0x98F |

| n | Address |
|----|---------|
| 16 | 0xA88 |
| 17 | 0xA89 |
| 18 | 0xA8A |
| 19 | 0xA8B |
| 20 | 0xA8C |
| 21 | 0xA8D |
| 22 | 0xA8E |
| 23 | 0xA8F |
| 24 | 0xB88 |
| 25 | 0xB89 |
| 26 | 0xB8A |
| 27 | 0xB8B |
| 28 | 0xB8C |
| 29 | 0xB8D |
| 30 | 0xB8E |
| 31 | 0xB8F |

| Bit | Default | Name | Description |
|-----|---------|----------------------|--|
| 7–6 | — | Rx-Stuff-IMA Counter | This field contains a count of the number of Near-End Receive cell stuffing events. Upon a read of this address, the contents of the counter is transferred to a register that is accessible to the microprocessor bus and the counter is cleared. |
| 5 | — | — | Reserved. |
| 4 | — | — | Reserved. |
| 3 | — | Waiting for SW Timer | 1 = a transition of the Receive LSM is waiting for an enable from software 0 = no transition of the LSM is waiting for software |
| 2–0 | — | NE Rx LSM State | 0 = Not In Group 1 = Unusable—no reason given 2 = Unusable—Fault 3 = Unusable—Mis-connected 4 = Unusable—Blocked 5 = Unusable—Failed 6 = Usable 7 = Active |

2.6.7 IMA_RX_LNK n _DEFECT (Receive Link Defects Register)

This register provides state and status information for the Receive link. This register is primarily **read-only** except for bit 1 which is read/write.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x890 |
| 1 | 0x891 |
| 2 | 0x892 |
| 3 | 0x893 |
| 4 | 0x894 |
| 5 | 0x895 |
| 6 | 0x896 |
| 7 | 0x897 |
| 8 | 0x990 |
| 9 | 0x991 |
| 10 | 0x992 |
| 11 | 0x993 |
| 12 | 0x994 |
| 13 | 0x995 |
| 14 | 0x996 |
| 15 | 0x997 |

| n | Address |
|----|---------|
| 16 | 0xA90 |
| 17 | 0xA91 |
| 18 | 0xA92 |
| 19 | 0xA93 |
| 20 | 0xA94 |
| 21 | 0xA95 |
| 22 | 0xA96 |
| 23 | 0xA97 |
| 24 | 0xB90 |
| 25 | 0xB91 |
| 26 | 0xB92 |
| 27 | 0xB93 |
| 28 | 0xB94 |
| 29 | 0xB95 |
| 30 | 0xB96 |
| 31 | 0xB97 |

| Bit | Default | Name | Description |
|-----|---------|------------------------|--|
| 7 | — | Δ (LIF Defect) | 1 = The LIF defect has changed state since the last time this register was read 0 = The LIF defect has not changed state |
| 6 | — | LIF Defect | 1 = The LIF defect is currently active 0 = The LIF defect is inactive |
| 5 | — | Δ (LODS Defect) | 1 = The LODS defect has changed state since the last time this register was read 0 = The LODS defect has not changed state |
| 4 | — | LODS Defect | 1 = The LODS defect is currently active 0 = The LODS defect is inactive |
| 3 | — | Δ (RDI Defect) | 1 = The RDI defect has changed state since the last time this register was read 0 = The RDI defect has not changed state |
| 2 | — | RDI Defect | 1 = The RDI defect is currently active 0 = The RDI defect is inactive |
| 1 | 0 | PHY Defect | 1 = A PHY defect is active 0 = All PHY defects are inactive |
| 0 | — | Rx_TRL Error | This bit is set high if the transition detector for the Rx_TRL input detects a bad signal. This bit is active high and is reset upon reading this address. |

2.6.8 IMA_FE_TX_LNK n _CFG (FE Transmit Configuration Register)

This **read-only** register provides Far-End Transmit configuration information for the Receive link.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x898 |
| 1 | 0x899 |
| 2 | 0x89A |
| 3 | 0x89B |
| 4 | 0x89C |
| 5 | 0x89D |
| 6 | 0x89E |
| 7 | 0x89F |
| 8 | 0x998 |
| 9 | 0x999 |
| 10 | 0x99A |
| 11 | 0x99B |
| 12 | 0x99C |
| 13 | 0x99D |
| 14 | 0x99E |
| 15 | 0x99F |

| n | Address |
|----|---------|
| 16 | 0xA98 |
| 17 | 0xA99 |
| 18 | 0xA9A |
| 19 | 0xA9B |
| 20 | 0xA9C |
| 21 | 0xA9D |
| 22 | 0xA9E |
| 23 | 0xA9F |
| 24 | 0xB98 |
| 25 | 0xB99 |
| 26 | 0xB9A |
| 27 | 0xB9B |
| 28 | 0xB9C |
| 29 | 0xB9D |
| 30 | 0xB9E |
| 31 | 0xB9F |

| Bit | Default | Name | Description |
|-----|---------|------------------|--|
| 7–6 | — | Frame Length (M) | This field contains the contents of the frame length field for the ICP cell arriving on this facility. 0 = M is 32 1 = M is 64 2 = M is 128 3 = M is 256 |
| 5 | — | IMA Version | (IMA OAM Label value) 1 = IMA v1.1 0 = IMA v1.0 |
| 4–0 | — | Link ID | This field contains the contents of the Link ID field for the ICP cell arriving on this facility. Range: 0x0–0x1F. |

NOTE:

The value in this register is undefined when there is no valid IMA cell stream present on the link. The value in this register is also undefined for a maximum of two seconds following the creation of a group containing this link.

2.6.9 IMA_FE_LNK_n_STATE (FE Link Status Register)

This **read-only** register provides Far-End link status information for the facility.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x8A0 |
| 1 | 0x8A1 |
| 2 | 0x8A2 |
| 3 | 0x8A3 |
| 4 | 0x8A4 |
| 5 | 0x8A5 |
| 6 | 0x8A6 |
| 7 | 0x8A7 |
| 8 | 0x9A0 |
| 9 | 0x9A1 |
| 10 | 0x9A2 |
| 11 | 0x9A3 |
| 12 | 0x9A4 |
| 13 | 0x9A5 |
| 14 | 0x9A6 |
| 15 | 0x9A7 |

| n | Address |
|----|---------|
| 16 | 0xAA0 |
| 17 | 0xAA1 |
| 18 | 0xAA2 |
| 19 | 0xAA3 |
| 20 | 0xAA4 |
| 21 | 0xAA5 |
| 22 | 0xAA6 |
| 23 | 0xAA7 |
| 24 | 0xBA0 |
| 25 | 0xBA1 |
| 26 | 0xBA2 |
| 27 | 0xBA3 |
| 28 | 0xBA4 |
| 29 | 0xBA5 |
| 30 | 0xBA6 |
| 31 | 0xBA7 |

| Bit | Default | Name | Description |
|-----|---------|-----------------|---|
| 7-5 | — | FE Tx LSM State | 0 = Not In Group 1 = Unusable—No reason given 2 = Unusable—Fault 3 = Unusable—Mis-connected 4 = Unusable—Blocked 5 = Unusable—Failed 6 = Usable 7 = Active |
| 4-2 | — | FE Rx LSM State | 0 = Not In Group 1 = Unusable—No reason given 2 = Unusable—Fault 3 = Unusable—Mis-connected 4 = Unusable—Blocked 5 = Unusable—Failed 6 = Usable 7 = Active |

| Bit | Default | Name | Description (Continued) |
|-----|---------|------------------------|---|
| 1-0 | — | FE Rx Defect Indicator | 0 = No Defects 1 = Physical link defect 2 = LIF defect 3 = LODS defect |

2.6.10 IMA_RX_LNK n _ID (Receive Link ID Register)

This register, in conjunction with IMA_RX_LNK n _CTL register, configures the IMA link attributes for the Receive port.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x8A8 |
| 1 | 0x8A9 |
| 2 | 0x8AA |
| 3 | 0x8AB |
| 4 | 0x8AC |
| 5 | 0x8AD |
| 6 | 0x8AE |
| 7 | 0x8AF |
| 8 | 0x9A8 |
| 9 | 0x9A9 |
| 10 | 0x9AA |
| 11 | 0x9AB |
| 12 | 0x9AC |
| 13 | 0x9AD |
| 14 | 0x9AE |
| 15 | 0x9AF |

| n | Address |
|----|---------|
| 16 | 0xAA8 |
| 17 | 0xAA9 |
| 18 | 0xAAA |
| 19 | 0xAAB |
| 20 | 0xAAC |
| 21 | 0xAAD |
| 22 | 0xAAE |
| 23 | 0xAAF |
| 24 | 0xBA8 |
| 25 | 0xBA9 |
| 26 | 0xBAA |
| 27 | 0xBAB |
| 28 | 0xBAC |
| 29 | 0xBAD |
| 30 | 0xBAE |
| 31 | 0xBAF |

| Bit | Default | Name | Description |
|-----|---------|-----------------|--|
| 7 | — | — | Reserved. Set to 0 |
| 6 | — | — | Reserved. Set to 0 |
| 5 | 0 | Link Misconnect | 1 = Link Misconnect Failure is active 0 = Link Misconnect Failure is inactive |
| 4-0 | 0 | Link ID | This field contains the Receive Link ID assigned to this facility. Range: 0x00-0x1F |

2.6.11 IMA_RX_LNK n _IV_CNT (IMA Violation Counter Register)

This **read-only** register contains a count of the IV-IMA Anomalies for the Receive link.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x8B0 |
| 1 | 0x8B1 |
| 2 | 0x8B2 |
| 3 | 0x8B3 |
| 4 | 0x8B4 |
| 5 | 0x8B5 |
| 6 | 0x8B6 |
| 7 | 0x8B7 |
| 8 | 0x9B0 |
| 9 | 0x9B1 |
| 10 | 0x9B2 |
| 11 | 0x9B3 |
| 12 | 0x9B4 |
| 13 | 0x9B5 |
| 14 | 0x9B6 |
| 15 | 0x9B7 |

| n | Address |
|----|---------|
| 16 | 0xAB0 |
| 17 | 0xAB1 |
| 18 | 0xAB2 |
| 19 | 0xAB3 |
| 20 | 0xAB4 |
| 21 | 0xAB5 |
| 22 | 0xAB6 |
| 23 | 0xAB7 |
| 24 | 0xBB0 |
| 25 | 0xBB1 |
| 26 | 0xBB2 |
| 27 | 0xBB3 |
| 28 | 0xBB4 |
| 29 | 0xBB5 |
| 30 | 0xBB6 |
| 31 | 0xBB7 |

| Bit | Default | Name | Description |
|-----|---------|----------------|--|
| 7-0 | — | IV-IMA Counter | This field contains a count of the ICP-ERR, ICP-INV, and ICP-MIS anomalies. Writing a 0x01 to address 0x8B0 will freeze the value of all the IV-IMA and OIF-IMA counters in the defined registers. The internal counters are cleared by this action. After all the registers have been read, writing a 0x00 to address 0x8B0 will release the “freeze” and the defined registers will reflect the current anomaly count. |

2.6.12 IMA_RX_LNK n _OIF_CNT (Out-of-IMA Frame Counter Register)

This **read-only** register contains a count of the OIF-IMA Anomalies for the Receive link.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x8B8 |
| 1 | 0x8B9 |
| 2 | 0x8BA |
| 3 | 0x8BB |
| 4 | 0x8BC |
| 5 | 0x8BD |
| 6 | 0x8BE |
| 7 | 0x8BF |
| 8 | 0x9B8 |
| 9 | 0x9B9 |
| 10 | 0x9BA |
| 11 | 0x9BB |
| 12 | 0x9BC |
| 13 | 0x9BD |
| 14 | 0x9BE |
| 15 | 0x9BF |

| n | Address |
|----|---------|
| 16 | 0xAB8 |
| 17 | 0xAB9 |
| 18 | 0xABA |
| 19 | 0xABB |
| 20 | 0xABC |
| 21 | 0xABD |
| 22 | 0xABE |
| 23 | 0xABF |
| 24 | 0xBB8 |
| 25 | 0xBB9 |
| 26 | 0xBBA |
| 27 | 0xBBB |
| 28 | 0xBBC |
| 29 | 0xBBD |
| 30 | 0xBBE |
| 31 | 0xBBF |

| Bit | Default | Name | Description |
|-----|---------|-----------------|--|
| 7 | — | — | Reserved. |
| 6 | — | — | Reserved. |
| 5 | — | — | Reserved. |
| 4 | — | — | Reserved. |
| 3-0 | — | OIF-IMA Counter | This field contains a count of the OIF anomalies. Writing a 0x01 to address 0x8B0 will freeze the value of all the IV-IMA and OIF-IMA counters in the defined registers. The internal counters are cleared by this action. After all the registers have been read, writing a 0x00 to address 0x8B0 will release the “freeze” and the defined registers will reflect the current anomaly count. |

2.6.13 IMA_FE_TX_LNK n _GRP_ID (FE Transmit Group ID Register)

This **read-only** register contains the value of the IMA ID field acquired from the received ICP for the Receive link.

Hex Address

| n | Address |
|----|---------|
| 0 | 0x8C0 |
| 1 | 0x8C1 |
| 2 | 0x8C2 |
| 3 | 0x8C3 |
| 4 | 0x8C4 |
| 5 | 0x8C5 |
| 6 | 0x8C6 |
| 7 | 0x8C7 |
| 8 | 0x9C0 |
| 9 | 0x9C1 |
| 10 | 0x9C2 |
| 11 | 0x9C3 |
| 12 | 0x9C4 |
| 13 | 0x9C5 |
| 14 | 0x9C6 |
| 15 | 0x9C7 |

| n | Address |
|----|---------|
| 16 | 0xAC0 |
| 17 | 0xAC1 |
| 18 | 0xAC2 |
| 19 | 0xAC3 |
| 20 | 0xAC4 |
| 21 | 0xAC5 |
| 22 | 0xAC6 |
| 23 | 0xAC7 |
| 24 | 0xBC0 |
| 25 | 0xBC1 |
| 26 | 0xBC2 |
| 27 | 0xBC3 |
| 28 | 0xBC4 |
| 29 | 0xBC5 |
| 30 | 0xBC6 |
| 31 | 0xBC7 |

| Bit | Default | Name | Description |
|-----|---------|--------------------|--|
| 7-0 | — | Actual Rx Group ID | This field contains the value of the Group ID field from the ICP cells for this facility. Range: 0x00-0xFF |

NOTE: The value in this register is undefined when there is no valid IMA cell stream present on the link. The value in this register is also undefined for a maximum of two seconds following the creation of a group containing this link.

2.7 ATM Cell Capture Registers

The ATM Cell Capture registers allow an ATM cell to be captured from a facility for diagnostic purposes.

NOTE:

When a facility is configured to be part of an IMA Group, a valid cell stream must be present on the input port or the values contained in these registers are undefined. The values in these registers are also undefined for a maximum of two seconds following the creation of a group containing the specified facility in 0xE30. If the facility is configured for passthrough mode, the above restrictions do not apply.

2.7.1 0xE00-0xE2F—CELL_CAP_PAYLD n (Capture Payload Contents Register)

These registers hold the 48 byte payload contents of a captured ATM Cell. These registers are **read-only**.

| Bit | Default | Name | Description |
|-----|---------|------------|--|
| 7-0 | 0 | ATMPLD n | Contains one byte of the 48 byte payload contents of a captured ATM Cell. The first byte is stored in register 0xE00 and the remainder of the 48 bytes are stored consecutively in registers up to location 0xE2F. |

2.7.2 0xE30—CAP_FAC (Capture Facility Register)

The capture facility register configures the facility that the ATM cells will be captured from.

| Bit | Default | Name | Description |
|-----|---------|--------|--|
| 7-5 | — | — | Reserved |
| 4-0 | 0 | CAPFCL | This field is programmed with the facility that ATM cells will be captured from. |

2.7.3 0xE31—CAP_CNTL (Capture Control Register)

The capture control register enables the capture circuit to store an incoming ATM cell as well as determine the type of ATM cell stored

| Bit | Default | Name | Description |
|-----|---------|---------|---|
| 7-2 | — | — | Reserved |
| 1 | 0 | CAPTYPE | This bit selects whether the next incoming ICP cell is stored or simply the next ATM cell, regardless of type, is stored. 0 = ICP Cell only 1 = Any cell (Data Cell, Filler Cell, or ICP/SICP Cell) |
| 0 | 0 | ENCAP | Enables the capture circuit to store the next incoming cell qualified by the cell type programmed in bit 1. This bit is written to a '1' to arm the capture circuit to store the ATM cell. This bit is should be written to a '0' once the ATM cell is captured. See register 0xE32 for the capture status. |

2.7.4 0xE32—CAP_STAT (Capture Status Register)

The capture status register indicates the status of the ATM cell capture.

| Bit | Default | Name | Description |
|-----|---------|---------|--|
| 7-1 | | — | Reserved |
| 0 | 0 | CELLCAP | This bit shows whether an ATM cell has been captured. This status bit is only valid when the Capture Control bit is enabled. 1 = Cell has been stored 0 = Cell has not been stored |



3.0 Product Specification

3.1 Absolute Maximum Ratings

The absolute maximum ratings in Table 3-1 indicate the maximum stresses that the M2852x can tolerate without risking permanent damage. These ratings are not typical of normal operation of the device. Exposure to absolute maximum rating conditions for extended periods of time may affect the device's reliability. This device should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

Table 3-1. Absolute Maximum Ratings (General)

| Parameter | Value |
|--|-------------------------|
| Supply Voltage - VDD33 | -0.5 to +3.6 V |
| Supply Voltage - VDD18 | -0.5 to +1.98 V |
| ESD Voltage (VGG) | -0.5 to +5.5 V |
| Input Voltage | -0.5 to (VDD33 + 1.89V) |
| Storage Temperature | -40 °C to 125 °C |
| Operating Temperature Range | -40 °C to 85 °C |
| Lead Temperature | +240 °C for 10 seconds |
| Junction Temperature | +125 °C |
| Static Discharge Voltage (Human Body Model) | ±2000 V |
| Static Discharge Voltage (Charge Device Model) | ±350 V |
| Latch-up Current | ±150 mA at 85 °C |
| DC Input Current | ±20 mA |
| NOTE: Please refer to Mindspeed SMT application note for the Pb-free devices and for the detail explanation of how JEDEC determines the reflow temperatures based on package thickness: http://mindspeed.com/mspd/support/quality/SMT-PB-free.pdf | |

Table 3-2. Absolute Maximum Ratings (M28525/M28529)

| Parameter | Value |
|--------------------------|---------|
| θ_{JA} No Airflow | ~20°C/W |

3.2 Recommended Operating Conditions

Table 3-3. Recommended Operating Conditions

| Symbol | Parameter | Minimum | Nominal | Maximum | Units |
|--------|-------------------------------|---------|---------|---------|-------|
| VDD33 | 3.3V Power supply | 3.135 | 3.3 | 3.465 | V |
| VDD18 | 1.8V Power supply | 1.71 | 1.8 | 1.89 | V |
| Tamb | Ambient operating temperature | -40 | 25 | 85 | °C |

3.3 DC Characteristics

Table 3-4 lists the DC characteristics of the M2852x. Table 3-5 lists Power Characteristics of the device.

Table 3-4. DC Characteristics

| Parameter | Minimum | Typical | Maximum | Comments |
|--|---------|----------------------|---------|---|
| Power Supply VDD33 | 3.0 | 3.3 | 3.6 | VDC $\pm 10\%$ |
| Power Supply VDD18 | 1.71 | 1.8 | 1.89 | VDC $\pm 5\%$ |
| ESD Voltage VGG (3.3 V or 5 V) ^(1,2) | 3.0 | 3.3/5 ⁽³⁾ | 5.5 | VDC |
| Input Low Voltage (VIL)—TTL | 0 | — | 0.8 | VDC |
| Input High Voltage (VIH)—TTL | 2.0 | — | 5.25 | VDC |
| Output Voltage Low (TTL) | — | — | 0.4 | Volts; $I_{OH} = 4.0 \text{ mA}$ |
| Output Voltage High (TTL) | 2.4 | — | — | Volts; $I_{OH} = 1500 \mu\text{A}$ |
| Input Leakage Current | -10 | — | 10 | μA ; $V_{in} = \text{PWR or GND}$ |
| Three-state Output Leakage Current | -10 | — | 10 | μA ; $V_{out} = \text{PWR or GND}$ |
| Input Capacitance | — | — | 7 | pF |
| Output Capacitance | — | — | 7 | pF |
| Bidirectional Capacitance | — | — | 7 | pF |
| Footnote: (1) With 5 V logic input, VGG should be tied to 5 V. With 3.3 V logic input, VGG should be tied to 3.3 V. VGG must be equal or greater than power supply voltage. (2) When VGG is operated at 5 V, sequence VGG to VDD33 as discussed in Chapter 4.0 . (3) Typical value for VGG is 3.3 or 5 V. | | | | |

Table 3-5. Power Characteristics (M28529)

| Conditions | Parameter | Minimum | Typical | Maximum | Comments |
|--|-----------|---------|---------|---------|----------|
| E1 Utopia-Serial IMA_SysClk = 49.152MHz IMA_RefClk = 49.152MHz MicroClk = 25MHz 8 IMA Groups with 4 Links each | VDD33 | — | 100 | — | mW |
| | VDD18 | — | 290 | — | mW |
| T1 Utopia-Serial IMA_SysClk = 37.056MHz IMA_RefClk = 49.152MHz MicroClk = 25MHz 8 IMA Groups with 4 Links each | VDD33 | — | 100 | — | mW |
| | VDD18 | — | 240 | — | mW |
| Interleaved Highway Utopia-Serial IMA_SysClk = 49.152MHz IMA_RefClk = 49.152MHz MicroClk = 25MHz 8 IMA Groups with 4 Links each | VDD33 | — | 100 | — | mW |
| | VDD18 | — | 355 | — | mW |
| E1 Utopia-Utopia IMA_SysClk = 49.152MHz IMA_RefClk = 49.152MHz MicroClk = 25MHz 8 IMA Groups with 4 Links each | VDD33 | — | 200 | — | mW |
| | VDD18 | — | 260 | — | mW |
| DSL 2.304Mbs Utopia-Utopia IMA_SysClk = 66MHz IMA_RefClk = 49.152MHz MicroClk = 66MHz 8 IMA Groups with 4 Links each | VDD33 | — | 235 | — | mW |
| | VDD18 | — | 410 | — | mW |
| DSL 5.4Mbs Utopia-Utopia IMA_SysClk = 66MHz IMA_RefClk = 49.152MHz MicroClk = 66MHz 8 IMA Groups with 4 Links each | VDD33 | — | 300 | — | mW |
| | VDD18 | — | 425 | — | mW |

3.4 Timing Specifications

This section provides timing diagrams and descriptions for the various interfaces of the M2852x. The timing relationship labels are numbered when they occur more than once in a diagram, so each label is unique. This numbering aids in identifying the appropriate label in the timing table. Signals are measured at the 50% point of the changing edge, except for those involving high impedance transitions, which are measured at 10% and 90%.

Figure 3-1 and Figure 3-2 illustrate how input and output waveforms are defined.

Figure 3-1. Input Waveform

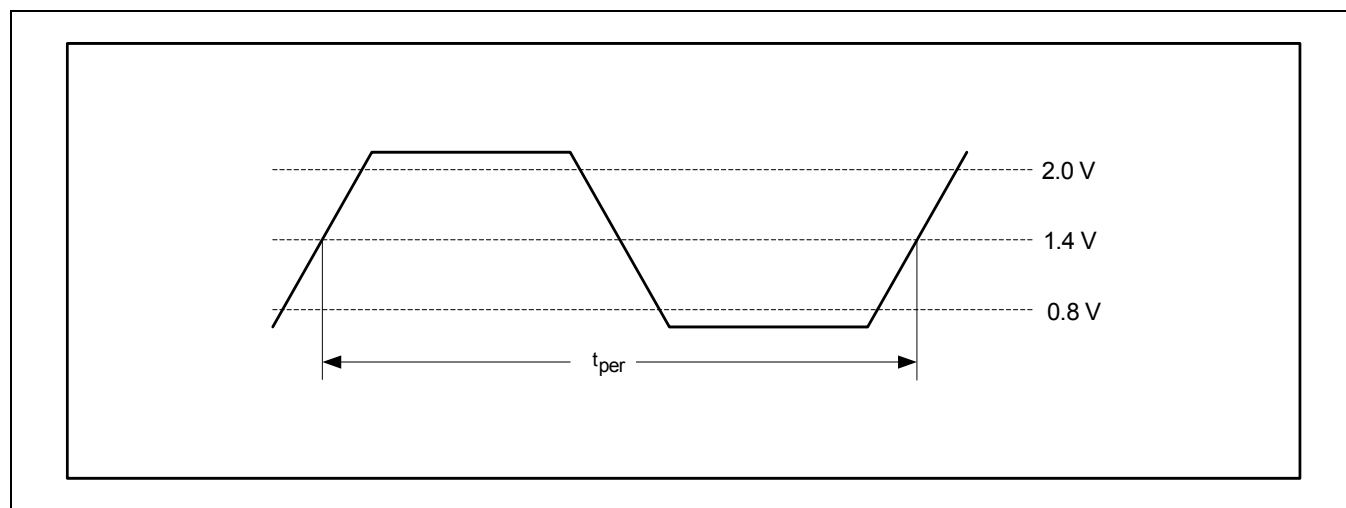
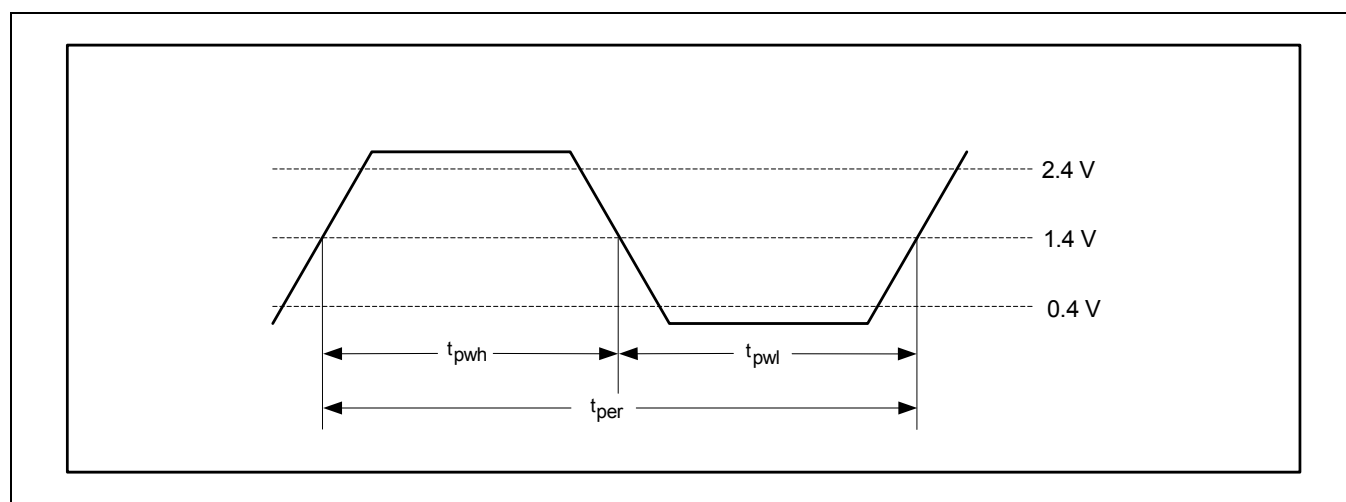


Figure 3-2. Output Waveform



3.4.1 Reset Timing

Figure 3-3 and Table 3-6 show the timing requirements for the asynchronous reset input to the device.

Figure 3-3. Reset Timing

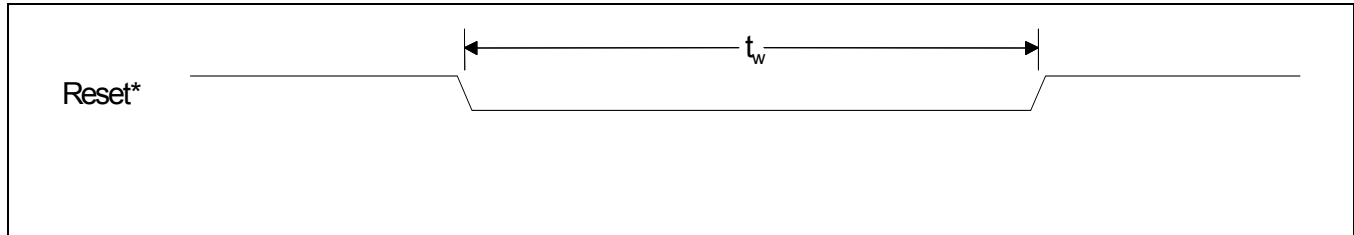


Table 3-6. Reset Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|--------|---------------------------|---------|---------|---------|-------|
| t_w | Reset minimum pulse width | 100 | | | ns |

3.4.2 Microprocessor Timing

Figures 3-4 through 3-7 and Tables 3-7 through 3-10 show the timing requirements and characteristics of the microprocessor interface. Capacitive load on all signals is 50pF.

Figure 3-4. Microprocessor Timing —Asynchronous Read

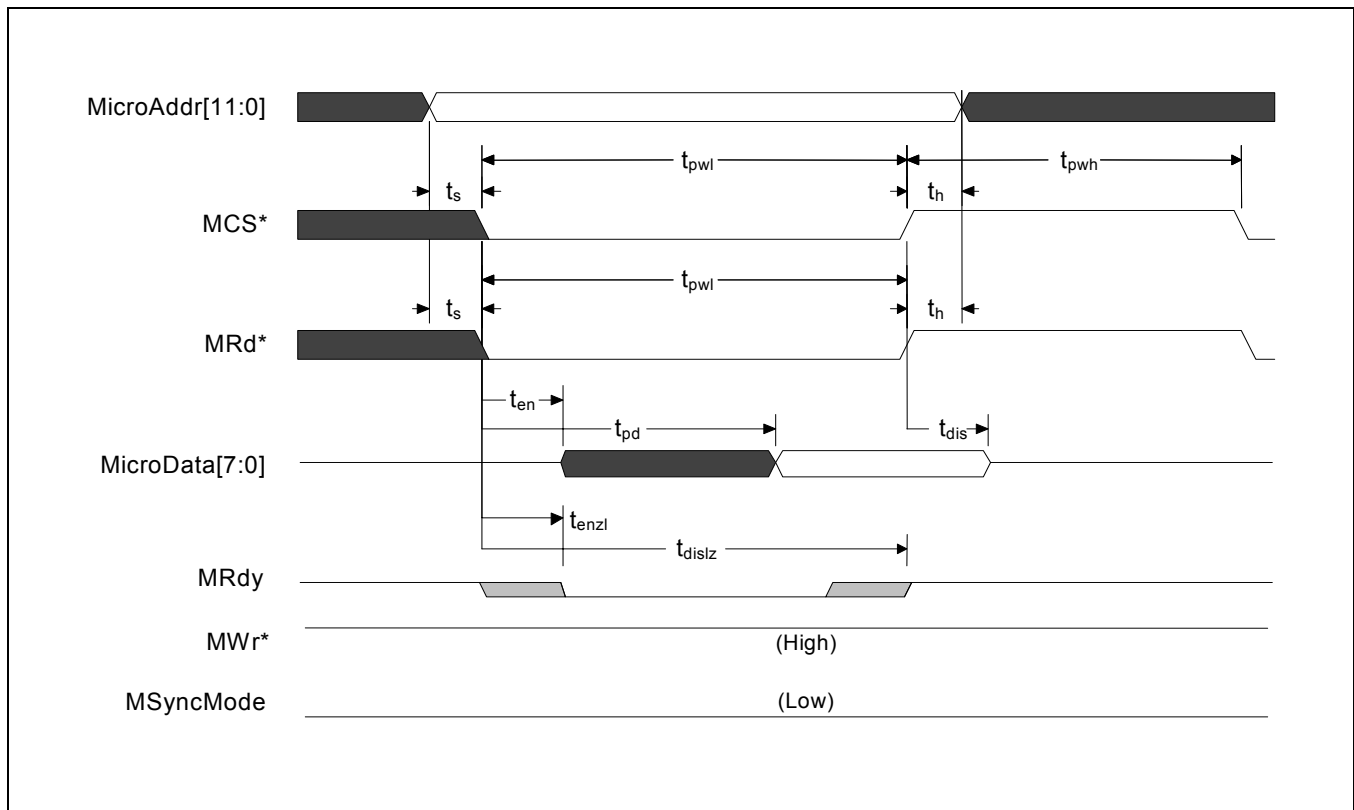


Table 3-7. Microprocessor Timing Parameters - Asynchronous Read

| Label | Description | Minium | Maximum | Units |
|-------------|---|---------------|--------------------|-------|
| t_{per} | Microprocessor Clock ⁽¹⁾ | 15 | | ns |
| t_{pwh} | Pulse Width High | $4 * t_{per}$ | — | ns |
| t_{pwl} | Pulse Width Low | $4 * t_{per}$ | — | ns |
| t_s | Setup, MicroAddr[11:0] to the falling edge of (MCS* + MRd*) ⁽²⁾ | 2 | — | ns |
| t_h | Hold, MicroAddr[11:0] from the rising edge of (MCS* + MRd*) ⁽³⁾ | 7 | — | ns |
| t_{en} | Enable, MicroData[7:0] from the falling edge of (MCS* + MRd*) ⁽²⁾ | 4 | 10 | ns |
| t_{pd} | Propagation Delay, MicroData[7:0] from the falling edge of (MCS* + MRd*) ⁽²⁾ | $2 * t_{per}$ | $3 * t_{per} + 10$ | ns |
| t_{dis} | Disable, MicroData[7:0] from the rising edge of (MCS* + MRd*) ⁽³⁾ | 4 | 10 | ns |
| t_{enzl} | Enable, MRdy from the falling edge of (MCS* + MRd*) ⁽²⁾ | 4 | 10 | ns |
| t_{dislz} | Disable, MRdy from the falling edge of (MCS* + MRd*) ⁽²⁾ | $3 * t_{per}$ | $4 * t_{per} + 10$ | ns |

Footnote:
 (1) The microprocessor clock is required by internal logic but has no relationship with the I/O signals.
 (2) Timing starts from whichever is asserted last.
 (3) Timing relative to whichever goes inactive first.
 (4) Timing relative to a 50pF load.

Figure 3-5. Microprocessor Timing —Asynchronous Write

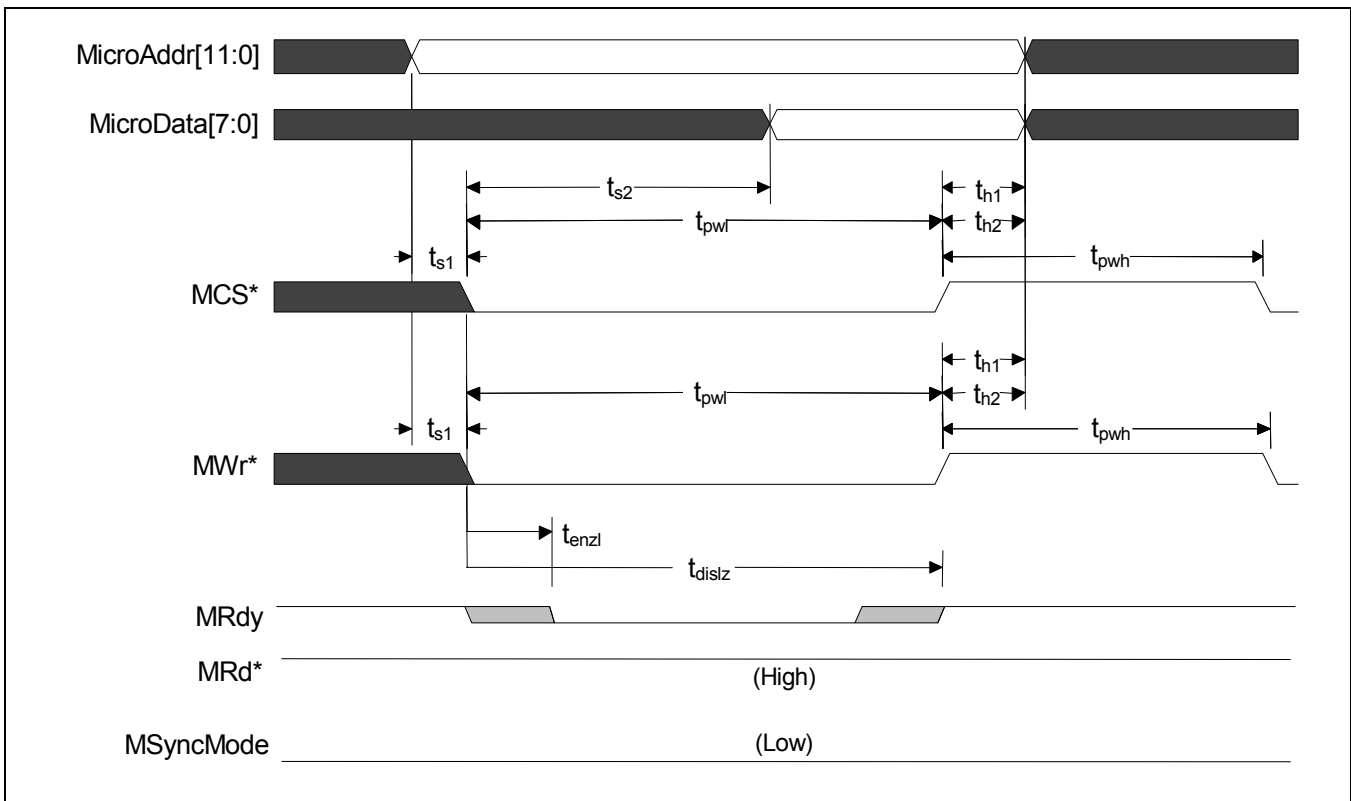


Table 3-8. Microprocessor Timing Parameters - Asynchronous Write

| Label | Description | Minimum | Maximum | Units |
|-------------|---|---------------|--------------------|-------|
| t_{per} | Microprocessor Clock ⁽¹⁾ | 15 | | ns |
| t_{pwl} | Pulse Width Low (MCS* + MWR*) | $4 * t_{per}$ | — | ns |
| t_{pwh} | Pulse Width High (MCS* + MWR*) | $4 * t_{per}$ | — | ns |
| t_{s1} | Setup, MicroAddr[11:0] to the falling edge of (MCS* + MWR*) ⁽²⁾ | 2 | — | ns |
| t_{h1} | Hold, MicroAddr[11:0] from the rising edge of (MCS* + MWR*) ⁽³⁾ | 7 | — | ns |
| t_{s2} | Setup, MicroData[7:0] from the falling edge of (MCS* + MWR*) ⁽²⁾ | — | t_{per} | ns |
| t_{h2} | Hold, MicroData[6:0] from the rising edge of (MCS* + MWR*) ⁽³⁾ | 7 | — | ns |
| t_{enzl} | Enable, MRdy from the falling edge of (MCS* + MWR*) ⁽²⁾ | 4 | 10 | ns |
| t_{dislz} | Disable, MRdy from the falling edge of (MCS* + MWR*) ⁽²⁾ | $3 * t_{per}$ | $4 * t_{per} + 10$ | ns |

Footnote:

- (1) The microprocessor clock is required by internal logic but has no relationship with the I/O signals.
- (2) Timing starts from whichever is asserted last.
- (3) Timing relative to whichever goes inactive first.
- (4) Timing relative to a 50pF load.

Figure 3-6. Microprocessor Timing —Synchronous Read

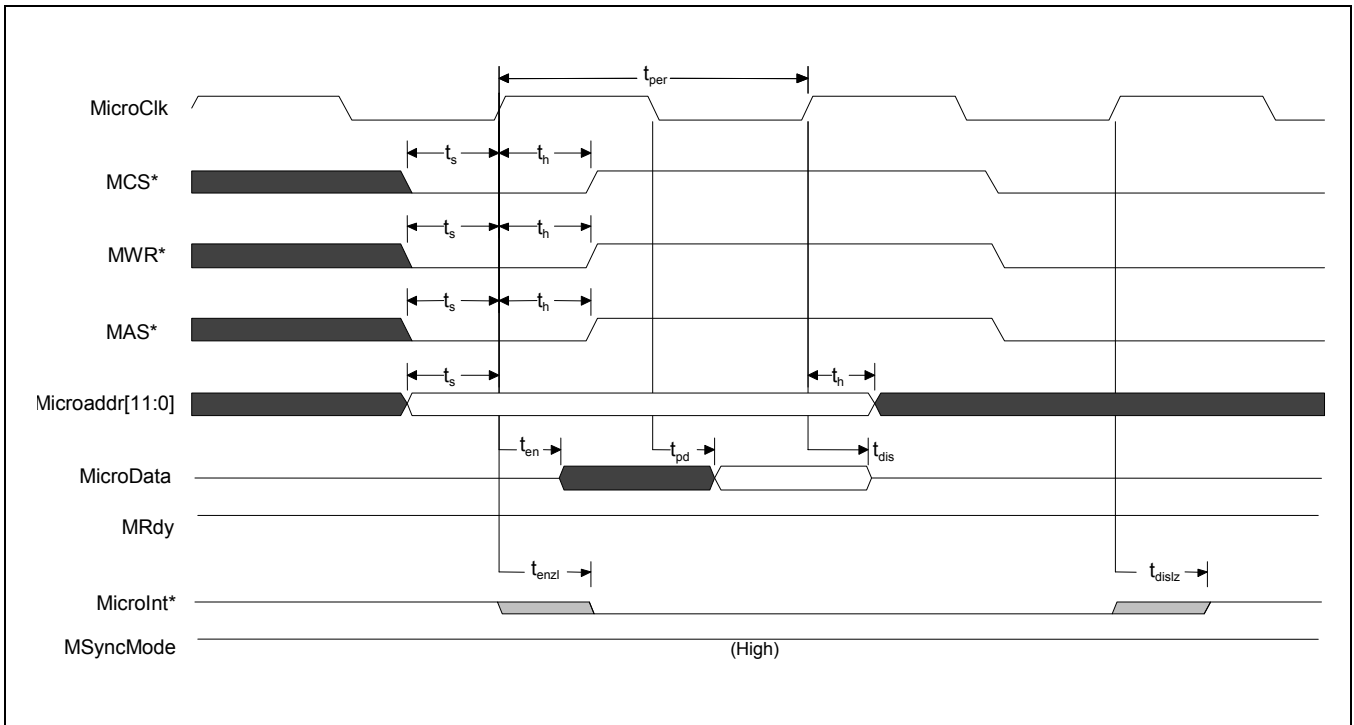


Table 3-9. Microprocessor Timing Parameters - Synchronous Read

| Label | Description | Minimum | Maximum | Units |
|-------------|---|---------|---------|-------|
| t_{per} | Microprocessor Clock Period | 40 | | ns |
| t_{duty} | Microprocessor Clock Period Duty Cycle | 40 | 60 | % |
| t_s | Setup to the rising edge of MicroClk | 5 | — | ns |
| t_h | Hold from the rising edge of MicroClk | 2 | — | ns |
| t_{en} | Enable from the rising edge of MicroClk | 2 | 15 | ns |
| t_{pd} | Propagation Delay from the rising edge of MicroClk | 2 | 26 | ns |
| t_{dis} | Propagation Delay from the falling edge of MicroClk | 2 | 15 | ns |
| t_{enzl} | Enable from the rising edge of MicroClk | 2 | 15 | ns |
| t_{dislz} | Disable from the rising edge of MicroClk | 2 | 15 | ns |

Footnote:
 (1) Timing relative to a 50pF Load

Figure 3-7. Microprocessor Timing —Synchronous Write

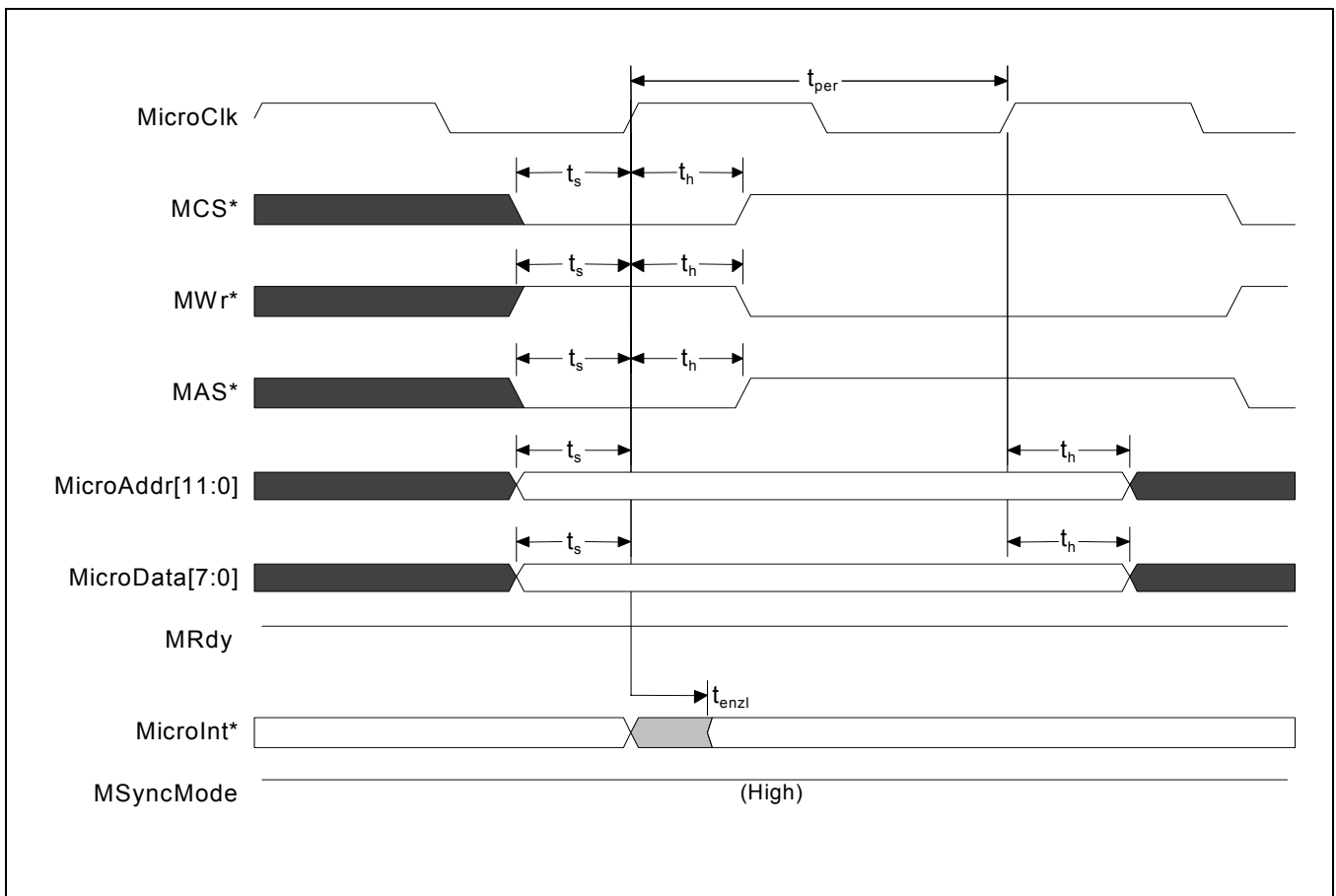


Table 3-10. Microprocessor Timing Parameters - Synchronous Write

| Label | Description | Minimum | Maximum | Units |
|------------|---|---------|---------|-------|
| t_{per} | Microprocessor clock period | 40 | | ns |
| t_{duty} | Microprocessor Clock Period Duty Cycle | 40 | 60 | % |
| t_s | Setup to the rising edge of MicroClk | 5 | — | ns |
| t_h | Hold from the rising edge of MicroClk | 2 | — | ns |
| t_{enzl} | Enable from the rising edge of MicroClk | 2 | 15 | ns |

Footnote:
 (1) Timing relative to a 50pF load

3.4.3 PHY-side Interface Timing (Serial Mode)

The PHY-side interface on the MaxIMA supports three different modes of operation, serial, interleaved and UTOPIA. Figure 3-8 through 3-13 show the timing diagrams for T1/E1/DSL mode. Table 3-11 and Table 3-12 show the PHY-side timing requirements for T1/E1/DSL mode.

Figure 3-8. PHY-side Serial T1/E1/DSL Mode Transmit Timing (TxClkPol = 0, TxDatShft = 0)

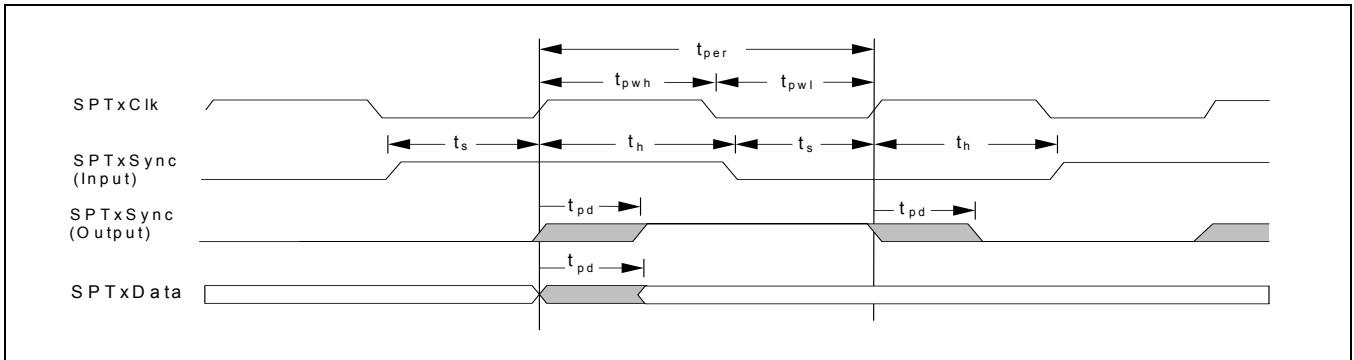


Figure 3-9. PHY-Side Serial T1/E1/DSL Mode Transmit Timing (TxClkPol = 1, TxDatShft = 0)

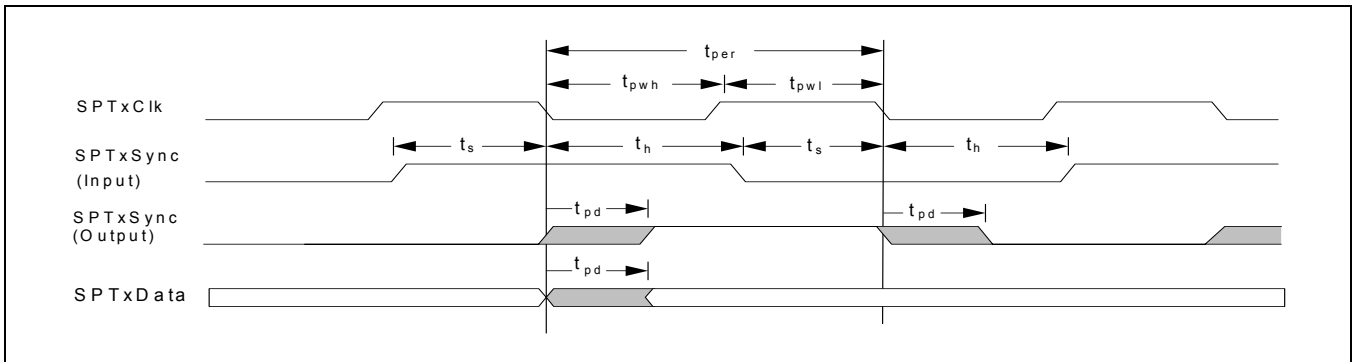


Figure 3-10. PHY-Side Serial T1/E1/DSL Mode Transmit Timing (TxClkPol = 0, TxDatShft = 1)

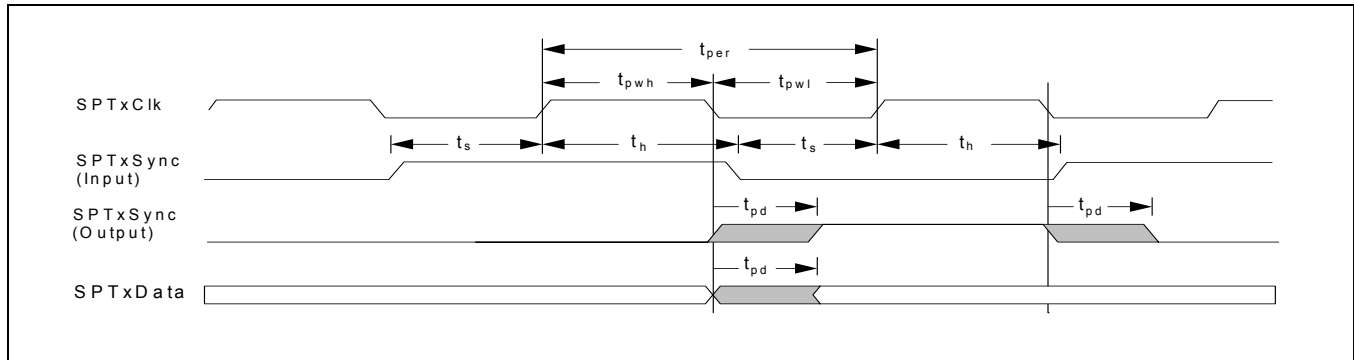


Figure 3-11. PHY-Side Serial T1/E1/DSL Mode Transmit Timing (TxClkPol = 1, TxDatShft = 1)

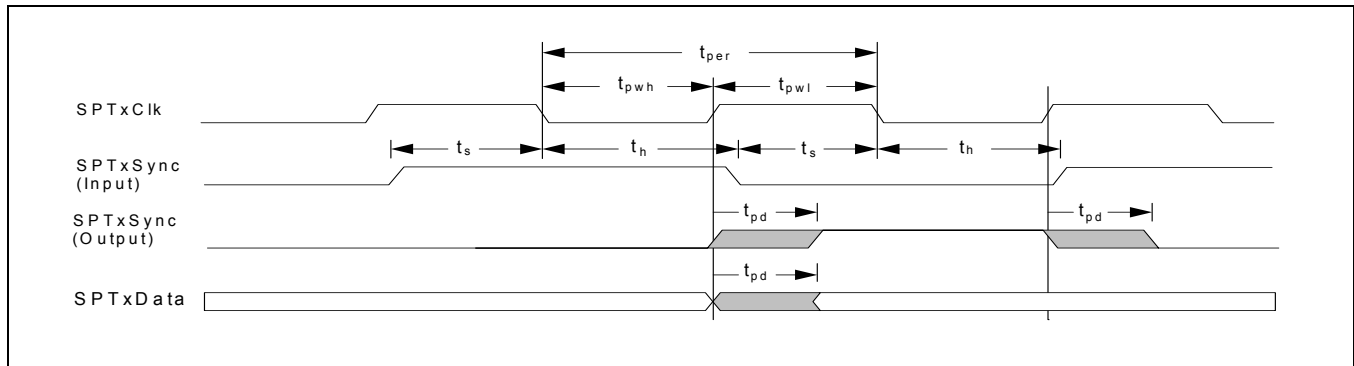


Table 3-11. PHY-side Serial T1/E1/DSL Mode Transmit Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|-----------|---|---------|---------|---------|-------|
| t_{per} | Serial transmit clock period | 50 | | | ns |
| t_{pwh} | Serial clock pulse width (high) | 20 | | | ns |
| t_{pwl} | Serial clock pulse width (low) | 20 | | | ns |
| t_s | Setup to sptxclk rise(fall) ⁽¹⁾ edge | 5 | | | ns |
| t_h | Hold from sptxclk rise(fall) ⁽¹⁾ edge | 3 | | | ns |
| t_{pd} | Delay from sptxclk rise(fall) ⁽¹⁾ edge | 1 | | 20 | ns |

Footnote:

(1) Timing synchronized to falling edge when TxClkPol = 1

General Note:

1. The TxClkPol (bit 3) in the IOMODE register determines whether timing is referenced to the positive or negative clock edge.
2. All outputs are assumed to have 20 pF loading.

Figure 3-12. PHY-side Serial T1/E1/DSL Mode Receive Timing (Positive Clock Edge Timing- RxClkPol = 0)

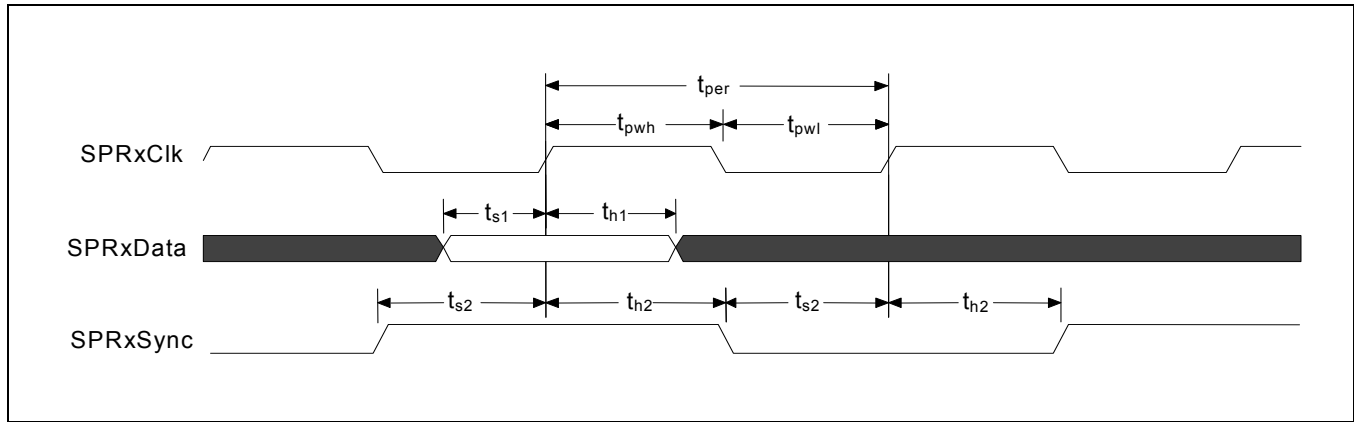


Figure 3-13. PHY-side Serial T1/E1/DSL Mode Receive Timing (Negative Clock Edge Timing- RxClkPol = 1)

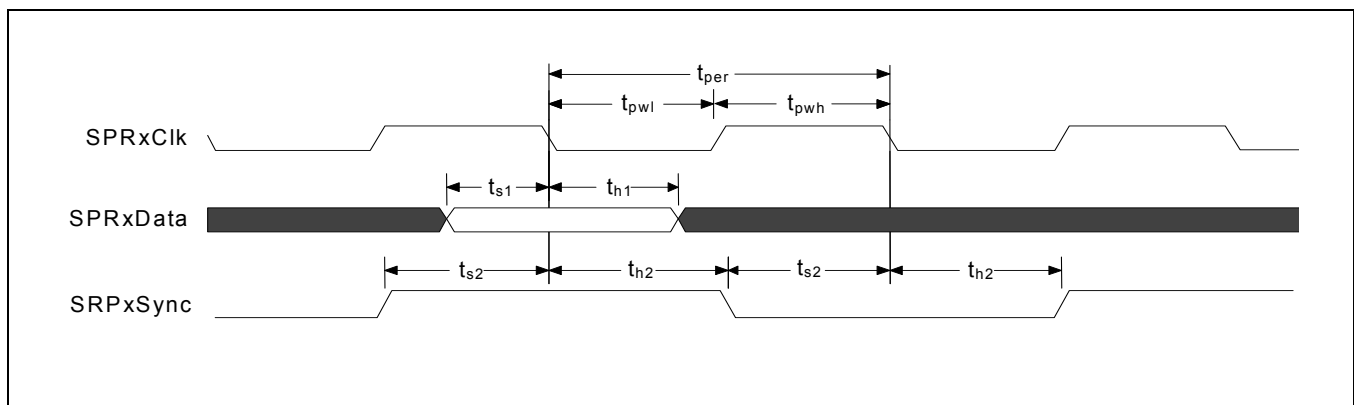


Table 3-12. PHY-side Serial T1/E1/DSL Mode Receive Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|-----------|--|---------|---------|---------|-------|
| t_{per} | Serial receive clock period | 50 | | | ns |
| t_{pwh} | Serial receive clock pulse width (high) | 20 | | | ns |
| t_{pwl} | Serial receive clock pulse width (low) | 20 | | | ns |
| t_{s1} | Setup to sprxclk rise(fall) ⁽¹⁾ edge | 5 | | | ns |
| t_{h1} | Hold from sprxclk rise(fall) ⁽¹⁾ edge | 3 | | | ns |
| t_{s2} | Setup to sprxclk rise(fall) ⁽¹⁾ edge | 5 | | | ns |
| t_{h2} | Hold from sprxclk rise(fall) ⁽¹⁾ edge | 3 | | | ns |

Footnote:

(1) Timing Synchronized to falling clock edge when RxClkPol = 1

General Note:

1. The RxClkPol (bit 5) in the IOMODE register determines whether timing is synchronized to the positive or negative clock edge.
2. All outputs are assumed to have 20 pF loading.

3.4.4 Fractional T1/E1 Mode Timing

Figure 3-14 and show the PHY-side interface timing when configured for Fractional T1/E1 mode. Table 3-13 and 3-14 show the PHY-side timing requirements for Fractional T1/E1 mode.

Figure 3-14. Fractional T1/E1 Transmit Timing

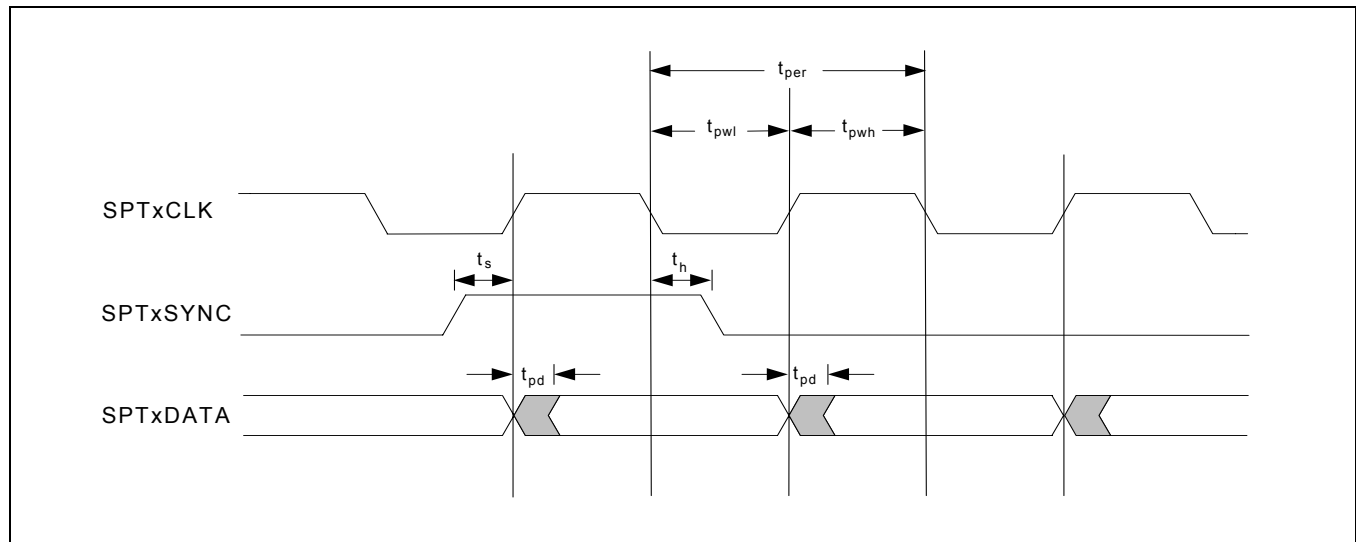


Table 3-13. Fractional T1/E1 Transmit Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|-----------|--|---------|---------|---------|-------|
| t_{per} | Fractional transmit clock period | 50 | | | ns |
| t_{pwh} | Fractional transmit clock pulse width (high) | 20 | | | ns |
| t_{pwl} | Fractional transmit clock pulse width (low) | 20 | | | ns |
| t_s | Set up time to sptxclk rising edge | 5 | | | ns |
| t_h | Hold time from sptxclk falling edge | 5 | | | ns |
| t_{pd} | Delay from sptxclk rising edge | 1 | | 20 | ns |

Figure 3-15. Fractional T1/E1 Receive Timing

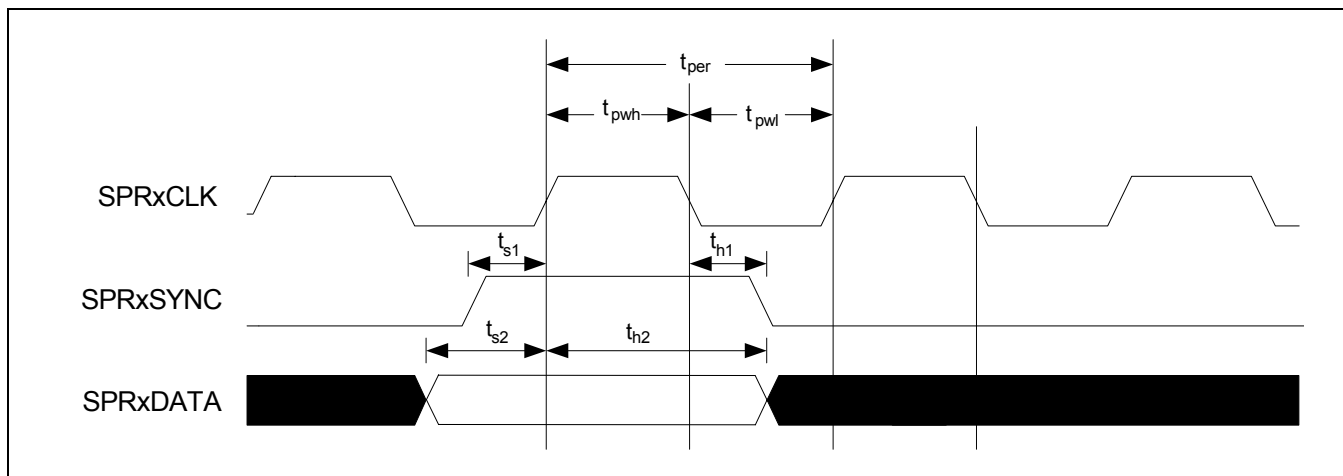


Table 3-14. Fractional T1/E1 Receive Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|-----------|---|---------|---------|---------|-------|
| t_{per} | Serial receive clock period | 50 | | | ns |
| t_{pwh} | Serial receive clock pulse width (high) | 20 | | | ns |
| t_{pwl} | Serial receive clock pulse width (low) | 20 | | | ns |
| t_{s1} | Setup to sprxclk rising edge | | 5 | | ns |
| t_{h1} | Hold from sprxclk falling edge | | 5 | | ns |
| t_{s2} | Setup to sprxclk rising edge | | 10 | | ns |
| t_{h2} | Hold from sprxclk rising edge | | 10 | | ns |

3.4.5 PHY-side Interface Mode (Interleaved Highway)

Figure 3-16 and 3-21 show the PHY-side interface timing when configured for Interleaved Highway mode. Table 3-15 and 3-16 show the PHY-side timing requirements for Interleaved Highway mode.

Figure 3-16. PHY-side Interleaved Highway Mode Transmit Timing (IHTxCIkPolx = 0, IHTxDatShftx = 0)

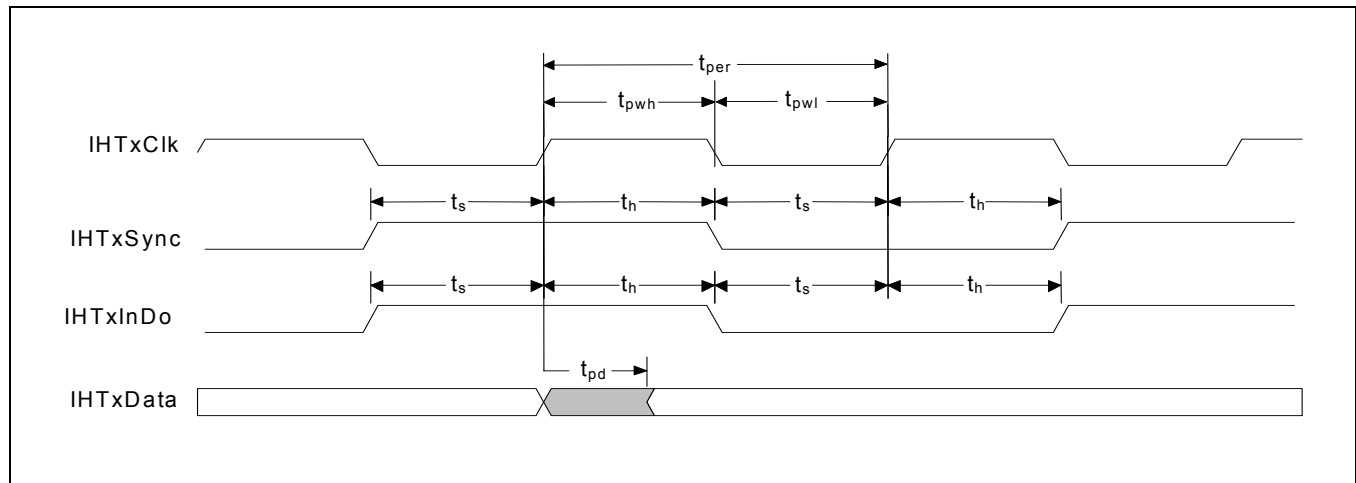


Figure 3-17. PHY-side Interleaved Highway Mode Transmit Timing (IHTxCIkPolx = 1, IHTxDatShftx = 0)

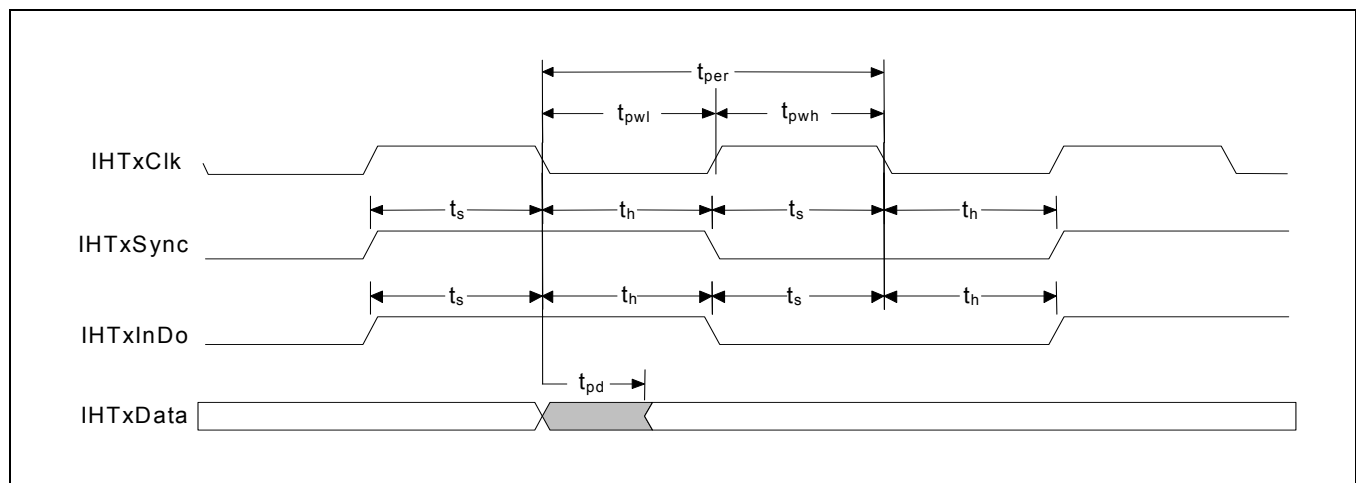


Figure 3-18. PHY-side Interleaved Highway Mode Transmit Timing (IHTxCIkPolx = 0, IHTxDatShftx = 1)

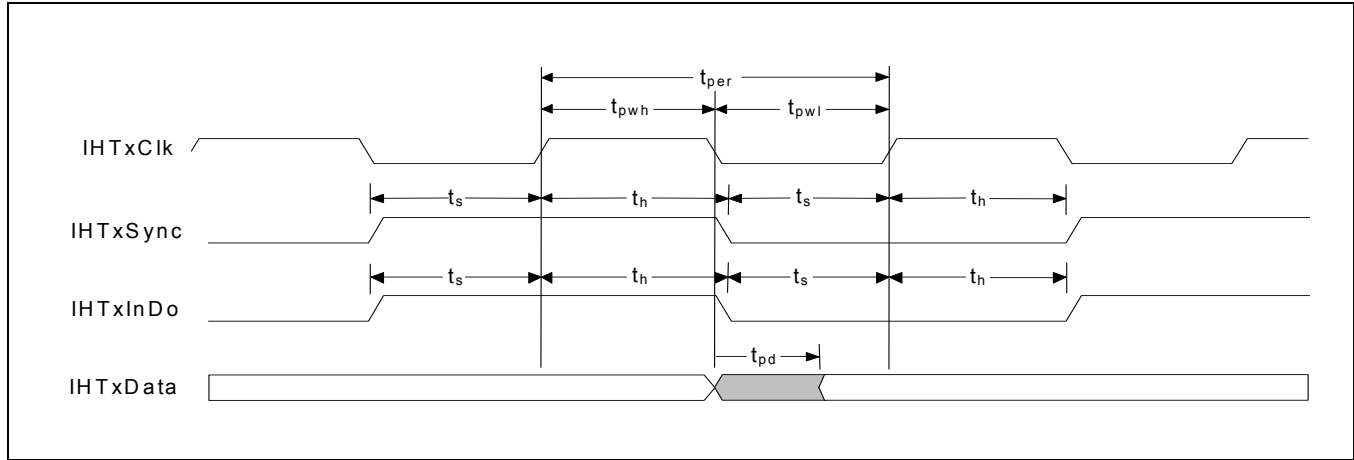


Figure 3-19. PHY-side Interleaved Highway Mode Transmit Timing (IHTxCIkPolx = 1, IHTxDatShftx = 1)

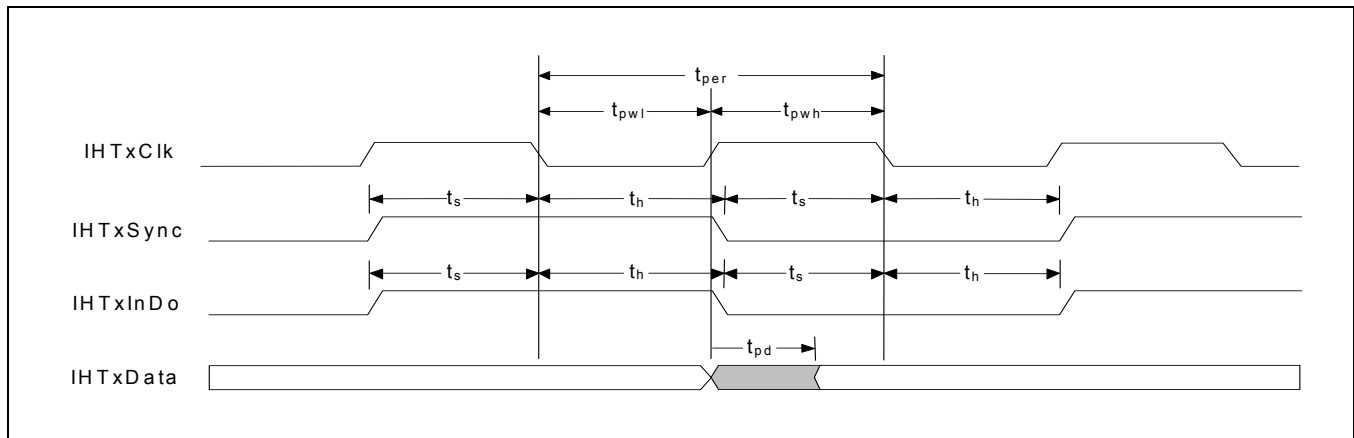


Table 3-15. PHY-side Interleaved Highway Mode Transmit Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|-----------|---|---------|---------|---------|-------|
| t_{per} | IH transmit clock period | 50 | | | ns |
| t_{pwh} | IH transmit clock pulse width (high) | 20 | | | ns |
| t_{pwl} | IH transmit clock pulse width (low) | 20 | | | ns |
| t_s | Setup to ihtxclk rise(fall) ⁽¹⁾ edge | 5 | | | ns |
| t_h | Hold from ihtxclk rise(fall) ⁽¹⁾ edge | 3 | | | ns |
| t_{pd} | Delay from ihtxclk rise(fall) ⁽¹⁾ edge | 2 | | 20 | ns |

Footnote:

(1) Timing synchronized to falling clock edge when IHTxCIkPolx = 1

General Note:

1. All outputs are assumed to have 20 pF loading.

Figure 3-20. PHY-side Interleaved Highway Mode Receive Timing (Positive Edge - IHRxCIkPolx = 0)

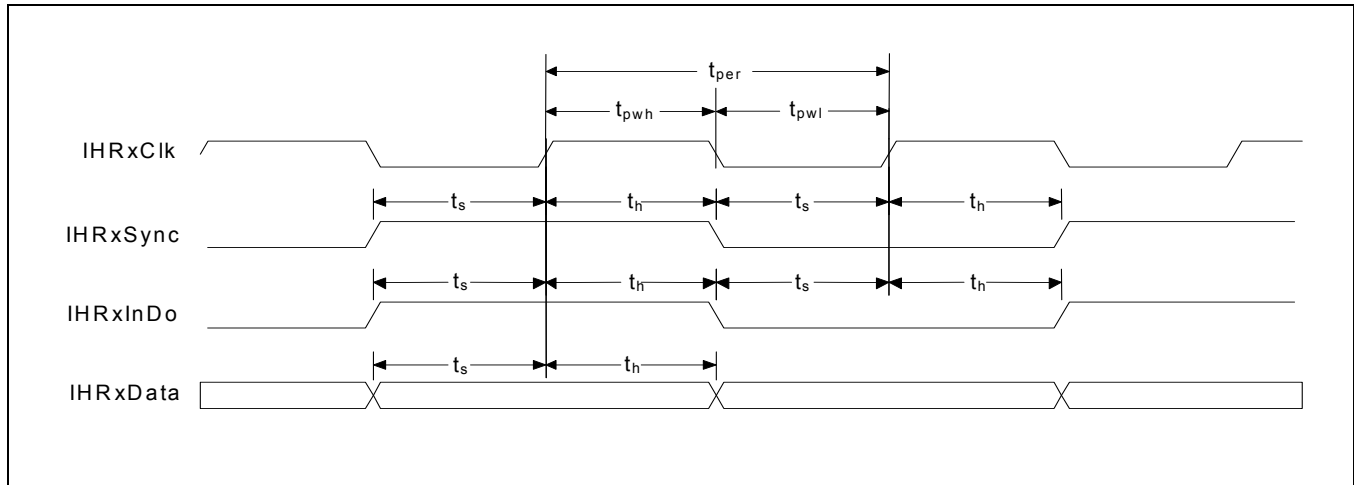


Figure 3-21. PHY-side Interleaved Highway Mode Receive Timing (Negative Edge - IHRxCIkPolx = 1)

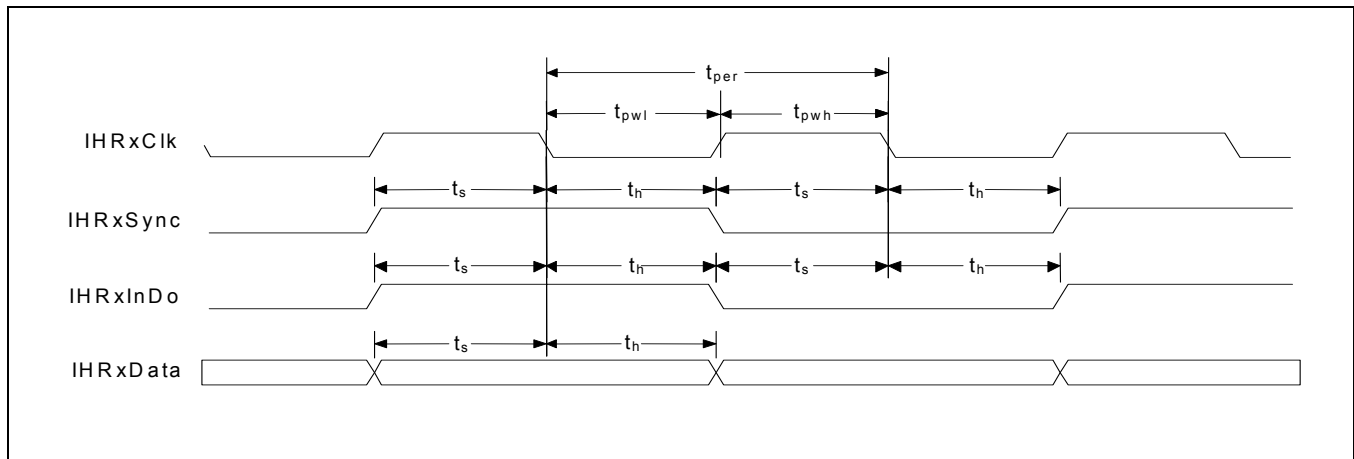


Table 3-16. PHY-side Interleaved Highway Mode Receive Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|-----------|--|---------|---------|---------|-------|
| t_{per} | IH receive clock period | 50 | | | ns |
| t_{pwh} | IH receive clock pulse width (high) | 20 | | | ns |
| t_{pwl} | IH receive clock pulse width (low) | 20 | | | ns |
| t_s | Setup to ihrxclk rise(fall) ⁽¹⁾ edge | 5 | | | ns |
| t_h | Hold from ihrxclk rise(fall) ⁽¹⁾ edge | 3 | | | ns |

Footnote:

(1) Timing synchronized with falling clock edge when RxClkPolx = 1

General Note:

1. All outputs are assumed to have 20 pF loading.

3.4.6 PHY-Side Interface Timing (UTOPIA)

Figures 3-22 through 3-23 and Tables 3-17 through 3-18 show the timing requirements and characteristics of the PHY-side UTOPIA interface.

Figure 3-22. PHY-side UTOPIA Transmit Timing

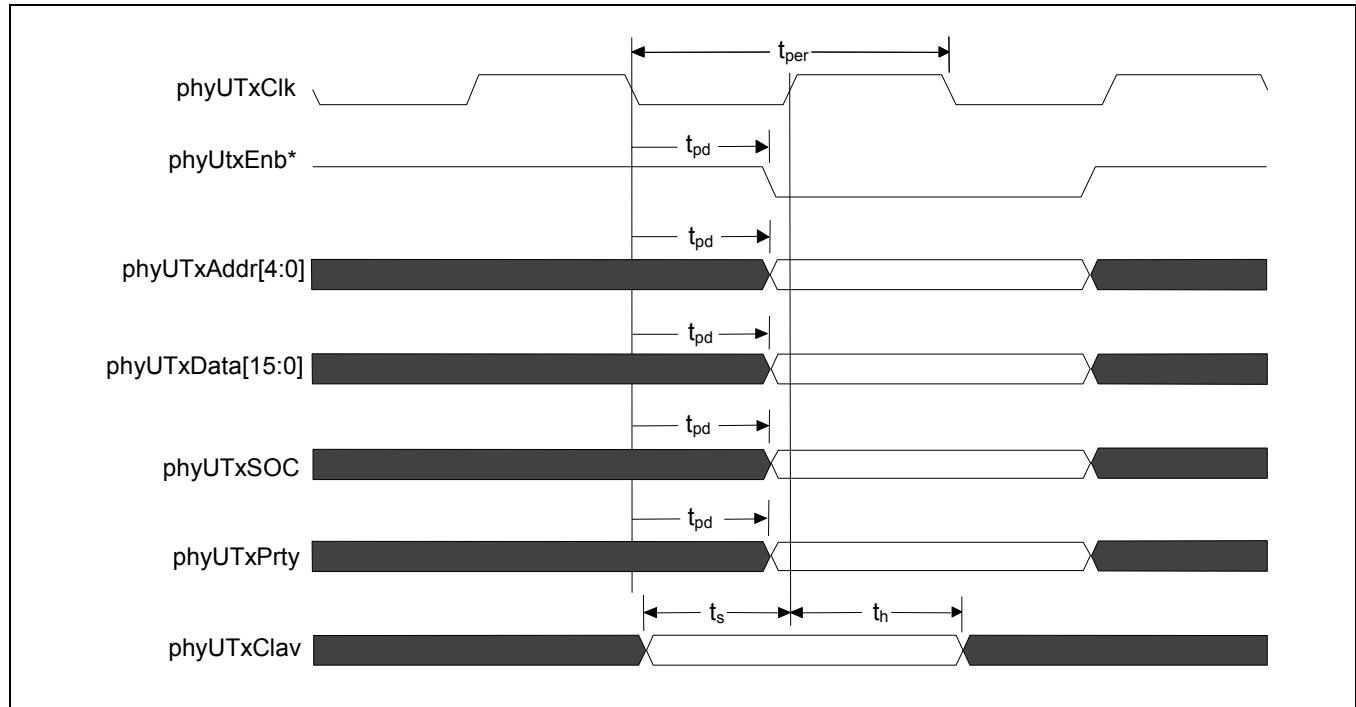


Table 3-17. PHY-side UTOPIA Transmit Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|-----------------|----------------------------------|---------|---------|---------|-------|
| $t_{per}^{(1)}$ | UTOPIA transmit clock period | 30.3 | | | ns |
| t_{duty} | UTOPIA transmit clock dutycycle | | 50 | | % |
| t_s | Setup to phyutxcclk rise edge | 8 | | | ns |
| t_h | Hold from phyutxcclk rise edge | 1 | | | ns |
| t_{pd} | Enable from phyutxcclk fall edge | -5 | | 7 | ns |

Footnote:

(1) This clock is a divide-by-2 of IMA_SysClk.

General Note:

1. Timing applies with 0-50pF loads on the outputs.

Figure 3-23. PHY-side UTOPIA Receive Timing

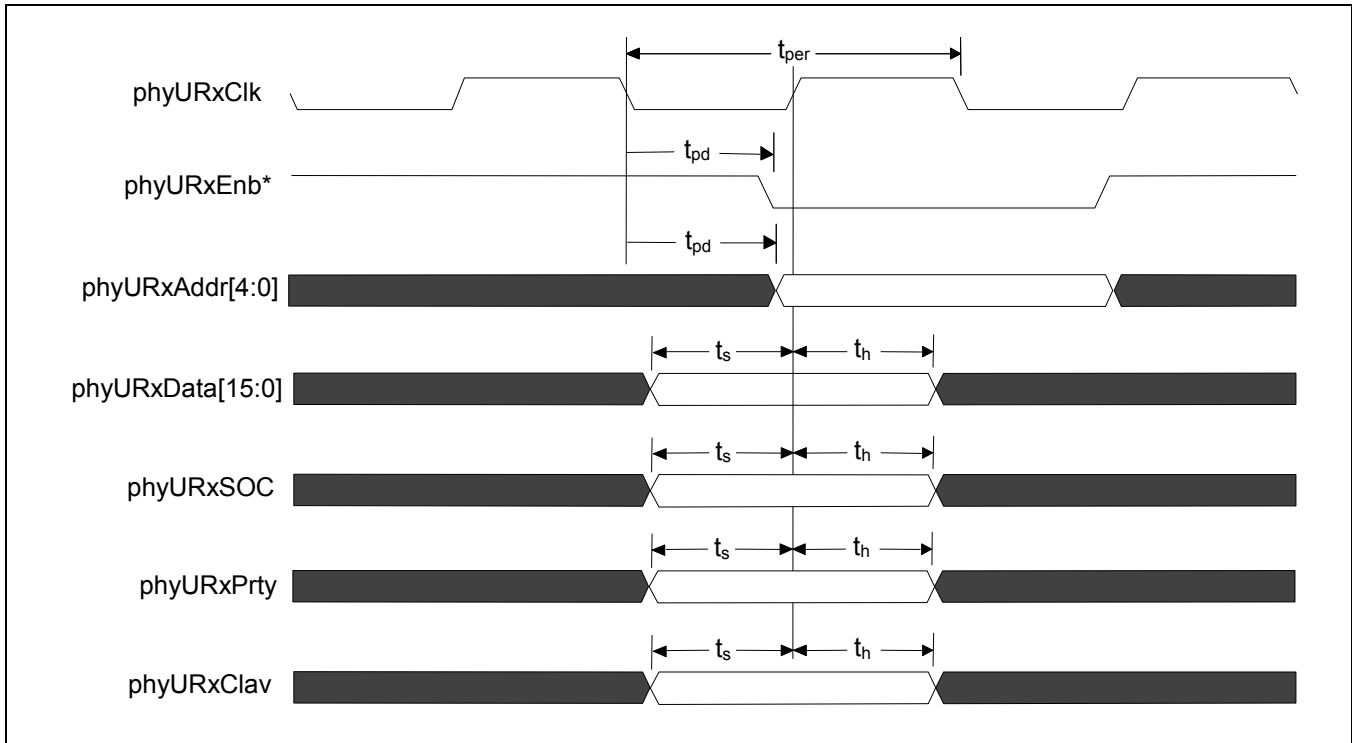


Table 3-18. PHY-side UTOPIA Receive Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|---------------------------------|----------------------------------|---------|---------|---------|-------|
| t _{per} ⁽¹⁾ | UTOPIA receive clock period | 30.3 | | | ns |
| t _{duty} | UTOPIA receive clock dutycycle | | 50 | | % |
| t _s | Setup to phyurxcclk rise edge | 8 | | | ns |
| t _h | Hold from phyurxcclk rise edge | 1 | | | ns |
| t _{pd} | Enable from phyurxcclk fall edge | -5 | | 7 | ns |

Footnote:

(1) This clock is a divide-by-2 of IMA_SysCk.

General Note:

1. Timing applies with 0-50pF loads on the outputs.

3.4.7 UTOPIA Interface Timing (ATM-Side)

Figures 3-24 through 3-25 and Tables 3-19 through 3-22 show the timing requirements and characteristics of the ATM-side UTOPIA interface.

Figure 3-24. ATM-side UTOPIA Transmit Timing

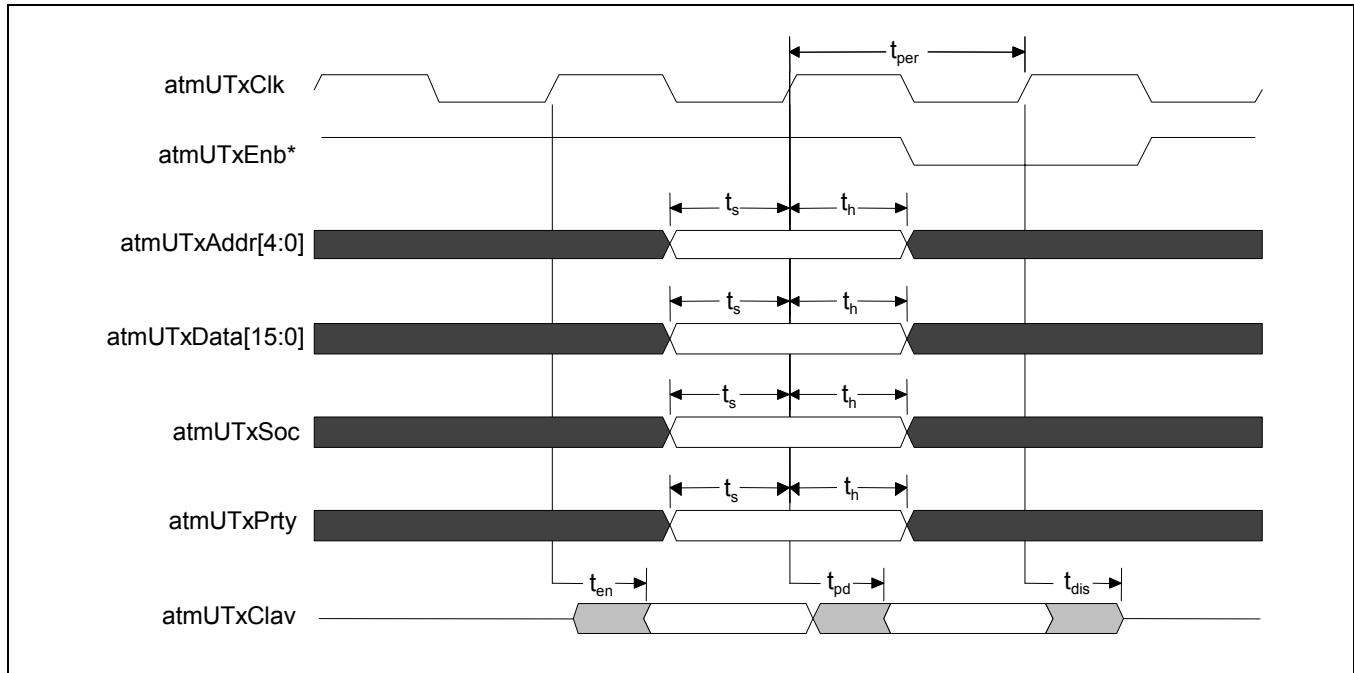


Table 3-19. ATM-side UTOPIA Transmit Timing Parameters (IMA Enabled - 16 Bit Mode)

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|------------|----------------------------------|-------------------|---------|---------|-------|
| t_{per} | UTOPIA transmit clock period | 20 ⁽¹⁾ | | | ns |
| t_{duty} | UTOPIA transmit clock dutycycle | 40 | | 60 | % |
| t_s | Setup to atmutxclk rise edge | 4 | | | ns |
| t_h | Hold from atmutxclk rise edge | 1 | | | ns |
| t_{pd} | Delay from atmutxclk rise edge | 1 | | 15 | ns |
| t_{en} | Enable from atmutxclk rise edge | 1 | | 15 | ns |
| t_{dis} | Disable from atmutxclk rise edge | 1 | | 15 | ns |

General Note:

1. Timing applies with 0-30pF loads on the outputs.

Table 3-20. ATM-side UTOPIA Transmit Timing Parameters (IMA Bypassed - 8/16 Bit Mode, IMA Enabled - 8 Bit Mode)

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|------------|---------------------------------|---------|---------|---------|-------|
| t_{per} | UTOPIA transmit clock period | 30.3 | | | ns |
| t_{duty} | UTOPIA transmit clock dutycycle | 40 | | 60 | % |
| t_s | Setup to atmuxclk rise edge | 8 | | | ns |
| t_h | Hold from atmuxclk rise edge | 1 | | | ns |
| t_{pd} | Delay from atmuxclk rise edge | 1 | | 20 | ns |
| t_{en} | Enable from atmuxclk rise edge | 1 | | 20 | ns |
| t_{dis} | Disable from atmuxclk rise edge | 1 | | 20 | ns |

General Note:
Timing applies with 0-30pF loads on the outputs.

Figure 3-25. ATM-side UTOPIA Receive Timing

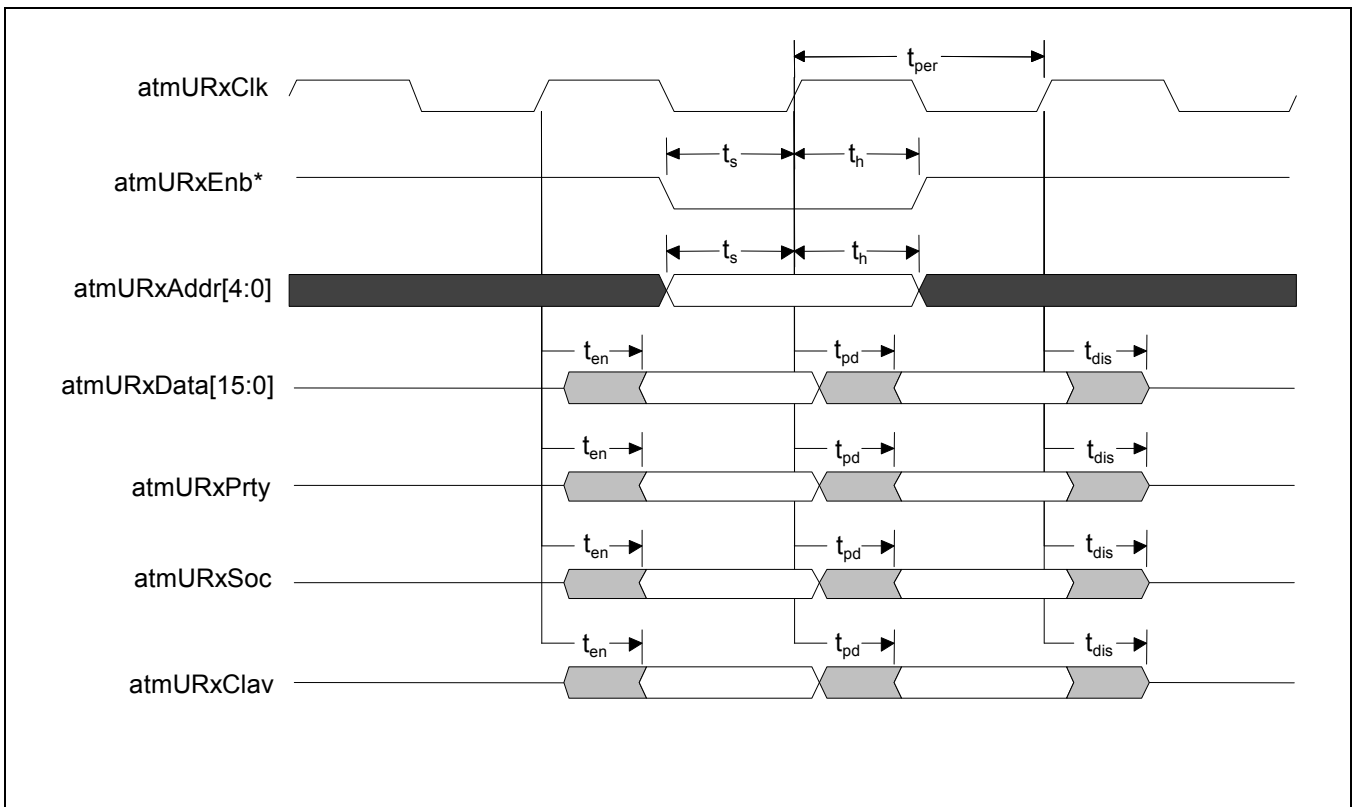


Table 3-21. ATM-side UTOPIA Receive Timing Parameters (IMA Enabled - 16 Bit Mode)

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|------------|----------------------------------|-------------------|---------|---------|-------|
| t_{per} | UTOPIA receive clock period | 20 ⁽¹⁾ | | | ns |
| t_{duty} | UTOPIA receive clock dutycycle | 40 | | 60 | % |
| t_s | Setup to atmurxclk rise edge | 4 | | | ns |
| t_h | Hold from atmurxclk rise edge | 1 | | | ns |
| t_{pd} | Delay from atmurxclk rise edge | 1 | | 15 | ns |
| t_{en} | Enable from atmurxclk rise edge | 1 | | 15 | ns |
| t_{dis} | Disable from atmurxclk rise edge | 1 | | 15 | ns |

General Note:
1. Timing applies with 0-30 pF loads on the outputs.

Table 3-22. ATM-side UTOPIA Receive Timing Parameters (IMA Bypassed - 8/16 Bit Mode, IMA Enabled - 8 Bit Mode)

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|------------|----------------------------------|---------|---------|---------|-------|
| t_{per} | UTOPIA receive clock period | 30.3 | | | ns |
| t_{duty} | UTOPIA receive clock dutycycle | 40 | | 60 | % |
| t_s | Setup to atmurxclk rise edge | 8 | | | ns |
| t_h | Hold from atmurxclk rise edge | 1 | | | ns |
| t_{pd} | Delay from atmurxclk rise edge | 1 | | 20 | ns |
| t_{en} | Enable from atmurxclk rise edge | 1 | | 20 | ns |
| t_{dis} | Disable from atmurxclk rise edge | 1 | | 20 | ns |

General Note:
1. Timing applies with 0-30 pF loads on the outputs.

3.4.8 External Memory Interface Timing Diagram

Figure 3-26. External Memory Timing

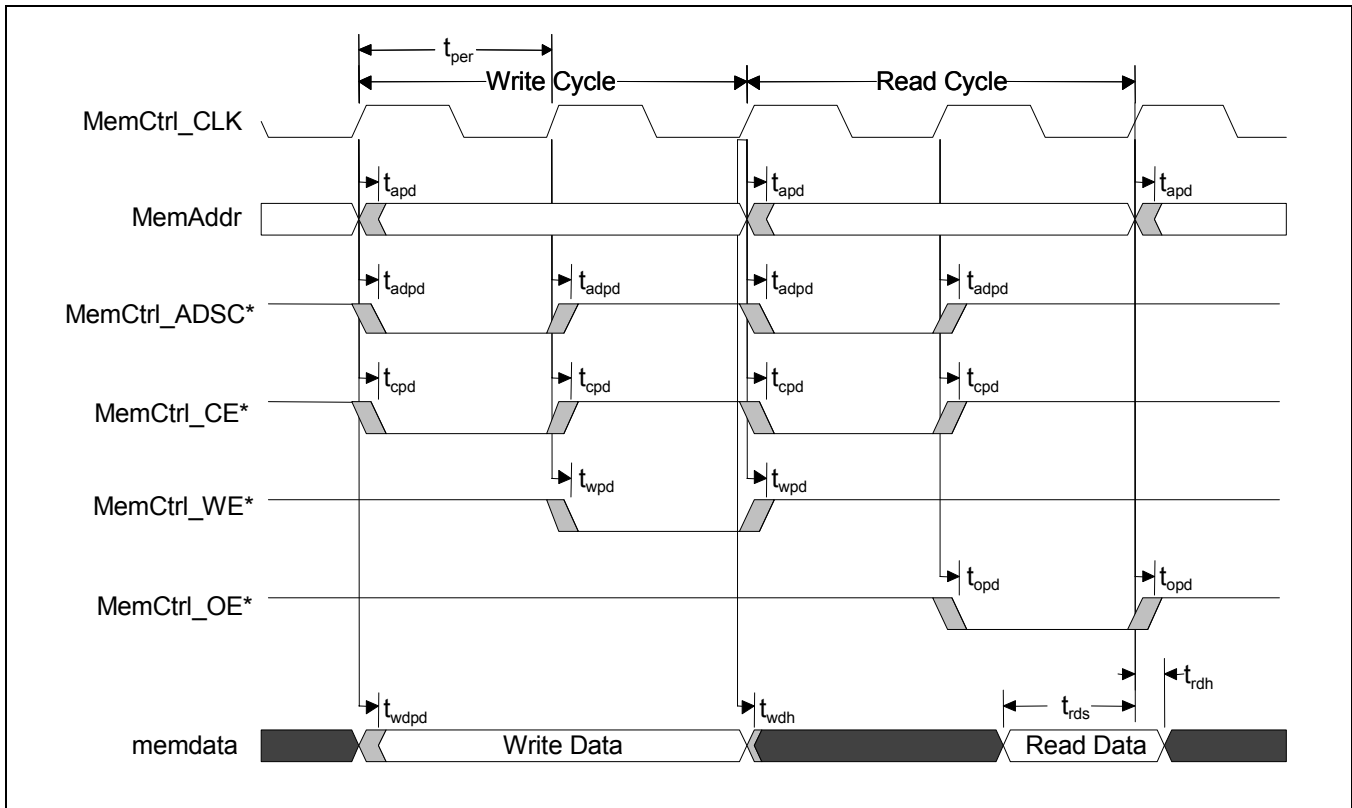


Table 3-23. External Memory Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|------------|---|---------|---------|---------|-------|
| t_{pwl} | Pulse Width Low | 8 | | - | ns |
| t_{pwh} | Pulse Width High | 8 | | - | ns |
| t_{per} | Period | 20 | | - | ns |
| t_{apd} | Propagation Delay, MemAddr from rising edge of MemCtrl_CLK | 1 | | 10 | ns |
| t_{adpd} | Propagation Delay, MemCtrl_ADSC from rising edge of MemCtrl_CLK | 1 | | 10 | ns |
| t_{cpd} | Propagation Delay, MemCtrl_CE* from rising edge of MemCtrl_CLK | 1 | | 10 | ns |
| t_{wpd} | Propagation Delay, MemCtrl_WE* from rising edge of MemCtrl_CLK | 1 | | 10 | ns |
| t_{opd} | Propagation Delay, MemCtrl_OE* from rising edge of MemCtrl_CLK | 1 | | 10 | ns |
| t_{wdpd} | Propagation Delay, valid write data from rising edge of MemCtrl_CLK | - | | 10 | ns |
| t_{wdh} | Hold, valid write data from rising edge of MemCtrl_CLK | 1 | | - | ns |
| t_{rds} | Setup, read data to rising edge of MemCtrl_CLK | 5 | | - | ns |
| t_{rdh} | Hold, read data from rising edge of MemCtrl_CLK | 1 | | - | ns |

Footnote:
 (1) All outputs are assumed to have a load of 20pf

3.4.9 JTAG Interface Timing

Figure 3-27 and Table 3-24 show the timing requirements and characteristics of the JTAG interface.

Figure 3-27. JTAG Timing

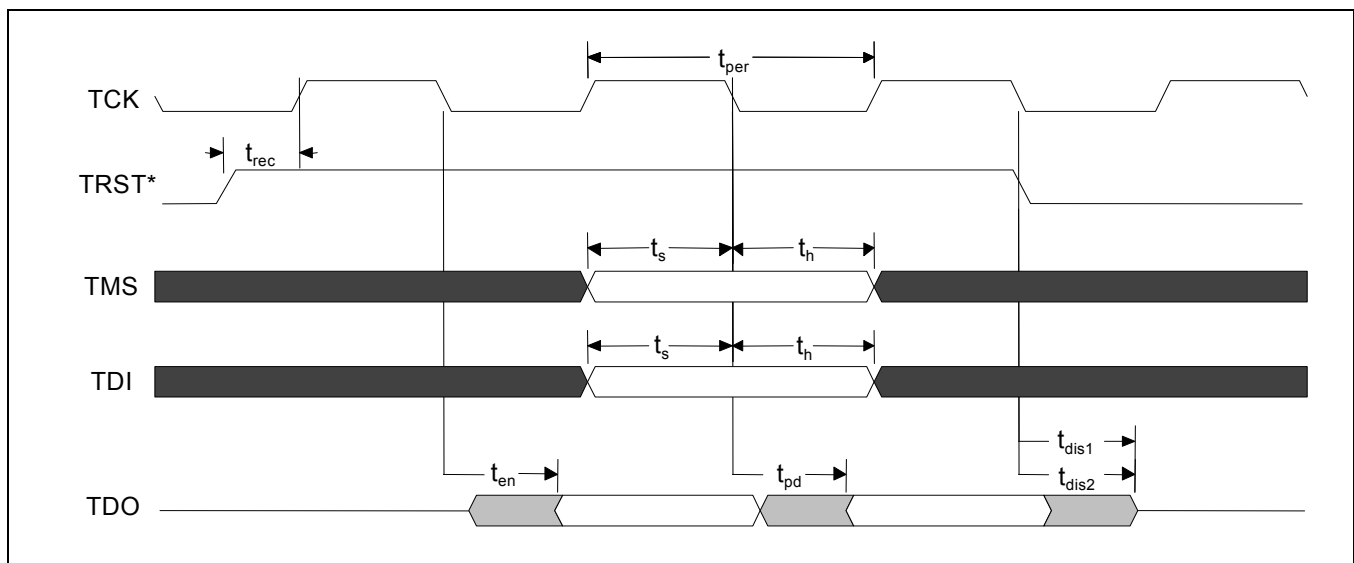


Table 3-24. JTAG Timing Parameters

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|------------|---|---------|---------|---------|-------|
| t_{per} | tck clock period | 100 | | | ns |
| t_{duty} | tck clock duty cycle | 40 | | 60 | % |
| t_{rec} | Recovery, tck rise edge from trst_n rise edge | 10 | | | ns |
| t_s | Setup to tck rise edge | 10 | | | ns |
| t_h | Hold from tck rise edge | 10 | | | ns |
| t_{pd} | Delay from tck fall edge | | | 15 | ns |
| t_{en} | Enable from tck fall edge | | | 15 | ns |
| t_{dis1} | Disable from tck fall edge | | | 15 | ns |
| t_{dis2} | Disable from tck fall edge | | | 15 | ns |

Footnote:
 (1) All outputs are assumed to have a load of 80pf

3.4.10 One-second Interface Timing

Figure 3-28 and Table 3-25 show the timing requirements and characteristics of the one-second interface.

Figure 3-28. One-second Timing

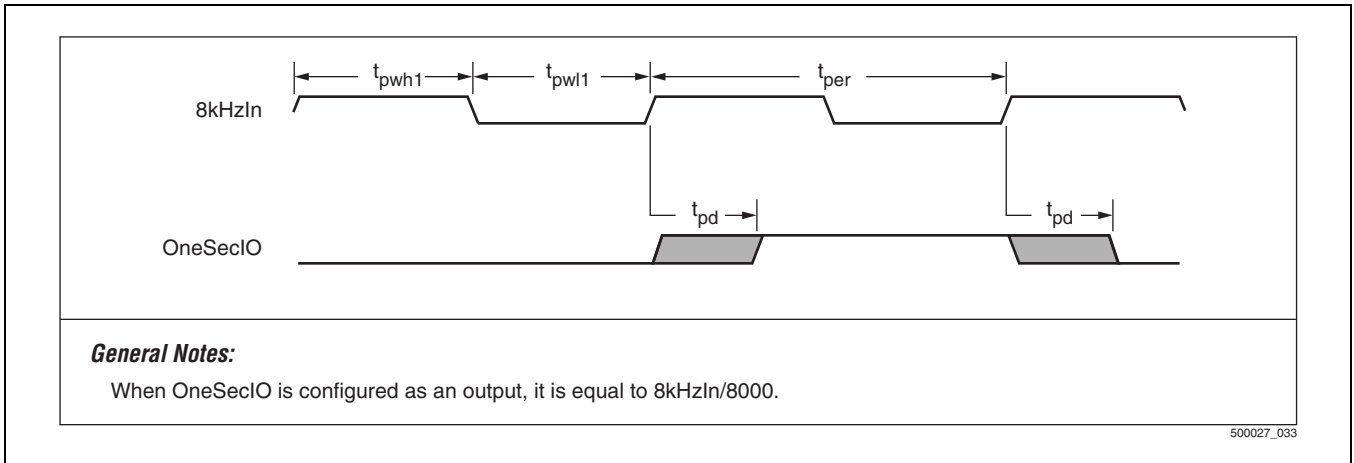


Table 3-25. One Second Timing Parameters

| Label | Description | Min | Max | Unit |
|-----------|--|------|-----|------|
| | 8KHzIn Clock Frequency | 0.01 | 100 | KHz |
| t_{per} | 8KHzIn Duty Cycle | 40% | 60% | |
| t_{pd} | Propagation Delay, OneSecOut from the rising edge of OneSecClk | 1 | 20 | ns |

3.5 Package Specification

3.5.1 Mechanical Description

The M28525/9 is a 484-ball, 27mm PBGA package. A mechanical drawing of the device is provided in [Figure 3-29](#) and [Figure 3-30](#).

Figure 3-29. M28525/9 Mechanical Drawing (Bottom View)

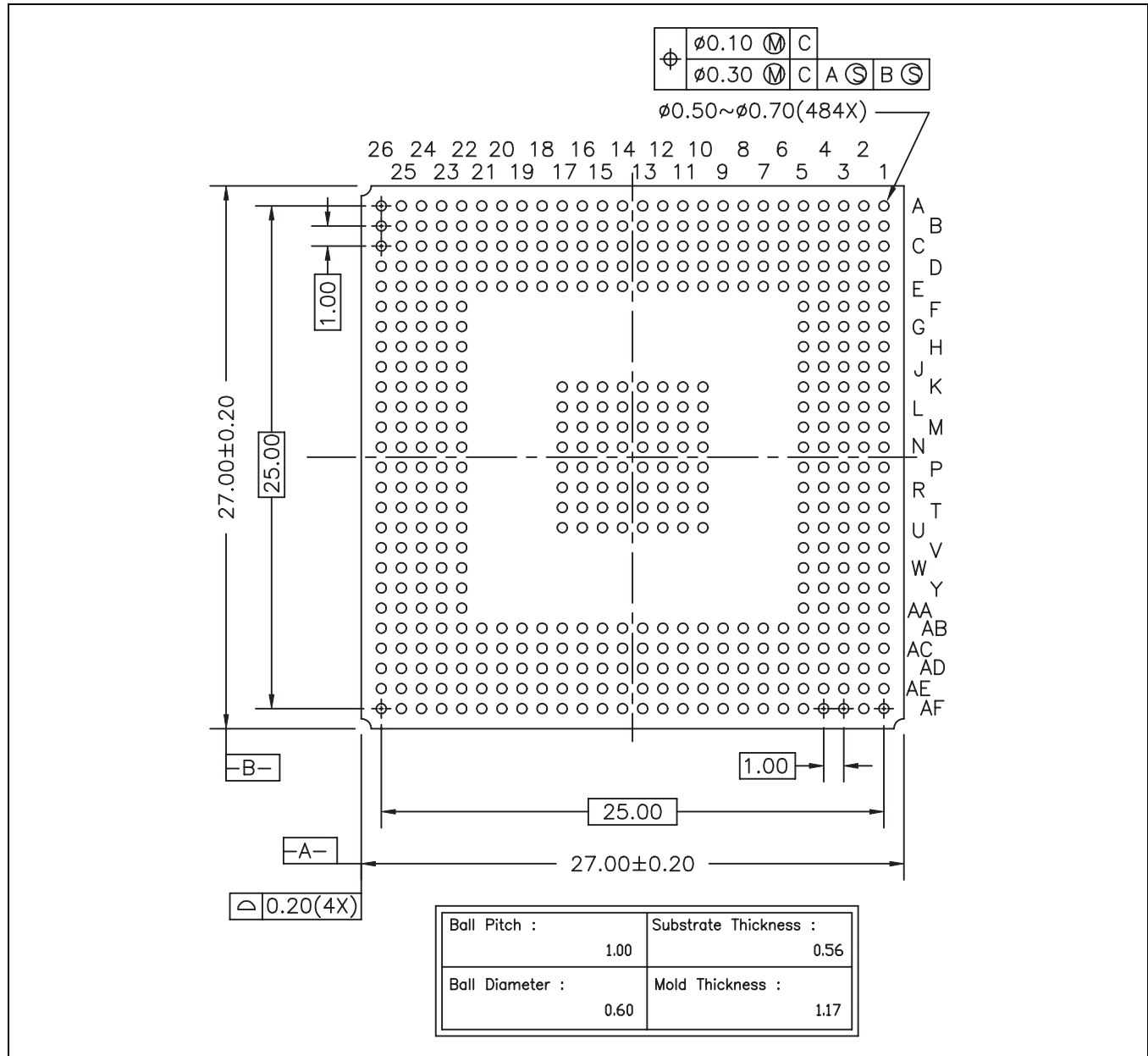
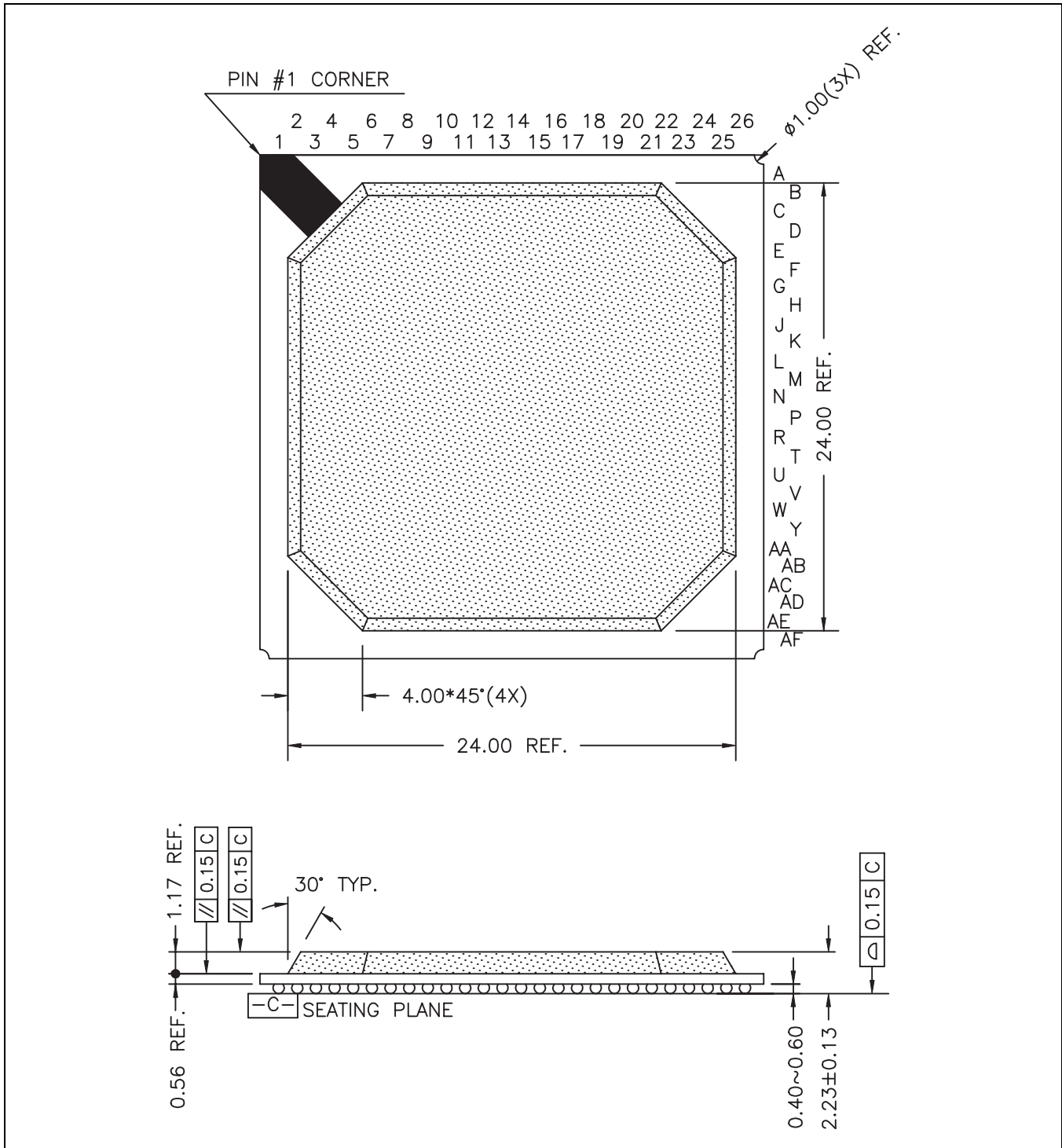


Figure 3-30. M28525/9 Mechanical Drawing (Top and Side Views)



3.6 Interface Pin Description

Figure 3-31. M28529 Pinout Diagram, UTOPIA-to-Serial (Bottom View)

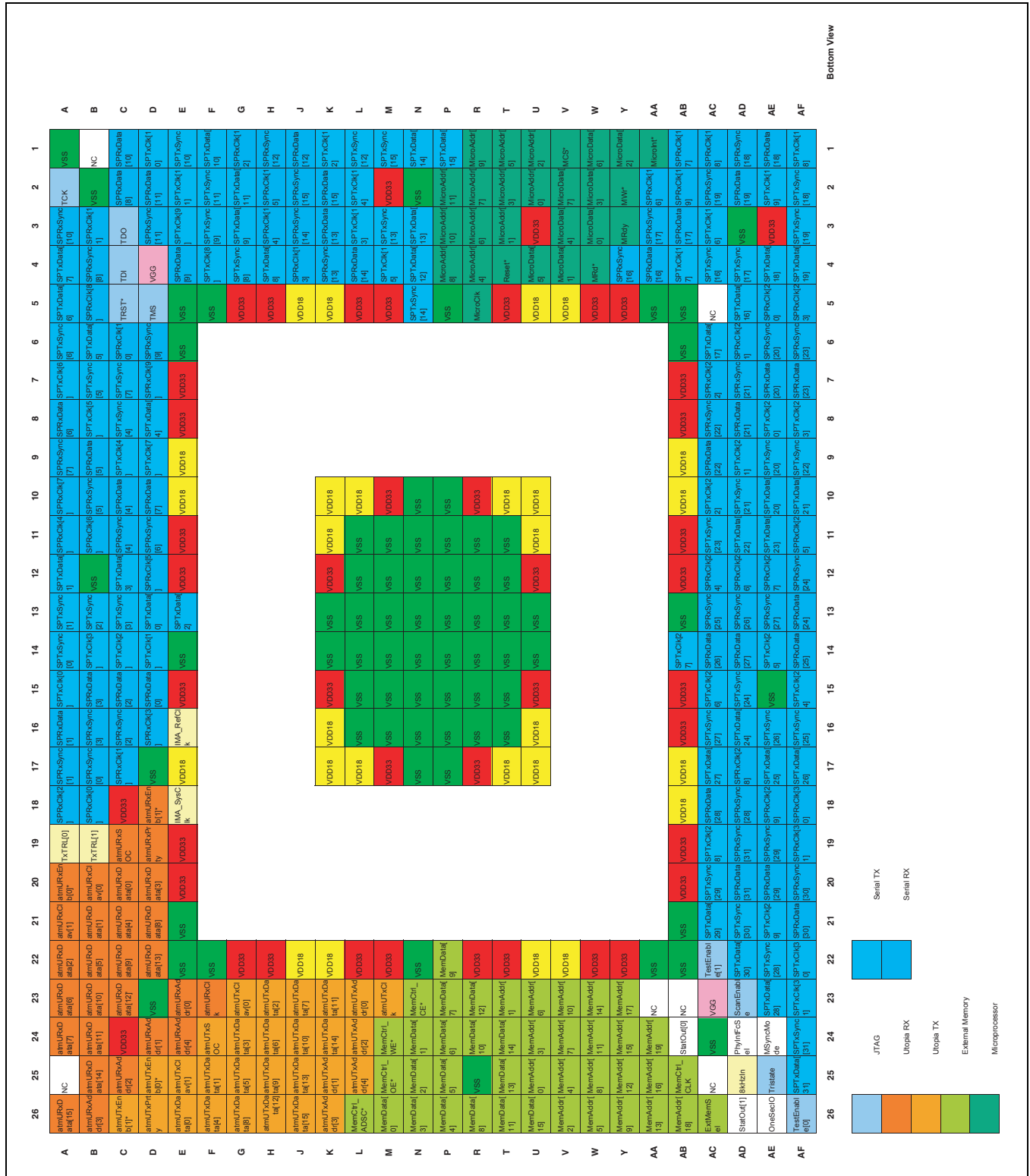
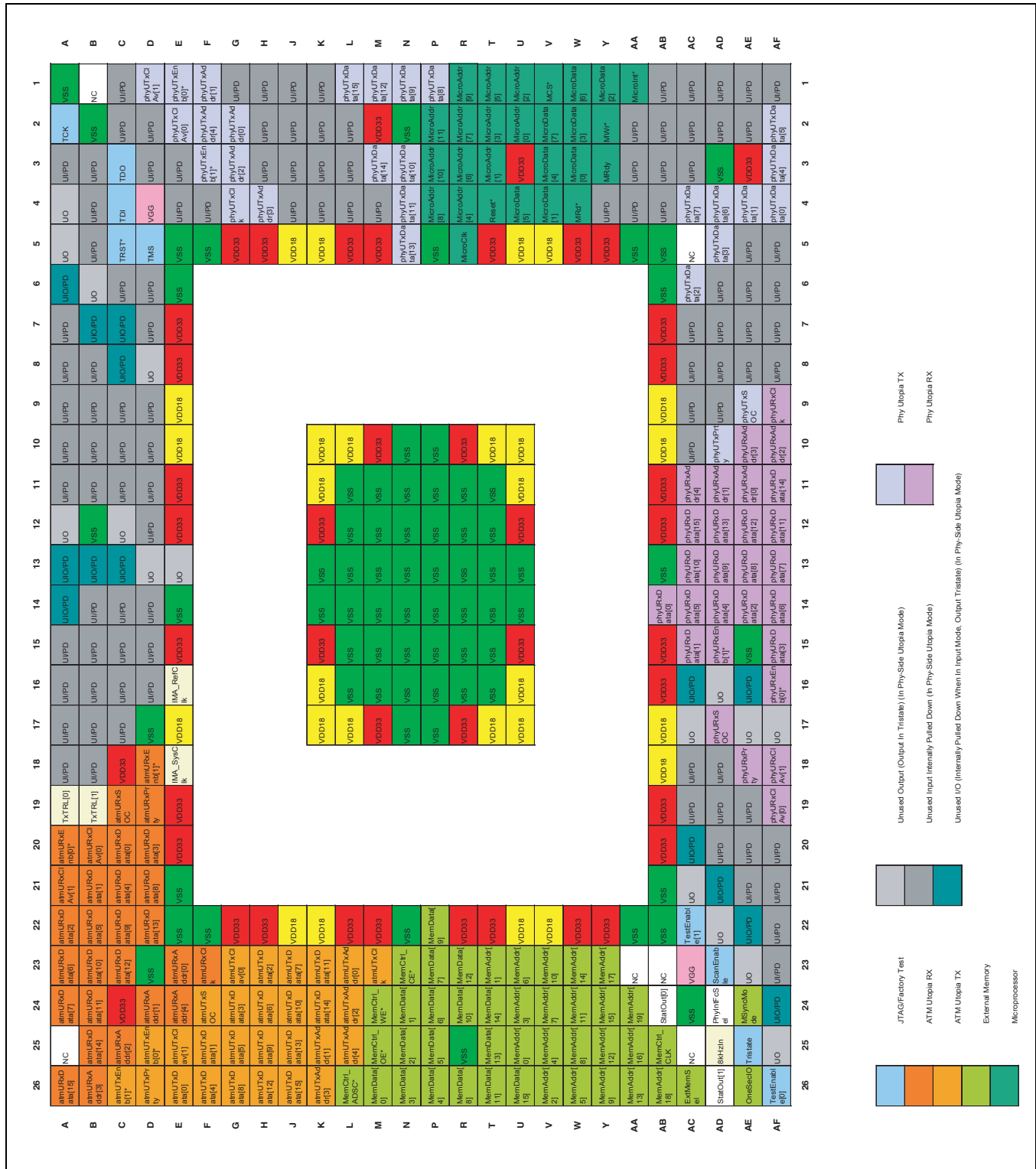


Figure 3-33. M28525/9 Pinout Diagram UTOPIA-to-UTOPIA (Bottom View)





4.0 Appendices

4.1 IMA Version 1.1 PICS Proforma

To evaluate conformance of a particular implementation, it is necessary to have a statement of which capabilities and options have been implemented for a given protocol. Such a statement is called a Protocol Implementation Conformance Statement (PICS).

4.1.1 Scope

This annex provides the PICS proforma for the Inverse Multiplexing for ATM (IMA) Version 1.1 Specification as described in AF-PHY-0086.001[A-1] in compliance with the relevant requirements, and in accordance with the relevant guidelines, given in ISO/IEC 9646-2[A-3].

4.1.2 Definitions

This document uses the following terms defined in ISO/IEC 9646-1[A-2]:

- a Protocol Implementation Conformance Statement (PICS) is a statement made by the supplier of an implementation or a system, stating which capabilities have been implemented for a given protocol,
- a PICS Proforma is a document in the form of a questionnaire, designed by the protocol specifier or the conformance test suite specifier, which when completed for an implementation or a system, becomes the PICS, and
- a static conformance review is a review of the extent to which the static conformance requirements are met by the implementation, accomplished by comparing the PICS with the static conformance requirements expressed in the relevant protocol specification.

4.1.3 Symbols and Conventions

M—Mandatory

O—Option (may be selected to suit the implementation, provided that any requirements applicable to the options are observed)

4.1.4 Conformance

The supplier of a protocol implementation, which is claimed to conform to AF-PHY-0086.001[A-1], is required to complete a copy of the PICS proforma provided in the following sections of this annex and is required to provide the information necessary to identify both the supplier and the implementation.

4.1.5 IMA PICS Proforma

4.1.5.1 Global Statement of Conformance

The implementation described in this PICS Proforma meets all of the mandatory requirements of the protocol specification.

Yes XX

No

Note: Answering “No” indicates non-conformance to the protocol specification. Non-supported mandatory capabilities are to be identified in the following tables, with an explanation in the “Comments” section of each table as to why the implementation is “non conforming”.

4.1.5.2 Instructions for Completing the PICS Proforma

Each question in this section refers to a major function of the protocol. Answering “Yes” to a particular question states that the implementation supports all of the mandatory procedures for that function, as defined in the referenced section of AF-PHY-0086.001[A-1]. Answering “No” to a particular question in this section states that the implementation does not support that function of the protocol.

A supplier may also provide additional information, categorized as exceptional (X) or supplementary information. This additional information should be provided in the Support column as items labeled X<I> for exceptional or S<I> for supplementary information, respectively for cross-reference purposes, where <I> is any unambiguous number.

4.1.5.3 IMA Protocol Functions

Table 4-1. Basic IMA Protocol (BIP) Definition Functions (1 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-------|---|------------------|--------------|-------|---------------------------|
| BIP.1 | Does the implementation support a number N ($1 \leq N \leq 32$) of transmission links within an IMA group operating at the same nominal link cell rate (LCR)? | | M | (R-1) | Yes <u>X</u> No <u> </u> |
| BIP.2 | Does the implementation support the IMA interface connected to another interface over clear channel facilities (implies cells generated by transmit IMA shall only be terminated at the receive IMA)? | | M | (R-2) | Yes <u>X</u> No <u> </u> |
| BIP.3 | Does the interface specific TC sublayer of the implementation pass all cells to the IMA sublayer or provide an indication that a cell was received (this includes HEC errored cells)? | | M | (R-3) | Yes <u>X</u> No <u> </u> |
| BIP.4 | Does the implementation prohibit cell rate decoupling at the interface specific TC sublayer? | | M | (R-4) | Yes <u>X</u> No <u> </u> |
| BIP.5 | Does the implementation assign a LID unique within the IMA group to each Tx IMA link on each physical link? | | M | (R-5) | Yes <u>X</u> No <u> </u> |
| BIP.6 | Does the implementation ensure that the LID does not change while the link is a member of the IMA group? | | M | (R-6) | Yes <u>X</u> No <u> </u> |
| BIP.7 | Does the implementation distribute ATM cells arriving from the ATM layer over the N links in a cyclic round-robin fashion, and on a cell-by-cell basis? | | M | (R-7) | Yes <u>X</u> No <u> </u> |
| BIP.8 | Does the implementation distribute ATM cells over the links using an ascending order based on the LID assigned to each link within the IMA group? | | M | (R-8) | Yes <u>X</u> No <u> </u> |

Table 4-1. Basic IMA Protocol (BIP) Definition Functions (2 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--------|---|------------------|--------------|--------|--------------------|
| BIP.9 | Does the implementation support the ICP cell format defined in Table 2 on page 31 to convey IMA configuration, synchronization, status, and defect information to the far-end? | | M | (R-9) | Yes <u>X</u> No __ |
| BIP.10 | Does the implementation perform cell rate decoupling by inserting IMA Filler cells in place of ATM cells when there is no cell available at the ATM layer? | | M | (R-10) | Yes <u>X</u> No __ |
| BIP.11 | Does the implementation accept, on receive, ATM cells from the N links according to ascending order based on the LID received in the ICP cells on the incoming link? | | M | (R-11) | Yes <u>X</u> No __ |
| BIP.12 | Does the implementation, on receive, compensate for link differential delays and rebuild the original ATM cell stream? | | M | (R-11) | Yes <u>X</u> No __ |
| BIP.13 | Does the implementation discard received Filler cells and cells with bad HEC? | | M | (R-11) | Yes <u>X</u> No __ |
| BIP.14 | Does the implementation process and discard incoming ICP cells? | | M | (R-11) | Yes <u>X</u> No __ |
| BIP.15 | Does the implementation aggregate, on receive, the ATM cell stream to the ATM layer? | | M | (R-11) | Yes <u>X</u> No __ |
| BIP.16 | Does the implementation preserve the order of incoming cells? | | M | (R-11) | Yes <u>X</u> No __ |
| BIP.17 | Does the implementation use the ICP cell to maintain IMA protocol synchronization? | | M | (R-12) | Yes <u>X</u> No __ |
| BIP.18 | Does the implementation use the ICP cell to maintain link delay synchronization? | | M | (R-12) | Yes <u>X</u> No __ |
| BIP.19 | Does the implementation transmit first the most significant bit of each octet of the IMA OAM cell? | | M | (R-13) | Yes <u>X</u> No __ |
| BIP.20 | Does the implementation support the same cell header for both the Filler and ICP cell formats as defined in Table 1 on page 28 and Table 2 on page 31? | | M | (R-14) | Yes <u>X</u> No __ |
| BIP.21 | Does the implementation use bit 7 of octet 7 (CID field) of the Filler and ICP cells to identify the IMA OAM cell as an ICP or Filler cell? | | M | (R-15) | Yes <u>X</u> No __ |
| BIP.22 | Does the implementation use octets 52-53 as specified in ITU-T Recommendation I.610 [A-5] for octets 52-53 of the OAM cells of the F1/F3 flows? | | M | (R-16) | Yes <u>X</u> No __ |
| BIP.23 | Does the implementation support the Filler cell format defined in Table 1 on page 28? | | M | (R-17) | Yes <u>X</u> No __ |
| BIP.24 | Does the implementation support the ICP cell format defined in Table 2 on page 31? | | M | (R-18) | Yes <u>X</u> No __ |
| BIP.25 | Does the implementation transmit the content of the link specific fields appearing in class A over the link for which these fields apply? | | M | (R-19) | Yes <u>X</u> No __ |
| BIP.26 | Does the implementation transmit the same content of fields appearing in classes B and C of the ICP cell over all links within an IMA group? | | M | (R-20) | Yes <u>X</u> No __ |
| BIP.27 | Does the implementation use the LID bits (bits 4-0 of octet 7) in the ICP cell to identify the Link ID (range being 0 to 31)? | | M | (R-21) | Yes <u>X</u> No __ |
| BIP.28 | Does the implementation use the "Tx State" field, located in the Link "x" Information field in an ICP cell, to report the transmit state of the IMA link on which the NE IMA is transmitting ICP cells carrying LID = "x" ("x" being a value between 0 and 31)? | | M | (R-22) | Yes <u>X</u> No __ |

Table 4-1. Basic IMA Protocol (BIP) Definition Functions (3 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--------|--|------------------|--------------|--------|---------------------------|
| BIP.29 | Does the implementation use the "Rx State", located in the Link "x" Information field in an ICP cell, to report the receive state of the incoming IMA link on which the FE IMA is transmitting ICP cells carrying LID = "x" ("x" being a value between 0 and 31)? | | M | (R-23) | Yes <u>X</u> No <u> </u> |
| BIP.30 | Does the implementation use the "Rx Defect Indicators" field, located in the Link "x" Information field in an ICP cell, to report the Rx defect indicators corresponding to the incoming IMA link on which the FE IMA is transmitting ICP cells carrying LID = "x" ("x" being a value between 0 and 31)? | | M | (R-24) | Yes <u>X</u> No <u> </u> |
| BIP.31 | Does the implementation always transmit ICP cells with Octet 50 unused and set to "0x6A" as defined in ITU-T Recommendation I.432 [A-4]? | | M | (R-25) | Yes <u>X</u> No <u> </u> |
| BIP.32 | Does the implementation reserve the End-to-End Channel field (Octet 51) as a proprietary channel? | | M | (R-26) | Yes <u>X</u> No <u> </u> |
| BIP.33 | Does the implementation set the End-to-End Channel field (Octet 51) to "0" when not using this field? | | M | (R-27) | Yes <u>X</u> No <u> </u> |
| BIP.34 | Does the implementation not rely on the processing of the End-to-End Channel field for any IMA functionality? | | M | (R-28) | Yes <u>X</u> No <u> </u> |
| BIP.35 | Does the implementation only consider the information within ICP cells exhibiting neither a HEC nor a CRC-10 error? | | M | (R-29) | Yes <u>X</u> No <u> </u> |
| BIP.36 | Does the implementation always transmit "0x03" over the OAM Label in the Filler and ICP cells? | | M | (R-30) | Yes <u>X</u> No <u> </u> |
| BIP.37 | If the implementation does not support the IMA version proposed by the OAM Label received from the far-end IMA unit, does the implementation report the "Config-Aborted - Unsupported IMA Version" state over the "Group Status and Control" field? | | M | (R-31) | Yes <u>X</u> No <u> </u> |
| BIP.38 | Does the implementation transmit IMA frames, composed of M consecutive cells, on each link within the IMA group? | | M | (R-32) | Yes <u>X</u> No <u> </u> |
| BIP.39 | Does the implementation send ICP cells on each link once per IMA frame, hence every M cells? | | M | (R-33) | Yes <u>X</u> No <u> </u> |
| BIP.40 | Does the implementation use the IFSN field in the ICP cell to indicate the sequence number of the IMA frame? | | M | (R-34) | Yes <u>X</u> No <u> </u> |
| BIP.41 | Does the implementation increment the IFSN field in the ICP cell from 0 to 255 and repeat the sequence? | | M | (R-35) | Yes <u>X</u> No <u> </u> |
| BIP.42 | Does the implementation increment the IFSN field in the ICP cell with each IMA frame on a per-link basis? | | M | (R-36) | Yes <u>X</u> No <u> </u> |
| BIP.43 | Within an IMA frame, does the implementation place identical IFSN values in the ICP cells sent on each link? | | M | (R-36) | Yes <u>X</u> No <u> </u> |
| BIP.44 | Does the implementation align the transmission of the IMA frame on all links within an IMA group? | | M | (R-37) | Yes <u>X</u> No <u> </u> |
| BIP.45 | Does the implementation use the ICP Cell Offset field (octet 9) to indicate the location of the ICP cell within the IMA frame of length M cells? | | M | (R-38) | Yes <u>X</u> No <u> </u> |
| BIP.46 | Does the implementation always set the value of the ICP cell offset between 0 and M-1 where M is the IMA frame length in cells? | | M | (R-39) | Yes <u>X</u> No <u> </u> |
| BIP.47 | Does the implementation distribute the ICP cells, from link to link within the IMA group, in a uniform fashion across the IMA frame? | | O | (O-1) | Yes <u>X</u> No <u> </u> |

Table 4-1. Basic IMA Protocol (BIP) Definition Functions (4 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--------|--|------------------|--------------|--------|--------------------|
| BIP.48 | Does the implementation select the offset of the ICP cell sent of any link when the link is assigned a LID? | | M | (R-40) | Yes <u>X</u> No __ |
| BIP.49 | Does the implementation retain the offset of the ICP cell sent on a given link until the link is no longer part of the group? | | M | (R-40) | Yes <u>X</u> No __ |
| BIP.50 | Does the implementation always use the Frame Length field in the ICP cell to indicate the value of M? | | M | (R-41) | Yes <u>X</u> No __ |
| BIP.51 | Does the implementation support M = 128? | | M | (R-42) | Yes <u>X</u> No __ |
| BIP.52 | Does the implementation support M = 32? | | O | (O-2) | Yes <u>X</u> No __ |
| BIP.53 | Does the implementation support M = 64? | | O | (O-2) | Yes <u>X</u> No __ |
| BIP.54 | Does the implementation support M = 256? | | O | (O-2) | Yes <u>X</u> No __ |
| BIP.55 | Does the implementation only change the value M at group start-up time? | | M | (R-43) | Yes <u>X</u> No __ |
| BIP.56 | Does the implementation use on transmit the value configured by the UM? | (O-2) | M | (CR-1) | Yes <u>X</u> No __ |
| BIP.57 | Does the implementation allow different values of M in both Tx and Rx directions? | (O-2) | M | (CR-2) | Yes <u>X</u> No __ |
| BIP.58 | Does the implementation synchronize its incoming links using the received M value for IMA frame synchronization? | (O-2) | M | (CR-3) | Yes <u>X</u> No __ |
| BIP.59 | Does the implementation abort the start-up procedure using the corresponding code in the Group Status and Control field of the ICP cell when it does not support the received M? | | M | (R-44) | Yes <u>X</u> No __ |
| BIP.60 | Does the implementation allow to configure the value M? | | O | (O-3) | Yes <u>X</u> No __ |
| BIP.61 | Does the implementation set the SCCI field to the previously transmitted SCCI field value, incremented modulo 256, to indicate a change on at least one of the fields appearing in octets 12 through 49 in the transmitted ICP cell? | | M | (R-45) | Yes <u>X</u> No __ |
| BIP.62 | Does the implementation use the SCCI field to identify received ICP cells for processing when ICP cells are monitored on more than one link, or when the monitored link has changed? | | M | (R-46) | Yes <u>X</u> No __ |
| BIP.63 | Does the implementation process the fields in octets 12 through 49 if the SCCI field has advanced beyond the SCCI value of the last processed ICP cell? | | M | (R-46) | Yes <u>X</u> No __ |
| BIP.64 | Does the implementation select the IMA ID at group start-up time? | | M | (R-47) | Yes <u>X</u> No __ |
| BIP.65 | Does the implementation transmit the IMA ID in the IMA ID field? | | M | (R-48) | Yes <u>X</u> No __ |
| BIP.66 | Does the implementation allow to configure the value of IMA ID? | | O | (O-4) | Yes <u>X</u> No __ |
| BIP.67 | Does the implementation use the "Group Symmetry Mode" field, specified in Table 2 on page 31, to indicate the symmetry of the IMA group? | | M | (R-49) | Yes <u>X</u> No __ |
| BIP.68 | Does the implementation ensure that the symmetry of the group is only established or changed at group start-up time? | | M | (R-50) | Yes <u>X</u> No __ |
| BIP.69 | Does the implementation support the Symmetrical Configuration and Operation mode? | | M | (R-51) | Yes <u>X</u> No __ |
| BIP.70 | Does the implementation support the Symmetrical Configuration and Asymmetrical Operation mode? | | O | (O-5) | Yes <u>X</u> No __ |

Table 4-1. Basic IMA Protocol (BIP) Definition Functions (5 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--|---|------------------|--------------|--------|--------------------|
| BIP.71 | Does the implementation support the Asymmetrical Configuration and Operation mode? | | 0 | (O-6) | Yes <u>X</u> No __ |
| BIP.72 | Does the implementation abort the start-up procedure using the appropriate code defined in the "Group Status and Control" field of the ICP cell (as specified in Table 2 on page 31) if the NE does not support the symmetry mode proposed by the FE? | | M | (R-52) | Yes <u>X</u> No __ |
| BIP.73 | Does the implementation abort the start-up procedure using the appropriate code defined in the "Group Status and Control" field of the ICP cell (as specified in Table 2 on page 31) if the symmetry mode proposed by the FE and the configured symmetry mode of the NE do not match? | | M | (R-52) | Yes <u>X</u> No __ |
| BIP.74 | In order to allow a fast recovery when (O-5) or (O-6) is used at the NE and when the FE IMA unit can only be configured to the "Symmetrical Configuration and Operation" mode, does the implementation adjust to "Symmetrical Configuration and Operation". | | 0 | (O-7) | Yes <u>X</u> No __ |
| BIP.75 | Does the implementation support only the valid combinations of group symmetry modes at each end of the IMA virtual link as specified in Table 4 on page 36? | | M | (R-53) | Yes <u>X</u> No __ |
| BIP.76 | Does the implementation allow configuration of the group mode? | | 0 | (O-8) | Yes <u>X</u> No __ |
| Comments: Maximum group size is 8 links. | | | | | |

Table 4-2. QoS Requirements Functions

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-----------|---|------------------|--------------|--------|--------------------|
| QOS.1 | Does the implementation support all ATM traffic/QoS classes supported by the ATM layer? | | M | (R-54) | Yes <u>X</u> No __ |
| Comments: | | | | | |

Table 4-3. CTC and ITC Operation Functions (1 of 2)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-------|---|------------------|--------------|--------|--------------------|
| CIT.1 | Does the implementation indicate to the FE in which transmit clock mode it is running in the "Transmit Clock Mode" field in the ICP cell? | | M | (R-55) | Yes <u>X</u> No __ |
| CIT.2 | Does the implementation support the CTC mode in the transmit direction? | | M | (R-56) | Yes <u>X</u> No __ |
| CIT.3 | Does the implementation only indicate to the FE that it is in the CTC mode when all the "transmit" clocks of the links in the group are derived from the same source? | | M | (R-57) | Yes <u>X</u> No __ |
| CIT.4 | Does the implementation support the ITC mode in the transmit direction? | | 0 | (O-9) | Yes <u>X</u> No __ |
| CIT.5 | Does the implementation indicate that it is in the ITC mode even if all the transmit clocks of the links in the group are derived from the same source? | | 0 | (O-10) | Yes <u>X</u> No __ |
| CIT.6 | Does the implementation use the cell stuffing procedure to prevent link transmit buffer under-run or over-run? | (O-9) | M | (CR-4) | Yes <u>X</u> No __ |
| CIT.7 | Does the implementation indicate a stuff event in the ICP cell preceding a stuff event using the mandatory LSI codes specified in Table 2 on page 30? | | M | (R-58) | Yes <u>X</u> No __ |

Table 4-3. CTC and ITC Operation Functions (2 of 2)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-----------|--|------------------|--------------|--------|--------------------|
| CIT.8 | Does the implementation perform stuffing by repeating the ICP cell containing the LSI code indicating that “this cell is 1 out of 2 ICP cells comprising the stuff event”? | | M | (R-59) | Yes <u>X</u> No __ |
| CIT.9 | Does the implementation also indicate an incoming stuff event in the fourth, third, and second ICP preceding the stuff event using the optional LSI codes? | | O | (O-11) | Yes <u>X</u> No __ |
| CIT.10 | At any given link, does the implementation ensure it does not introduce a stuff event more than once every 5*M ICP, Filler and ATM layer cells? | | M | (R-60) | Yes <u>X</u> No __ |
| CIT.11 | Does the implementation remove one of any two consecutive ICP cells with LSI code indicating “this cell is 1 out of the 2 ICP cells comprising the stuff event”? | | M | (R-61) | Yes <u>X</u> No __ |
| CIT.12 | Does the implementation ensure that the SICP cell is not counted as a cell for the purposes of determining the IMA round-robin sequence? | | M | (R-61) | Yes <u>X</u> No __ |
| CIT.13 | Does the implementation support CTC and ITC modes on receive? | | M | (R-62) | Yes <u>X</u> No __ |
| CIT.14 | Does the implementation inform the UM of a mismatch between the FE and NE IMA transmit clock modes? | | M | (R-63) | Yes <u>X</u> No __ |
| CIT.15 | Does the implementation ensure that a restart is not caused if the implementation detects a mismatch between the FE and NE Transmit clock modes? | | M | (R-63) | Yes <u>X</u> No __ |
| CIT.16 | Does the implementation rely on at least one ICP cell with a correct CRC-10 in order to process the incoming stuff cell indication code (this is recommended)? | | O | (O-12) | Yes <u>X</u> No __ |
| Comments: | | | | | |

Table 4-4. IMA Data Cell (IDC) Rate Implementation Functions (1 of 2)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-------|--|------------------|--------------|--------|--------------------|
| IDC.1 | Does the implementation ensure on transmit that a Filler cell is not injected if an ATM layer cell is available for scheduling? | | M | (R-64) | Yes <u>X</u> No __ |
| IDC.2 | Does the implementation only check on transmit that an ATM layer cell is available and accept that cell only when the Tx IDCC ticks? | | M | (R-64) | Yes <u>X</u> No __ |
| IDC.3 | Does the implementation only select the TRL from the set of links whose transmit state is Active? | | M | (R-65) | Yes <u>X</u> No __ |
| IDC.4 | If there is no link in the Active state, does the implementation select one of the links in the Usable state, if any, or one of the links in the Unusable state otherwise? | | M | (R-66) | Yes <u>X</u> No __ |
| IDC.5 | Does the implementation only select or change the TRL during the following situations: during group start-up, when the previously selected TRL's transmit state changes from Active to any other state (e.g., Usable, Unusable, or Not In Group) while another link's transmit state is Active, or when the previously selected TRL's transmit state changes from Usable to Unusable or Not In Group while another link's transmit state is Active or Usable? | | M | (R-67) | Yes <u>X</u> No __ |

Table 4-4. IMA Data Cell (IDC) Rate Implementation Functions (2 of 2)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-----------|---|------------------|--------------|--------|--------------------|
| IDC.6 | Does the implementation indicate the selected or changed TRL to the FE over the “Transmit Timing Information” field in the ICP cell? | | M | (R-68) | Yes <u>X</u> No __ |
| IDC.7 | Does the implementation derive the Tx IDCC from the selected TRL according to Equation 1 on page 40? | | M | (R-69) | Yes <u>X</u> No __ |
| IDC.8 | When running in the CTC mode, does the implementation introduce a stuff event every 2048 ICP, Filler and ATM layer cells on all links? | | M | (R-70) | Yes <u>X</u> No __ |
| IDC.9 | Does the implementation introduce a stuff event every 2048 ICP, Filler and ATM layer cells on the TRL? | (0-9) | M | (CR-5) | Yes <u>X</u> No __ |
| IDC.10 | Does the implementation introduce stuff events on links other than the TRL in order to compensate for the timing difference between the TRL and the other links? | (0-9) | M | (CR-6) | Yes <u>X</u> No __ |
| IDC.11 | Does the implementation remove CDV attributed to the presence of ICP cells by a mechanism equivalent to providing a small smoothing buffer into which cells are placed after reordering and after removing ICP cells? | | M | (R-71) | Yes <u>X</u> No __ |
| IDC.12 | If the TRL is in the Working state and the FE has, for at least 100 milliseconds, identified a given link as the TRL, does the implementation derive the Rx IDCR using the incoming link indicated by the FE as the TRL? | | M | (R-72) | Yes <u>X</u> No __ |
| IDC.13 | Does the implementation have an equivalent behavior to the following: when the IMA data cell clock at the receiver ticks, one cell is removed from the smoothing buffer; if the cell is a Filler cell, then the Filler cell is discarded and nothing passed to the ATM layer; if the cell is not a Filler cell, then it is passed to the ATM layer? | | M | (R-73) | Yes <u>X</u> No __ |
| Comments: | | | | | |

Table 4-5. Link Differential Delay (LDD) Functions

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-----------|--|------------------|--------------|--------|--------------------|
| LDD.1 | Does the implementation introduce a differential delay among the constituent links of a maximum of 2.5 cell times at the physical link rate? | | M | (R-74) | Yes <u>X</u> No __ |
| LDD.2 | Does the implementation tolerate up to at least 25 milliseconds of link differential delay on receive? | | M | (R-75) | Yes <u>X</u> No __ |
| LDD.3 | Does the implementation allow configuring the link differential delay tolerance? | | 0 | (0-13) | Yes <u>X</u> No __ |
| Comments: | | | | | |

Table 4-6. IMA Interface Operation (IIO) Functions (1 of 4)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-------|--|------------------|--------------|--------|--------------------|
| IIO.1 | Does the implementation support the Tx LSM defined in Table 8 on page 52? | | M | (R-76) | Yes <u>X</u> No __ |
| IIO.2 | Does the implementation support the Rx LSM defined in Table 9 on page 53? | | M | (R-77) | Yes <u>X</u> No __ |
| IIO.3 | Does the implementation signal the current state of the Tx LSM to the FE IMA unit via the ICP cells? | | M | (R-78) | Yes <u>X</u> No __ |

Table 4-6. IMA Interface Operation (IIO) Functions (2 of 4)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--------|--|------------------|--------------|--------|------------|
| IIO.4 | Does the implementation perform the actions corresponding to the Tx LSM sub-states? | | M | (R-78) | Yes_X_No__ |
| IIO.5 | Does the implementation update the Tx LSM according the occurrence of the events listed in Table 8 on page 52? | | M | (R-78) | Yes_X_No__ |
| IIO.6 | Does the implementation treat sequentially the incoming events that trigger the Tx LSM, although the order of treatment is implementation specific if these events appear simultaneously? | | M | (R-78) | Yes_X_No__ |
| IIO.7 | Does the implementation signal the current state of the Rx LSM to the FE IMA unit via the ICP cells? | | M | (R-78) | Yes_X_No__ |
| IIO.8 | Does the implementation perform the actions corresponding to the Rx LSM sub-states? | | M | (R-78) | Yes_X_No__ |
| IIO.9 | Does the implementation update the Rx LSM according the occurrence of the events listed in Table 9 on page 53? | | M | (R-78) | Yes_X_No__ |
| IIO.10 | Does the implementation treat sequentially the incoming events that trigger the Rx LSM, although the order of treatment is implementation specific if these events appear simultaneously? | | M | (R-78) | Yes_X_No__ |
| IIO.11 | Does the implementation report any change of the Tx and Rx LSMs within the next 2*M (where M is the M used by the IMA transmitter) cells on that link over the "Tx State" and "Rx State" fields of the Link Information field (refer to Table 3 on page 32)? | | M | (R-79) | Yes_X_No__ |
| IIO.12 | Does the implementation use one of the Unusable encodings when reporting the Unusable state? | | M | (R-80) | Yes_X_No__ |
| IIO.13 | Does the implementation use "Inhibited", "Failed", "Fault" or "Mis-connected" as a reason when reporting the Unusable state? | | O | (O-14) | Yes_X_No__ |
| IIO.14 | Does the implementation re-evaluate the TX and Rx LSMs state upon each incoming ICP cell with new state indication? | | M | (R-81) | Yes_X_No__ |
| IIO.15 | Does the implementation allow the valid combinations of Tx and Rx LSM states and disallow the invalid combinations when running in the Symmetrical Configuration and Operation mode? | | M | (R-82) | Yes_X_No__ |
| IIO.16 | Does the implementation allow the valid combinations of Tx and Rx LSM states and disallow the invalid combinations when running in the Symmetrical Configuration and Asymmetrical Operation mode? | | M | (R-82) | Yes_X_No__ |
| IIO.17 | Does the implementation allow all combinations of Tx and Rx LSM states when running in the Asymmetrical Configuration and Operation mode? | | M | (R-82) | Yes_X_No__ |
| IIO.18 | Does the implementation report any GSM states, with the exception of the Not Configured state, to the FE group using the corresponding value defined in the "Group Status and Control" field? | | M | (R-83) | Yes_X_No__ |
| IIO.19 | Does the implementation always send over each link the same value in the "Group Status and Control" field for at least 2 consecutive IMA frames? | | M | (R-84) | Yes_X_No__ |
| IIO.20 | Does the implementation validate the Rx OAM Label, Rx M, and Rx IMA ID over at least one link before moving into the Start-up-Ack state? | | M | (R-85) | Yes_X_No__ |
| IIO.21 | Does the implementation use the validated Rx OAM Label, Rx M, and Rx IMA ID to achieve IMA frame synchronization as defined in Section 11 on page 68? | | M | (R-86) | Yes_X_No__ |

Table 4-6. IMA Interface Operation (IIO) Functions (3 of 4)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--------|--|------------------|--------------|--------|--------------------|
| IIO.22 | Does the implementation ensure that at least P _{Tx} links in the transmit direction and P _{Rx} links in the received direction can be moved into the Active state before moving the GSM into the Operational state? | | M | (R-87) | Yes <u>X</u> No __ |
| IIO.23 | Does the implementation ensure that P _{Tx} is greater than zero? | | M | (R-88) | Yes <u>X</u> No __ |
| IIO.24 | Does the implementation ensure that P _{Rx} is greater than zero? | | M | (R-88) | Yes <u>X</u> No __ |
| IIO.25 | Does the implementation ensure that P _{Tx} and P _{Rx} are equal when the configured in the Symmetrical Configuration and Operation mode? | | M | (R-89) | Yes <u>X</u> No __ |
| IIO.26 | Does the implementation allow configuration of the value of P _{Tx} ? | | O | (O-15) | Yes <u>X</u> No __ |
| IIO.27 | Does the implementation allow configuration of the value of P _{Rx} ? | | O | (O-15) | Yes <u>X</u> No __ |
| IIO.28 | Does the implementation report the Config-Aborted state for at least one second when the configuration requested by the FE is unacceptable? | | M | (R-90) | Yes <u>X</u> No __ |
| IIO.29 | Does the implementation support the GSM state transitions as defined in 13 on page 60? | | M | (R-91) | Yes <u>X</u> No __ |
| IIO.30 | Does the implementation determine and report that the group is up when both the local and remote GSMs are Operational? | | M | (R-92) | Yes <u>X</u> No __ |
| IIO.31 | Does the implementation determine and report that the group is down when either the local or the remote GSM is not operational? | | M | (R-92) | Yes <u>X</u> No __ |
| IIO.32 | Does the implementation report the proper reasons why the GSM is not operational? | | M | (R-92) | Yes <u>X</u> No __ |
| IIO.33 | Does the implementation report the highest priority reason according to Table 14 on page 61? | | M | (R-92) | Yes <u>X</u> No __ |
| IIO.34 | Does the implementation report the entrance of the GTSM into the Down state to the UM and ATM Layer Management? | | M | (R-93) | Yes <u>X</u> No __ |
| IIO.35 | Is the report of the entrance of the GTSM into the Down state the only notification to the ATM Layer Management about Physical Layer defects or failures? | | M | (R-93) | Yes <u>X</u> No __ |
| IIO.36 | Does the implementation report the return of the GTSM to the Up state to the UM and ATM Layer Management? | | M | (R-94) | Yes <u>X</u> No __ |
| IIO.37 | Does the implementation ensure it does not drop any ATM layer cells when adding or recovering links while the GSM is maintained in the Operational state? | | M | (R-95) | Yes <u>X</u> No __ |
| IIO.38 | Does the implementation ensure that it does not drop any ATM layer cells when deleting or inhibiting links while the GSM is maintained in the Operational state? | | M | (R-96) | Yes <u>X</u> No __ |
| IIO.39 | When running the group start-up procedure, does the implementation ensure that all accepted links have their states changed to Tx=Usable in the same update of the ICP cell? | | M | (R-97) | Yes <u>X</u> No __ |
| IIO.40 | When running the group start-up procedure and after the Tx state of all accepted links has been reported in a previous update of the ICP cell, does the implementation ensure that all accepted links have their states changed to Rx=Active in the same update of the ICP cell? | | M | (R-98) | Yes <u>X</u> No __ |
| IIO.41 | When running the group start-up procedure and after the Rx state of all accepted links has been reported in a previous update of the ICP cell, does the implementation ensure that all accepted links have their states changed to Tx=Active in the same update of the ICP cell? | | M | (R-99) | Yes <u>X</u> No __ |

Table 4-6. IMA Interface Operation (IIO) Functions (4 of 4)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--------|---|------------------|--------------|---------|--------------------|
| IIO.42 | When running the group start-up procedure, does the implementation wait a minimum of one second, unless all the configured links are being reported Tx=Usable by FE, before reporting links Rx=Active? | | M | (R-100) | Yes <u>X</u> No __ |
| IIO.43 | When running the group start-up procedure, does the implementation wait a minimum of one second, unless all the configured links are being reported Rx=Active by FE, before reporting links Tx=Active? | | M | (R-101) | Yes <u>X</u> No __ |
| IIO.44 | Does the implementation synchronize the insertion of new links or recovered links added using the slow recovery mechanism, defined in Section 12.1.3.1 on page 74, within the IMA RR? | | M | (R-102) | Yes <u>X</u> No __ |
| IIO.45 | Does the implementation execute only one LASR procedure per IMA group at any time (even if more than one link is inserted at the same time)? | | M | (R-103) | Yes <u>X</u> No __ |
| IIO.46 | Does the implementation delay the insertion of one or more new links or a possible slow link recovery when the LASR is in progress until the link addition procedure is completed or aborted? | | M | (R-104) | Yes <u>X</u> No __ |
| IIO.47 | When running the LASR procedure, does the implementation ensure that all the inserted links have their states changed to Tx=Usable in the same update of the ICP? | | M | (R-105) | Yes <u>X</u> No __ |
| IIO.48 | When running the LASR procedure and after the Tx state of all accepted links has been reported Usable in a previous update of the ICP cell, does the implementation ensure that all the inserted links have their states changed to Rx=Active in the same update of the ICP cell? | | M | (R-106) | Yes <u>X</u> No __ |
| IIO.49 | When running the LASR procedure and after the Rx state of all accepted links has been reported Active in a previous update of the ICP cell, does the implementation ensure that all the inserted links have their states changed to Tx=Active in the same update of the ICP cell? | | M | (R-107) | Yes <u>X</u> No __ |
| IIO.50 | When running the LASR procedure, does the implementation wait a minimum of one second, unless all the inserted links are being reported Tx=Usable by FE, before reporting links Rx=Active? | | M | (R-108) | Yes <u>X</u> No __ |
| IIO.51 | When running the LASR procedure, does the implementation wait a minimum of one second, unless the inserted links are being reported Rx=Active by FE, before reporting links Tx=Active? | | M | (R-109) | Yes <u>X</u> No __ |

Table 4-7. IMA Frame Synchronization (IFS) Mechanism Functions (1 of 2)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-------|--|------------------|--------------|---------|--------------------|
| IFS.1 | Does the implementation perform IMA frame synchronization on each link, based on the IFSM defined in Figure 19 on page 69 and Table 16 on page 69? | | M | (R-110) | Yes <u>X</u> No __ |
| IFS.2 | Does the implementation operate the IFSM for each link independently of any link defects and link delay compensation? | | M | (R-111) | Yes <u>X</u> No __ |
| IFS.3 | Does the implementation support the default value 2 for Alpha(α)? | | M | (R-112) | Yes <u>X</u> No __ |
| IFS.4 | Does the implementation support the default value 2 for Beta(β)? | | M | (R-112) | Yes <u>X</u> No __ |
| IFS.5 | Does the implementation support the default value 1 for Gamma(γ)? | | M | (R-112) | Yes <u>X</u> No __ |
| IFS.6 | Does the implementation support the value 1 for Alpha(α)? | | O | (O-16) | Yes <u>X</u> No __ |

Table 4-7. IMA Frame Synchronization (IFS) Mechanism Functions (2 of 2)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|---|---|------------------|--------------|---------|-----------------------------------|
| IFS.7 | Does the implementation support the value 1 for Beta(β)? | | 0 | (O-16) | Yes <u>X</u> No __ |
| IFS.8 | Does the implementation support the value 3 for Beta(β)? | | 0 | (O-16) | Yes <u>X</u> No __ |
| IFS.9 | Does the implementation support the value 4 for Beta(β)? | | 0 | (O-16) | Yes <u>X</u> No __ |
| IFS.10 | Does the implementation support the value 5 for Beta(β)? | | 0 | (O-16) | Yes <u>X</u> No __ |
| IFS.11 | Does the implementation support the value 2 for Gamma(γ)? | | 0 | (O-16) | Yes <u>X</u> No __ |
| IFS.12 | Does the implementation support the value 3 for Gamma(γ)? | | 0 | (O-16) | Yes <u>X</u> No __ |
| IFS.13 | Does the implementation support the value 4 for Gamma(γ)? | | 0 | (O-16) | Yes <u>X</u> No __ |
| IFS.14 | Does the implementation support the value 5 for Gamma(γ)? | | 0 | (O-16) | Yes <u>X</u> No __ |
| IFS.15 | Does the implementation assume that any occurrence of HEC/CRC errored cell in the ICP cell position was an ICP cell? | | M | (R-113) | Yes <u>X</u> No __ |
| IFS.16 | Does the implementation ignore the cell content of a HEC/CRC errored cell in the ICP cell position? | | M | (R-113) | Yes <u>X</u> No __ |
| IFS.17 | Does the implementation go into the Hunt state from any other state when no longer getting cells from the physical layer? | | 0 | (O-17) | Yes <u>X</u> No __ |
| IFS.18 | Does the implementation maintain IMA frame synchronization for cases 1, 2, 3, and 6 identified in Figure 20 on page 71? | | M | (R-114) | Yes <u>X</u> No __ |
| IFS.19 | Does the implementation maintain IMA frame synchronization for case 4 identified in Figure 20 on page 71? | | 0 | (O-18) | Yes <u>X</u> No __ Need (O-11) |
| IFS.20 | Does the implementation maintain IMA frame synchronization for case 5 identified in Figure 20 on page 71? | | 0 | (O-18) | Yes <u>X</u> No __ |
| IFS.21 | Does the implementation maintain IMA frame synchronization for case 7 identified in Figure 20 on page 71 when passing stuff indication over more than one of the previous ICP cells and when Beta(β) is greater than 2? | | 0 | (O-19) | Yes <u>X</u> No __ Need (O-11) |
| Comments: (O-11) required to support (O-18) and (O-19). | | | | | |

Table 4-8. IMA Interface OAM Operation Functions (1 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-------|---|------------------|--------------|---------|--------------------|
| OAM.1 | Does the implementation report the following link remote defect indicators: link defects, LIF, and LODS? | | M | (R-115) | Yes <u>X</u> No __ |
| OAM.2 | If several defects are detected at the same time, does the implementation report the defect with the highest priority, as listed in Table 17 on page 72? | | M | (R-116) | Yes <u>X</u> No __ |
| OAM.3 | Does the implementation report any Rx defect to the far-end IMA within the next 2*M cells to be transmitted after the defect state has been entered as specified in Section 12.1.3 on page 72 (where M is the M used by the IMA transmitter)? | | M | (R-117) | Yes <u>X</u> No __ |
| OAM.4 | Does the implementation perform error handling as specified in Figure 21 on page 73 and Figure 22 on page 74? | | M | (R-118) | Yes <u>X</u> No __ |
| OAM.5 | On a given link, does the implementation pass to the ATM layer from the IMA sublayer any cells accumulated before the occurrence of an OCD or OIF anomaly on that link? | | M | (R-119) | Yes <u>X</u> No __ |

Table 4-8. IMA Interface OAM Operation Functions (2 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--------|--|------------------|--------------|---------|--------------------|
| OAM.6 | Does the implementation inhibit the passing from the IMA sublayer to the ATM layer of any cells received on a link during an OCD or OIF anomaly condition reported on that link? | | M | (R-120) | Yes <u>X</u> No __ |
| OAM.7 | Does the implementation replace with Filler cells all ATM layer cells received on a link after an OCD or OIF anomaly condition has been detected on that link? | | M | (R-121) | Yes <u>X</u> No __ |
| OAM.8 | Does the implementation only report an Rx defect in the backward direction after LIF or LODS defect state is entered? | | M | (R-122) | Yes <u>X</u> No __ |
| OAM.9 | Does the implementation report the LIF or LODS defect as specified in Section 12.1.2 on page 72? | | M | (R-123) | Yes <u>X</u> No __ |
| OAM.10 | Does the implementation detect errored ICP cells as indicated in Table 18 on page 77? | | M | (R-124) | Yes <u>X</u> No __ |
| OAM.11 | Does the implementation detect invalid ICP cells as indicated in Table 18 on page 77? | | M | (R-124) | Yes <u>X</u> No __ |
| OAM.12 | Does the implementation detect missing ICP cells as indicated in Table 18 on page 77? | | M | (R-124) | Yes <u>X</u> No __ |
| OAM.13 | Does the implementation report OIF events as indicated in Table 18 on page 77? | | M | (R-124) | Yes <u>X</u> No __ |
| OAM.14 | Does the implementation report LIF defects as indicated in Table 18 on page 77? | | M | (R-124) | Yes <u>X</u> No __ |
| OAM.15 | Does the implementation report LODS defects as indicated in Table 18 on page 77? | | M | (R-124) | Yes <u>X</u> No __ |
| OAM.16 | Does the implementation report RDI-IMA defects as indicated in Table 18 on page 77? | | M | (R-124) | Yes <u>X</u> No __ |
| OAM.17 | Does the implementation increment IV-IMA for every detected errored, invalid or missing ICP cell, except during seconds when a SES-IMA or UAS-IMA condition is reported, as indicated in Table 19 on page 77? | | M | (R-125) | Yes <u>X</u> No __ |
| OAM.18 | Does the implementation increment OIF-IMA for each reported OIF anomaly, except during seconds when a SES-IMA or UAS-IMA condition is reported, as indicated in Table 19 on page 77? | | O | (O-20) | Yes <u>X</u> No __ |
| OAM.19 | Does the implementation increment SES-IMA for every one second interval containing $\geq 30\%$ of the ICP cells counted as IV-IMA, as indicated in Table 19 on page 77? | | M | (R-126) | Yes <u>X</u> No __ |
| OAM.20 | Does the implementation increment SES-IMA for every one interval of one second containing one or more link defects (e.g., LOS, OOF/LOF, AIS, and LCD), except during seconds when an UAS-IMA condition is reported, as indicated in Table 19 on page 77? | | M | (R-126) | Yes <u>X</u> No __ |
| OAM.21 | Does the implementation increment SES-IMA for every one second interval containing one or more LIF link defects, except during seconds when an UAS-IMA condition is reported, as indicated in Table 19 on page 77? | | M | (R-126) | Yes <u>X</u> No __ |
| OAM.22 | Does the implementation increment SES-IMA for every one second interval containing one or more LODS link defects, except during seconds when a UAS-IMA condition is reported, as indicated in Table 19 on page 77? | | M | (R-126) | Yes <u>X</u> No __ |

Table 4-8. IMA Interface OAM Operation Functions (3 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--------|---|------------------|--------------|---------|--------------------|
| OAM.23 | Does the implementation increment SES-IMA-FE for every one second interval containing one or more RDI-IMA defect, except during seconds when a UAS-IMA-FE condition is reported, as indicated in Table 19 on page 77? | | M | (R-127) | Yes <u>X</u> No __ |
| OAM.24 | Does the period of NE unavailability begin at the onset of 10 contiguous SES-IMA (including the first 10 seconds to enter the UAS-IMA condition), as indicated in Table 19 on page 77? | | M | (R-128) | Yes <u>X</u> No __ |
| OAM.25 | Does the period of NE unavailability end at the onset of 10 contiguous seconds with no SES-IMA (excluding the last 10 seconds to exit the UAS-IMA condition), as indicated in Table 19 on page 77? | | M | (R-128) | Yes <u>X</u> No __ |
| OAM.26 | Does the implementation increment UAS-IMA for each one second interval when the UAS-IMA condition is reported, as indicated in Table 19 on page 77? | | M | (R-128) | Yes <u>X</u> No __ |
| OAM.27 | Does the period of FE unavailability begin at the onset of 10 contiguous SES-IMA (including the first 10 seconds to enter the UAS-IMA condition), as indicated in Table 19 on page 77? | | M | (R-129) | Yes <u>X</u> No __ |
| OAM.28 | Does the period of FE unavailability end at the onset of 10 contiguous seconds with no SES-IMA-FE (excluding the last 10 seconds to exit the UAS-IMA-FE condition), as indicated in Table 19 on page 77? | | M | (R-129) | Yes <u>X</u> No __ |
| OAM.29 | Does the implementation increment UAS-IMA-FE for each one second interval when the UAS-IMA-FE condition is reported, as indicated in Table 19 on page 77? | | M | (R-129) | Yes <u>X</u> No __ |
| OAM.30 | Does the implementation increment Tx-UUS-IMA for each second when the NE Tx LSM is Unusable, as indicated in Table 19 on page 77? | | M | (R-130) | Yes <u>X</u> No __ |
| OAM.31 | Does the implementation increment Rx-UUS-IMA for each second when the NE Rx LSM is Unusable, as indicated in Table 19 on page 77? | | M | (R-131) | Yes <u>X</u> No __ |
| OAM.32 | Does the implementation increment Tx-UUS-IMA-FE for each second when the FE Tx LSM is reported Unusable, as indicated in Table 19 on page 77? | | M | (R-132) | Yes <u>X</u> No __ |
| OAM.33 | Does the implementation increment Rx-UUS-IMA-FE for each second when the FE Rx LSM is reported Unusable, as indicated in Table 19 on page 77? | | M | (R-133) | Yes <u>X</u> No __ |
| OAM.34 | Does the implementation increment Tx-FC each time the Tx-Mis-Connected link failure condition is entered, as indicated in Table 19 on page 77? | | M | (R-134) | Yes <u>X</u> No __ |
| OAM.35 | Does the implementation increment Tx-FC each time the Tx-Fault link failure condition is entered, as indicated in Table 19 on page 77? | | M | (R-134) | Yes <u>X</u> No __ |
| OAM.36 | Does the implementation increment Rx-FC each time the LIF link failure condition is entered, as indicated in Table 19 on page 77? | | M | (R-135) | Yes <u>X</u> No __ |
| OAM.37 | Does the implementation increment Rx-FC each time the LODS link failure condition is entered, as indicated in Table 19 on page 77? | | M | (R-135) | Yes <u>X</u> No __ |
| OAM.38 | Does the implementation increment Rx-FC each time the Rx-Mis-Connected link failure condition is entered, as indicated in Table 19 on page 77? | | M | (R-135) | Yes <u>X</u> No __ |
| OAM.39 | Does the implementation increment Rx-FC each time the Rx-Fault link failure condition is entered, as indicated in Table 19 on page 77? | | M | (R-135) | Yes <u>X</u> No __ |
| OAM.40 | Does the implementation increment Tx-FC-FE each time the Tx-Unusable-FE link failure condition is entered, as indicated in Table 19 on page 77? | | O | (O-21) | Yes <u>X</u> No __ |

Table 4-8. IMA Interface OAM Operation Functions (4 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--------|--|------------------|--------------|---------|--------------------|
| OAM.41 | Does the implementation increment Rx-FC-FE each time the RFI-IMA link failure condition is entered, as indicated in Table 19 on page 77? | | 0 | (O-22) | Yes <u>X</u> No __ |
| OAM.42 | Does the implementation increment Rx-FC-FE each time the Rx-Unusable-FE link failure condition is entered, as indicated in Table 19 on page 77? | | 0 | (O-22) | Yes <u>X</u> No __ |
| OAM.43 | Does the implementation increment Tx-Stuff-IMA for each stuff event inserted in the transmit direction, as indicated in Table 19 on page 77? | | 0 | (O-23) | Yes <u>X</u> No __ |
| OAM.44 | Does the implementation increment Rx-Stuff-IMA for each stuff event detected in the receive direction, except during seconds when a SES-IMA or UAS-IMA condition is reported, as indicated in Table 19 on page 77? | | 0 | (O-24) | Yes <u>X</u> No __ |
| OAM.45 | Does the implementation increment GR-UAS-IMA for each second when the GTSM is down, as indicated in Table 19 on page 77? | | M | (R-136) | Yes <u>X</u> No __ |
| OAM.46 | Does the implementation increment GR-FC each time the Config-Aborted group failure condition is entered, as indicated in Table 19 on page 77? | | M | (R-137) | Yes <u>X</u> No __ |
| OAM.47 | Does the implementation increment GR-FC each time the Insufficient-Links group failure condition is entered, as indicated in Table 19 on page 77? | | M | (R-137) | Yes <u>X</u> No __ |
| OAM.48 | Does the implementation increment GR-FC-FE each time the Start-up-FE group failure condition is entered, as indicated in Table 19 on page 77? | | 0 | (O-25) | Yes <u>X</u> No __ |
| OAM.49 | Does the implementation increment GR-FC-FE each time the Config-Aborted-FE group failure condition is entered, as indicated in Table 19 on page 77? | | 0 | (O-25) | Yes <u>X</u> No __ |
| OAM.50 | Does the implementation increment GR-FC-FE each time the Insufficient-Links-FE group failure condition is entered, as indicated in Table 19 on page 77? | | 0 | (O-25) | Yes <u>X</u> No __ |
| OAM.51 | Does the implementation increment GR-FC-FE each the Blocked-FE group failure condition is entered, as indicated in Table 19 on page 77? | | 0 | (O-25) | Yes <u>X</u> No __ |
| OAM.52 | Does the implementation accumulate IMA performance parameters over 15 minute intervals? | | 0 | (O-26) | Yes <u>X</u> No __ |
| OAM.53 | Does the implementation accumulate IMA performance parameters over 24 hour intervals? | | 0 | (O-27) | Yes __ No <u>X</u> |
| OAM.54 | Does the implementation keep the current/previous and recent data? | (O-26) | M | (CR-7) | Yes <u>X</u> No __ |
| OAM.55 | Does the implementation use the current data for threshold crossing? | (O-26) | M | (CR-8) | Yes __ No <u>X</u> |
| OAM.56 | Does the implementation keep the current/previous and recent data? | (O-27) | M | (CR-9) | Yes __ No <u>X</u> |
| OAM.57 | Does the implementation use the current data for threshold crossing? | (O-27) | M | (CR-10) | Yes __ No <u>X</u> |
| OAM.58 | Does the implementation report a LIF failure alarm for the persistence of a LIF defect at the NE? | | M | (R-138) | Yes <u>X</u> No __ |
| OAM.59 | Does the implementation report a LODS failure alarm for the persistence of a LODS defect at the NE? | | M | (R-139) | Yes <u>X</u> No __ |
| OAM.60 | Does the implementation report a RFI-IMA failure alarm for the persistence of a RDI-IMA defect at the NE? | | M | (R-140) | Yes <u>X</u> No __ |
| OAM.61 | Does the implementation report Tx-Mis-Connected failure alarm when the Tx link is detected as mis-connected? | | M | (R-141) | Yes <u>X</u> No __ |
| OAM.62 | Does the implementation report Rx-Mis-Connected failure alarm when the Rx link is detected as mis-connected? | | M | (R-142) | Yes <u>X</u> No __ |

Table 4-8. IMA Interface OAM Operation Functions (5 of 5)

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|---|--|------------------|--------------|---------|------------|
| OAM.63 | Does the implementation report a Tx Fault failure alarm for any implementation specific Tx fault declared at the NE? | | O | (O-28) | Yes_X_No__ |
| OAM.64 | Does the implementation report a Rx Fault failure alarm for any implementation specific Rx fault declared at the NE? | | O | (O-29) | Yes_X_No__ |
| OAM.65 | Does the implementation report a Tx-Unusable-FE failure alarm when it receives Tx-Unusable from FE? | | M | (R-143) | Yes_X_No__ |
| OAM.66 | Does the implementation report a Rx-Unusable-FE failure alarm when it receives Rx-Unusable from FE? | | M | (R-144) | Yes_X_No__ |
| OAM.67 | Does the implementation report a Start-up-FE failure alarm when it receives this signal from FE (the declaration of this failure alarm may be delayed to ensure the FE remains in Start-up)? | | M | (R-145) | Yes_X_No__ |
| OAM.68 | Does the implementation report a Config-Aborted failure alarm when the FE tries to use unacceptable configuration parameters? | | M | (R-146) | Yes_X_No__ |
| OAM.69 | Does the implementation report a Config-Aborted-FE failure alarm when the FE reports unacceptable configuration parameters? | | M | (R-147) | Yes_X_No__ |
| OAM.70 | Does the implementation report an Insufficient-Links failure alarm when less than P _{Tx} transmit links or P _{Rx} receive links are active? | | M | (R-148) | Yes_X_No__ |
| OAM.71 | Does the implementation report an Insufficient-Links-FE failure alarm when the FE reports that less than P _{Tx} transmit links or P _{Rx} receive links are active? | | M | (R-149) | Yes_X_No__ |
| OAM.72 | Does the implementation report a Blocked-FE failure alarm when the FE reports that it is blocked? | | M | (R-150) | Yes_X_No__ |
| OAM.73 | Does the implementation report GR-Timing-Mismatch when the FE transmit clock mode is different than the NE transmit clock mode? | | M | (R-151) | Yes_X_No__ |
| OAM.74 | In the case of the LIF, LODS, RFI-IMA and Fault failure alarms, does the implementation support 2.5 ± 0.5 seconds as a default persistence checking time to enter a failure alarm condition? | | M | (R-152) | Yes_X_No__ |
| OAM.75 | In the case of the LIF, LODS, RFI-IMA and Fault failure alarms, does the implementation support 10 ± 0.5 seconds as a default persistence clearing time to exit the failure alarm condition? | | M | (R-152) | Yes_X_No__ |
| OAM.76 | In the case of the LIF, LODS, RFI-IMA and Fault failure alarms, does the IMA allow configuration of other values for default persistence checking time to enter a failure alarm condition? | | O | (O-30) | Yes_X_No__ |
| OAM.77 | In the case of the LIF, LODS, RFI-IMA and Fault failure alarms, does the IMA allow configuration of other values for default persistence checking time to exit the same failure alarm condition? | | O | (O-30) | Yes_X_No__ |
| OAM.78 | Does the implementation ensure that the Tx-Fault failure alarm, as defined in (O-28) on page 79, is not cleared until the fault that led to the declaration of the alarm is no longer present for the duration specified to clear the alarm in (R-152) on page 80? | (O-28) | M | (CR-11) | Yes_X_No__ |
| OAM.79 | Does the implementation ensure that the Rx-Fault failure alarm, as defined in (O-29) on page 79, is not cleared until the fault that led to the declaration of the alarm is no longer present for the duration specified to clear the alarm in (R-152) on page 80? | (O-29) | M | (CR-12) | Yes_X_No__ |
| Comments: 24 hour PM intervals require external software. No threshold crossing feature in driver. Link Fault failures are not defined in standard. | | | | | |

Table 4-9. Test Pattern Procedure (TPP) Functions

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|-----------|--|------------------|--------------|---------|--------------------|
| TPP.1 | Does the implementation activate the Test Pattern procedure in the transmit direction? | | 0 | (0-31) | Yes <u>X</u> No __ |
| TPP.2 | Does the implementation use the Test Link Command field in the ICP cell (as defined in the Tx Test Control field in Table 2 on page 31) to request the FE to activate the loop back of the test pattern contained in the Tx Test Pattern field? | (0-31) | M | (CR-12) | Yes <u>X</u> No __ |
| TPP.3 | Does the implementation use the Tx LID field defined in the Tx Test Control field in Table 2 on page 31 to identify to the FE which transmit link the FE should extract the Tx Test Pattern from in the received ICP cells? | (0-31) | M | (CR-12) | Yes <u>X</u> No __ |
| TPP.4 | Does the implementation send any changed values of the Test Link Command, Tx LID and Tx Test Pattern fields in ICP cells for at least 2 consecutive IMA frames over each link within the IMA group? | (0-31) | M | (CR-12) | Yes <u>X</u> No __ |
| TPP.5 | Does the implementation continue to send the same values of the Test Link Command, Tx LID and Tx Test Pattern fields as long as the IMA transmitter wants the FE IMA unit to loop back the test pattern? | (0-31) | M | (CR-12) | Yes <u>X</u> No __ |
| TPP.6 | Does the implementation monitor the incoming ICP cells on the links already recognized in the group to detect a change of the Test Link Command? | | M | (R-153) | Yes <u>X</u> No __ |
| TPP.7 | If the Test Link Command field is detected as active over the links already recognized in the group and over the test link, does the implementation copy the value of the Tx Test Pattern field received from the test link, indicated over the Tx LID field, into the Rx Test Pattern field on every subsequent ICP cell sent over all outgoing links in the group? | | M | (R-154) | Yes <u>X</u> No __ |
| TPP.8 | Does the implementation continue sending the same value over the Rx Test Pattern field until the IMA transmitter has received an indication to stop looping the pattern, to loop a new pattern received from the same link over the Tx Test Pattern, or to loop the test pattern received from another link (indicated over the Tx LID field)? | | M | (R-155) | Yes <u>X</u> No __ |
| TPP.9 | Does the implementation return the "0xFF" pattern over the Rx Test Pattern field when the incoming test command is inactive or the test link is not detected? | | M | (R-156) | Yes <u>X</u> No __ |
| TPP.10 | Does the implementation only handle one test pattern per IMA group at any given time? | | M | (R-157) | Yes <u>X</u> No __ |
| Comments: | | | | | |

Table 4-10. IMA Interaction with Plane Management Functions

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|--|--|------------------|--------------|---------|--------------------|
| IPM.1 | Does the implementation process IMA group configuration indications received from the Plane Management? | | M | (R-158) | Yes <u>X</u> No __ |
| IPM.2 | Does the implementation process IMA link addition/deletion indications received from the Plane Management? | | M | (R-158) | Yes <u>X</u> No __ |
| IPM.3 | Does the implementation send IMA service operational status change indications to the Plane Management? | | M | (R-158) | Yes <u>X</u> No __ |
| IPM.4 | Does the implementation send Tx/Rx cell rate change indications to the Plane Management? | | M | (R-158) | Yes <u>X</u> No __ |
| Comments: Plane Management software required to interface with driver API. | | | | | |

Table 4-11. Management Information Base (MIB) Functions

| Item | Protocol feature | Cond. for Status | Status Pred. | Ref. | Support |
|---|--|------------------|--------------|---------|--------------------|
| MIB.1 | Does the implementation support a UM based on SNMP? | | 0 | (O-32) | Yes <u>X</u> No __ |
| MIB.2 | Does the implementation implement the mandatory objects in the IMA-MIBs defined in Appendix A on page 106? | (O-32) | M | (CR-17) | Yes __ No <u>X</u> |
| MIB.3 | Does the implementation implement the optional objects in the IMA MIBs defined in Appendix A on page 106? | (O-32) | 0 | (O-33) | Yes __ No <u>X</u> |
| Comments: Support for MIB objects implemented. Requires SNMP agent software to create MIB using driver API. | | | | | |

4.1.6 PICS Proforma References

1. The ATM Forum, AF-PHY-0086.001, Inverse Multiplexing for ATM (IMA) Specification Version 1.1.
2. ISO/IEC 9646-1: 1990, Information technology - Open systems interconnection - Conformance testing methodology and framework - Part 1: General concepts (See also ITU-T Recommendation X.290 (1991)).
3. ISO/IEC 9646-2: 1990, Information technology - Open systems interconnection - Conformance testing methodology and framework - Part 2: Abstract test suite specification (See also ITU-T Recommendation X.291 (1991)).
4. ITU-T Recommendation I.432 Series, “B-ISDN User-Network Interface - Physical Layer Specification”, April 1996.
5. ITU-T Recommendation I.610, “B-ISDN Operation and Maintenance Principles and Functions”, 1995.

4.2 Boundary Scan

Please contact Mindspeed for information and files for Boundary Scan.

4.3 Power Sequencing

The VGG pin provides ESD protection when interfacing with 5V systems. VGG must be connected to 5V for 5V I/O tolerance. When 5V tolerance is not required it is recommended that VGG be tied to the same power supply as VDD33.

During power up and power down the designer should take caution as VGG should not exceed VDD33 by more than 3.6V, except for short durations identified in the note below. VGG must never be less than VDD33 by more than 0.5V.

NOTE: VGG can exceed VDD33 by up to 5V ($\pm 10\%$) for short durations of less than 10 ms.
VGG must never be less than VDD33 by more than 0.5V.

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