

# NPN Epitaxial Planar Transistor

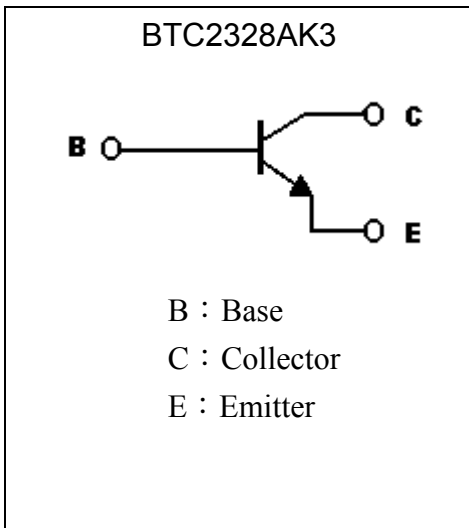
## BTC2328AK3

$BV_{CEO}$	30V
$I_C$	2A
$R_{CESAT(MAX)}$	333mΩ

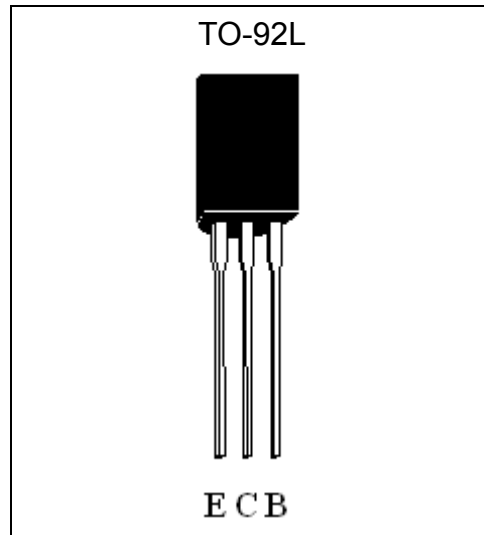
### Features

- Low Saturation Voltage,  $V_{CE(sat)}=0.5V(max)@I_C=1.5A, I_B=30mA$
- Complementary to BTA928AK3
- Pb-free lead plating and halogen-free package

### Symbol

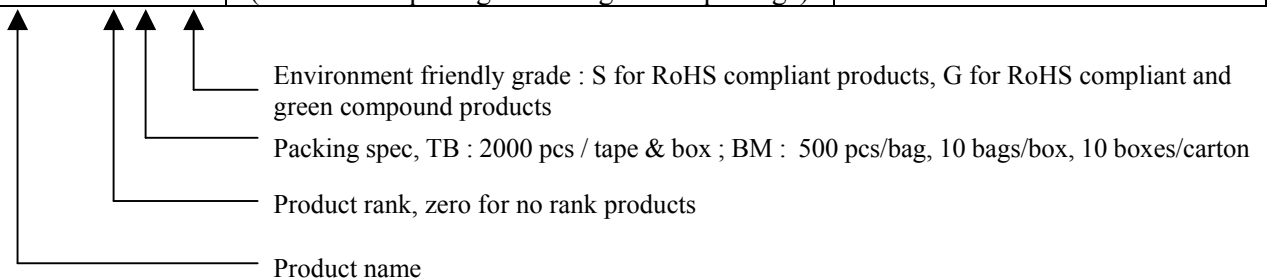


### Outline



### Ordering Information

Device	Package	Shipping
BTC2328AK3-0-TB-G	TO-92L (Pb-free lead plating and halogen-free package)	2000 pcs / tape & box
BTC2328AK3-0-BM-G	TO-92L (Pb-free lead plating and halogen-free package)	500 pcs / bag, 10 bags/box, 10 boxes/carton





**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V <sub>CBO</sub>	80	V
Collector-Emitter Voltage	V <sub>CEO</sub>	30	
Emitter-Base Voltage	V <sub>EBO</sub>	6	
Collector Current(DC)	I <sub>C</sub>	2	A
Collector Current(Pulsed) (Note 1)	I <sub>CP</sub>	5	
Base Current	I <sub>B</sub>	0.5	
Power Dissipation	P <sub>D</sub>	1	W
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	125	°C/W
Operating Junction Temperature and Storage Range	T <sub>j</sub> ; T <sub>stg</sub>	-55~+150	°C

Note 1: Single pulse, Pw≤300μs, Duty Cycle≤2%.

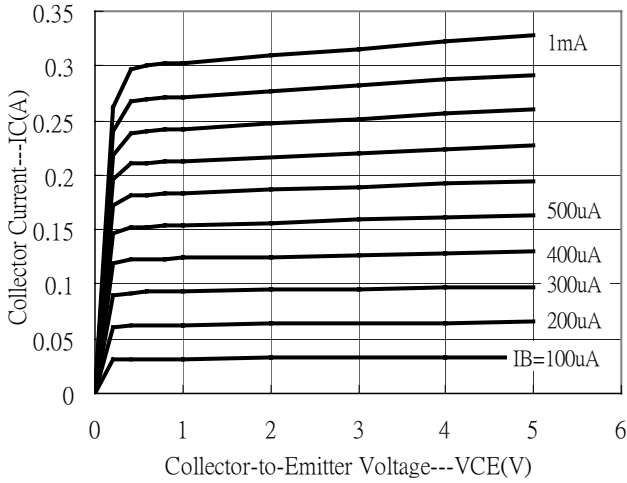
**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CBO</sub>	80	-	-	V	I <sub>C</sub> =100μA
BV <sub>CEO</sub>	30	-	-	V	I <sub>C</sub> =10mA
BV <sub>EBO</sub>	6	-	-	V	I <sub>E</sub> =100μA
I <sub>CBO</sub>	-	-	100	nA	V <sub>CB</sub> =80V
I <sub>EBO</sub>	-	-	100	nA	V <sub>EB</sub> =6V
V <sub>CE(sat)</sub> *	-	-	500	mV	I <sub>C</sub> =1.5A, I <sub>B</sub> =30mA
R <sub>CE(sat)</sub> *	-	-	333	mΩ	I <sub>C</sub> =1.5A, I <sub>B</sub> =30mA
V <sub>BE(sat)</sub> *	-	-	1.2	V	I <sub>C</sub> =1.5A, I <sub>B</sub> =30mA
V <sub>BE(on)</sub> *	-	-	1	V	V <sub>CE</sub> =2V, I <sub>C</sub> =500mA
h <sub>FE</sub> *	160	-	320	-	V <sub>CE</sub> =2V, I <sub>C</sub> =500mA
f <sub>T</sub>	120	270	-	MHz	V <sub>CE</sub> =5V, I <sub>C</sub> =500mA
C <sub>ob</sub>	-	16.5	30	pF	V <sub>CB</sub> =10V, I <sub>E</sub> =0A, f=1MHz

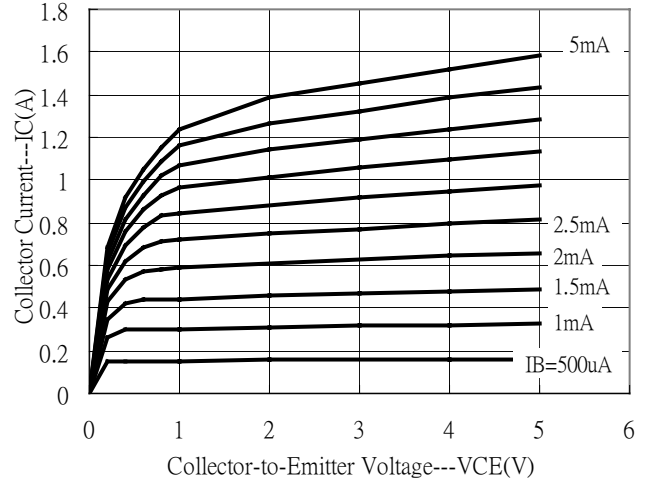
\*Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%

**Typical Characteristics**

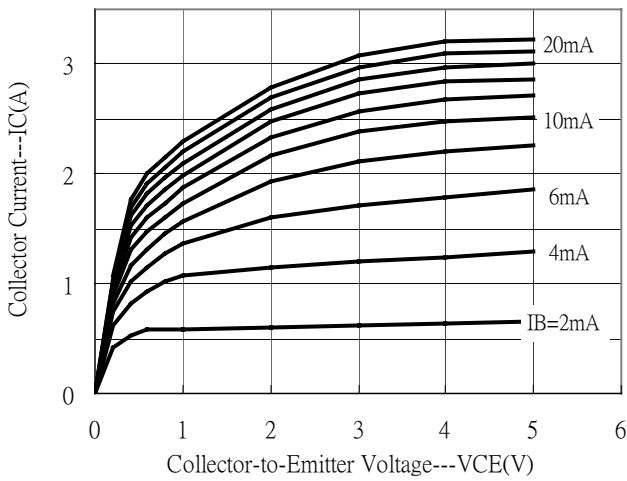
Emitter Grounded Output Characteristics



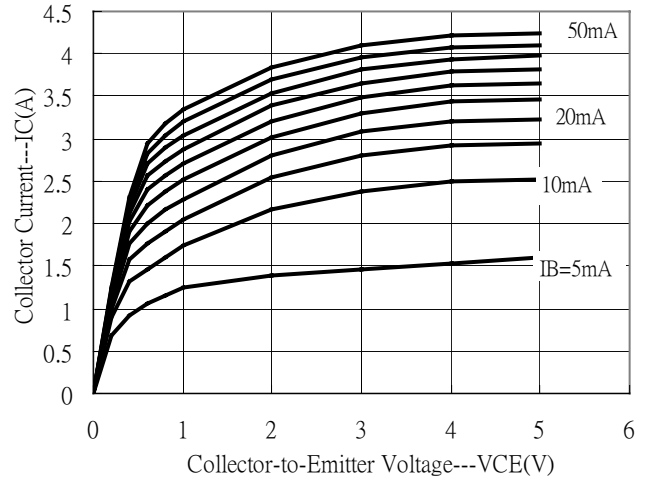
Emitter Grounded Output Characteristics



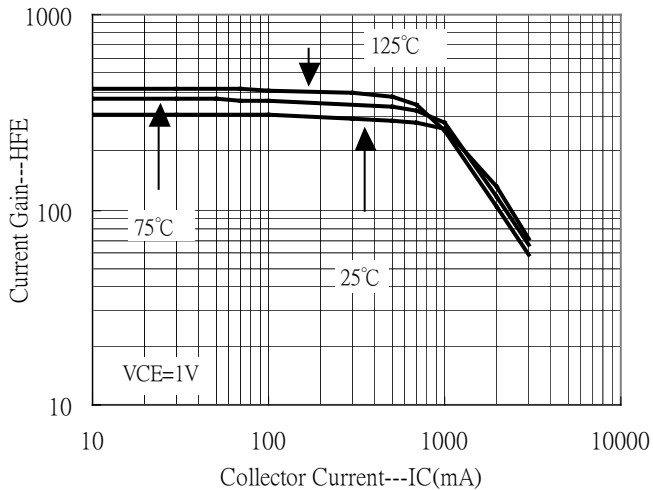
Emitter Grounded Output Characteristics



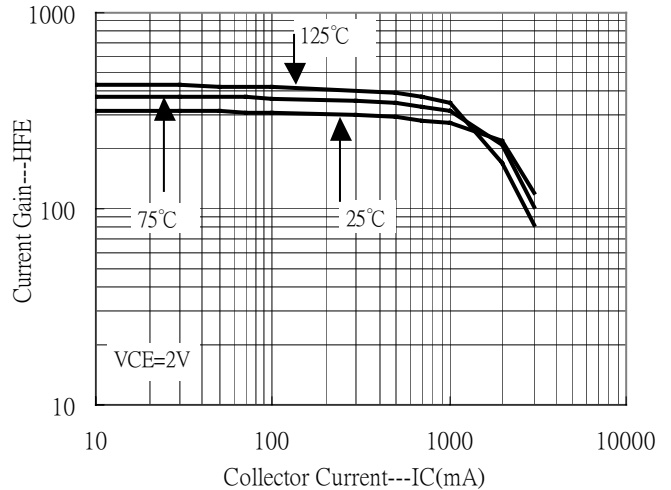
Emitter Grounded Output Characteristics



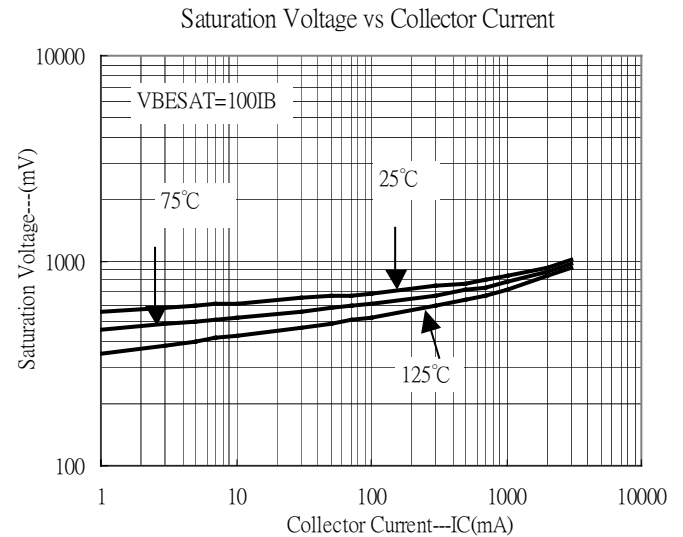
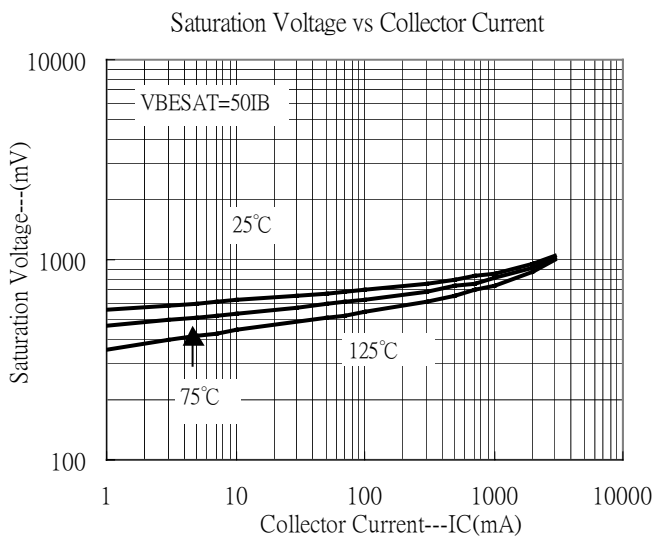
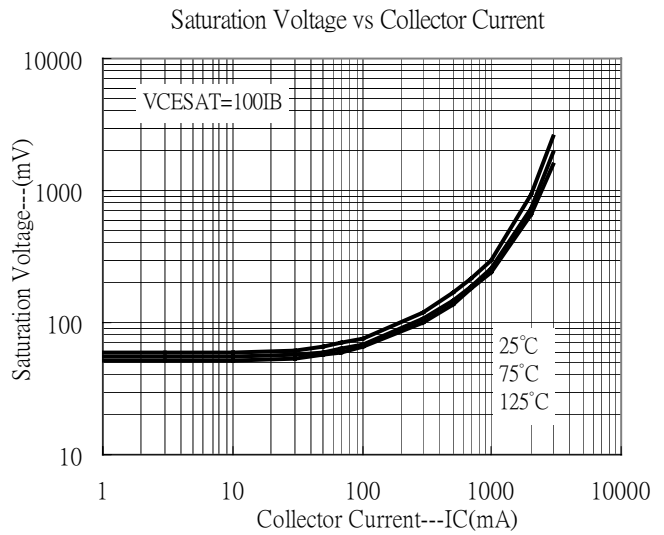
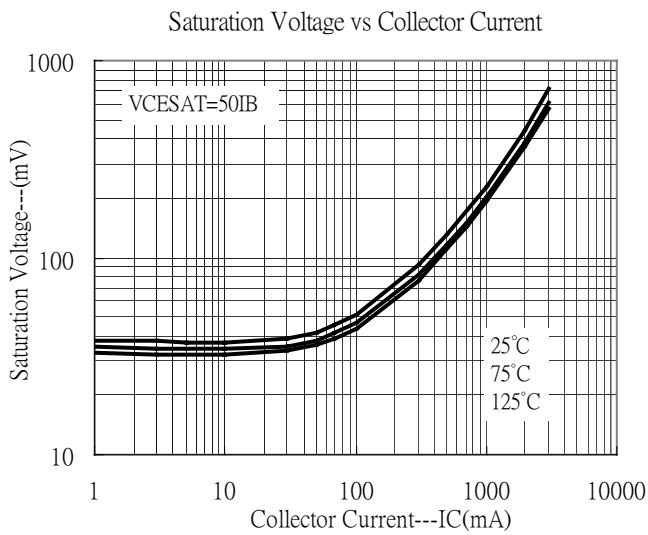
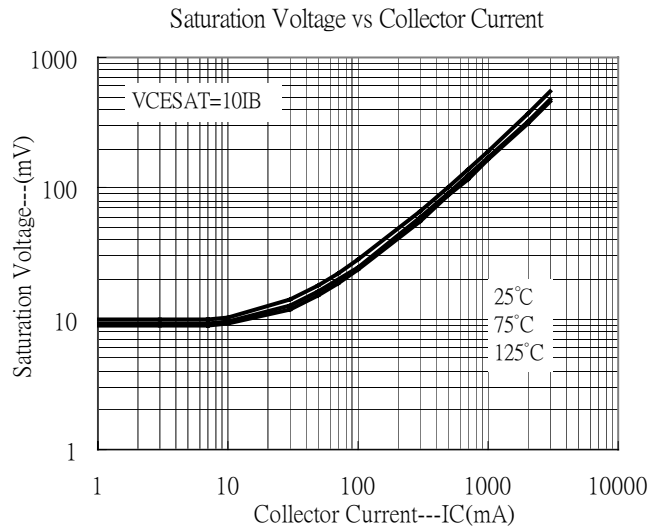
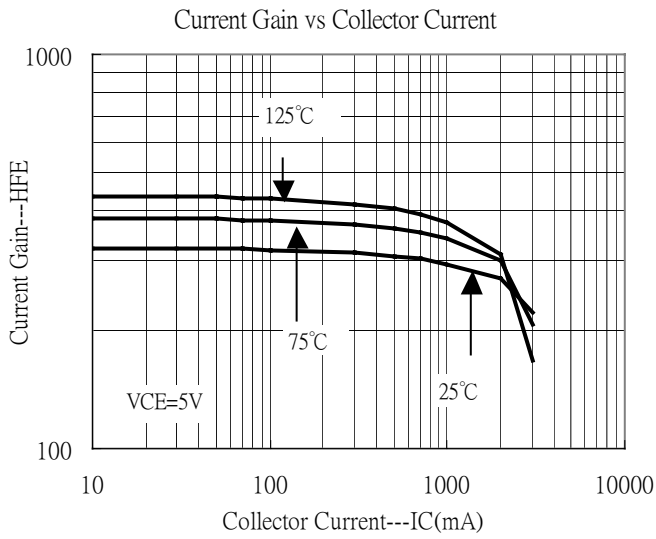
Current Gain vs Collector Current



Current Gain vs Collector Current

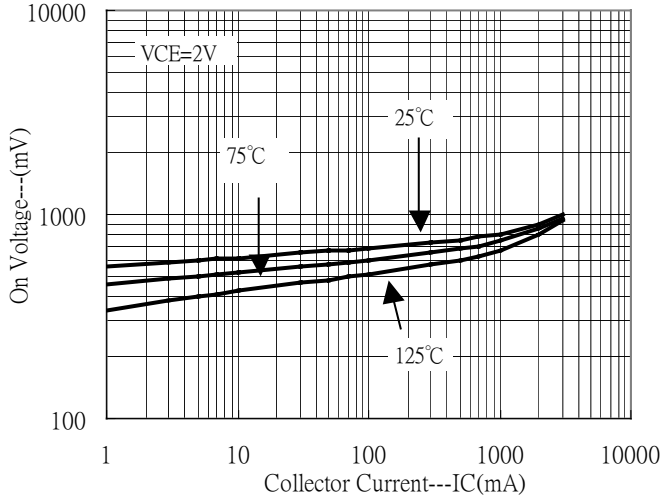


**Typical Characteristics(Cont.)**

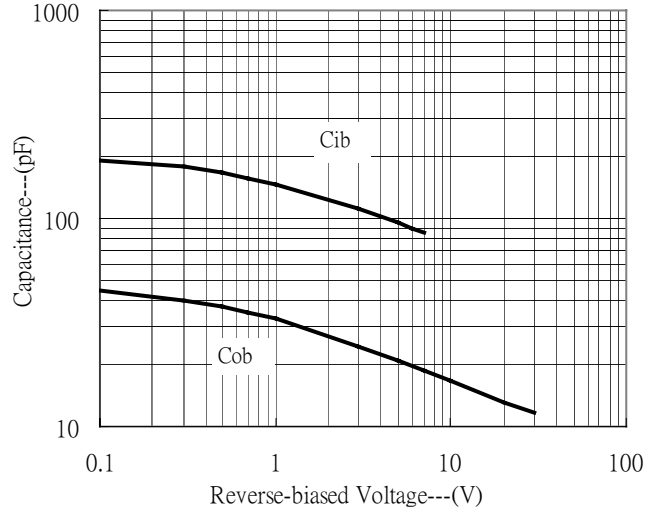


**Typical Characteristics(Cont.)**

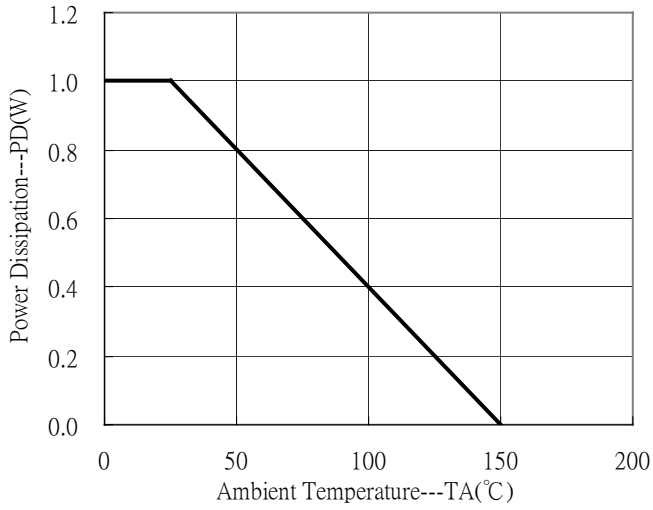
On Voltage vs Collector Current



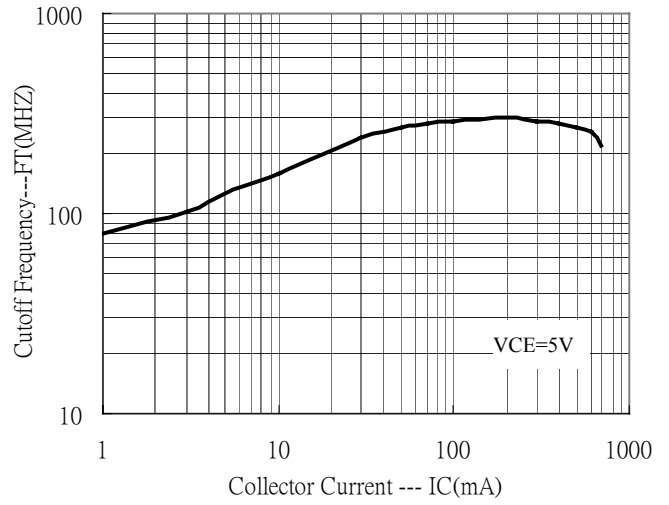
Capacitance vs Reverse-biased Voltage



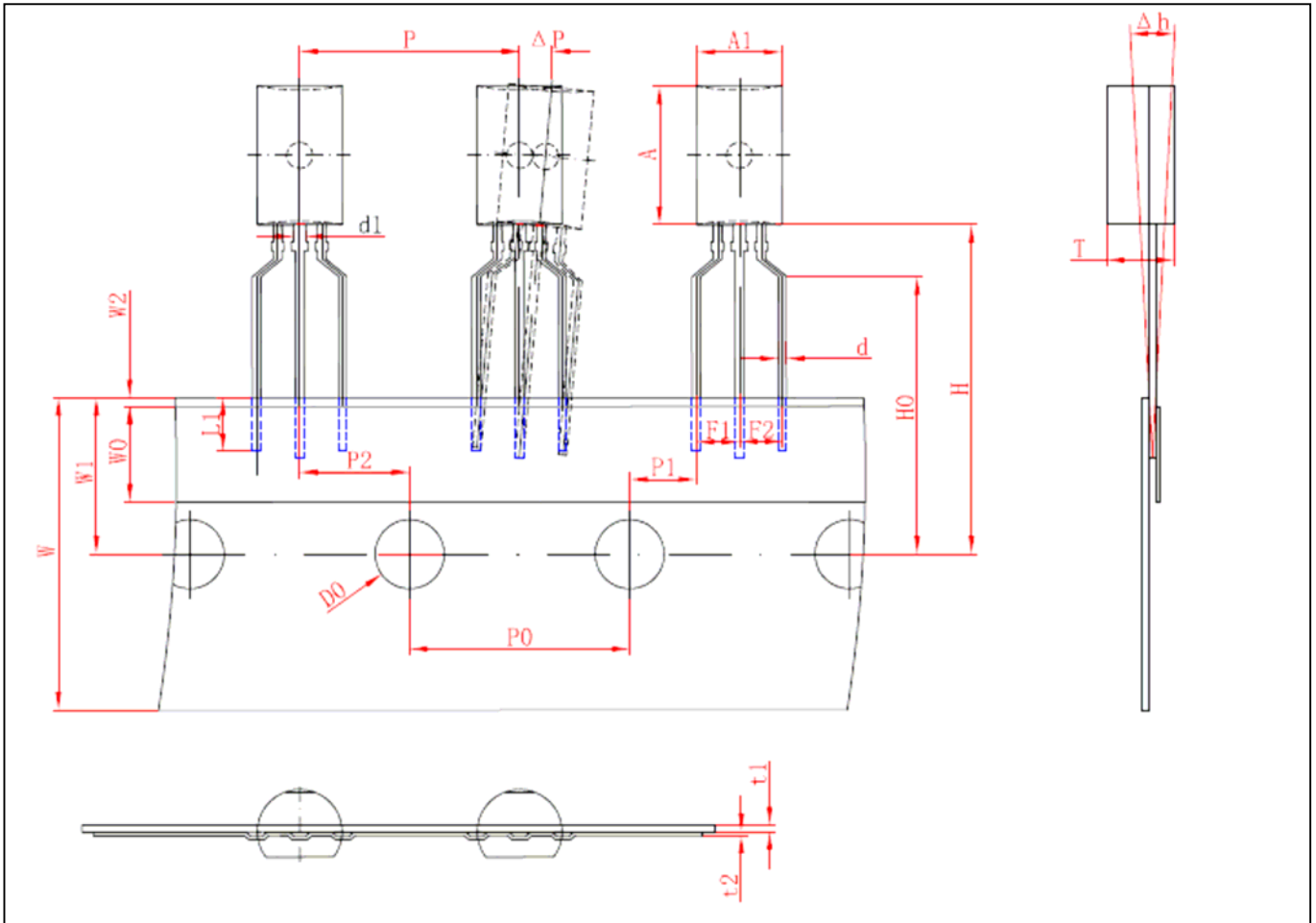
Power Derating Curve



Cutoff Frequency vs Collector Current



**TO-92L Taping Outline**

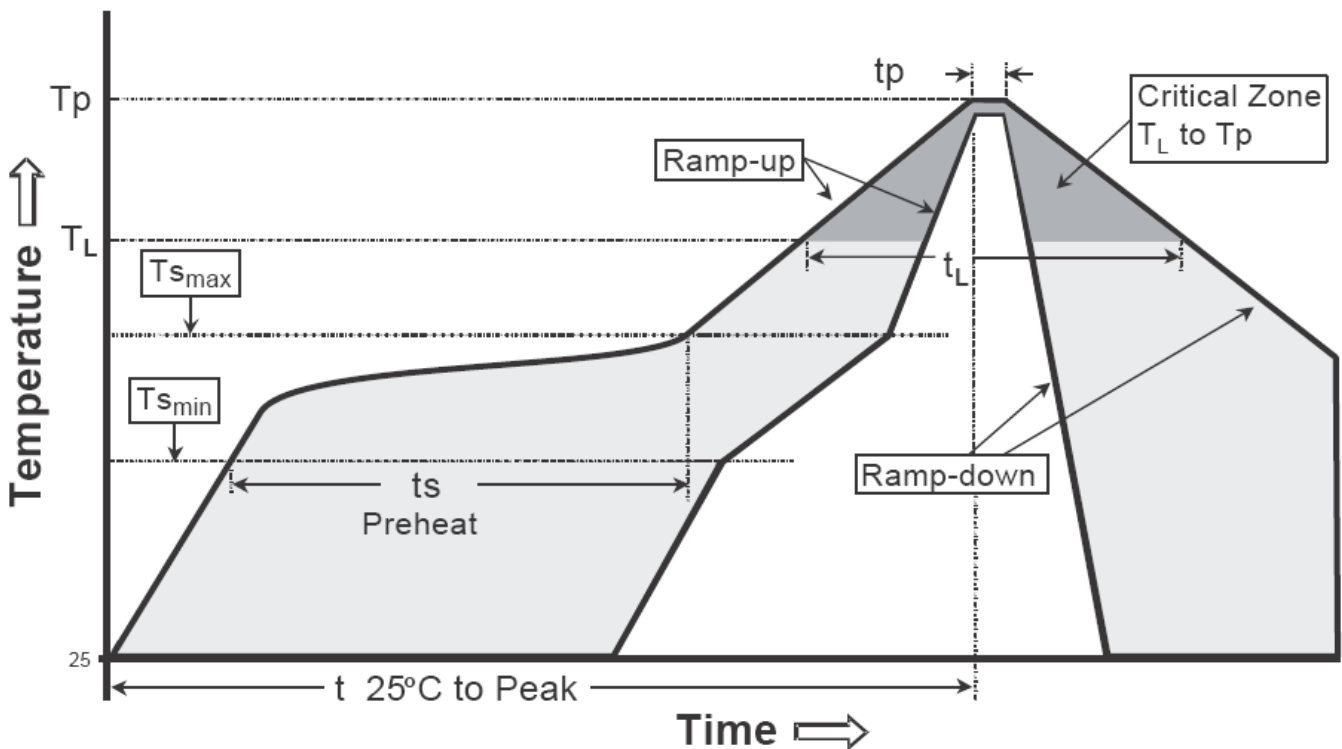


DIM	Item	Millimeters	
		Min.	Max.
A1	Component body width	4.70	5.10
A	Component body height	7.80	8.20
T	Component body thickness	3.70	4.10
d	Lead wire diameter	0.35	0.55
d1	Lead wire diameter 1	0.60	0.80
P	Pitch of component	12.40	13.00
P0	Feed hole pitch	12.50	12.90
P2	Hole center to component center	6.05	6.65
F1, F2	Lead to lead distance	2.20	2.80
Δh	Component alignment, F-R	-1.00	1.00
W	Tape width	17.50	19.00
W0	Hole down tape width	5.50	6.50
W1	Hole position	8.50	9.50
W2	Hole down tape position	-	1.00
H	Height of component from tape center	19.00	21.00
H0	Lead wire clinch height	15.50	16.50
L1	Lead wire (tape portion)	2.50	-
D0	Feed hole diameter	3.80	4.20
t1	Taped lead thickness	0.35	0.45
t2	Carrier tape thickness	0.15	0.25
P1	Position of hole	3.55	4.15
ΔP	Component alignment	-1.00	1.00

**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

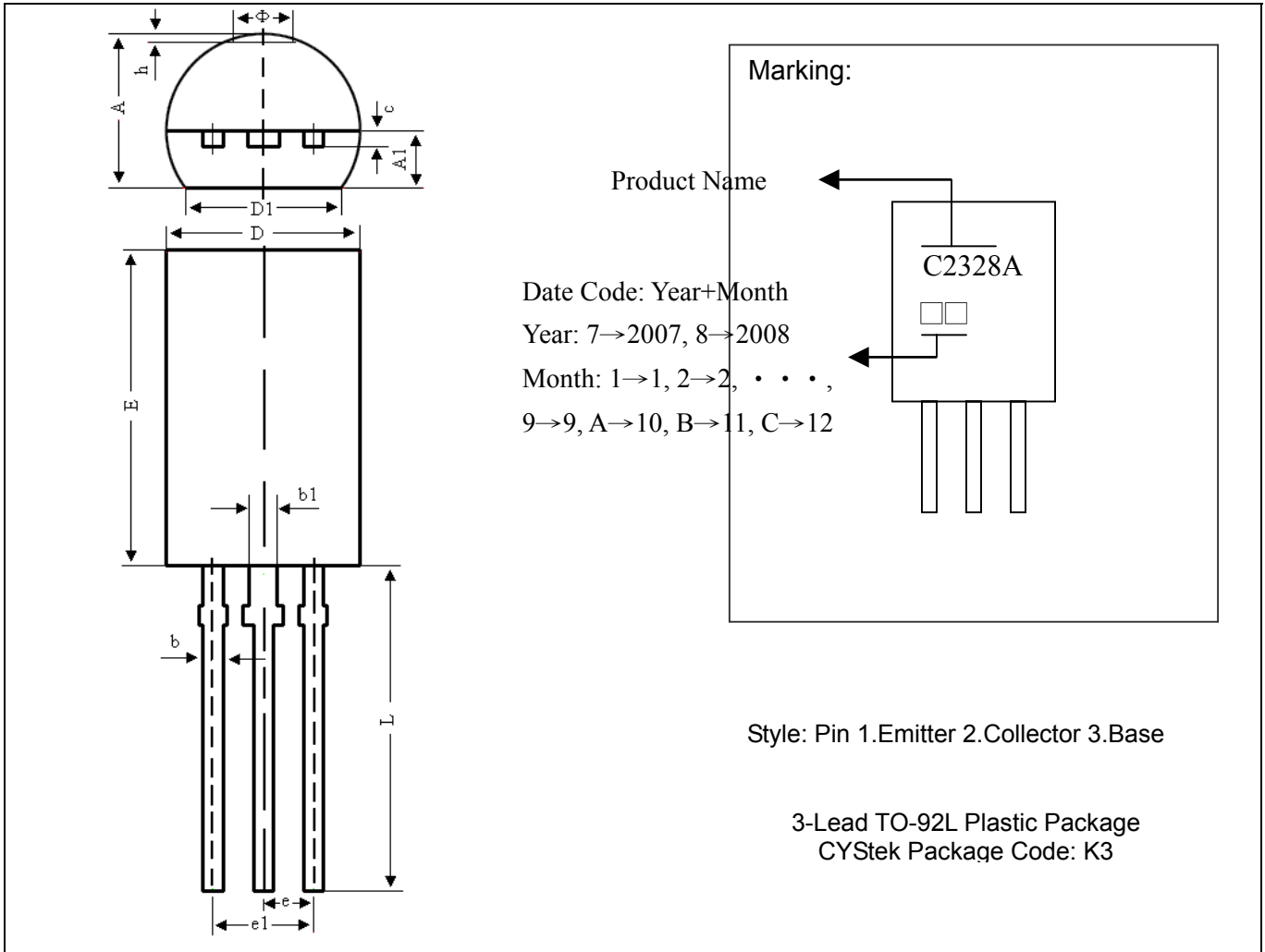
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-92L Dimension**



\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.146	0.161	3.700	4.100	E	0.307	0.323	7.800	8.200
A1	0.050	0.062	1.280	1.580	e	*0.05		*1.270	
b	0.014	0.022	0.350	0.550	e1	0.096	0.104	2.440	2.640
b1	0.024	0.031	0.600	0.800	L	0.543	0.559	13.800	14.200
c	0.014	0.018	0.350	0.450	phi	-	0.063	-	1.600
D	0.185	0.201	4.700	5.100	h	0.000	0.012	0.000	0.300
D1	0.157	-	4.000	-					

**Notes:** 1. Controlling dimension: millimeters.  
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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