Datasheet

System Power Supply ICs for Automotive Camera Modules

Camera Module System Power Supply ICs for CMOS Sensor

BD8682MUV-M

●General Description

BD8682MUV-M is a power supply for a camera module that is connected directly to the battery voltage. LDOs for the CMOS sensor, a DC/DC converter for the ISP and a wide input range step-down DC/DC converter are integrated. Furthermore, because of its integrated variable output functionality, it can be used with various configurations of CMOS sensors and ISP.
BD8682MUV-M is available in VQFN32SV5050 package, making it ideal for small camera modules.

●Features

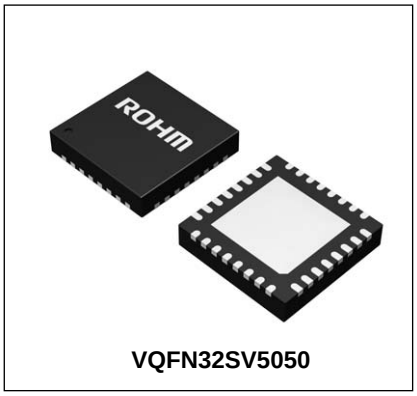
- CH1: Integrated high voltage type Nch MOSFET step-down DC/DC converter (variable output voltage via external resistors)
- CH2: Pch output LDO (selectable output: 2.8V or 3.3V)
- CH3: Pch output LDO (selectable output: 1.8V or OFF)
- CH4: Integrated Pch MOSFET step-down DC/DC converter. (selectable output: 1.5V, 1.2V, 1.8V).
- Synchronous rectification (CH1 and CH4)
- Reset for CH2 LDO
- Integrated overvoltage, undervoltage and overcurrent protection (10ms timer latch)
- 11ms off timer
- Sequence control for all outputs
- Small package: VQFN32SV5050
- AEC-Q100 Qualified

●Key Specifications

- Input voltage range: 5.9V to 40V
- Standby current: 10μA (Max.)
- Operating temperature range: -40℃ to +105℃
- Switching frequency (ch1): 500kHz (Typ.)
- Switching frequency (ch4): 1MHz (Typ.)
- Output current (ch1): 500mA (Max.)
- Output current (ch2): 130mA (Max.)
- Output current (ch3): 60mA (Max.)
- Output current (ch4): 250mA (Max.)

●Package

	W (Typ.) x D (Typ.) x H (Max.)
VQFN32SV5050	5.00mm x 5.00mm x 1.00mm



VQFN32SV5050

●Applications

Camera systems using CMOS sensors such car cameras and surveillances cameras.

●Typical Application Circuit

Application circuit schematic1

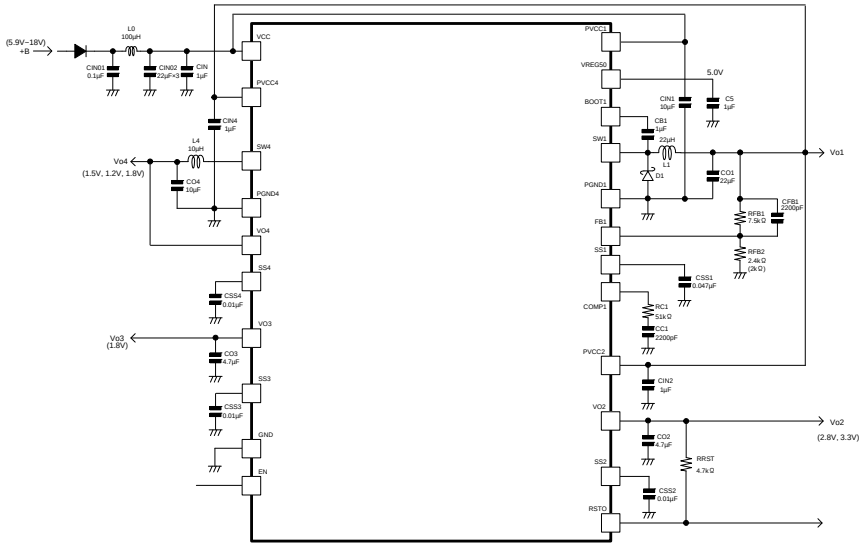


Figure 1. Application circuit schematic 1

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

●**Pin Configuration**

(TOP VIEW)

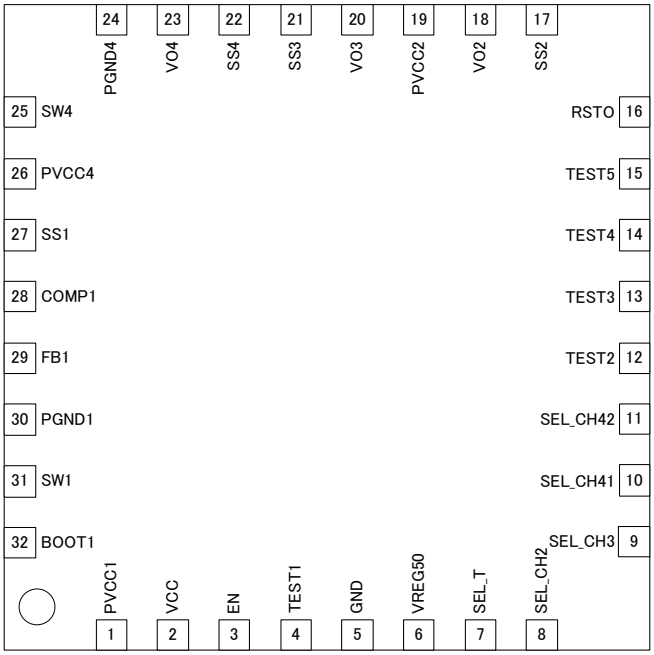


Figure 2. Pin Configuration

●**Pin Description**

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	PVCC1	Power supply pin for CH1 DC/DC	17	SS2	Soft start time setting pin for CH2 LDO
2	VCC	Power supply pin	18	VO2	Output pin for CH2 LDO
3	EN	Control pin (input for reverse signal)	19	PVCC2	Power supply pin for CH2 LDO
4	TEST1	Test pin 1	20	VO3	Output pin for CH3 LDO
5	GND	Ground pin	21	SS3	Soft start time setting pin for CH3 LDO
6	VREG50	Internal regulator output pin	22	SS4	Soft start time setting pin for CH4 DC/DC
7	SEL_T	EN mode setting pin	23	VO4	Output voltage detection pin for CH4 DC/DC
8	SEL_CH2	Output voltage select pin for CH2 LDO	24	PGND4	Power ground pin for CH4 DC/DC
9	SEL_CH3	Output voltage select pin for CH3 LDO	25	SW4	Output pin for CH4 DC/DC
10	SEL_CH41	Output voltage select pin 1 for CH4 DC/DC	26	PVCC4	Power supply pin for CH4 DC/DC
11	SEL_CH42	Output voltage select pin 2 for CH4 DC/DC	27	SS1	Soft start time setting pin for CH1 DC/DC
12	TEST2	Test pin 2	28	FB1	Error amp input pin for CH1 DC/DC
13	TEST3	Test pin 3	29	COMP1	Error amp Output pin for CH1 DC/DC
14	TEST4	Test pin 4	30	PGND1	Power ground pin for CH1 DC/DC
15	TEST5	Test pin 5	31	SW1	Output pin for CH1 DC/DC
16	RSTO	Reset output pin for CH2 LDO	32	BOOT1	Bootstrap pin for CH1 DC/DC

*Test pins 1 through 5 should be connected to ground.
SEL pins should be connected to VREG50 or ground.

●**Block Diagram**

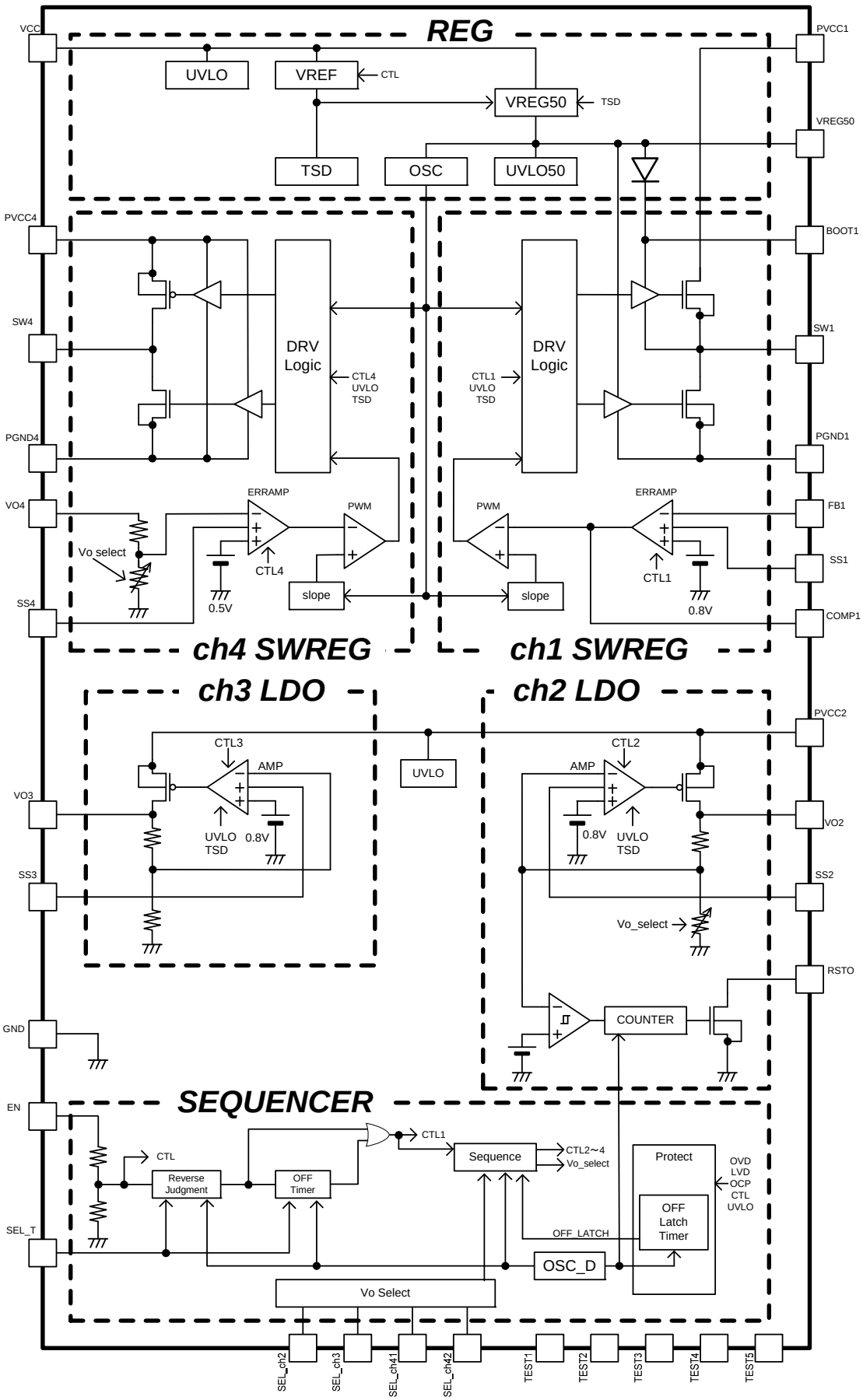


Figure 3. Block diagram

●Description of Blocks

1. Reverse determination, OFF timer block (SEL_T pin)
   When SEL_T pin is High (connected to VREG50), “Reverse determination” and “OFF Timer” are activated. Details are shown on page 12. (See Timing chart 1)
   When SEL_T pin is Low (connected to GND), “Reverse determination” and “OFF Timer” are not activated. Therefore, EN pin controls whether the circuit is ON or OFF. (See Timing chart 2)

2. Sequencer (filter)

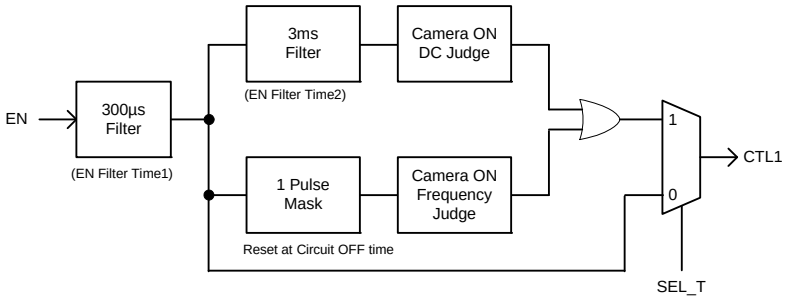


Figure 4. Sequencer Block

The Sequencer block has a “300µs filter” and a “1 pulse mask” to counter noise from the EN pin.
The “1 pulse mask” block is reset after 164ms (Typ.).
When the EN signal pulse has too high a duty cycle, i.e. the signal is not detected as a pulse by the above filter, the BD8682MUV-M will starts up in a DC determination.

3. Output voltage select block (SEL_CH2 to CH4)
   The output voltage of VO2, VO3 and VO4 are selectable by SEL_CH2, SEL_CH3, SEL_CH41 and SEL_CH42 pin. Each pin needs to be connected to VREG50 or GND for a High or Low signal respectively.

SEL_CH2	Vo2
Low	2.8V
High	3.3V

SEL_CH3	Vo3
Low	OFF
High	1.8V

SEL_CH42	SEL_CH41	Vo4
Low	Low	1.5V
Low	High	1.2V
High	Low	1.8V
High	High	Prohibit

4. VREG50 Block
   This block generates the 5V supply of the internal circuitry. This function requires an external buffer capacitor connected to the VREG50 pin. We recommend a ceramic capacitor of 1µF or higher, or one with low ESR with short leads to VREG50 pin and ground is recommended.
   VREG50 has a UVLO function. The UVLO shuts off every output and resets every timer (sequencer timer latch, and RSTO delay time).
   Note: VREG50 has a 100mA current capability (Typ.). This is only to supply to the internal circuitry. Not to supply to other circuitry.

5. Timer Latch Block
   If the following protections are activated for 10ms, “Timer Latch” is activated and the circuit is shut down as off latch.
   Protections: Overcurrent, overvoltage, short circuit (CH1)
   Overcurrent, overvoltage, undervoltage (CH2, CH3, CH4)
   To release OFF Latch, activate VCC UVLO or VREG50 UVLO or EN or TSD. (See Timing Chart 6 on page.11)

6. TSD Block
   In case power dissipation is continuously exceeded the chip temperature (Tj) will rise, TSD will be activated and all outputs and VREG50 will be turned off. The circuit will reactive when the temperature drops down again.
   The output voltage and timer latch are reset when TSD is activated.

7. Protection Blocks

Pin name	Protection	Function	Note
VCC	UVLO	All outputs are turned off	Reset of the OFF Timer Latch
VREG50	UVLO	All outputs are turned off	Reset of the OFF Timer Latch
Vo1 (SW1, FB1)	OCP	ON Duty limited every cycle	SW1 ON duty is limited and the output voltage lowered.
	OCP + Timer Latch	OFF Latch	Reset the OFF Latch by UVLO, EN or TSD
	SCP + Timer Latch		
	OVP	Ch1 internal FET is turned OFF	
	OVP + Timer Latch	OFF Latch	Reset the OFF Latch by UVLO, EN or TSD
PVCC2 PVCC4	OVP	Ch1 internal FET is turned OFF	
	OVP + Timer Latch	OFF Latch	Reset the OFF Latch by UVLO, EN or TSD
Vo2	OCP + Timer Latch	OFF Latch	Reset the OFF Latch by UVLO, EN or TSD
	UVD + Timer Latch		
	OVD + Timer Latch		
Vo3	OCP + Timer Latch	OFF Latch	Reset the OFF Latch by UVLO, EN or TSD
	UVD + Timer Latch		
	OVD + Timer Latch		
Vo4 (SW4)	OCP	ON Duty is limited every cycle	SW4 ON duty is limited and the output voltage lowered.
	OCP + Timer Latch	OFF Latch	Reset OFF Latch by UVLO, EN or TSD
	UVD + Timer Latch		
	OVD + Timer Latch		
Other	TSD	All outputs and VREG50 are turned off	Auto recovery, release OFF Timer Latch

(UVLO: Undervoltage lockout circuit, OVD: Overvoltage detection, UVD: Undervoltage detection, OCP: Overcurrent protection, SCP: Short current protection, Timer Latch: Typ.10ms, OVP: Overvoltage protection, TSD: Thermal shutdown)

●**Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Unit
VCC pin voltage	VCC	-0.3 to 40[*1]	V
EN pin voltage	EN	-0.3 to 40	V
PVCC1 pin voltage	PVCC1	-0.3 to 40[*1*2]	V
VREG50 pin voltage	VREG50	-0.3 to 6[*3]	V
BOOT1 pin voltage	BOOT1	-0.3 to 45	V
BOOT1-SW1 pin voltage	BOOT1-SW1	-0.3 to 6	V
SW1 pin voltage	SW1	-0.3 to PVCC1 + 0.3	V
PVCC2 pin voltage	PVCC2	-0.3 to 6[*1]	V
PVCC4 pin voltage	PVCC4	-0.3 to 6[*1]	V
SW4 pin voltage	SW4	-0.3 to PVCC4 + 0.3	V
SS pin voltage	SS1 to 4	-0.3 to 6[*4]	V
FB pin voltage	FB1	-0.3 to 6[*4]	V
COMP pin voltage	COMP1	-0.3 to 6[*4]	V
VO2 pin voltage	VO2	-0.3 to 6[*5]	V
VO3 pin voltage	VO3	-0.3 to 6[*5]	V
VO4 pin voltage	VO4	-0.3 to 6[*6]	V
RSTO pin voltage	RSTO	-0.3 to 6[*5]	V
SEL_CH2 pin voltage	SEL_CH2	-0.3 to VREG50 + 0.3	V
SEL_CH3 pin voltage	SEL_CH3	-0.3 to VREG50 + 0.3	V
SEL_CH41 pin voltage	SEL_CH41	-0.3 to VREG50 + 0.3	V
SEL_CH42 pin voltage	SEL_CH42	-0.3 to VREG50 + 0.3	V
SEL_T pin voltage	SEL_T	-0.3 to VREG50 + 0.3	V
TEST pin voltage	TEST1 to 5	-0.3 to VREG50 + 0.3	V
Power dissipation	Pd	0.88[*7]	W
Storage temperature range	Tsts	-55 to +150	℃
Maximum Junction Temperature	Tj	+150	℃

*1 Pd should not be exceeded.
*2 VCC-0.3V < PVCC1 < VCC+0.3V
*3 Should not exceed VCC+0.3V
*4 Should not exceed VREG50+0.3V
*5 Should not exceed PVCC2+0.3V
*6 Should not exceed PVCC4+0.3V
*7 7.04mW/℃ reduction when Ta≧25℃, if mounted on a double layer PCB 70mm×70mm×1.6mm

●**Recommended Operating Rating(s)**

Parameter	Min.	Max.	Unit
VCC, PVCC1	5.9	18	V
PVCC2, PVCC4	3.0	4.0	V
SW1 Load current	-	500	mA
VO2 Load current	-	130	mA
VO3 Load current	-	60	mA
SW4 Load current	-	250	mA
Operating temperature range	-40	+105	℃

●**Electrical Characteristic(s)**

(Unless otherwise specified, Ta=25℃, VCC=PVCC1=12V, PVCC2=PVCC4=3.3V, EN=5V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Standby current	I_{STB1}	-	0	10	μA	EN=0.0V
Circuit current	I_{CC2}	2.5	5.0	12.0	mA	
UVLO operating voltage of VCC	V_{UVLO}	4.3	4.6	4.9	V	Ta=-40 to 105℃
UVLO hysteresis voltage of VCC	V_{UVLO_Hys}	500	750	990	mV	Ta=-40 to 105℃
VREG50 voltage	VREG50	4.5	5.0	5.5	V	
UVLO operating voltage of VREG50	V_{UVLO50}	3.5	3.8	4.1	V	Ta=-40 to 105℃
UVLO hysteresis voltage of VREG50	V_{UVLO50_Hys}	200	300	390	mV	Ta=-40 to 105℃
CH1, High voltage step-down DC/DC converter						
Feedback reference voltages 1	VFB1	0.784	0.800	0.816	V	FB1=COMP1 voltage
Oscillator Frequency 1	F_{OSC1}	0.4	0.5	0.6	MHz	
SS1 charge current	I_{SS1}	1.0	2.5	4.0	μA	V_{SS1}=0.5V
SS1 cramp voltage	V_{SS1CLM}	1.0	1.3	1.6	V	
SS1 protection circuit detection start voltage	V_{SS1PON}	1.0	1.3	1.6	V	V_{SS1} voltage(L→H)
SW1 NMOS overcurrent protection	I_{OCP1}	510	-	-	mA	
CH2, LDO						
2.8V Output voltage	Vo2_28	2.744	2.800	2.856	V	Ivo2=5mA, SET_CH2=GND
3.3V Output voltage	Vo2_33	3.234	3.300	3.366	V	Ivo2=5mA, SET_CH2=VREG50 PVCC2=3.8V
Discharge resistor	R_{V2DIS}	200	400	600	Ω	EN=0V, Vo=2.8V
SS2 charge current	I_{SS2}	1.0	2.5	4.0	μA	V_{SS2}=0.5V
SS2 cramp voltage	V_{SS2CLM}	1.0	1.3	1.6	V	
SS2 protection circuit detection start voltage	V_{SS2PON}	1.0	1.3	1.6	V	
Vo2 undervoltage detection	V_{UVD2}	Vo2× 0.25	Vo2× 0.40	Vo2× 0.55	V	V_{Vo2} voltage((H→L)
Vo2 overvoltage detection	V_{OVD2}	Vo2× 1.35	Vo2× 1.50	Vo2× 1.65	V	V_{Vo2} voltage((L→H)
ch2 PMOS Over current protection detection	I_{OCP2}	140	-	-	mA	
Reset						
RSTO detect voltage	V_{RSTO1}	Vo2× 0.84	Vo2× 0.86	Vo2× 0.88	V	V_{Vo2}(H→L)
RSTO release voltage	V_{RSTO2}	Vo2× 0.89	Vo2× 0.93	Vo2× 0.97	V	V_{Vo2}(L→H)
RSTO ON resistance	R_{RSTO}	50	100	150	Ω	I_{RSTO}=1mA
RSTO leakage current	I_{RSTO}	-	0	10	μA	RSTO=5V
RSTO delay time	T_{RSTO}	16	20	24	ms	
CH3, LDO						
1.8V Output voltage	Vo3_18	1.764	1.800	1.836	V	Ivo3=5mA, SET_CH3=VREG50 PVCC2=3.8V
Discharge resistance	R_{V3DIS}	200	400	600	Ω	EN=0V, Vo=1.8V
SS3 charge current	I_{SS3}	1.0	2.5	4.0	μA	V_{SS3}=0.5V
SS3 cramp voltage	V_{SS3CLM}	1.0	1.3	1.6	V	
SS3 protection circuit detection start voltage	V_{SS3PON}	1.0	1.3	1.6	V	
Vo3 undervoltage detection	V_{UVD3}	Vo3× 0.25	Vo3× 0.40	Vo3× 0.55	V	V_{Vo3} voltage (H→L)
Vo3 overvoltage detection	V_{OVD3}	Vo3× 1.35	Vo3× 1.50	Vo3× 1.65	V	V_{Vo3} voltage (L→H)
ch3 PMOS overcurrent protection	I_{OCP3}	70	-	-	mA	

* Pd should not be exceeded.

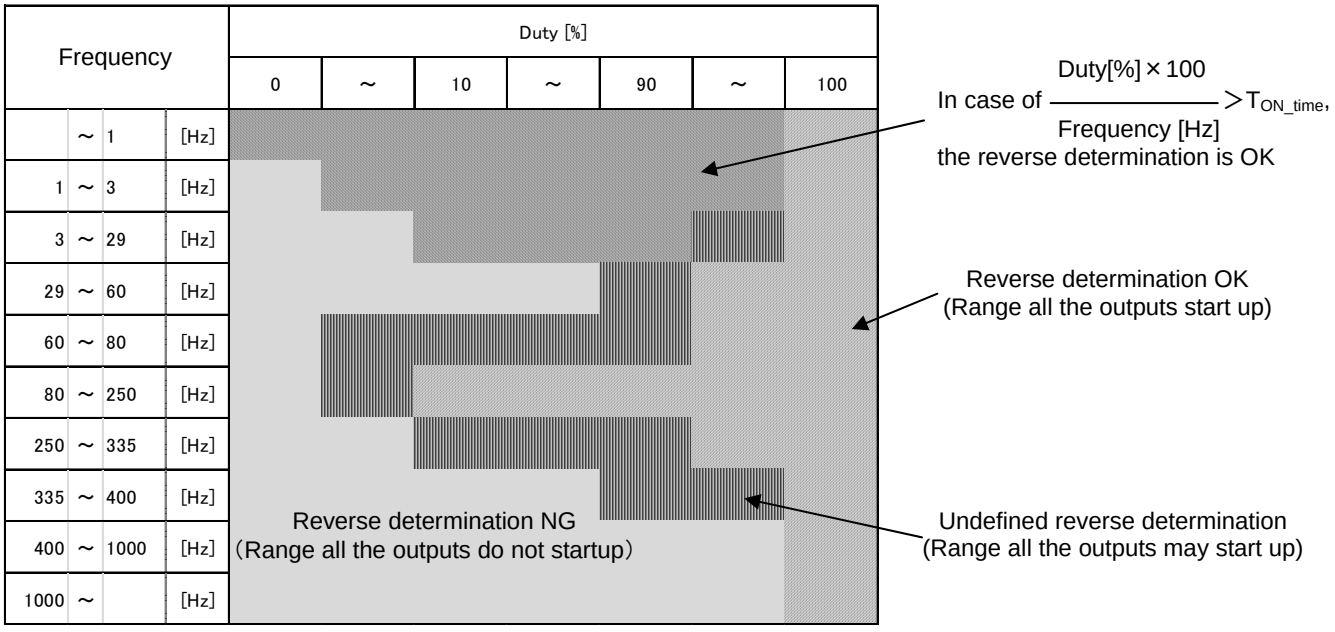
●**Electrical Characteristic(s)**

(Unless otherwise specified, Ta=25℃, VCC=PVCC1=12V, PVCC2=PVCC4=3.3V, EN=5V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
CH4, Step-down DC/DC converter						
1.5V Output Voltage	Vo4_15	1.470	1.500	1.530	V	SET_CH41=GND SET_CH42=GND
1.2V Output Voltage	Vo4_12	1.176	1.200	1.224	V	SET_CH41=VREG50 SET_CH42=GND PVCC4=3.8V
1.8V Output Voltage	Vo4_18	1.764	1.800	1.836	V	SET_CH41=GND SET_CH42=VREG50 PVCC4=3.8V
Oscillator Frequency 4	F_{OSC4}	0.8	1.0	1.2	MHz	
Discharge resistor	R_{V4DIS}	200	400	600	Ω	EN=0V, Vo4=1.5V
SS4 charge current	I_{SS4}	1.0	2.5	4.0	μA	V_{SS4}=0.5V
SS4 cramp Voltage	V_{SS4CLM}	0.7	1.0	1.3	V	
SS4 protection circuit detection start voltage	V_{SS4PON}	0.7	1.0	1.3	V	
Vo4 undervoltage detection	V_{UVD4}	Vo4×0.25	Vo4×0.40	Vo4×0.55	V	V_{Vo4} Voltage(H→L)
Vo4 overvoltage detection	V_{OVD4}	Vo4×1.35	Vo4×1.50	Vo4×1.65	V	V_{Vo4} Voltage(L→H)
SW4 PMOS overcurrent protection	I_{OCP4}	260	-	-	mA	
Sequencer (Reverse determination)						
EN filter time 1	T_{FIL1}	200	300	400	μs	For Camera ON Frequency determination
EN filter time 2	T_{FIL2}	2.4	3	3.6	ms	For Camera ON Time determination
OFF timer time	OFF Timer	10	11	12	s	SEL_T=VREG50 (Ta = -40 to +105℃)
Camera ON FAST frequency	Fperiod_f	250	-	335	ms	
Camera ON SLOW frequency	Fperiod_s	60	-	80	Hz	
Camera ON time(DC input)	Ton_time	24	30	36	Hz	
EN full down resistance	REN	200	400	600	ms	
EN input threshold voltage	VEN_Ta	3.0	3.7	4.4	kΩ	
Other						
Timer latch time	TLATCH	8	10	12	ms	

*Pd should not be exceeded.

●**Sequencer range (SEL_T=VREG50)**



●**Typical Performance Curve (Reference data)**

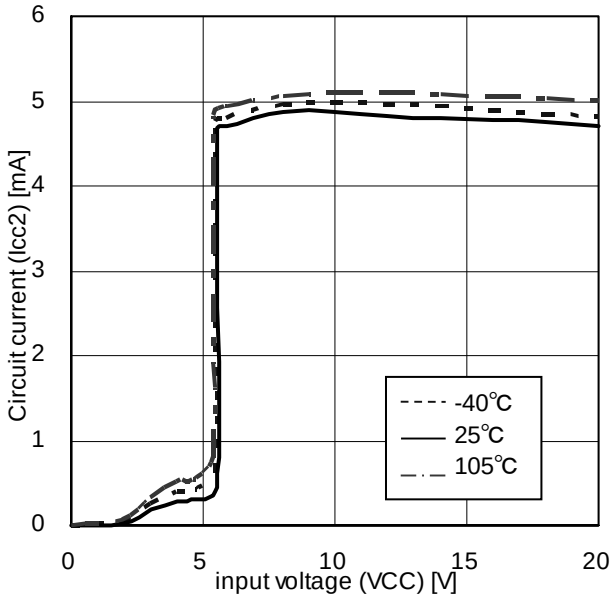


Figure 5. circuit current vs. power supply

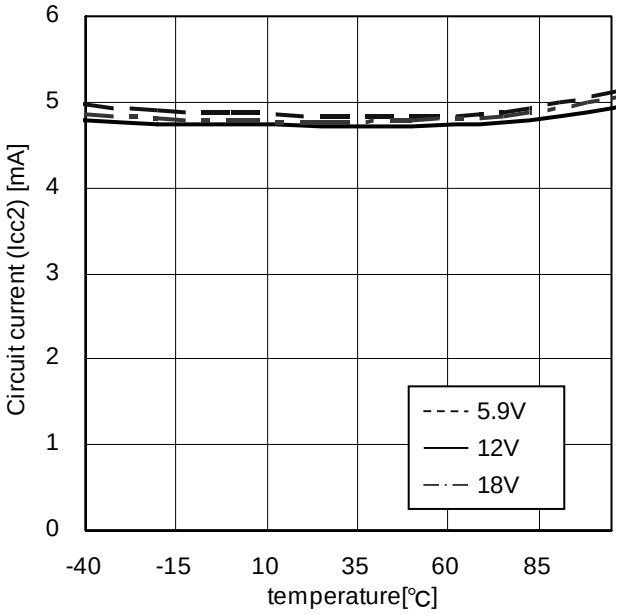


Figure 6. circuit current vs. temperature

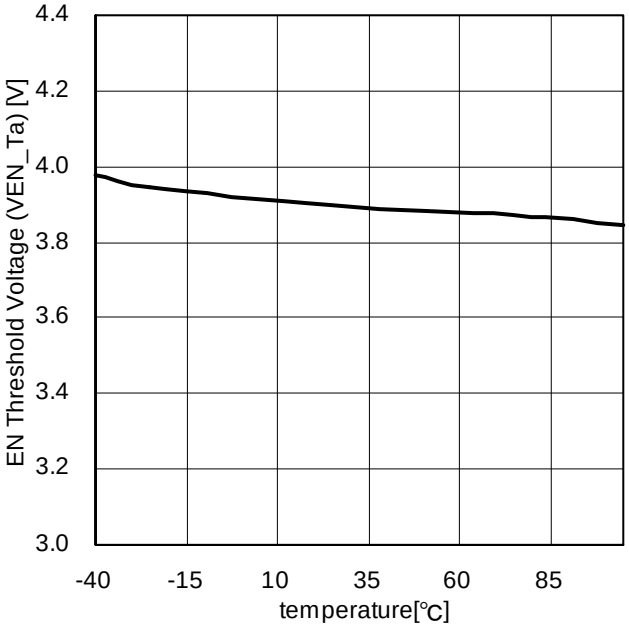


Figure 7. EN threshold voltage vs. temperature

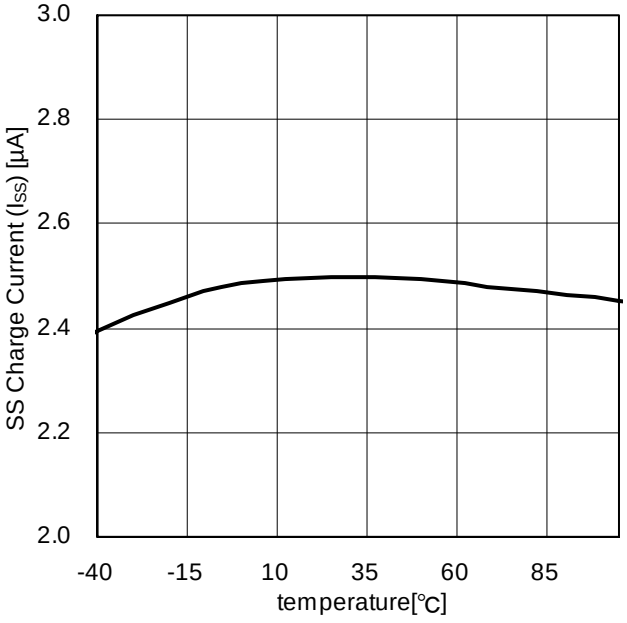


Figure 8. SS charge current vs. temperature

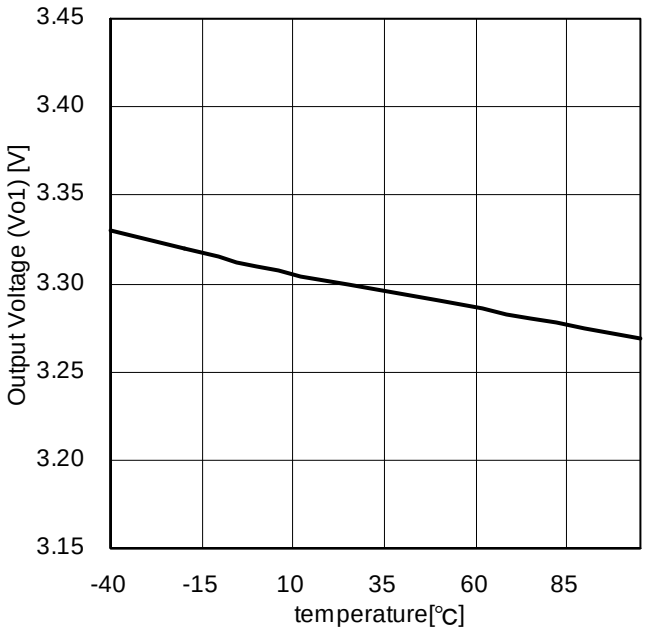


Figure 9. 3.3V Output voltage (CH1) vs. temperature

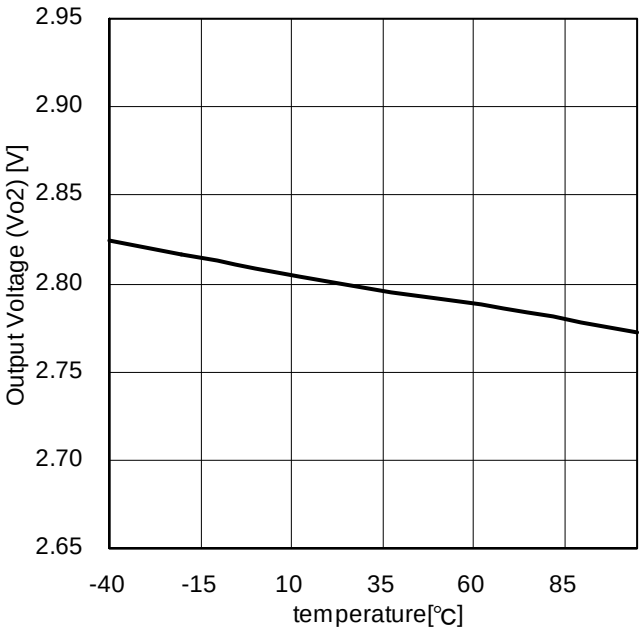


Figure 10. 2.8V Output voltage (CH2) vs. temperature

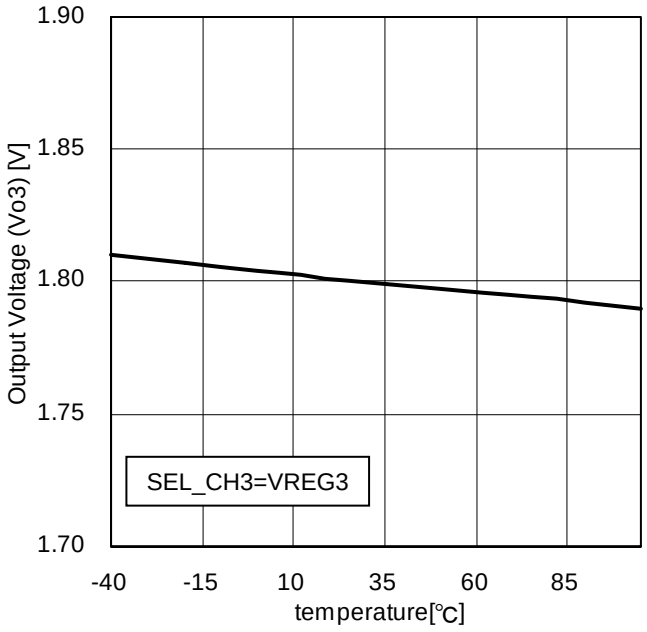


Figure 11. 1.8V Output voltage (CH3) vs. temperature

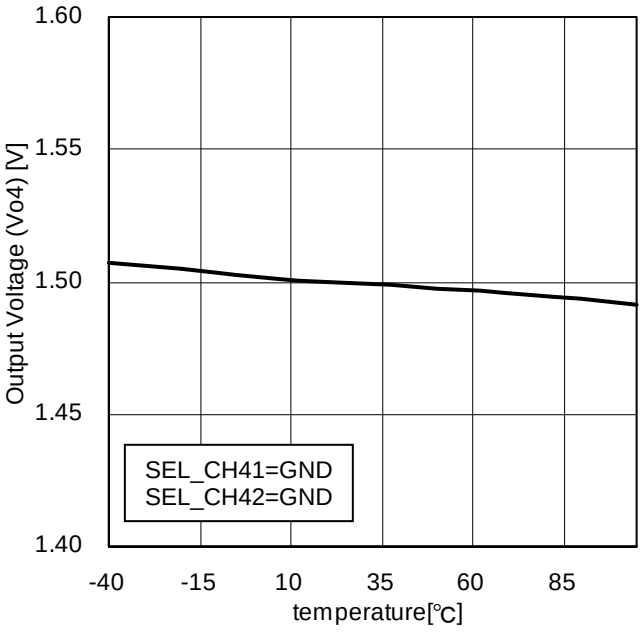


Figure 12. 1.5V Output voltage (CH4) vs. temperature

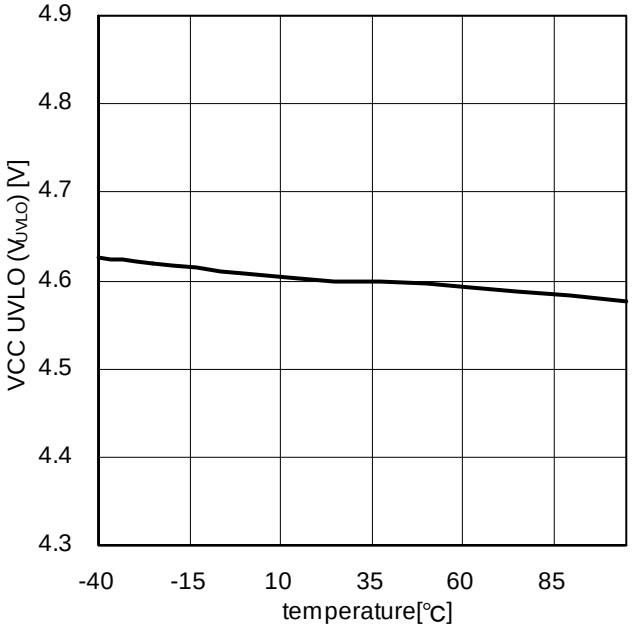


Figure 13. VCC UVLO operating voltage vs. temperature

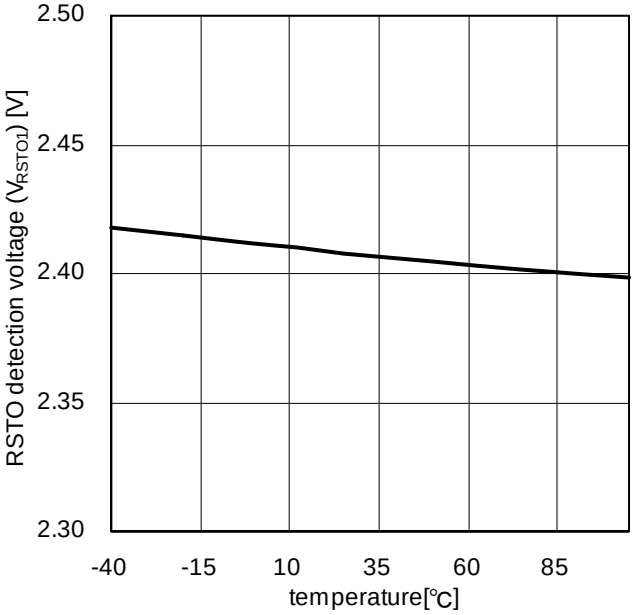


Figure 14. RSTO detect voltage vs. temperature

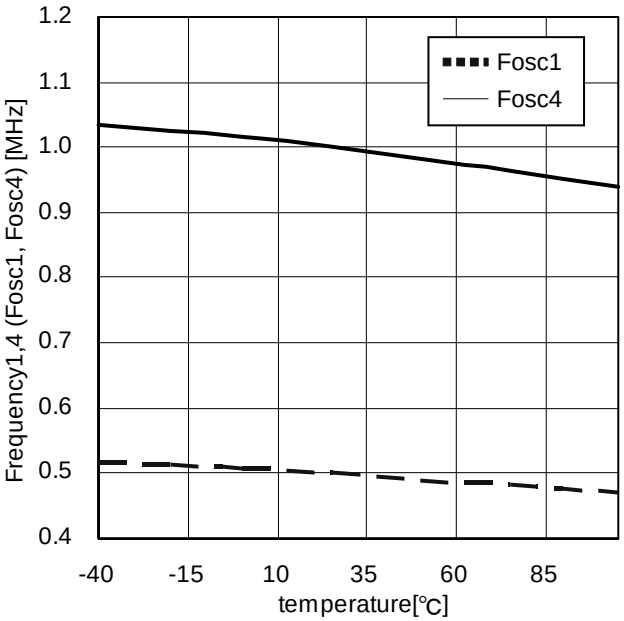


Figure 15. Frequency1, 4 vs. temperature

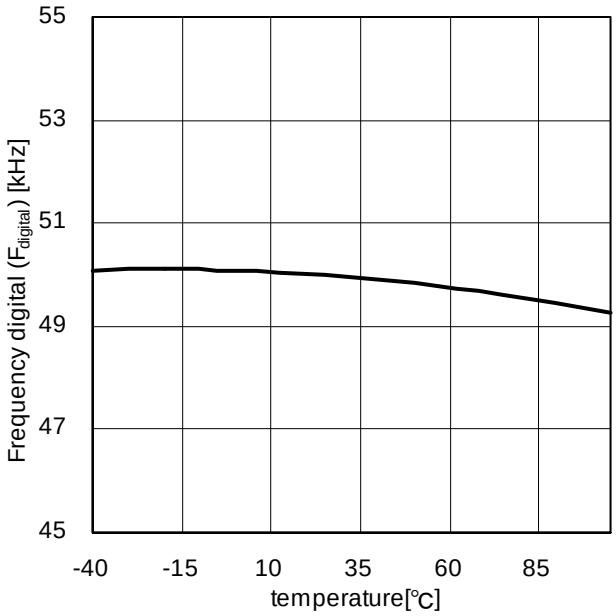
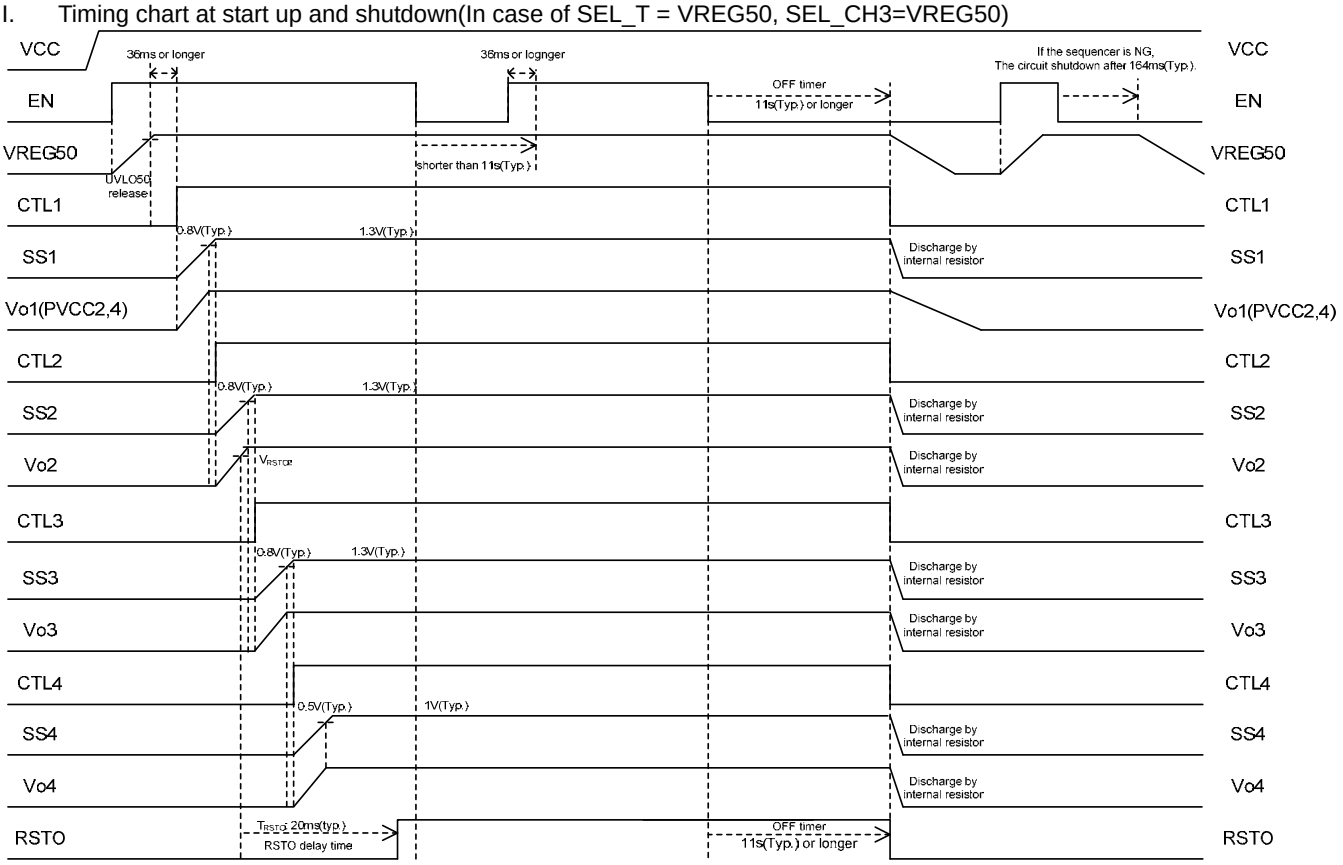


Figure 16. Frequency of OSC_D vs. temperature

●**Timing Chart**

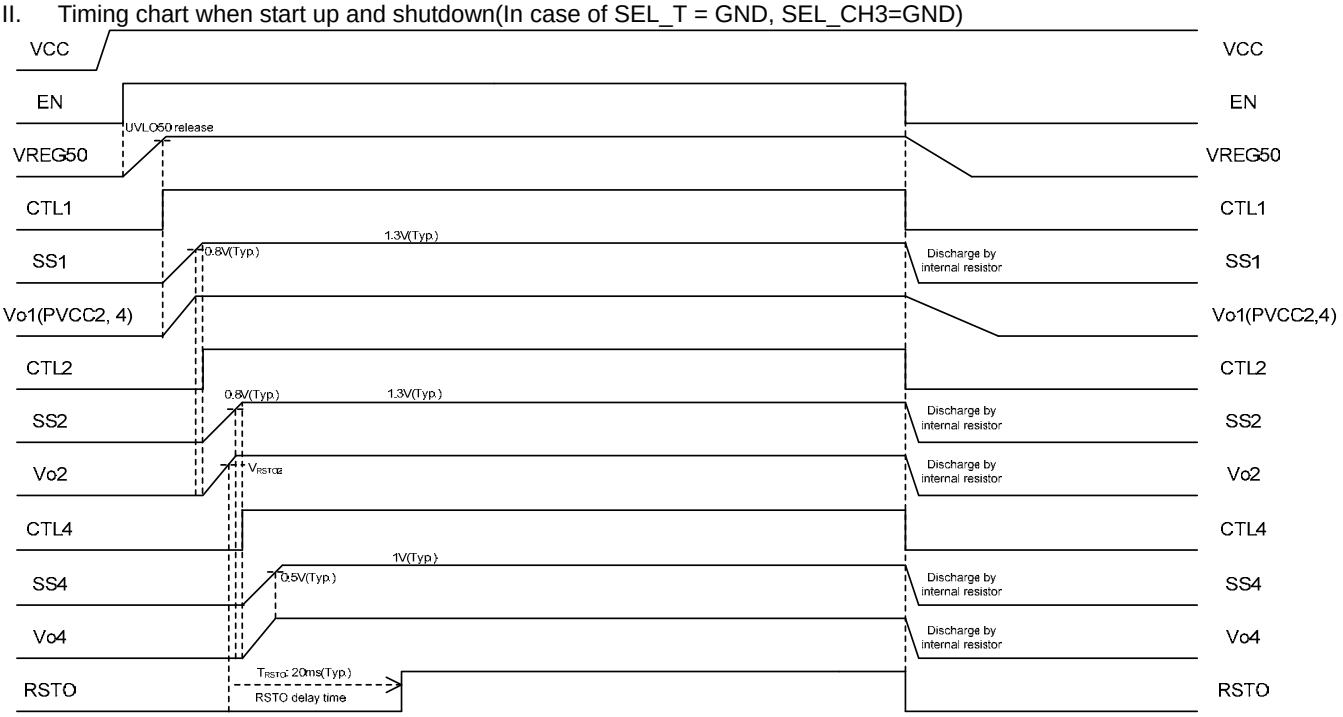
I. Timing chart at start up and shutdown(In case of SEL_T = VREG50, SEL_CH3=VREG50)



(*: EN filter time 1 is omitted.)

Figure17. Timing Chart 1 (start up and shutdown)

II. Timing chart when start up and shutdown(In case of SEL_T = GND, SEL_CH3=GND)



(*: EN filter time 1 is omitted.)

Figure18. Timing Chart 2 (start up and shutdown)

III. Operating pattern of camera ON signal

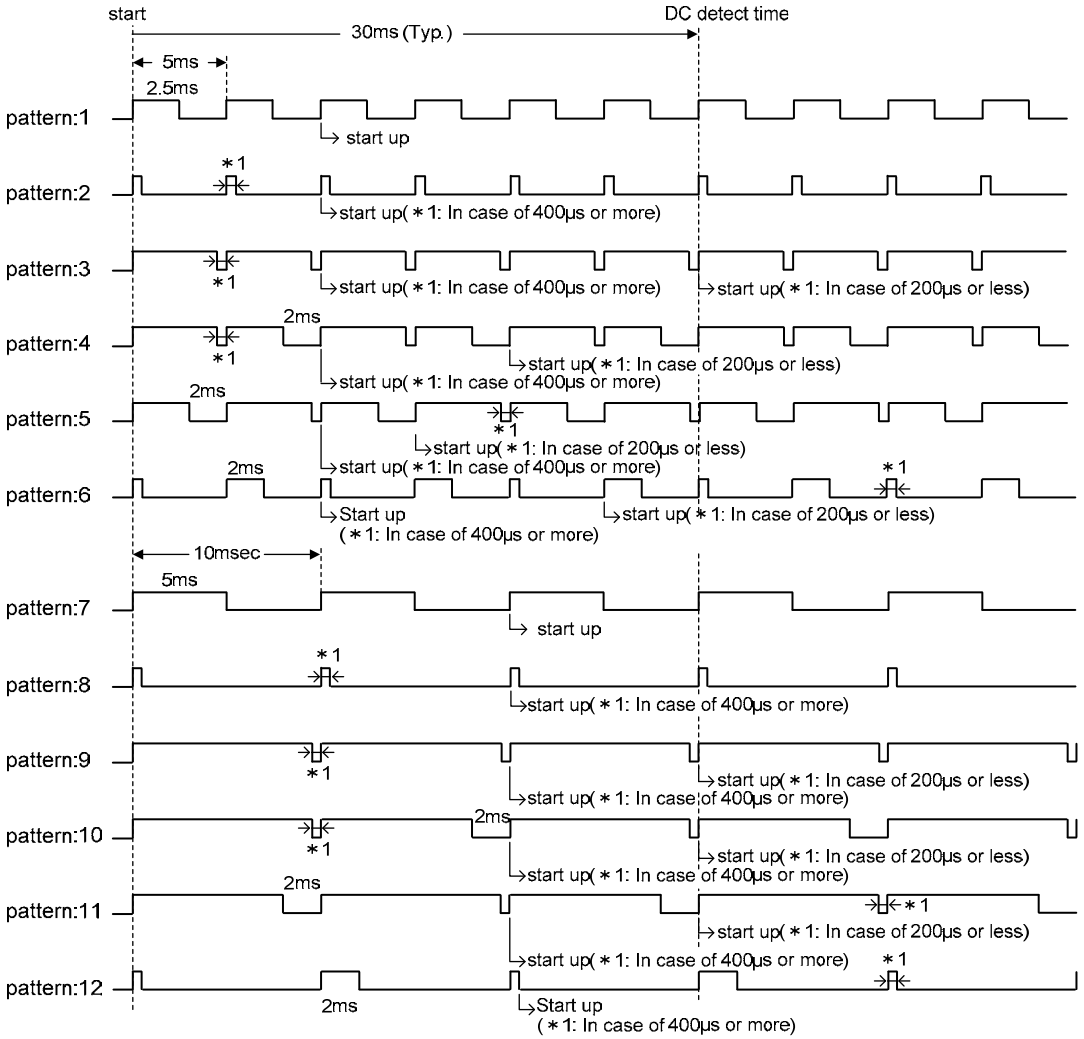


Figure 19. Timing Chart 3

IV. Timer Latch release method

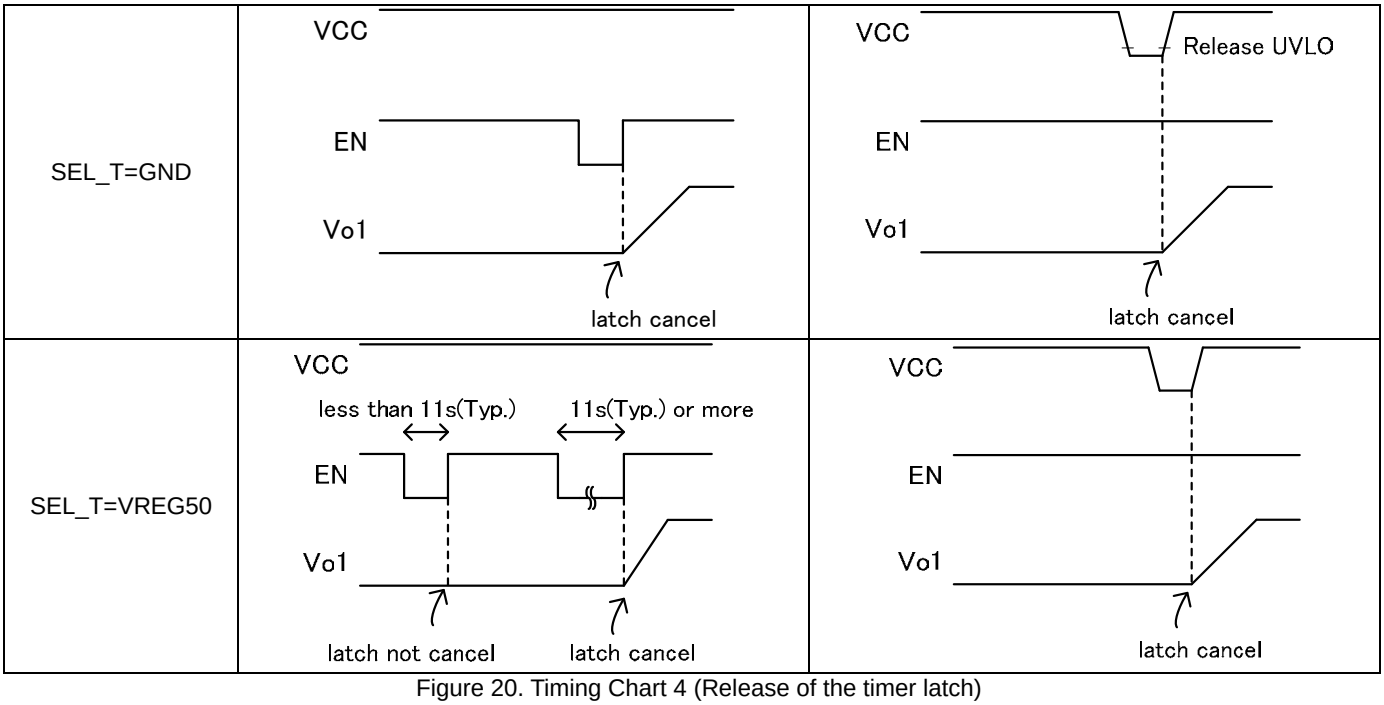
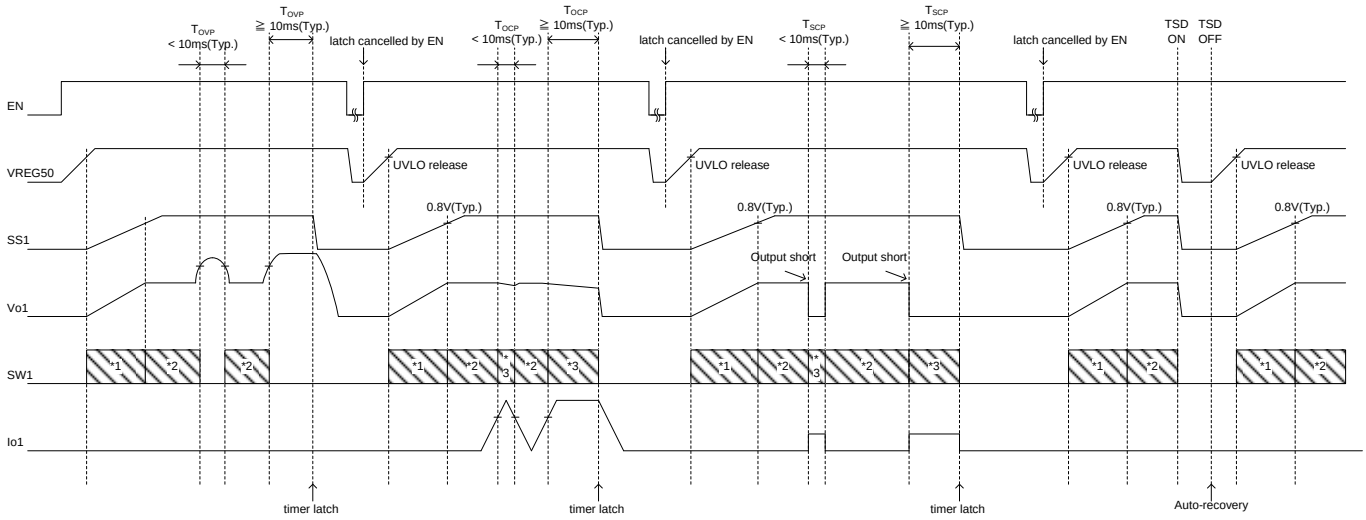


Figure 20. Timing Chart 4 (Release of the timer latch)

V. CH1 protection function



*1: Duty is controlled by soft start
*2: Normal switching operation
*3: Duty is limited every cycle.

Figure21. Timing Chart 5 (CH1 protection function)

VI. CH2 protection function (the similar to CH3)

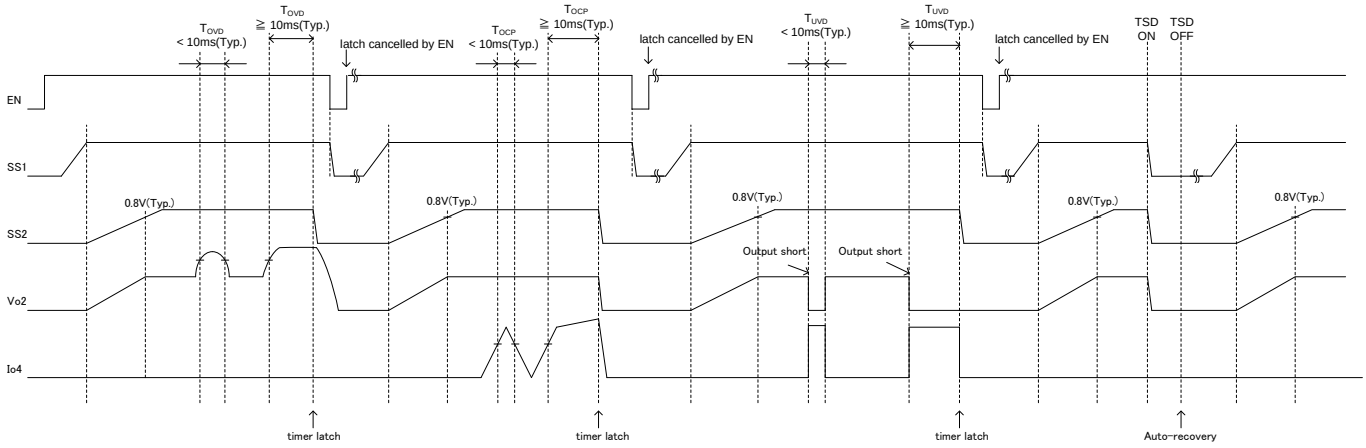
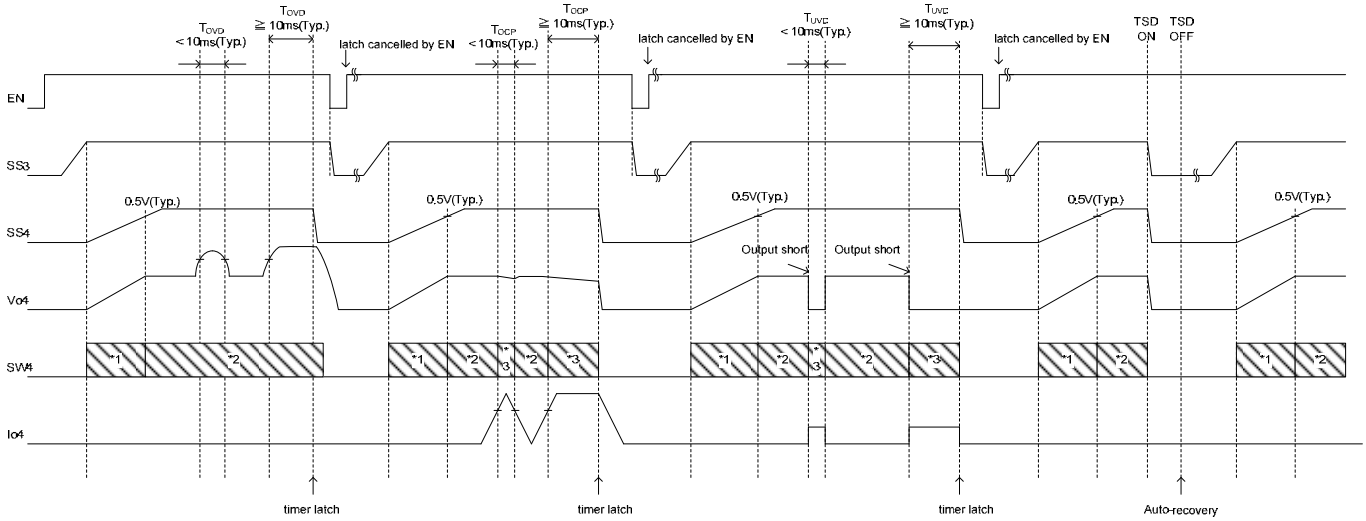


Figure 22. Timing Chart 6 (CH2, 3 protection function)

VII. CH4 protection function



*1: Duty is controlled by soft start
*2: Normal switching operation
*3: Duty is limited every cycle.

Figure 23. Timing Chart 7 (CH4 protection function)

●**Application Examples**

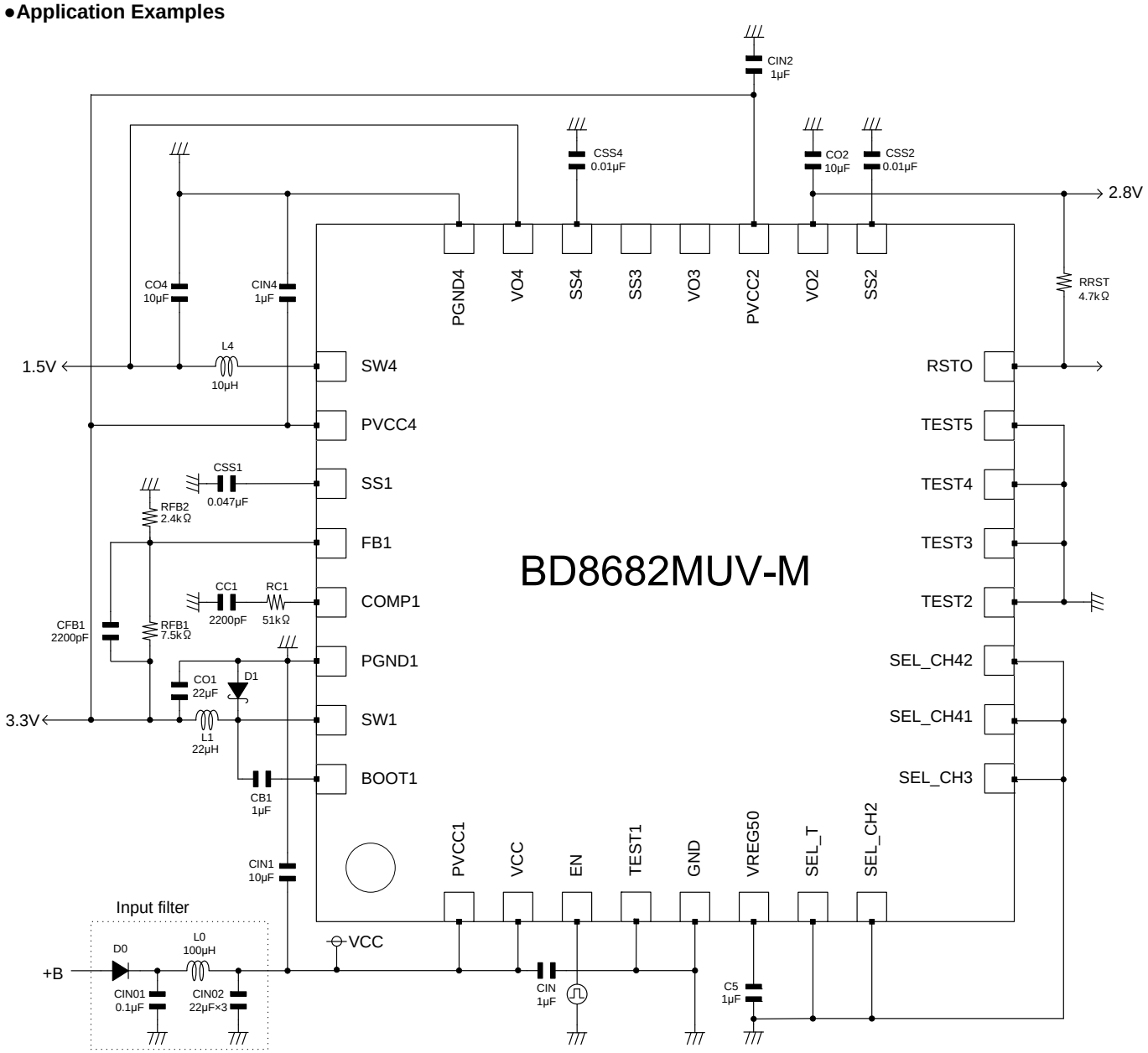


Figure 24. Application circuit schematic 2
(Sequencer disabled. Vo1=3.3V, Vo2=2.8V, Vo3=Not used, Vo4=1.5V)

Note: In case of not using input filter, the value of output fluctuation increase for input voltage (+B) fluctuation.
We recommend using input filter. Details are shown on page 20. (See “5. Input filter”)

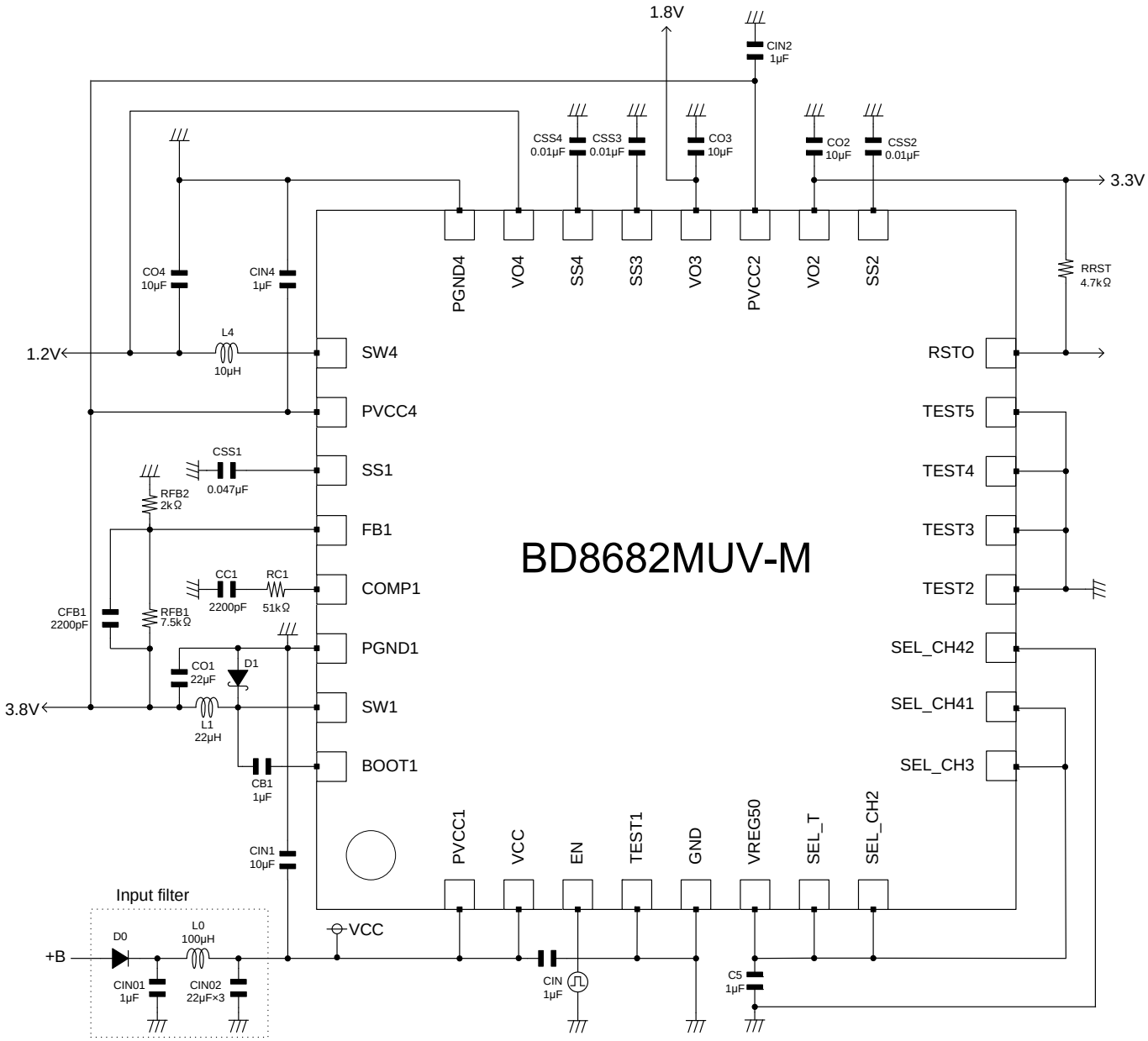


Figure 25. Application circuit schematic 3
(Sequencer disabled. Vo1=3.8V, Vo2=3.3V, Vo3=1.8V, Vo4=1.2V)

Note: In case of not using input filter, the value of output fluctuation increase for input voltage (+B) fluctuation.
We recommend using input filter. Details are shown on page 20. (See “5. Input filter”)

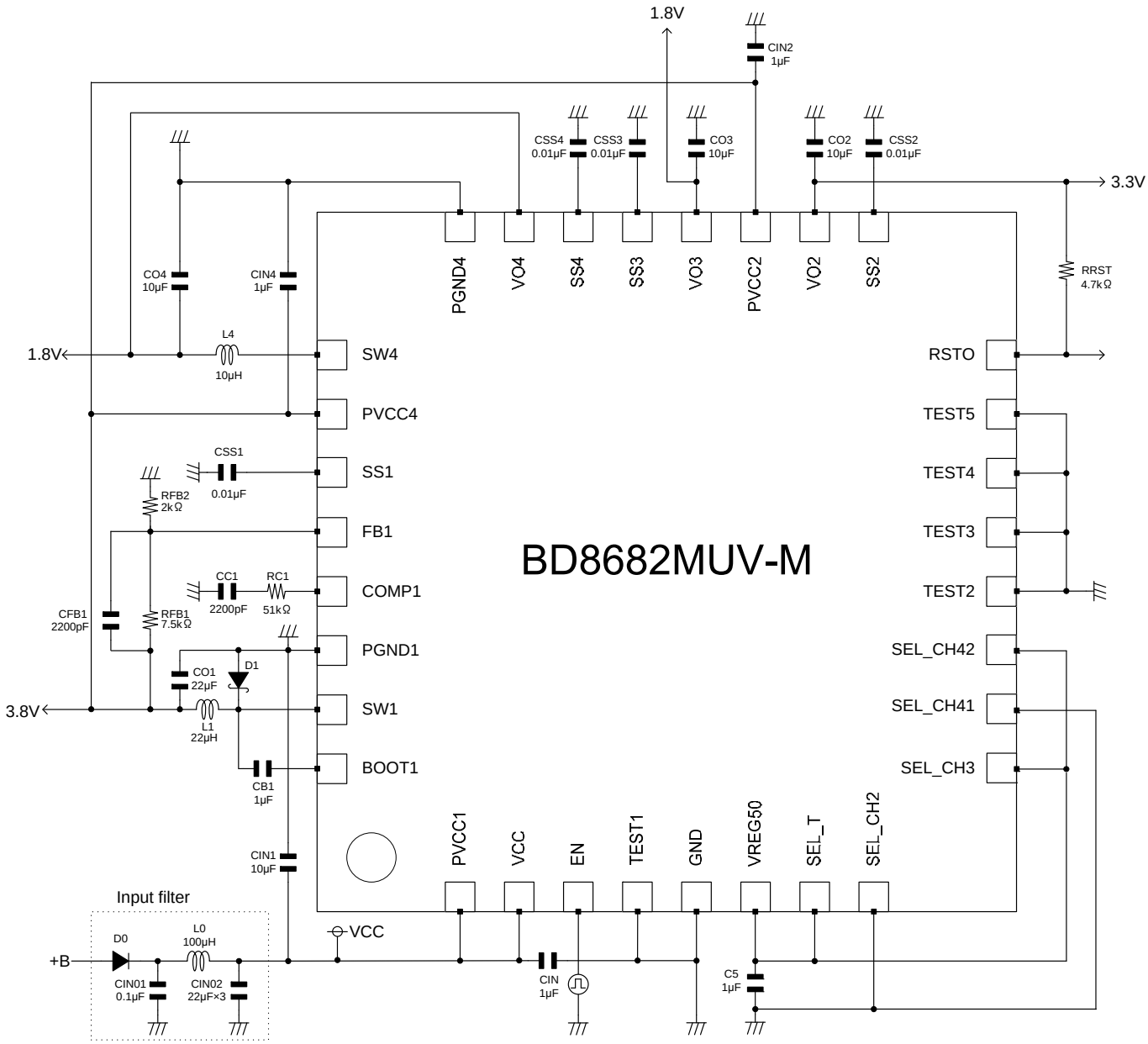


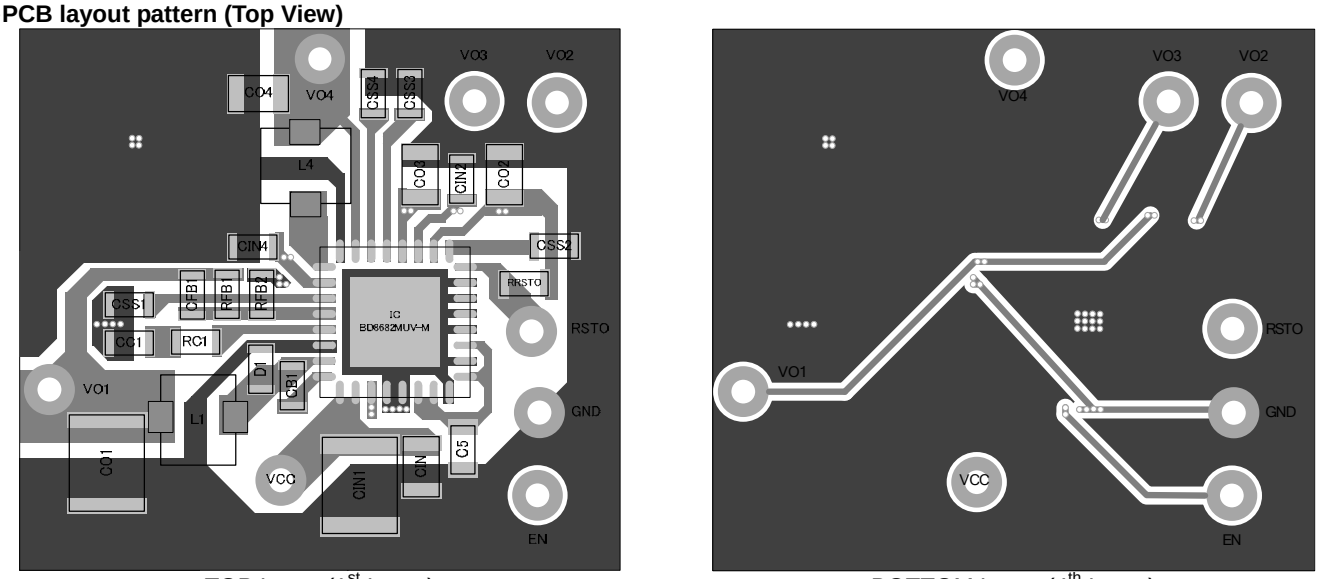
Figure 26. Application circuit schematic 4
(Sequencer disabled. Vo1=3.3V, Vo2=2.8V, Vo3=1.8V, Vo4=1.8V)

Note: In case of not using input filter, the value of output fluctuation increase for input voltage (+B) fluctuation.
We recommend using input filter. Details are shown on page 20. (See “5. Input filter”)

●**Parts list (Recommendation)**

Name	Value		Parts No	Size Code	Manufacturer	Note
IC	-	-	BD8682MUV-M	5x5mm	ROHM	
RFB1	7.5	[kΩ]	MCR03 series	1608	ROHM	
RFB2	2.4	[kΩ]	MCR03 series	1608	ROHM	In case of Vo1=3.8V, RFB2 = 2.0kΩ
RC1	51	[kΩ]	MCR03 series	1608	ROHM	
RRST	4.7	[kΩ]	MCR03 series	1608	ROHM	
CIN	1	[µF]	C2012X7R1H105K	2012	TDK	
CIN1	10	[µF]	C3225X7R1H106K	3225	TDK	
CIN2	1	[µF]	C1608X7R1C105K	1608	TDK	
CIN4	1	[µF]	C1608X7R1C105K	1608	TDK	
CO1	22	[µF]	C3225X7R1C226M	3225	TDK	
CO2	10	[µF]	C2012X7R1A106K	2012	TDK	
CO3	10	[µF]	C2012X7R1A106K	2012	TDK	
CO4	10	[µF]	C2012X7R1A106K	2012	TDK	
C5	1	[µF]	C1608X7R1C105K	1608	TDK	
CSS1	47	[nF]	GRM18 series	1608	murata	
CSS2	10	[nF]	GRM18 series	1608	murata	
CSS3	10	[nF]	GRM18 series	1608	murata	
CSS4	10	[nF]	GRM18 series	1608	murata	
CB1	1	[µF]	C1608X7R1C105K	1608	TDK	
CFB1	2.2	[nF]	GRM18 series	1608	murata	
CC1	2.2	[nF]	GRM18 series	1608	murata	
L1	22	[µH]	VLF302515M-220M-CA	3x2.5mm	TDK	
L4	10	[µH]	VLF302515M-100M-CA	3x2.5mm	TDK	
D1	-	-	RB160SS-40	1608	ROHM	
D0	-	-	RR264M-400	3.5x1.6mm	ROHM	Input filter
L0	100	[µH]	VLCF4024T-101M	4x4mm	TDK	
CIN01	0.1	[µF]	GRM188R11H104KA93	1608	murata	
CIN02	22x3	[µF]	GRM32EB31E226K	3225	murata	

●**PCB layout pattern (Top View)**



<TOP Layer (1st Layer)> <BOTTOM Layer (4th Layer)>

Figure 27. Board layout example (In case of Application circuit schematic 4. Input filter excluded.)

Note: We recommend that the number of layers is 4 or more.
In case of 4 layer, 2nd layer is ground layer, and 3rd layer is power supply layer.

●Selection of external components

1. Setting the output voltage (Vo1)

The output 1 voltage is determined by the equation below. Select a combination of RFB1 and RFB2 to obtain the required voltage.

A small resistance value leads to a drop in power efficiency. RFB1 also affects the phase compensation of Vo1.

Vo1 = VFB1 × (RFB1 + RFB2) / RFB2 [V]

Moreover, Vo1 voltage must be higher than Vo2 voltage + 0.5V.

Example: In case of Vo2 = 2.8V, Vo1 ≧ 3.3V.
In case of Vo2 = 3.3V, Vo1 ≧ 3.8V.

Note: Vo2, Vo3 and Vo4 are fixed and selectable voltages.

2. Setting the inductor (L1,L4) value

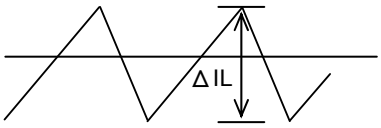


Figure 28.

The coil value significantly influences the output ripple current. As shown in the following equation, the larger the coil, and the higher the switching frequency, the lower the ripple current.

$$\Delta IL = \frac{(VCC-VOUT)\times VOUT}{L\times VCC\times f} \quad [A]$$

The optimal output ripple current setting is ca. 30% of the maximum current.

$$\Delta IL = 0.3\times IOUTmax. \quad [A]$$

$$L = \frac{(VCC-VOUT)\times VOUT}{\Delta IL\times VCC\times f} \quad [H]$$

(ΔIL: Output ripple current, f: switching frequency)

Care should be taken to not exceed the maximum current rating of the inductor since this will lead to magnetic saturation and consequently to a loss of efficiency. It is recommended to allow for sufficient margin to ensure that the peak current does not exceed the coil current rating. Use low resistance (DCR, ACR) coils to minimize coil loss and increase efficiency.

3. Setting the Shottky barrier diode selection

・Reverse voltage V_R > PVCC1(=VCC)
・Allowable current > output current + ripple current
* A value higher than the overcurrent protection value is recommended.
* Select a diode with a low forward voltage and fast recovery for high efficiency.

4. Setting the soft start time

The soft start function is necessary to prevent inrush of coil current and output voltage overshoot at startup.

$$T_{SS} = \frac{VREF \times C_{SS}}{I_{SS}(2.5\mu A\ Typ.)} [s]$$

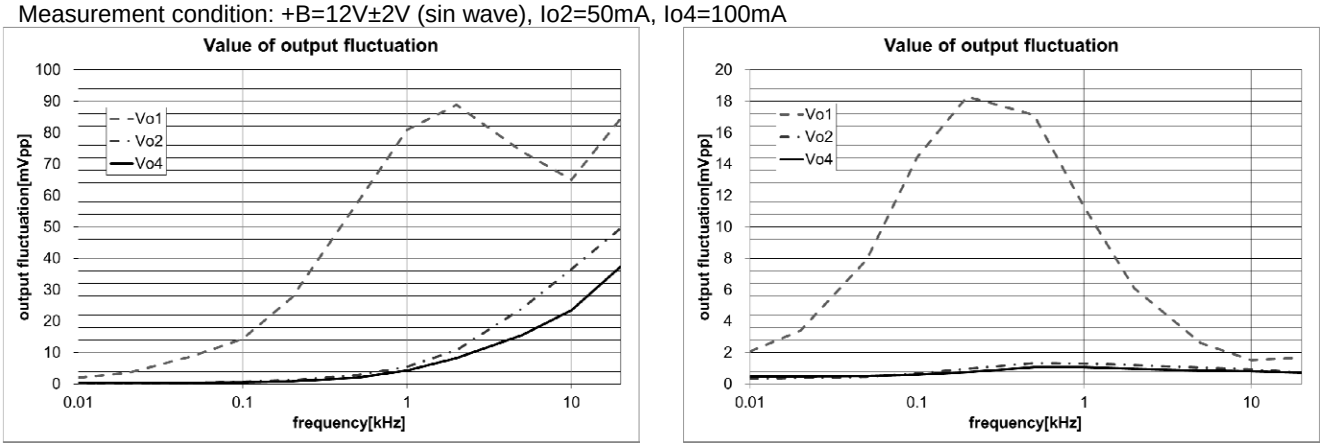
VREF: CH1=0.8V (Typ.), CH3=0.8V (Typ.), CH3=0.8V (Typ.), CH4=0.5V (Typ.)

There is a possibility that an overshoot is generated in the output due to the phase compensation value, output capacitor, etc. Therefore, verification and confirmation with the actual application is recommended. Use high accuracy components (e.g. X7R) when implementing sequential startups involving other power sources.

5. Input filter

In case of not using input filter, the values of output fluctuation increase for input voltage (+B) fluctuation at 500Hz or higher frequency. We recommend using input filter. In case of using input filter, the values of output fluctuation reduce at 500Hz or higher. The flowing graphs are output fluctuation vs. frequency.

Measurement condition: +B=12V±2V (sin wave), Io2=50mA, Io4=100mA



Not using input filter　　Using input filter

Figure 29. Output fluctuation (n case of Application circuit schematic 2)

●Power Dissipation

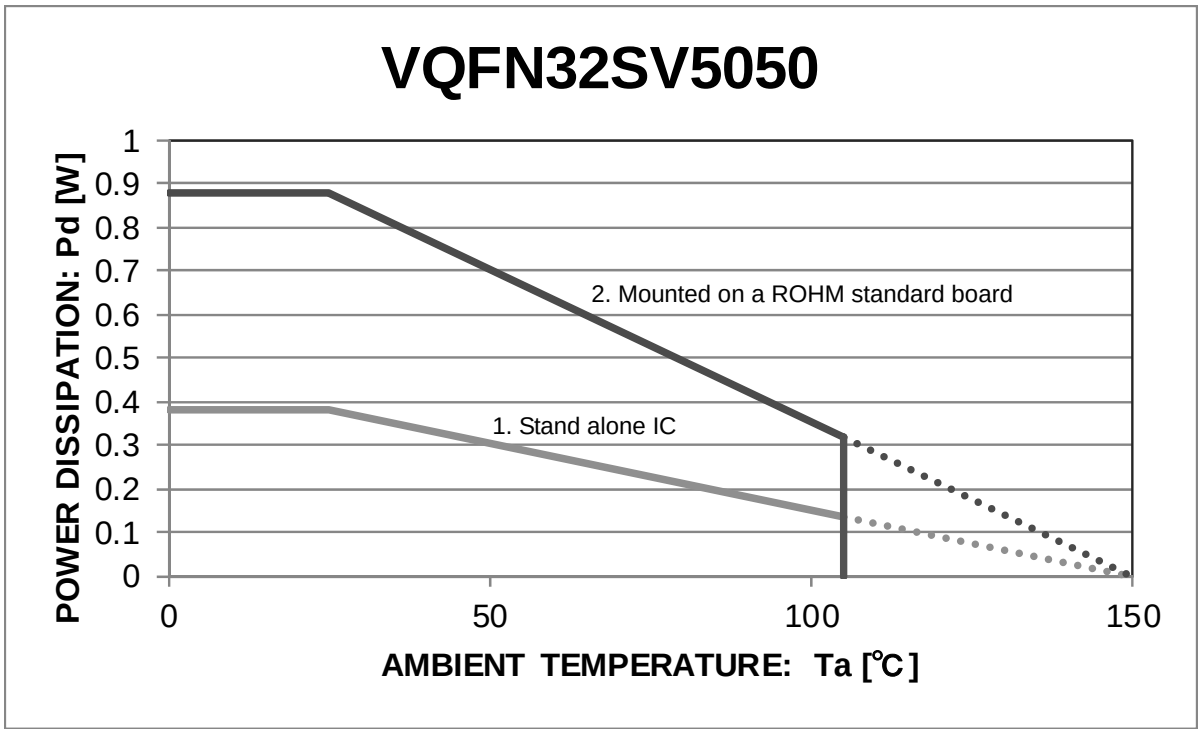


Figure 30. Power dissipation vs. temperature characteristics

1. Stand alone IC
   Power Dissipation: 0.38 [W]
   3.04mW/℃ reduction when Ta ≧25℃

2. Mounted on a ROHM standard board (70mm×70mm×1.6mm glass-epoxy board)
   Power Dissipation: 0.88 [W]
   7.04mW/℃ reduction when Ta ≧25℃

●**I/O equivalent circuits**

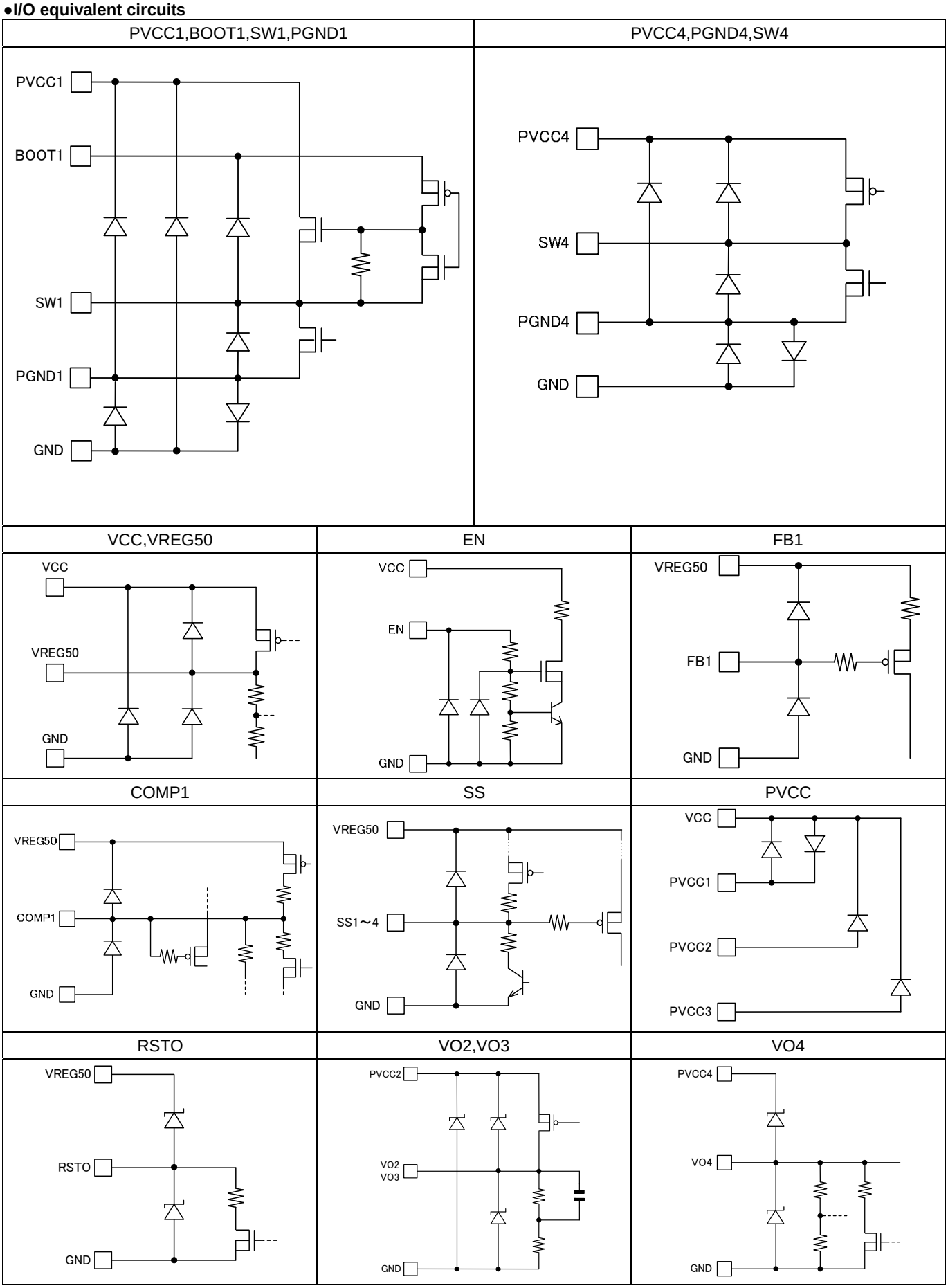


Figure 31. Equivalent circuits

●Operational Notes

1) Absolute maximum ratings
Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters may result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

2) Reverse connection to the power supply connector
A reverse connection to the power supply connector may result in damages to the IC. In order to prevent against reverse connection damages please use an external diode in series between the power supply and the power supply pin of the IC.

3) Power supply line
Because there is a return of regenerated current caused by the back electromotive force of the coil, please take countermeasures such as placing a bypass capacitor in the path of the regenerated current in close proximity of the supply ground pin of the IC. At low temperatures the capacitance of the electrolytic capacitor might decrease. Please give sufficient consideration to selecting suitable components.

4) GND electric potential
Keep the GND pin potential at the lowest (minimum) level under any operating condition. Furthermore, ensure that, including the transient, none of the pin's voltages are less than the GND pin voltage. Also, excluding the SW pin, the voltage of all pins should never drop below that of GND.

5) Thermal design
The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed for in the thermal design.

6) Inter-pin shorting and mounting errors
Ensure that when mounting the IC on the PCB the direction and position are correct. Incorrect mounting may result in damaging the IC. Also, shorts caused by dust entering between the output, input and GND pin may result in damaging the IC.

7) Operation in strong electromagnetic fields
Use caution when operating in the presence of strong electromagnetic fields, as this may cause the IC to malfunction.

8) Output capacitor
In some applications, the VCC and pin potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, while the external capacitor is charged, VCC shorts to GND.
We also recommend using reverse polarity diodes in series between all pins and the VCC pin.

9) Testing on application boards
The IC needs to be discharged after each test process as, while using the application board for testing, connecting a capacitor to a low-impedance pin may cause stress to the IC. As a protection from static electricity, ensure that the assembly setup is grounded and take sufficient caution with transportation and storage. Also, make sure to turn off the power supply when connecting and disconnecting the inspection equipment.

10) Input pins
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. Relations between each potential may form as shown in the example below, where a resistor and transistor are connected to a pin:
•With the resistor, when GND＞ Pin A, and with the transistor (NPN), when GND＞Pin B:
The P-N junction operates as a parasitic diode.
•With the transistor (NPN), when GND＞ Pin B:
The P-N junction operates as a parasitic transistor by interacting with the N layers of elements in proximity to the parasitic diode described above.
Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore do not employ any method in which parasitic diodes can operate such as applying a voltage to an input pin that is lower than the (P substrate) GND

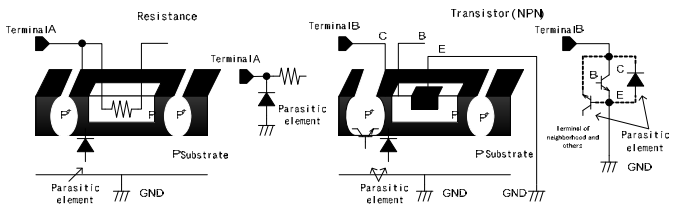


Figure 32. Example of IC's simple Structure

11) Ground wiring pattern
When both a small-signal GND and a high current GND are present, single-point grounding (at the set standard point) is recommended. This in order to separate the small-signal and high current patterns and to ensure that voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal GND. Similarly, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

12) Thermal shutdown circuit
This IC incorporates an integrated thermal shutdown circuit to prevent heat damage to the IC. Normal operation should be within the power dissipation rating, if however the rating is exceeded for a continued period, the junction temperature (Tj) will rise and the TSD circuit will be activated and turn all output pins and VREG50 OFF.
After the Tj falls below the TSD threshold the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13) TEST mode
Note that the IC will go into test mode when SS pins are supplied with 3V or more or when TEST pins are supplied any voltage. TEST pins must be connected GND at normal operation.

14) VREG50 PIN
VREG50 is output that supplies the internal circuit. We do not recommend using VREG50 for any other purpose.

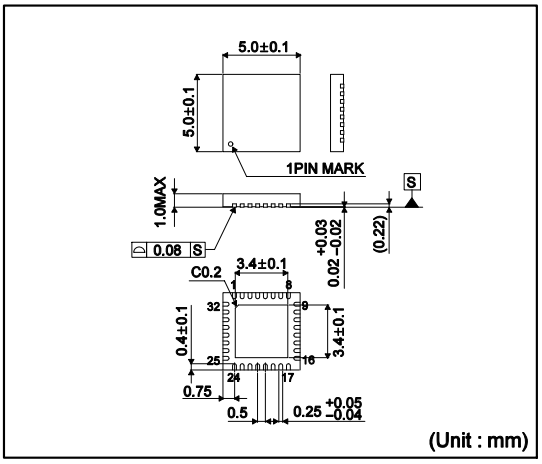
Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences between the translated and original version, the formal version takes priority

●**Ordering Information**

B D 8 6 8 2 M U V	ME 2
Part Number	Package MUV: VQFN
	Packaging and forming specification M: Automotive E2: Embossed tape and reel

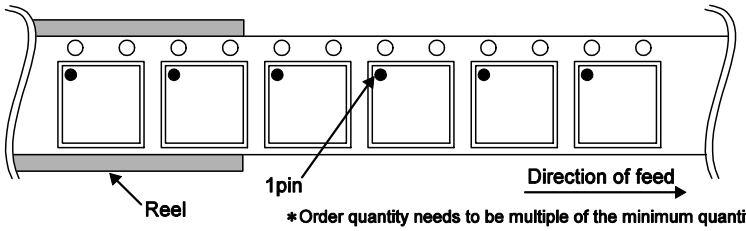
●**Physical Dimension Tape and Reel Information**

VQFN32SV5050



<Tape and Reel information>

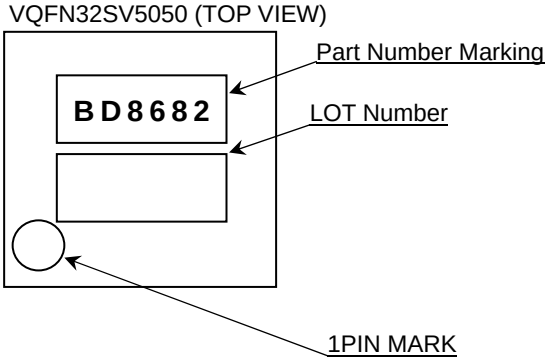
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●**Marking Diagram**

VQFN32SV5050 (TOP VIEW)



●**Revision History**

Date	Revision	Changes
22.Oct.2012	002	New Release
29.Nov.2013	003	1page : Addition “AEC-Q100 Qualified” at Features

Notice

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

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