



# STW25N95K3

N-channel 950 V, 0.32  $\Omega$ , 22 A, TO-247  
SuperMESH3™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>w</sub>
STW25N95K3	950 V	< 0.36 $\Omega$	22 A	400 W

- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitances
- Zener-protected

## Application

- Switching applications

## Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

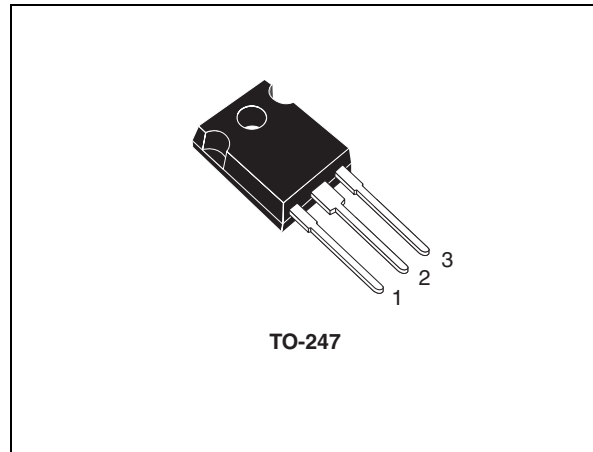


Figure 1. Internal schematic diagram

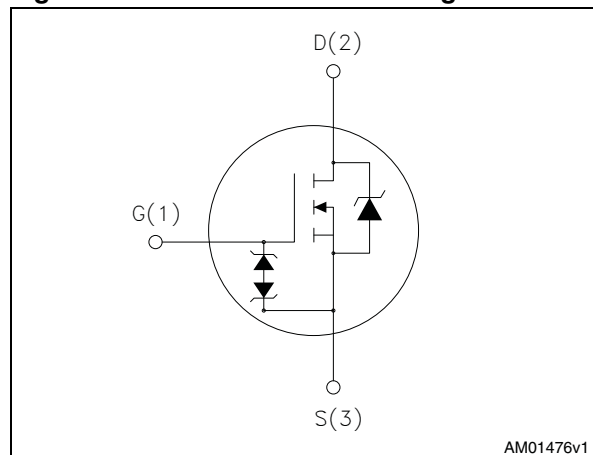


Table 1. Device summary

Order code	Marking	Package	Packaging
STW25N95K3	25N95K3	TO-247	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	22	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	13.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	88	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	400	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	28	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	450	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	5	V/ns
$V_{ESD(G-S)}$	G-S ESD (HBM $C=100\text{ pF}$ ; $R=1.5\text{ k}\Omega$ )	6000	V
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 22\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ , peak  $V_{DS} \leq V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.31	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
$T_J$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_{\text{case}} = 25^{\circ}\text{C}$  unless otherwise specified).

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_{\text{D}} = 1 \text{ mA}, V_{\text{GS}} = 0$	950			V
$I_{\text{DSS}}$	Zero gate voltage drain current ( $V_{\text{GS}} = 0$ )	$V_{\text{DS}} = \text{Max rating}$ $V_{\text{DS}} = \text{Max rating}, T_{\text{C}} = 125^{\circ}\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{\text{GSS}}$	Gate-body leakage current ( $V_{\text{DS}} = 0$ )	$V_{\text{GS}} = \pm 20 \text{ V}$			10	$\mu\text{A}$
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 150 \mu\text{A}$	3	4	5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on resistance	$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 11 \text{ A}$		0.32	0.36	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{\text{fs}}^{(1)}$	Forward transconductance	$V_{\text{DS}} = 15 \text{ V}, I_{\text{D}} = 11 \text{ A}$	-	22	-	S
$C_{\text{iSS}}$ $C_{\text{OSS}}$ $C_{\text{rSS}}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{\text{DS}} = 100 \text{ V}, f = 1 \text{ MHz},$ $V_{\text{GS}} = 0$	-	3680 246 2	-	pF pF pF
$C_{\text{o}(\text{tr})}^{(2)}$	Equivalent capacitance time related	$V_{\text{DS}} = 0 \text{ to } 760 \text{ V}, V_{\text{GS}} = 0$	-	198	-	pF
$C_{\text{o}(\text{er})}^{(3)}$	Equivalent capacitance energy related	$V_{\text{DS}} = 0 \text{ to } 760 \text{ V}, V_{\text{GS}} = 0$	-	278	-	pF
$R_{\text{g}}$	Gate input resistance	$f = 1 \text{ MHz}$ open drain	-	3	-	$\Omega$
$Q_{\text{g}}$ $Q_{\text{GS}}$ $Q_{\text{GD}}$	Total gate charge Gate-source charge Gate-drain charge	$V_{\text{DD}} = 760 \text{ V}, I_{\text{D}} = 22 \text{ A},$ $V_{\text{GS}} = 10 \text{ V}$ (see Figure 16)	-	105 23 57	-	nC nC nC

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%
2.  $C_{\text{OSS eq}}$  time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{OSS}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$
3.  $C_{\text{OSS eq}}$  energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{\text{OSS}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475 \text{ V}$ , $I_D = 11 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see Figure 15)	-	39	-	ns
$t_r$	Rise time			29		ns
$t_{d(off)}$	Turn-off-delay time			97		ns
$t_f$	Fall time			59		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				88	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 22 \text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 22 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_J = 25 \text{ }^\circ\text{C}$ (see Figure 17)	-	671		ns
$Q_{rr}$	Reverse recovery charge			17	$\mu\text{C}$	
$I_{RRM}$	Reverse recovery current			50	A	
$t_{rr}$	Reverse recovery time	$I_{SD} = 22 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 17)	-	803		ns
$Q_{rr}$	Reverse recovery charge			21	$\mu\text{C}$	
$I_{RRM}$	Reverse recovery current			52	A	

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{gs} = \pm 1 \text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

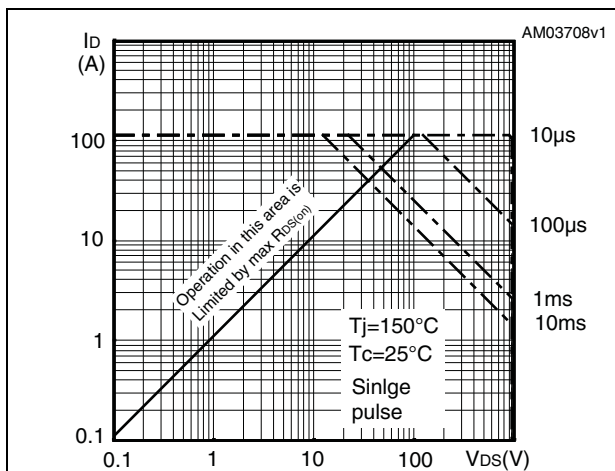


Figure 3. Thermal impedance

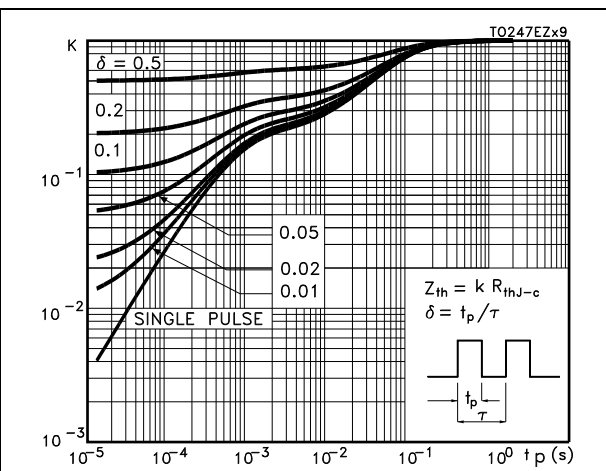


Figure 4. Output characteristics

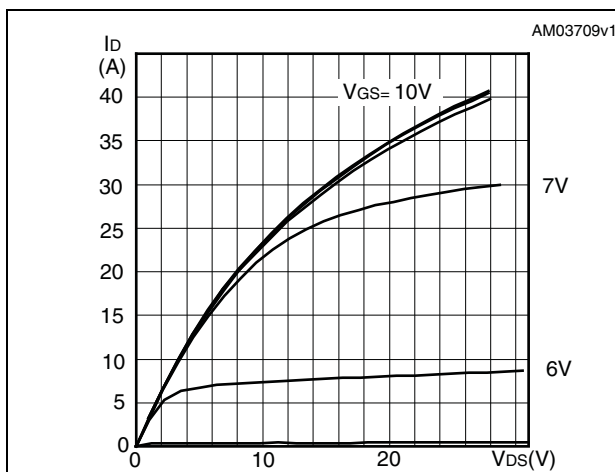


Figure 5. Transfer characteristics

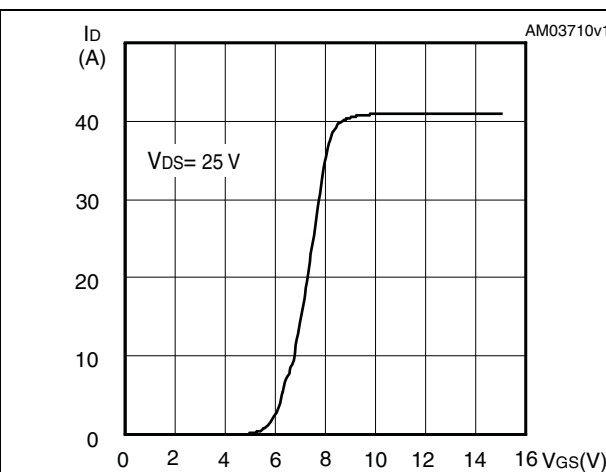


Figure 6. Normalized BV<sub>DSS</sub> vs temperature

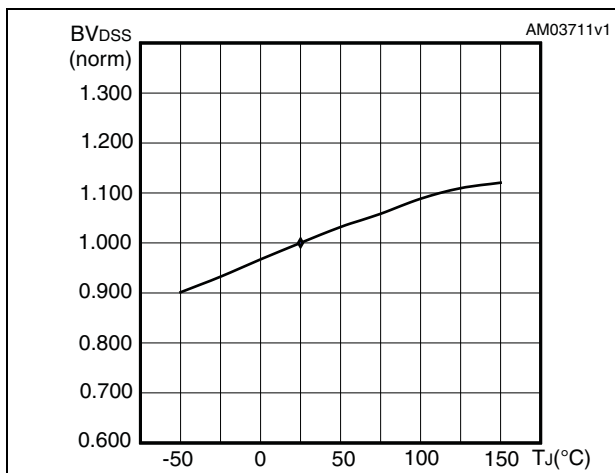


Figure 7. Static drain-source on resistance

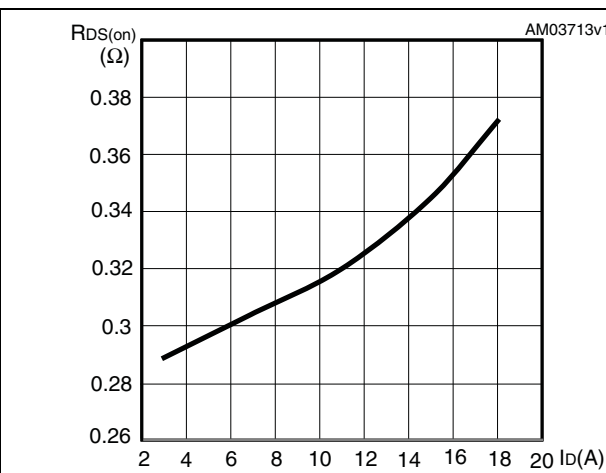


Figure 8. Output capacitance stored energy    Figure 9. Capacitance variations

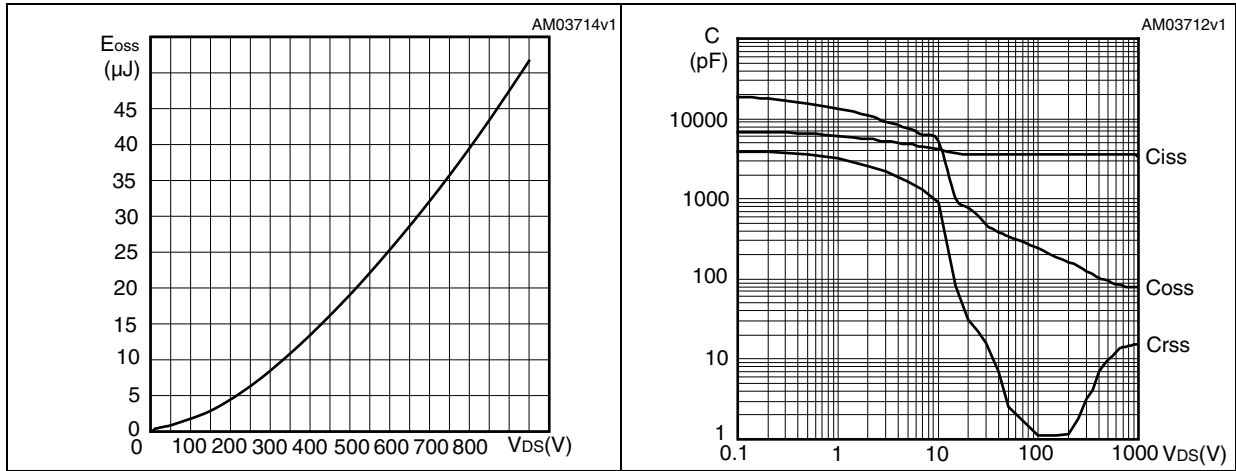


Figure 10. Gate charge vs gate-source voltage    Figure 11. Normalized on resistance vs temperature

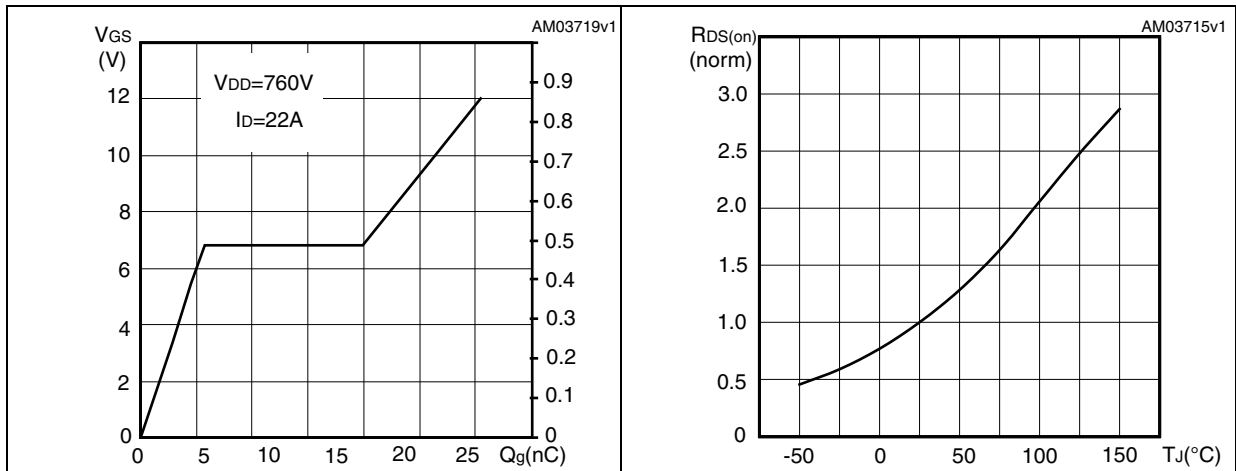


Figure 12. Normalized gate threshold voltage vs temperature    Figure 13. Maximum avalanche energy vs temperature

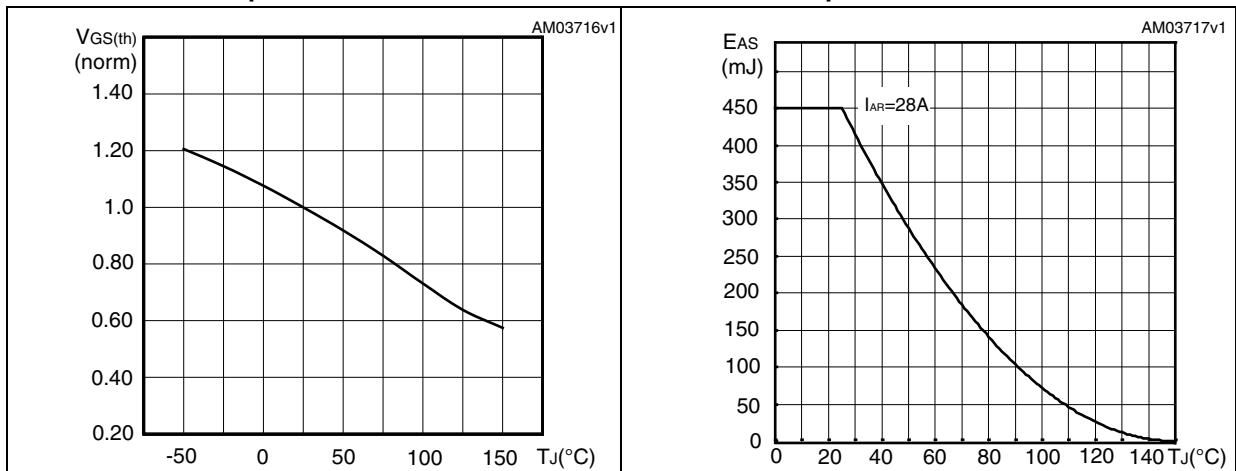
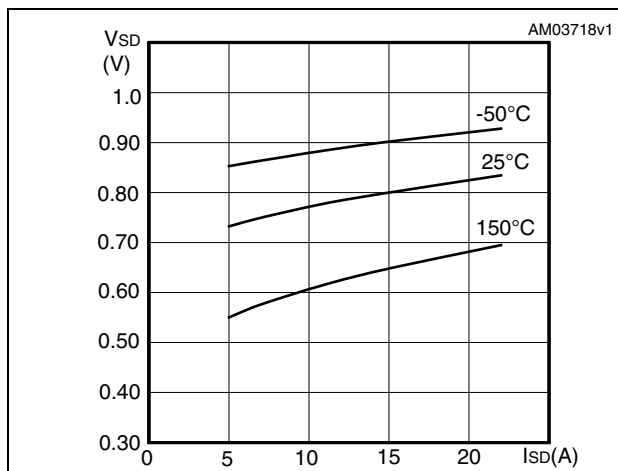


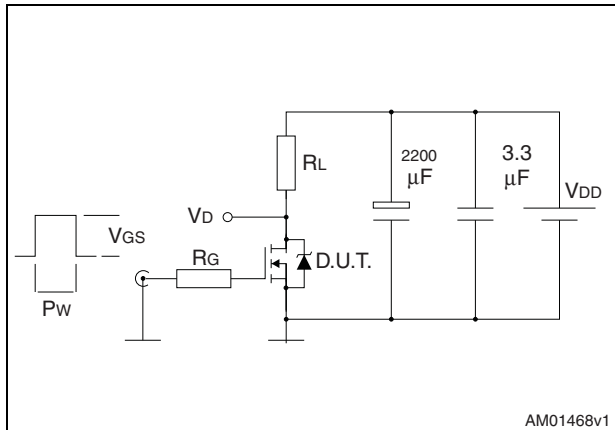
Figure 14. Source-drain diode forward characteristics





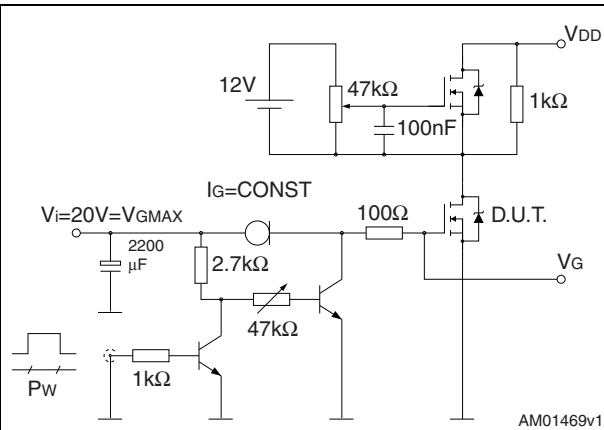
### 3 Test circuits

**Figure 15. Switching times test circuit for resistive load**



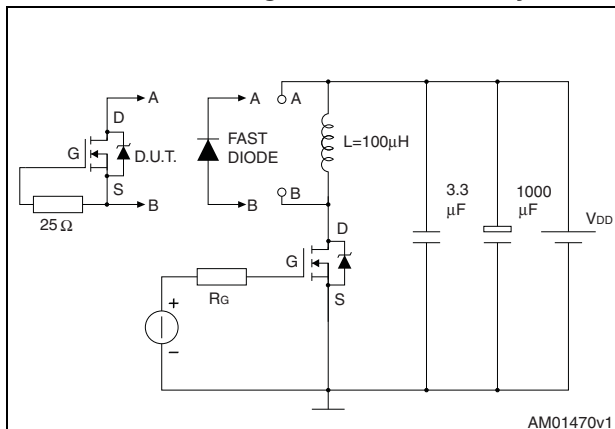
AM01468v1

**Figure 16. Gate charge test circuit**



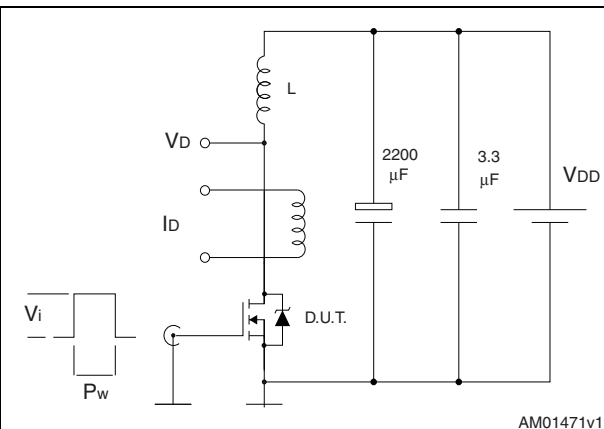
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**Figure 17. Test circuit for inductive load switching and diode recovery times**



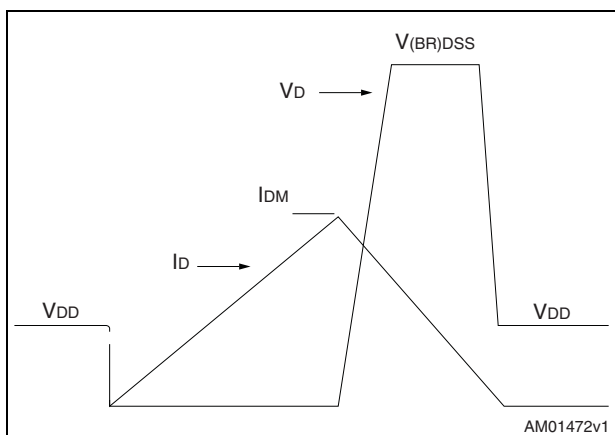
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**Figure 18. Unclamped inductive load test circuit**



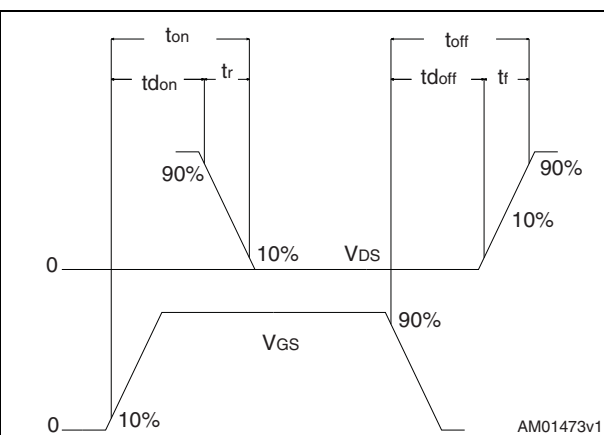
AM01471v1

**Figure 19. Unclamped inductive waveform**



AM01472v1

**Figure 20. Switching time waveform**



AM01473v1

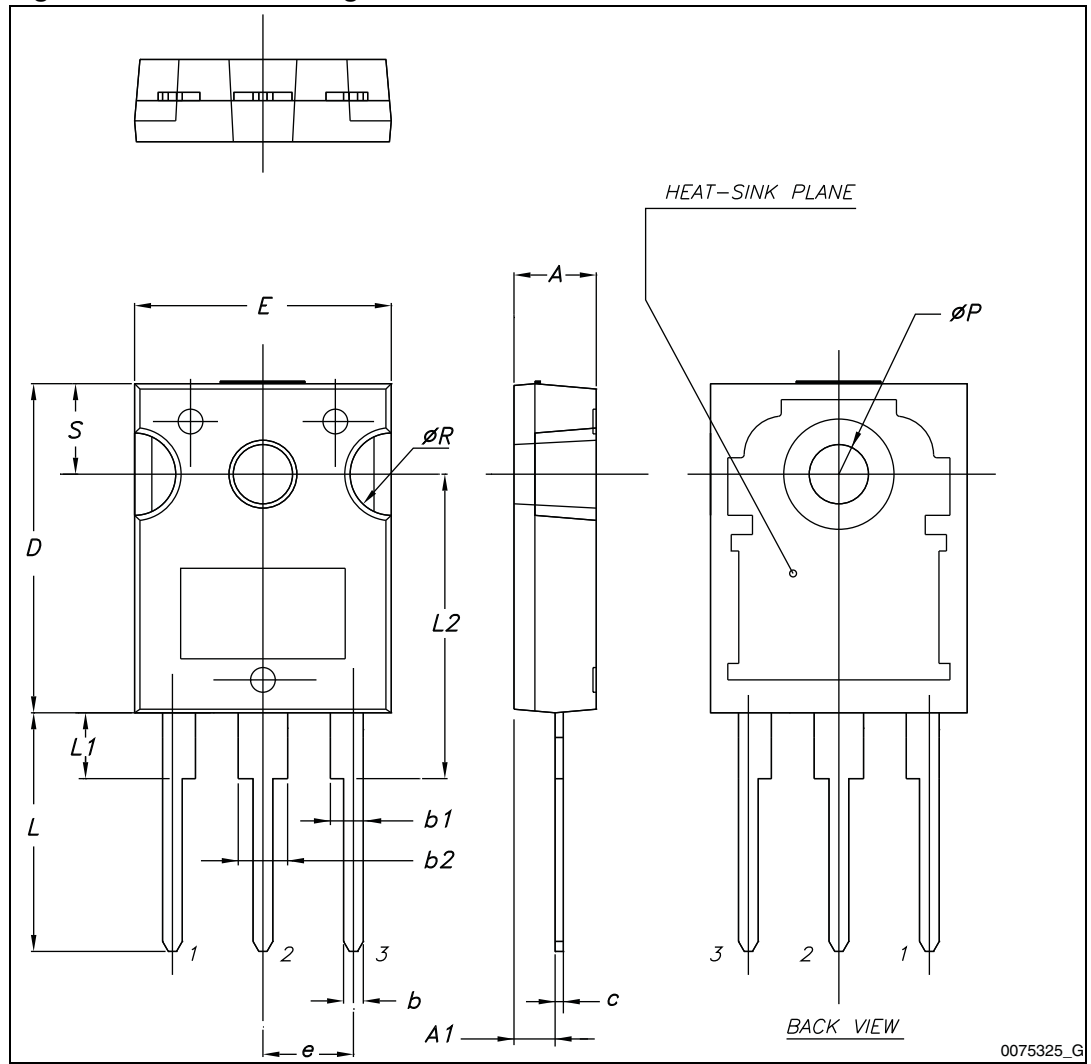
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 9. TO-247 mechanical data**

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 21. TO-247 drawing



## 5 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
27-Apr-2009	1	First release.
09-Jan-2012	2	Document status promoted from preliminary data to datasheet. Updated <a href="#">Section 4: Package mechanical data</a> .

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