

- CURRENT REGULATOR DIODES
- LEADLESS PACKAGE FOR SURFACE MOUNT
- CONSTANT CURRENT OVER WIDE VOLTAGE RANGE
- HIGH SOURCE IMPEDANCE
- METALLURGICALLY BONDED (-1)
- DOUBLE PLUG CONSTRUCTION

CDLL250  
thru  
CDLL257

### MAXIMUM RATINGS

Operating Temperature: -65°C to +175°C  
Storage Temperature: -65°C to +175°C  
DC Power Dissipation: 500 mW @ +50°C  
Power Derating: 4 mW / °C above +50°C

### ELECTRICAL CHARACTERISTICS @ 25°C, unless otherwise specified

TYPE NUMBER	REGULATOR CURRENT I <sub>p</sub> (mA) @ V <sub>S</sub> = 25V (Note 1)			MINIMUM DYNAMIC IMPEDANCE @V <sub>S</sub> = 25V Z <sub>S</sub> (KΩ) (Note 2)	MINIMUM KNEE IMPEDANCE @V <sub>K</sub> = 6.0 V Z <sub>K</sub> (KΩ) (Note 3)	MAXIMUM LIMITING VOLTAGE @ I <sub>L</sub> = 0.8 I <sub>p</sub> (min) V <sub>L</sub> (VOLTS)	PEAK OPERATING VOLTAGE VOLTS
	NOM	MIN	MAX				
CDLL250	5.10	4.59	5.61	100	4.0	3.67	80
CDLL251	5.60	5.04	6.16	90	4.0	4.03	80
CDLL252	6.20	5.58	6.82	80	3.0	4.46	70
CDLL253	6.80	6.12	7.48	70	2.0	4.90	70
CDLL254	7.50	6.75	8.25	50	1.5	5.40	60
CDLL255	8.20	7.38	9.02	30	1.5	5.90	60
CDLL256	9.10	8.19	10.01	20	1.0	6.55	50
CDLL257	10.00	9.00	11.10	10	1.0	7.20	50

**NOTE 1** Pulse measurement @ 1% duty cycle, 10 milliseconds maximum.

**NOTE 2** Z<sub>S</sub> is derived by superimposing A 90Hz RMS signal equal to 10% of V<sub>S</sub> on V<sub>S</sub>

**NOTE 3** Z<sub>K</sub> is derived by superimposing A 90Hz RMS signal equal to 10% of V<sub>K</sub> on V<sub>K</sub>

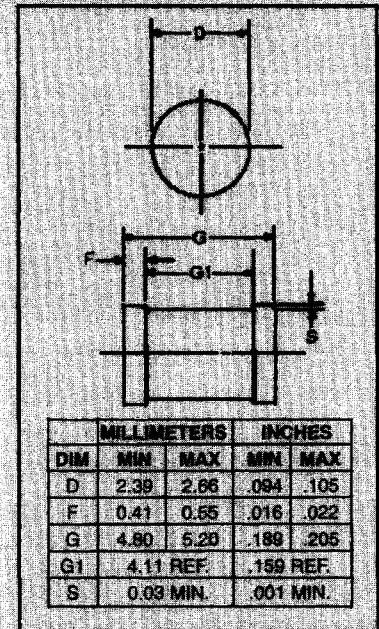


FIGURE 1

### DESIGN DATA

**CASE:** DO-213AB, Hermetically sealed glass case. (MELF, LL41)

**LEAD FINISH:** Tin / Lead

**THERMAL RESISTANCE:** Junction to End Cap = 50 °C/W maximum

**POLARITY:** Cathode end is banded.

**MOUNTING POSITION:** Any.

**MOUNTING SURFACE SELECTION:** The Axial Coefficient of Expansion (COE) of this Device is Approximately +6PPM/°C. The COE of the Mounting Surface System Should Be Selected To Provide A Suitable Match With This Device.



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